

Master's Thesis

Design of a 30 GHz PLL for use in Phased Arrays

Byron Murphy



Department of Electrical and Information Technology,
Faculty of Engineering, LTH, Lund University, 2016.



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Faculty of Engineering, LTH, Lund University
SE-221 00 Lund, Sweden

Abstract

This project includes the research and implementation of a high frequency phase-locked loop (30 GHz or more) for beamforming use in a phased antenna array. The phase-locked loop includes a quadrature voltage-controlled oscillator with a 10% tuning range and 417 degrees of phase control with a 10 degree resolution, a current mode latch in the divide-by-two configuration operates over the quadrature voltage-controlled oscillator's tuning range while consuming less than 583 uA of current, D-type flip flops in a divide-by-8 configuration, a phase-frequency detector, a charge-pump, and a loop filter. The quadrature voltage-controlled oscillator has a phase noise of -102.2 dBc/Hz at 1 MHz, less than 3.53 mA current consumption, and up to 185.6 dBc/Hz figure of merit. Additionally, an injection-locked frequency divider was explored as an optional first-stage divider. The phase-locked loop was implemented using the ST Microelectronics 65 nanometer design kit and simulated using Cadence Virtuoso. The circuit consumes 4.93 mA of current from a 1.2 V supply. Lastly, the bottlenecks that may be encountered while increasing the operating frequency of the phase-locked loop are discussed.

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CHAPTER 1

1 Introduction

In 5G MIMO systems, massive antenna configurations are expected to play a large role in increasing achievable data rates and traffic capacity. The ability to work at very high frequencies allows for a massive increase in available spectrum, due to wide band spectrum allocations at these frequencies. When much higher frequency bands above 10 GHz are used, wave lengths become small which allows for a large number of antenna elements without an unreasonably large physical size. Furthermore, phased array systems are becoming increasingly popular for high frequency wireless data links in low-cost applications thanks advancements made in silicon radio frequency integrated circuit technology as well as the enabling of electronic scanning of the antenna beam and beam-forming (or spatial filtering) of interferers in the receiver. The Shannon-Hartley theorem is shown in (1.1) where C is the channel capacity in bits per second, BW is the channel bandwidth in Hertz, S is the average signal power over the bandwidth in Watts, and N is the average power of the noise over the bandwidth in Watts. From (1.1) it can be seen that, by having more bandwidth available and obtaining a higher signal-to-noise ratio, the channel capacity is increased. Combined, these allow for more bandwidth, the improvement of signal-to-noise ratio, and thus, data rate[1].

$$C = BW * \log_2 \left(1 + \frac{S}{N} \right)$$

Equation 1.1: Shannon-Hartley Theorem

Phased array systems consist of an array of antennas in which the phase of the transmitted or received signals are adjusted in such a way as to steer the beam in a particular direction and suppress the beam in other directions. In doing so, the signal to noise ratio is increased. Digital baseband, analog base-band, local oscillator, and radio frequency beam-forming are four main architectures which exist for beam-forming in phased-array systems, and relate to where the phase shift is implemented. The digital beam-forming architecture is versatile, however, has a high penalty for complexity, chip area, and power consumption. This is because digital beamforming requires the entire signal chain to be duplicated from the

antenna to base-band for each antenna element. Analog beam-forming takes place in the analog domain after frequency down-conversion. Benefits from the analog beam-forming architecture are that phase shifting is easier at frequencies lower than the carrier and multiple analog-to-digital converters (as required by digital beam-forming) are no longer required. Local oscillator beam-forming is advantageous over digital and analog beam-forming because improved linearity can be obtained from it by combining the phase-shifted signals together in the current domain after the mixer to avoid large voltage build-up due to interfering signals. Unfortunately, the high frequency of operation in this architecture versus the base-band architectures presents some difficulties in realization. Radio frequency beamforming requires that a sacrifice between noise, linearity, phase resolution, power, and area must be made. Phase shifting can take place before or after the low-noise amplifier at the front-end. Depending on the location of the phase shifter, noise figure or power consumption and area will suffer[2][3].

As the number of antenna elements increase for wireless communications, such as allowed by a phased array, the signal can be increased and the noise can be reduced. This stems from the constructive and destructive interference performed by the phased array. The use of multiple antennas allows for the signal to noise ratio to be increased proportionally to the product of number of receive and transmit antennas. Thanks to spatial multiplexing, the signal power can be split between multiple channels so that the channel capacity can be made to grow linearly with the number of antennas. Finally, by employing transmit and receive diversity, issues such as frequency selectivity can be overcome. All of the aforementioned techniques result in an increase in the effective signal to noise ratio[1].

Phase-locked loops (PLLs) are control systems which are frequently seen in modern communications systems due to their versatility. PLLs synchronize signals from an oscillator to a reference signal in such a way that they operate at the same phase. PLLs are useful because they allow a designer to create a filtered version of a reference signal with control over how the output tracks the reference. Additionally, they can be used in the phase or frequency (de)modulation of signals. Lastly, part of their remarkable versatility in communications systems stems from their ability to synthesize a signal with a programmable frequency and phase offset from an input signal[4]. This is advantageous in phased-arrays and software-defined radios which require flexible radio-frequency hardware. Modern wireless

communication systems often have an input of a radio-frequency signal and an output of a base-band signal or vice-versa in reception and transmission, respectively. PLLs help facilitate frequency conversion by generating the local oscillator signal. The local oscillator signal is then used in a mixer for frequency conversion to and from base-band.

The goal of this work is to focus on the design and design issues concerning a PC-PLL for use in homodyne architectures. Adding the ability to control the phase allows for the PLL to be used in a phased-array system for local oscillator generation. The idea is to design a PLL which can be located at the antenna elements in a 5G MIMO system. Ideally, the PLL will exist at each antenna element and a reference clock is to be routed to each PLL. The target QVCO output frequency is 30 GHz, however, design bottlenecks encountered in obtaining a faster output frequency should be noted. Phase offsets due to mismatch in routing should be able to be digitally adjusted. Additionally, frequency tuning capabilities should allow for the compensation of process variations, of which, a 10% margin should be accounted for. The distribution of a relatively low frequency reference clock (about 1 GHz) allows for the PLL and its phase-adjustments to generate phase-coherent local oscillator signals at each antenna element without the need for worrying about high frequency routing.

CHAPTER 2

2 PLL Fundamentals

PLLs synchronize the signal from a voltage-controlled oscillator (VCO) with a reference signal so that they are phase-aligned. This is achieved by comparing the phase of the two signals and controlling the VCO so they maintain a constant phase relationship between the two during the locked state. The PLL system consists of a phase-frequency detector, loop filter, VCO, and a feedback path optionally containing a frequency divider. A block diagram of a typical PLL is shown in Fig. 2.1.

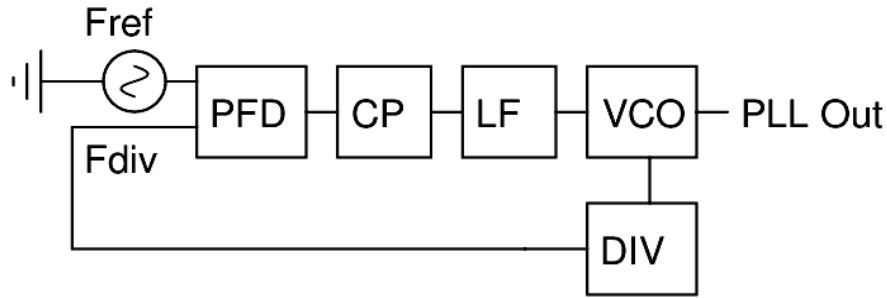


Fig. 2.1: PLL block diagram

The phase detector detects the phase difference of two signals and multiplies that difference with some gain, K_{vco} . The loop filter provides attenuation to obtain an advantageous response characteristic to the input of the VCO. It can also be said that the loop filter contributes a gain to the loop as well. The oscillator will provide a quadrature output at a frequency which is a multiple of a reference frequency, dependent on the feedback path's division ratio. The oscillator output frequency is ultimately controlled by the voltage or current input from the phase detector and loop filter. Thus, the oscillator has a gain which also contributes to the overall loop gain.

The output of the phase detector can be explained using (2.1) where N is the division ratio and F_{ref} is the reference frequency.

$$F_{out} = N * f_{ref}$$

Equation 2.1: Output of the PLL

In RF receivers, where the received signal is converted into either an intermediate frequency or DC, the PLL provides a local oscillator signal which is typically fed into a mixer for frequency conversion. If the phase noise of the local oscillator is too high, reciprocal mixing can occur, causing unwanted out-of-band signals to be mixed in-band- possibly masking a desired in-band signal.

The following sections will explore PLL system as a whole, and each fundamental block individually. This chapter should serve as a basis for understanding the work done and results found in the remaining chapters.

2.1 Phase-Locked Loop Basics

The PLL can be mathematically explained with the block diagram shown in (2.1.1).

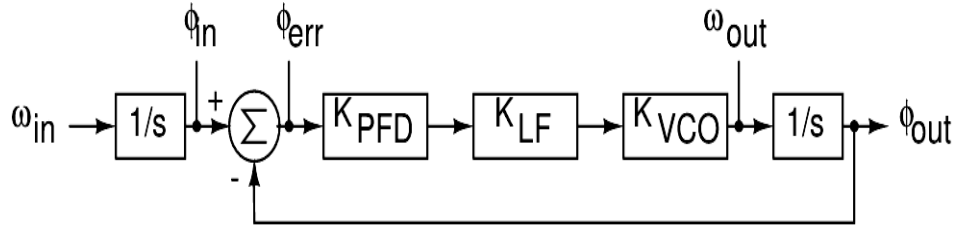


Fig. 2.1.1: PLL mathematical block diagram

The input to this block diagram is the reference signal which is at some frequency, ω_{in} , and some phase, ϕ_{in} . The phase error ϕ_{err} is the phase difference between the voltage-controlled output's phase and the reference signal's phase. It should be noted that phase is the integral of frequency, so, the frequency to phase conversion has been shown in s-notation. The phase-frequency detector converts the phase error to voltage with some gain K_{PFD} and the loop filter is some "gain" K_{LF} . The VCO converts the phase error voltage to frequency with some gain, K_{VCO} [4].

The output phase is related to the input phase using the general equation in (2.1.1).

$$\phi_{out}(\omega) = H(\omega) * \phi_{in}(\omega)$$

Equation 2.1.1: Input to output phase relationship

From (2.1.1), we can see that the output phase is a function of the input phase, which includes phase noise. By integrating the output phase over the frequency range of interest, or, the PLL bandwidth, the phase power (or

variance) of the output (or error) can be found in response to the input phase modulation (or modulations due to the VCO itself). It is also worthwhile noting that the PLL output functions as a low-pass filter for phase noise present before the VCO while the VCO phase error has a high-pass filter characteristic. A signal, $S(f_m)$, that is sinusoidally modulated by some other signal, f_m , with a phase deviation (or modulation index) m and center frequency ω_c can be expressed as in (2.1.2).

$$S(f_m) = \cos(\omega_c t + m \sin \omega_m t)$$

Equation 2.1.2: Modulated signal

The spectrum of (2.1.2) has a strong fundamental at ω_c and spurs at $\omega_c \pm i \cdot \omega_m$ when m is large. Here, 'i' are harmonics of ω_m . In many cases, the purpose of the PLL is to improve the output phase power spectral density (PPSD) relative to the input phase power spectral density[4].

When the phase error from the output to the input of the loop is small, the loop can be assumed to be linear. Fig. 2.1.2 shows the effect of the loop on the input PPSD. The phase error PSD at the input of the loop, introduced by the reference, follows the reference PPSD but reduced by the loop gain for modulation frequencies less than the loop bandwidth. The output PPSD due to noise at the input is reduced by the loop gain for frequencies greater than the loop bandwidth. Similarly, Fig. 2.1.3 shows how, at low frequencies, the output PPSD of the VCO follows the phase error PSD of itself but reduced by the loop gain. In comparing Fig. 2.1.2 and Fig. 2.1.3, it can be seen that the VCO tends to have a higher phase noise at lower frequency offsets while the input will tend to have a higher phase noise at high frequency offsets. This is due to attenuation of noise by the loop. Most often, the optimum bandwidth for the loop filter is at the point where the phase noise densities of the reference and VCO intersect[4].

This information infers that, in choosing the loop bandwidth, the phase noise of the reference, should be taken into account for the best output phase noise performance. If in-band noise is small, a larger loop bandwidth (but sufficiently less than the reference frequency) will result in minimized output noise due to the VCO[5].

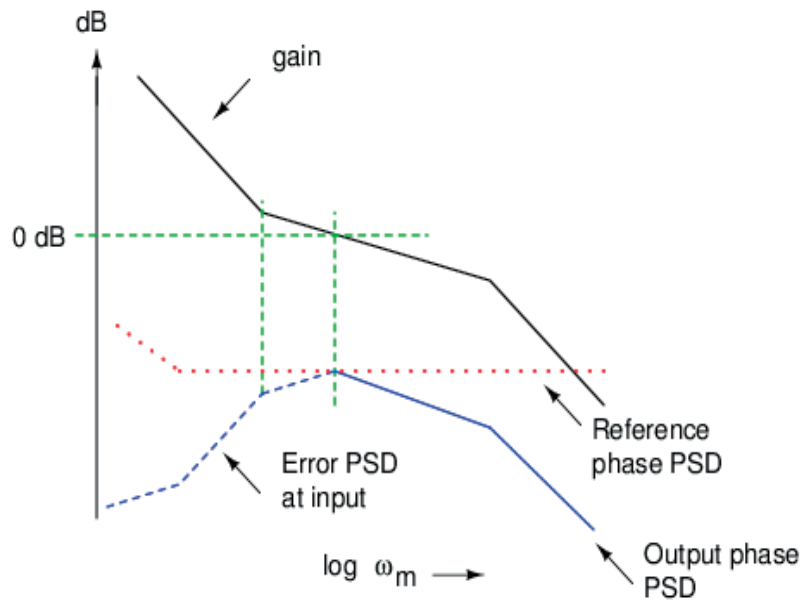


Fig. 2.1.2: Effect of loop on input phase noise

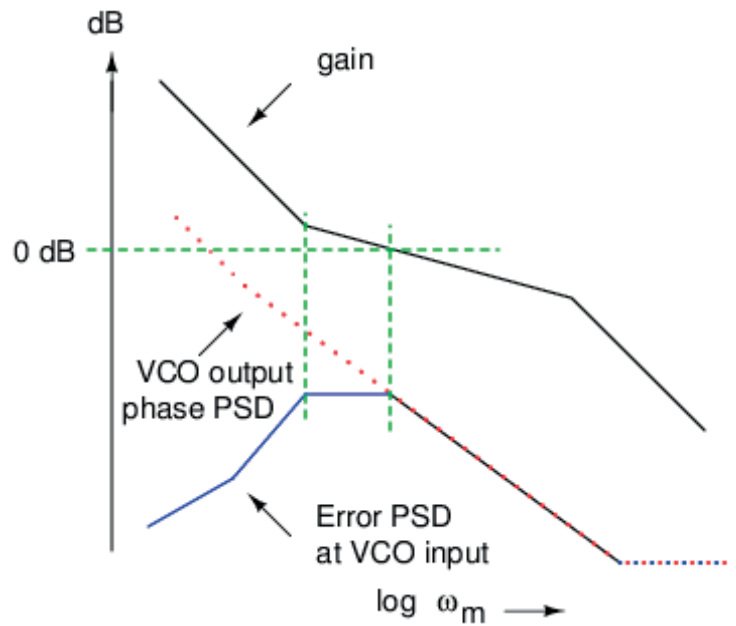


Fig. 2.1.3: Effect of loop on VCO phase noise

2.2 The Phase-Locked Loop System

The PLL has a few specifications that define its overall performance. These specifications are defined and described below[6].

The tuning range is defined by the minimum and maximum frequencies that the PLL can output while meeting system specifications. It is dependent upon the RF frequency of the application it will be used in.

The step size is the minimum change in frequency that the PLL can generate. Depending on the application, this may be big or small. Typically, this specification sets the minimum channel spacing in wireless communications systems.

The settling time denotes the time it takes for a system to change from one frequency to within a given distance of another frequency. This time is dependent upon the open-loop bandwidth and phase margin.

Spectral purity is desired in systems to minimize noise energy near the output signal. Spurious signals can degrade the spectrum and contribute to a noisy synthesizer. In order to keep a pure spectrum, it is important that no modulation takes place on the PLL input signal and unwanted noise is kept away from the VCO input. The effect of a spurious signal, f_m , on a voltage-controlled output signal can be shown mathematically in (2.2.1). Additionally, a pair of spurious signals is generated due to the modulation process of a sine-wave at base-band frequency that have an amplitude proportional to the local oscillator amplitude, as found in (2.2.2).

$$S_{vco} = A_{LO} \cos(2\pi f_{LO}t + \theta_p \sin(2\pi f_m t))$$

Equation 2.2.1: Characterization of output signal of a VCO

$$A_{spurious} = A_{LO} \frac{\theta}{2}$$

Equation 2.2.2: Amplitude of spurious signal vs. LO amplitude

The phase noise in a system represents unintended phase modulation in the carrier signal (phase noise in signal sources).

The hold-in (or synchronization) range is the difference between the maximum and minimum input frequency that the reference signal can be changed while maintaining a phase-locked condition.

The loop bandwidth is also an important parameter of a PLL, as it relates to the speed at which the PLL can achieve a lock and at what phase noise level. With a high loop bandwidth, one can expect a short locking time but

with an increased phase noise- as the high loop bandwidth will allow more noise at the input of the VCO. On the contrary, if the loop bandwidth is low, the time it takes to achieve the lock condition is increased, however, there will be less noise at the input of the VCO resulting in a better phase noise. A zero lock-time and zero phase noise is desired, however it is not practically possible and an application-dependent trade off must be made between lock-time and phase noise. (2.2.3) gives an expression for the loop bandwidth of a PLL where I_{CP} is the charge pump current, K_{VCO} is the charge pump gain, N is the division ratio, and K_{LPF} is a constant concerned with the loop filter[7].

$$BW_{LOOP} = \frac{I_{CP} K_{VCO}}{2\pi N} K_{LPF}$$

Equation 2.2.3: PLL's loop bandwidth expression

2.3 Phase-Frequency Detector

It is the phase detector's purpose to generate an output signal corresponding to the feedback signal's phase relative to the reference signal's phase. Phase-frequency detectors have the ability to produce an output when both the phase and frequency of the feedback signal differ from the reference signal.

Analog phase detectors, such as the double balanced diode and Gilbert cell mixers, provide sum and difference signals which are obtained from the two signals injected into it. When the input signals are the same in frequency, the difference frequency goes to zero while leaving the output at the difference frequency to be proportional to the phase. Filtering is required to suppress undesired signals, such as the sum frequency, harmonics, and input leakage. These undesired signals can cause issues in frequency synthesizer applications that other phase detectors can mitigate.

Digital phase detectors, such as the flip flop and exclusive-OR gate phase detectors, work well for square wave inputs. These types of phase detectors typically operate by outputting a logic high signal when the two input states are different and a 0 when they are the same. The time that the two input states are different indicates their relative phase. So, the digital phase detector output can be used to detect the phase difference between the two input signals. Unfortunately, the phase deviation of two perfectly in-phase signals can be positive or negative. These average output voltage of these types of phase detectors will be the same for a same negative and positive

phase deviation. Thus, only a linear phase detection range of 180 degrees can be obtained.

Many phase detectors exist, of which, the most commonly used is the sequential phase-frequency detector. This phase-frequency detector allows for both phase and frequency errors to be detected and utilized. Additionally, because the phase-frequency detector's output is only active at a fraction of the reference period, less noise is contributed to the loop. A simple and effective implementation of the sequential phase-frequency detector is shown in Fig. 2.3.1.

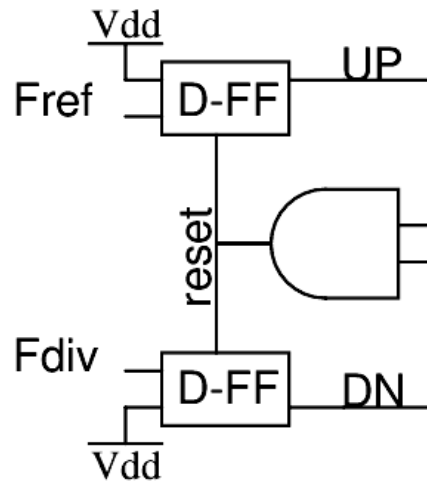


Fig. 2.3.1: A phase-frequency detector implementation

The phase detector has a constant of proportionality which represents the phase detector's gain. The constant of proportionality, often noted as K_p , relates to the output voltage due to the input phase change, and a standard equation is shown in 2.3.1.

$$K_p = \frac{V_{DD}}{2\pi}$$

Equation 2.3.1: Phase-Frequency detector gain

2.3.1 Phase Frequency Detector with Charge-Pump

The sequential phase detector has two outputs that control a charge pump, which sinks or sources current into the loop filter. The addition of the charge pump (and loop filter) transforms the phase-frequency detector output pulses into an analog voltage for the VCO. Typically, an UP signal is

generated to the charge pump when signal A leads signal B. A DN signal is generated to the charge pump when signal B leads signal A. When the PLL is in the locked condition, a detector will either generate two identical UP and DOWN pulses or a signal small enough to not generate a change to the VCO. Since both the UP and DOWN signals are accessible, the charge pump phase detector can theoretically exhibit a phase range from $\pm 2\pi$ radians.

As the loop becomes closer to in-lock, the UP and DOWN pulses become increasingly narrow. Phase-frequency detectors also can exhibit dead bands which represent an interval where the phases of the two base-band signals are close enough that the phase detector output can not accurately represent the phase difference or the charge pump cannot react to the narrow pulse. This phenomenon is called dead-zone and plagues phase-frequency detectors. Dead zones result in low loop gain and increased jitter. They are typically fixed by increasing the minimum pulse width of the UP and DOWN signals when the phase error is close to zero. This has an effect on the maximum frequency of the phase-frequency detector[4].

In order to increase the minimum pulse width of the UP and DN pulses of the phase-frequency detector, a delay is added to the reset pulse which is generated by a NAND gate in Fig. 2.3.1. This can be accomplished by delaying the NAND gate output with buffers, sized accordingly so that the propagation delay meets the minimum pulse width requirement for elimination of the dead zone. This technique eliminates the dead zone, however, a blind zone results which reduces the phase error detection range of the phase-frequency detector. An equation for the blind zone pulse duration is shown in (2.3.1.1), where T_{DFF} is the time from the rising edge of an input transition to the output transition in the phase-frequency detector, T_{min} is the minimum pulse duration necessary to eliminate the dead zone, T_d is the delay time of the reset circuitry, and T_{rst} is the pulse width of the reset signal. Given (2.3.1.1), by decreasing the propagation delay of the D-flip flop, the blind zone will be decreased and the maximum phase error detection range is increased[7].

$$T_{bz} = T_{DFF} + T_{min} + T_d = T_{DFF} + T_{rst} + 2T_d$$

Equation 2.3.1.1: Blind zone pulse duration

The maximum detection range can be calculated using (2.3.1.2), in which, T_p is the period of the input signal.

$$\Delta \theta_{max} = 4\pi \left(1 - \frac{T_{BZ}}{T_p}\right) = 4\pi \left(1 - \frac{T_{DFF} T_{rst} + 2 T_D}{T_p}\right)$$

Equation 2.3.1.2: Maximum phase error detection range

2.4 Charge Pump

Upon receiving the UP and DOWN pulses from the phase frequency detector, the charge pump will either sink or source current to/from the loop filter. When combined with the phase-frequency detector, the charge pump provides an ideally infinite DC gain with passive filters to provide an unbounded pull-in range for higher order PLLs. Some charge-pumps suffer from non-ideal obstacles such as current mismatch, switching time mismatch, leakage current, switching speed, and supply noise rejection. Various kinds of charge pumps exist which can help in reducing non-idealistic effects[8].

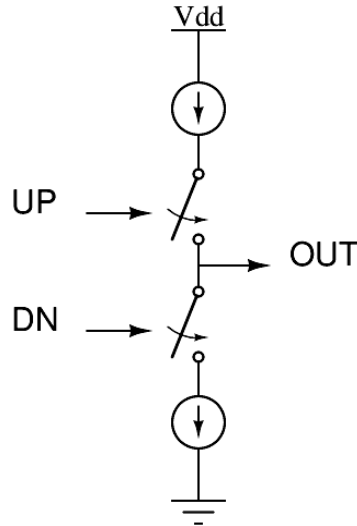


Fig. 2.4.1: A charge-pump model

Charge pumps generally fall into one of four categories: conventional tri-state, current-steering, differential input with single-ended output, and fully differential. More information regarding charge pump architectures can be found in [8]. These charge pumps are summarized in table 2.1.

Architecture	Power	Speed	Clock Skew
Tri-State	Low	Moderate	Moderate
Current Steering	High	High	Moderate
Diff. to Single-ended	Medium	Moderate	Low
Fully Diff.	High	High	Low

Table 2.1: Charge pump architectures

2.4.1 Leakage Current

If the charge pump has any leakage current then phase offsets, although typically negligible, can be observed. However, the reference spur due to leakage current can be dominant in frequency synthesizers. In this case, either the loop bandwidth should be narrowed or the charge pump current should be increased[8].

2.4.2 Timing Mismatch

Timing mismatch in the phase-frequency detector's output signals cause sidebands at the VCO's output. This mismatch can be generated due to the phase-frequency detector's output timing or charge pump's current source turn-on times being different.

2.4.3 Charge Pump Mismatch

A mismatch in the UP and DOWN currents can cause the loop filter to be either charged or discharged more than it should be, causing either a higher or lower output voltage after the loop filter. This results in a phase offset[8]. The charge pump mismatch can be exploited to provide phase offsets to compensate for mismatch in wires during routing, which also causes phase offsets. To accomplish this exploitation, digitally controlled current sources are added to the charge pump output. By statically injecting extra current into the loop filter during each cycle, the divided signal can be forced to lead the divided signal. The phase-frequency detector will then cause the charge pump to counteract the static injection by discharging the loop filter. Once a phase-lock is acquired, this behavior is repeated each cycle to obtain a fixed VCO output phase relative to the reference signal. The phase relation is given in (2.4.3.1), $\Delta\phi$ is the phase relation between the VCO and reference signal, N is the division ratio, I_{injected} is the injected static current, I_{pulse} is the charge pump's current pulse amplitude, and ϕ_{static} is delay due to the division path. The reference spurs will appear at a displacement equal to

that of the reference frequency. So, by increasing the reference frequency, the reference spurs will appear further away from the fundamental[3].

$$\Delta \phi = 2 \pi N \frac{I_{\text{injected}}}{I_{\text{pulse}}} + \phi_{\text{static}}$$

Equation 2.4.3.1: Relation of VCO output phase to reference phase

The net charge pump current is represented by (2.4.3.2), where I_{pump} is the up and down current from the charge pump.

$$I = I_{\text{pump}} \frac{\Delta \phi}{2 \pi}$$

Equation 2.4.3.2: Net charge pump current

Since leakage is such a large issue with respect to control-line ripple, cascoding in charge pumps is an important technique that reduces leakage. In addition to cascoding, using large devices (to mitigate mismatches) and a large overdrive may be used to reduce leakage[9].

2.5 Loop Filter

The loop filter provides an integration of the charge pump output signal as well as a zero to ensure stability[9]. In phase detectors which act as a current source, the loop filter provides current to voltage conversion to tune the VCO. Two types of loop filters exist- passive and active loop filters. Each type has topologies which exist to add poles and zeros to control loop stability. Loop filters can be of multiple orders for more stability, however, a filter order that is too high may affect the PLL response time by contributing to phase lag. In a general sense, noise and control signal will exist at the phase-frequency detector or charge pump output and it is the loop filter's duty to filter the noise or control signal (produced by the phase detection process) so it does not appear at the VCO input. Noise at the VCO input will appear at the VCO output multiplied by the VCO gain. Thus, noise at the input of the VCO will appear as phase noise at the output. On the contrary, if the loop filter bandwidth is too low, the time it takes to obtain a phase-lock will be come affected, which may cause issues in systems where fast channel switching is required[9]. A third order passive loop filter is shown in Fig. 2.5.1.

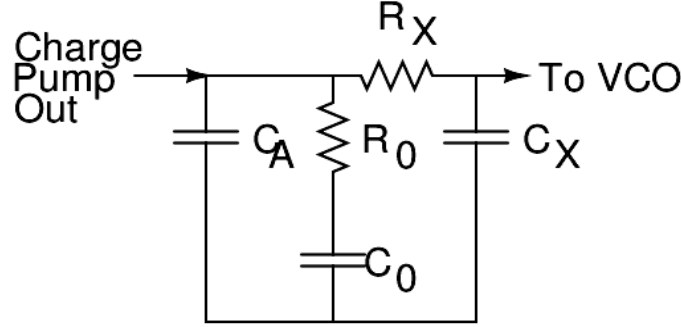


Fig. 2.5.1: 3rd order passive loop filter

In Fig. 2.5.1, the $R_0 C_0$ network is a lead-lag filter and resistor R_0 adds a loop-stabilizing zero to the otherwise pure integration caused by C_0 . Capacitor C_A suppresses the reference spur and the $R_X C_X$ network provides a low pass filter for additional filtering. Resistor R_0 has a large thermal noise contribution which increases the VCO's phase noise[10].

The transfer function, H_{LF} , of the loop filter is shown in (2.5.1). For readability, τ_0 is short-hand for $R_0 C_0$ and τ_X is short-hand for $R_X C_X$.

$$H_{LF}(s) = \frac{s\tau_0 + 1}{s(s^2\tau_0\tau_X C_A + s\tau_X C_0 + s\tau_0 C_A + s\tau_X C_A + s\tau_0 C_X + C_0 + C_X + C_A)}$$

Equation 2.5.1: 3rd order filter transfer function

In addition to the local oscillator signal, the PLL will tend to also output an unwanted sideband, also known as a reference spur. The reference spur can be reduced by decreasing the VCO gain or by reducing the amplitude of the periodic ripples caused by the reference. With respect to the loop filter, the ripple is reduced by inserting a small capacitor in parallel with the lead-lag filter, which is capacitor C_A in Fig. 2.5.1[11]. As discussed previously, leakage currents in the charge pump also can increase the power of the reference spur seen at the VCO.

The phase margin can be designed using the approximation in (2.5.2)

$$PM \approx \text{atan}\left(\sqrt{b+1}\right) - \text{atan}\left(\frac{1}{\sqrt{b+1}}\right)$$

Equation 2.5.2: Approximation for phase margin

where

$$b = \frac{C_0}{C_A + C_X}$$

Equation 2.5.3: Phase margin parameter relation to loop filter capacitors

The crossover frequency can be set by choosing values for R_0 and C_0 using (2.5.4) below.

$$\omega_c \approx \frac{\sqrt{(b+1)}}{R_0 C_0}$$

Equation 2.5.4: Crossover frequency approximation

If I_{CP} , K_{VCO} , and the division ratio N are known, the value of the zero-making capacitor is found using (2.5.5).

$$C_0 = \frac{I}{2\pi} \frac{K_0}{N} \frac{b}{\sqrt{(b+1)}} \frac{1}{\omega_c^2}$$

Equation 2.5.5: Calculating C_0 given loop parameters

Then R_0 is calculated using (2.5.6) where τ_z is a time constant given by (2.5.7).

$$R_0 = \frac{\tau_z}{C_0}$$

Equation 2.5.6: Calculating the zeroing resistor value

$$\tau_z \approx \frac{\sqrt{(b+1)}}{\omega_c}$$

Equation 2.5.7: Time constant calculation for R_0

Lastly, a filtering versus stability trade-off can be calculated by selecting a time constant τ_x from (2.5.8) where (2.5.9) is satisfied.

$$\tau_x = R_X C_X$$

Equation 2.5.8: Time constant for filtering vs stability

$$0.01 < \frac{\tau_x}{\tau_z} < 0.1$$

Equation 2.5.9: Limits for τ_x

2.6 Quadrature Voltage-Controlled Oscillator

The VCO outputs a signal at a frequency which is a function of the input tuning voltage, fundamental frequency, and VCO gain as shown in (2.6.1).

$$\omega_{out} = f_c + v_{tune} * K_{VCO}$$

Equation 2.6.1: Ideal VCO transfer function

It is an essential part of the PLL and, as such, two popular types were considered for the design of the 30 GHz PLL. Many topologies exist which exhibit different phase noises, tuning ranges, maximum output frequencies, areas, and power consumptions. Of the existing topologies, there are generally two categories: ring oscillators and LC oscillators. A basic form of ring oscillators consists of cascaded inverters which rely the propagation delay of each inverter to realize the oscillation frequency. LC oscillators rely on amplifying the output of an LC tank at resonant frequency to provide the oscillation. At operating frequencies of around 30 GHz, LC-type oscillators dominate in performance compared to ring oscillators. It should be noted that ring oscillators are expected to be the best candidates for implementing mm-wave CMOS VCOs when frequencies reach higher than 60 GHz[12]. Thus, this project will adopt and explore the LC oscillator topology exclusively.

A differential approach is attractive because it performs well in high-noise environments by rejecting common-mode noise, has a well defined return path, and has better isolation due to cross-coupling techniques used to reduce the impact of gate-to-drain capacitance and drain-to-source conductance[3]. For this reason, a differential approach has been chosen for the design of the 30 GHz VCO.

This project requires a QVCO which means 0-, 90-, 180-, and 270- degree outputs are needed to achieve high spectrum-efficient modulation in wireless communications systems. There are usually four ways to generate a quadrature signal: RC-CR phase shifters, poly-phase filters, divide-by-2 and clock windowing to generate phases at half frequency, and by synchronizing two VCOs together in parallel or series. The RC-CR phase shifter's accuracy depends on the variation in impedance and conductance resulting from the fabrication process. The poly-phase filter method narrows the operating bandwidth, attenuates input signal power more than the first method, and has a large power consumption overhead. The third method consumes more power than the others but provides a wider bandwidth. The method chosen in this work consists of connecting two identical VCOs together in series to achieve a quadrature output. This method was termed the top series QVCO (TS-QVCO) since the quadrature

coupling transistors are located above the cross-coupled negative resistance transistors and in series with them[13].

The QVCO is formed by coupling two identical VCOs in such a way that they operate in-phase and anti-phase. A study was conducted on the design trade-offs between the single phase differential, parallel, and two different series QVCO topologies. In a fair comparison between the two S-QVCO topologies, namely the TS-QVCO and bottom series QVCO (BS-QVCO), the S-QVCO topologies out-performed the P-QVCO by 8 dB at a 1M offset[14]. Additionally, the strong trade-off between the quadrature signal accuracy and coupling strength in the P-QVCO topology can be avoided by using the S-QVCO topology. A fair comparison between the TS- and BS-QVCO's was also completed and the TS-QVCO outperformed the BS-QVCO in phase noise simulations in as well as phase error measurements.

This is a simple implementation that results in a low quadrature error, large tuning range, large bandwidth, and low amplitude error at the cost of double the power consumption of a single-phase differential VCO and a slightly degraded phase noise[15][13].

2.6.1 Cross-Coupled VCO

The cross-coupled LC VCO uses cross-coupled transistor pairs and an LC resonant tank to generate the oscillation frequency, as shown in Fig. 2.6.1.1.

The Barkhausen criteria states that, for a closed-loop system to oscillate once it has an input applied, the loop must take on a unity loop transmission magnitude and sustain net zero phase-shift around the loop[9].

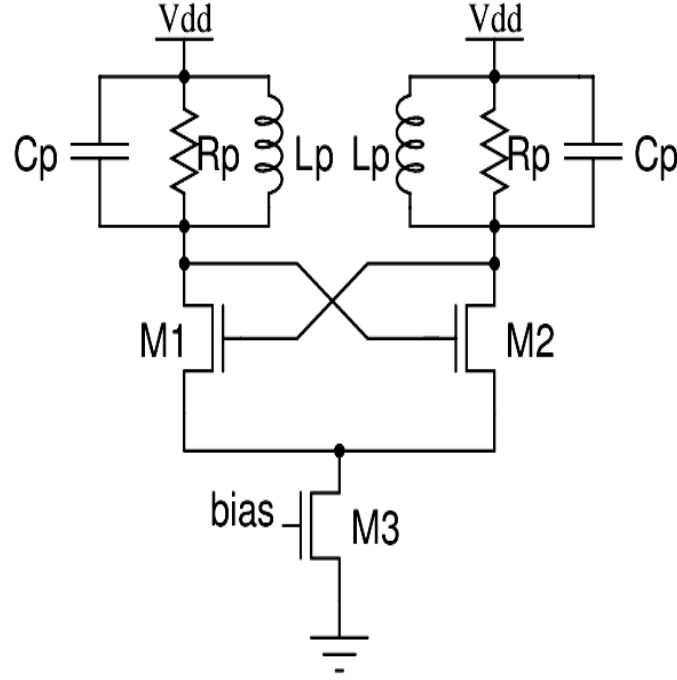


Fig. 2.6.1.1: Typical LC type oscillator

Since the energy storage components involved are lossy, a negative impedance, g_m , (or positive feedback) is needed to cancel the loss, seen as R_p in Fig. 2.6.1.1, to keep the oscillation from decaying. R_p can be found given an equivalent series resistance of the inductor and capacitor in (2.6.1.1). In addition, L_p and C_p can be found given their quality factors, as shown in (2.6.1.2) and (2.6.1.3). Lastly, the tank loaded Q-factor is given in (2.6.1.4), where ω_0 is the fundamental oscillation frequency.

$$R_p = \frac{R_{cs}(1+Q_{cs}^2)R_{ls}(1+Q_{ls}^2)}{R_{cs}(1+Q_{cs}^2)+R_{ls}(1+Q_{ls}^2)}$$

Equation 2.6.1.1: Equivalent tank parallel resistance

$$L_p = L_s \frac{1+Q_{ls}^2}{Q_{ls}^2}$$

Equation 2.6.1.2: Equivalent inductor parallel inductance

$$C_p = C_s \frac{Q_{cs}^2}{1 + Q_{cs}^2}$$

Equation 2.6.1.3: Equivalent capacitor parallel capacitance

$$Q_{\text{loaded}} = \frac{R_p}{\omega_0 L}$$

Equation 2.6.1.4: Loaded tank Q-factor

The cross-coupled pair (M_1 , M_2) provides this negative impedance. To satisfy the Barkhausen criteria, the g_m of the amplifier needs to be greater than $1/R_p$. That is, (2.6.1.5) must be satisfied. Typically, a g_m of about three times the required g_m for oscillation is chosen to guarantee oscillation throughout process, voltage, and temperature variations.

$$g_m > \frac{1}{R_p}$$

Equation 2.6.1.5: Oscillation condition requirement

Some trade-offs exist in using all PMOS, all NMOS, or complementary cross-coupled topologies. Complementary cross-coupling results in voltage limitations while a single pair of cross-coupling transistors results in current limitations. NMOS-only designs have an advantage over PMOS-only ones in that they can achieve a lower phase-noise due to its maximum output signal swing being higher, assuming the same inductance is used. In low-power applications, such as mobile wireless communications, a complementary design is more suitable because it achieves a better phase noise per unit current and area[16].

The capacitance of the VCO is tuned using varactors to adjust the output frequency. To reduce the size of the varactor, capacitors can be switched in using digital signals to change the frequency band of the oscillator without degrading the phase noise too much. Additionally, the node at the tail current source of the cross-coupled transistors has a second-order harmonic of the oscillation. Thermal noise in the tail current source transistor near this frequency will add to the phase noise of the oscillator. A filtering technique, using an inductor to resonate with the stray capacitance to ground, can create a large impedance at the tail node for the second-order harmonic frequency. This method will keep the differential pair from loading the resonator while in the triode region. A large capacitor to ground

can be placed at the tail current source's MOSFET's drain terminal to short frequencies near the second harmonic to ground[17].

2.6.2 Oscillation Frequency

The oscillation frequency is dictated in a behavioral model according to its tank inductance and capacitance, shown in (2.6.2.1). However, in practical circuits, the oscillation frequency is also a function of the series component quality factors, as in (2.6.2.2).

$$\omega_{osc} = \frac{1}{\sqrt{L_p(C_{tune} + C_{fixed} + C_{par})}}$$

Equation 2.6.2.1: Behavioral oscillation frequency

$$\omega_{osc} = \frac{\sqrt{(L_s - C_s R_{ls}^2)}}{\sqrt{(C_s L_s)} \sqrt{(L_s - C_s R_{cs}^2)}}$$

Equation 2.6.2.2: Practical oscillation frequency

2.6.3 Start-up Requirements and Oscillation Voltage

In order for oscillation to occur after the initial transient, the Barkhausen criteria must be satisfied. For this to happen, there must be enough negative resistance to cancel the loss of the tank in order to guarantee oscillation[18]. This is accomplished by setting the widths of the cross-coupled transistors to the minimum length that guarantees oscillation while biased at the minimum current and also accounting for some margin of error.

The tank voltage is proportional to the bias current and tank parallel resistance. The equation for the output voltage is given in (2.6.3.1).

$$V_{out} = \frac{4}{\pi} I_{bias} R_p$$

Equation 2.6.3.1: Oscillator output voltage

The inductor Q-factor is chosen to guarantee low phase noise, sufficient oscillation voltage, and start-up requirements. A minimal inductance relaxes tuning-range constraints by increasing the capacitance budget. The cross-coupled transistors are selected to have a minimum length to reduce parasitic capacitance and maximize transconductance[19].

The bias is chosen so that sufficient voltage swing is met throughout each frequency band. It is the purpose of the cross-coupled transistors to provide

negative resistance to compensate for the loss of the LC tank, however, if the cross-coupled transistor sizes become too large, they contribute to phase noise due to the inclusion of their non-linear capacitance to the total tank capacitance. The inductor equivalent series resistance is modeled so that performance is simulated accurately. Otherwise, the inductor appears less lossy and more-likely to oscillate along with less phase noise.

2.6.4 Tuning Range and Gain

A frequency plan outlines the total bandwidth that the VCO will need to operate in. The varactor and capacitor sizes are selected such that the VCO satisfies the design's tuning range. When digitally controlled tuning bits switch in a capacitor, the capacitors are chosen such that each discrete frequency step results in a partial frequency overlap. In this way, the entire frequency band is guaranteed to be able to be reached. The VCO gain is defined as the change in output frequency with respect to the change in input voltage (2.6.4.1).

$$K_{VCO} = \frac{F_{out2} - F_{out1}}{V_{ctrl2} - V_{ctrl1}}$$

Equation 2.6.4.1: VCO Gain equation

The tuning varactor controls the gain at each frequency band. As the varactor becomes larger, a larger maximum capacitance is inserted into the LC tank over the tuning voltage range. This translates to the output frequency range becoming higher. Thus, the overall gain increases and the VCO output frequency is more sensitive to voltage changes at the input. The gain is chosen to be the smallest value which covers the tuning range required to minimize phase noise degradation due to amplitude-modulated to phase-modulated noise conversion. This is due to the effective varactor capacitance depending, not only on the control voltage, but also on the oscillation amplitude. The sensitivity of a MOS varactor's effective capacitance can be analyzed using (2.6.4.2). Here, C_{eff} is the effective varactor capacitance, C_{max} and C_{min} are the maximum varactor capacitances, respectively, V_{eff} is the effective threshold voltage, and A is the amplitude of oscillation.

$$\frac{\partial C_{eff}}{\partial A} = \frac{C_{max} - C_{min}}{\pi} \times \frac{2V_{eff}}{A^2} \times \sqrt{1 - \left(\frac{V_{eff}}{A}\right)^2}$$

Equation 2.6.4.2: Varactor sensitivity to amplitude

The amplitude modulation to frequency modulation is therefore obtained by taking the partial derivative of the output frequency with respect to amplitude, as is done in (2.6.4.3)[20].

$$K_{AMFM} = \frac{\partial \omega_0}{\partial A} = -\frac{1}{2} \frac{\omega_0}{C_{eff}} \frac{\partial C_{eff}}{\partial A}$$

Equation 2.6.4.3: Amplitude to frequency modulation

In addition, smaller components in the loop filter may be used[3].

2.6.5 Phase Noise

Ideally the PLL, when in a locked state, should result in the VCO synthesizing a signal at a continuous frequency. Noise contributions at the VCO input can cause output jitter in the frequency domain, or phase noise. Unfortunately the varactor has a non-linear junction capacitance and, combined with a steep tuning slope, converts amplitude modulation noise to phase modulation noise[21]. As the varactor channel length decreases, the Q-factor increases, leaving the tuning range also reduced[3]. Capacitors tend to have a much higher Q and are controlled via switches digitally.

The Q-factor of the inductor is typically the lowest of the LC tank and most important with regard to phase noise degradation. As operating frequency increases, however, the varactor Q-factor degrades and will have a noticeable affect on phase-noise. Eventually, the tank Q-factor can only be improved by sacrificing the VCOs tuning range[22]. Various high Q-factor inductors have been developed for high frequencies between 30 GHz and 60 GHz. These include ranges from 17 to 23.5[3]. As previously mentioned, the VCO's control voltage has an effect on the phase noise because input noise appears multiplied by the VCO gain and contributed to the output. Phase noise can be improved by limiting control voltage noise.

The cross-coupled transistors have a non-linear capacitance which also contributes to phase noise. The transistors are chosen to be small enough to provide the required transconductance and not contribute much to capacitance at the output node. Better phase noise can be had by lowering the gain and increasing the number of digital tuning bits. Knowing that the tank Q-factor, thus oscillation amplitude, changes over the tuning range, a circuit can be used to optimize the bias current for each tuning band. This circuit is called an automatic gain control (AGC) circuit which measures the output amplitude to provide some feedback to the tail current source.

The AGC circuit can boost the g_m at start-up and lower the g_m once oscillation is sustained[6].

The phase noise for the cross-coupled VCO can be approximated using the tank Q-factor, oscillation frequency, offset frequency from f_{osc} , Boltzmann's constant, thermal temperature, tank parallel resistance, tail current, and α - a coefficient for g_m scaling. The equation for accomplishing the above task is given in (2.6.5.1). Leeson's expression for single sideband phase noise in dBc/Hz is shown in (2.6.5.2), where f_c is the 1/f corner frequency, F is the noise factor and P_s is the output power[6].

$$L(f_m)_{MOSFET} = \frac{1}{2} \frac{1}{Q_{LC}^2} \left(\frac{f_{osc}}{f_m} \right)^2 k T \frac{\left(\frac{2}{3} \alpha + 1 \right)}{R_p I_{tail}^2}$$

Equation 2.6.5.1: Phase noise to carrier ratio for an LC MOS VCO

$$L(f_m) = 10 * \log \left[\frac{1}{2} \left(\left(\frac{f_{osc}}{2 Q_{LC} f_m} \right)^2 + 1 \right) \left(\frac{f_c}{f_m} + 1 \right) \left(\frac{F k T}{P_s} \right) \right]$$

Equation 2.6.5.2: Leeson's phase noise expression

The varactor causes frequency FM modulation of the VCO due to noise voltage or current at the device. The noise modulation of the varactor is given by (2.6.5.3).

$$V_n^2 = 4 K T R_{var}$$

Equation 2.6.5.3: Varactor noise modulation

The tail transistor acts as a current source and any noise due to the transistor is frequency translated by the negative resistance transistors. The up-converted noise appears as a dual sideband around fundamental frequency. The differential pair contributes noise to the voltage-controlled output while the pair is in its active region. The tank loss adds to output noise as well[23].

Large contributors to the noise in an oscillator are due to the thermal noise and flicker noise. As current flows through the MOSFET thermal noise can be found in the channel between the drain and source, given in (2.6.5.4), when in the linear region. At the saturation point and beyond, the noise can be approximated to be (2.6.5.5). In (2.6.5.4) and (2.6.5.5), k is Boltzmann's

constant, T is the absolute temperature, g_0 is the channel conductance at zero drain-source voltage, and g_m is the MOSFET's transconductance[24].

$$i_d^2 = 4 k T g_0$$

Equation 2.6.5.4: Thermal noise, linear region

$$i_d^2 = 4 k T \left(\frac{2}{3}\right) g_m$$

Equation 2.6.5.5: Thermal noise, saturation and beyond

Flicker noise is found by using the Hooge equation and integrating this equation over several sections of the MOSFET channel. The total flicker noise power spectrum can be calculated using the mobility fluctuation model to be (2.6.5.6), with a noise voltage spectrum density of (2.6.5.7). Here, a_1 is the Hooge $1/f$ noise parameter which is empirically found to be about 0.002 in homogenous metals and semiconductors, q is the elementary charge, m is the mobility, V_{GS} is the gate to source voltage, V_T is the threshold voltage, I_{DS} is the drain to source current, L is the length, f is the operating frequency, C_{ox} is the oxide capacitance, and W is the width of the transistor[24].

$$i_f^2 = a_1 \frac{q m_f (V_{GS} - V_T) I_{DS}}{L^2 f}$$

Equation 2.6.5.6: Noise power spectrum, flicker noise

$$v_f^2 = a_1 \frac{q m_f (V_{GS} - V_T)}{2 m_{eff} C_{ox} W L f}$$

Equation 2.6.5.7: Noise voltage power spectrum, flicker noise

The previous four equations provide a valuable insight into optimizing the phase noise given a noise summary of the VCO. The equations can be applied to each parasitic element that can be found in the first order model of Fig. 2.6.5.1.

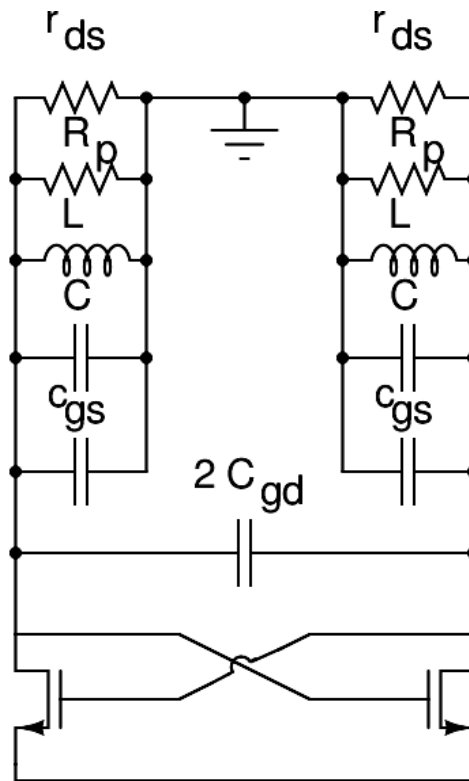


Fig. 2.6.5.1: VCO with some parasitic elements shown

A single side-band characteristic of the phase noise of an oscillator is shown in Fig. 2.6.5.2.

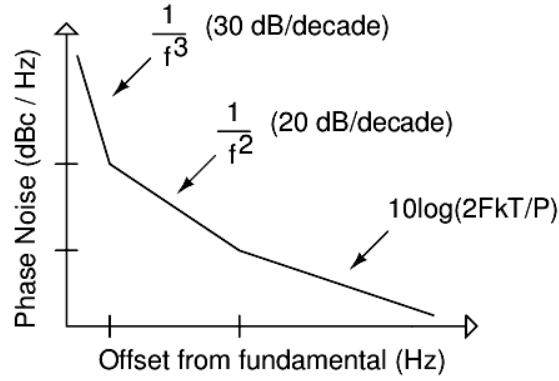


Fig. 2.6.5.2: Phase noise single side-band characteristic

2.6.6 Power Dissipation

The power dissipation of the VCO is useful in conjunction with other parameters because it can gauge the power consumption used to make the oscillator work, as well as to see how well it works. To find the power dissipation, the steady-state DC current is found and multiplied by the supply voltage. An equation for the power dissipation is given in (2.6.6.1).

$$P_{\text{dissipated}} = I_{ss} * V_{DD}$$

Equation 2.6.6.1: Power dissipation equation

2.6.7 Fig. of merit

A fair figure of merit allows for a comparison of VCOs while including the important parameters discussed previously. Although many figure of merits exist, a standard one is given in (2.6.7.1)[25].

$$FOM = [-PN(\Delta\omega) + 20\log_{10}\left(\frac{f_{osc}}{\Delta\omega}\right) - 10\log_{10}(P_{DC,mW})]$$

Equation 2.6.7.1: Standard figure of merit

In (2.6.7.1), PN is the phase noise at a frequency offset, $\Delta\omega$, from the carrier and $P_{DC,mW}$ is the steady-state DC power consumption of the VCO.

2.7 Frequency Dividers

Conventional PLLs will use some sort of frequency divider for the feedback path although these dividers tend to consume a large portion of the total PLL's power. The VCO outputs an RF frequency that may eventually be divided down to the reference frequency. Regenerative frequency dividers are widely used, however, they require additional circuitry to work correctly. Parametric frequency dividers use a non-linear component, such as a varactor diode, in order to create a subharmonic oscillation. However, a high Q-factor diode is required and hard to realize in modern silicon technologies. Injection-locked frequency dividers make use of synchronizing an oscillator with an injected signal and can be used in low-power applications[26]. Digital dividers typically have a limited frequency range that prevents operation at very high RF frequencies such as in this application. In addition, digital dividers have a power consumption that is proportional to the input frequency. At some point the operating frequency versus power consumption of digital dividers is not as efficient as injection-locked frequency dividers [9]. Furthermore, the digital dividers cause spurious disruptions on the supply during each switch, which can disrupt sensitive analog blocks, such as the nearby VCO, from proper operation[3]. The dividers which are actually used in the design will be covered more in detail. For some completeness, other dividers will be briefly discussed.

2.7.1 Regenerative Frequency Divider

A regenerative frequency divider, also called a Miller divider, may operate over a wide bandwidth and large range of input levels. A block diagram of this divider can be seen in Fig. 2.7.1.1. The mixer outputs a sum and difference frequency of the input and feedback signal. The divider has a feedback path which includes an amplifier, filter, and power divider. The amplifier can amplify the signal in the case of any conversion loss while the filter (low pass) filters out the sum frequency. These mixers can operate while maintaining low $1/f$ noise and noise floor performance. Unfortunately, they require an excess amount of circuitry, making it unattractive for use as a divider in low power systems[26][27].

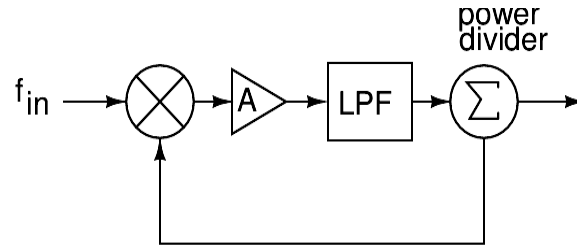


Fig. 2.7.1.1: Regenerative frequency divider block diagram

2.7.2 Parametric Frequency Divider

Varactor diodes have a non-linear capacitance versus voltage. Using this fact, when applying an input frequency to it, a negative resistance is generated which corresponds to an output signal at half of the input frequency. Isolation networks must be added to separate the input currents from the output currents[27]. These isolation networks are tuned networks, meaning an extra level of unattractiveness is added to the parametric frequency divider due to an added number of inductors to the design. A block diagram of such a frequency divider is shown in Fig. 2.7.2.1.

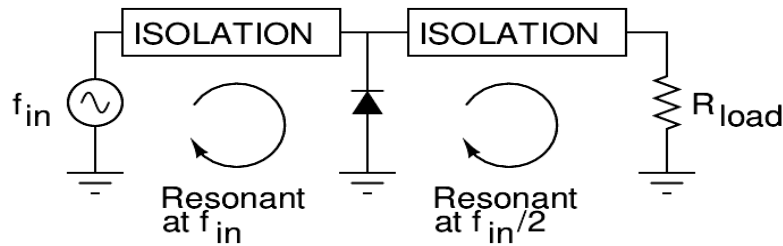


Fig. 2.7.2.1: Parametric frequency divider

2.7.3 Injection-Locked Frequency Divider

There are three kinds of injection locked frequency dividing, depending on a ratio of the injected signal to the free-running oscillator frequency. If the injected signal's frequency is the same as the free-running frequency, then the injection-locked oscillator is termed a first-harmonic injection-locked oscillator. If the injected signal's frequency is a subharmonic, or an integer division, of the free-running oscillator frequency then it is called a subharmonic injection-locked oscillator. Similarly, if the injected signal's frequency is a superharmonic, or multiple of, the free-running oscillator frequency, then it is called a superharmonic injection-locked oscillator[26].

In Fig. 2.7.3.1, a model of an injection locked frequency divider is shown. If v_i is zero, the injection-locked oscillator can be said to be free-running. If v_i is non-zero and meets injection-locked criteria (gain and phase conditions), the injection-locked oscillator can be said to be injection-locked. The $F(NL)$ block is a non-linear component which has an output that contains harmonics and intermodulation terms between v_i and v_o . $H(\omega)$ is a frequency selective block and a function of an angular frequency ω . The diagram shows the positive feedback which is necessary for the oscillation conditions to be met. An expression for the output of $F(NL)$ can be seen in (2.7.3.1) where $K_{m,n}$ is an intermodulation coefficient from the summation of v_i and v_o , ω_o is the frequency of the output signal, and ϕ is the phase difference between v_i and v_o . After passing through $H(\omega)$, a signal with frequency ω_o can be expressed as in (2.7.3.2)[26].

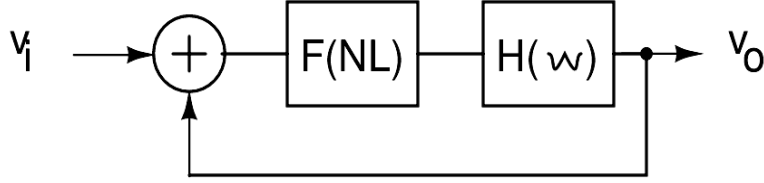


Fig. 2.7.3.1: Model of an ILFD

$$F(NL) = f(v_i + v_o) = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} K_{m,n} \cos(m\omega_i t + m\phi) \cos(n\omega_o t)$$

Equation 2.7.3.1: Nonlinear block output

$$F(NL)_{\omega_o} = K_{0,1} \cos(\omega_o t) + \frac{1}{2} \sum_{m=1}^{\infty} K_m N_m \pm 1 \cos(\omega_o t + m\phi)$$

Equation 2.7.3.2: Output components at ω_o

The model and equations above help explain how the injection of a signal into the tank, along with non-linear components and a tuned circuit can realize an output at frequency ω_o . Fundamental (and simultaneous) equations for a superharmonic injection-locked oscillator's output voltage and phase for a given injection signal amplitude and offset frequency are shown in (2.7.3.3) and (2.7.3.4). Variable N is the division ratio, ω_r is the resonant frequency, H_0 is the transfer function of the frequency selective block at the free-running frequency, and Q is the tank Q-factor.

$$V_o = H_o \left[K_{0,1} + \frac{1}{2} \sum_{m=1}^{\infty} K_{m, Nm \pm 1} \sin(m\varphi) \right]$$

Equation 2.7.3.3: Superharmonic oscillator's output voltage, real values

$$2V_o Q \Delta \frac{\omega}{\omega_r} = \frac{H_o}{2} \sum_{m=1}^{\infty} K_{m, Nm \pm 1} \sin(m\varphi)$$

Equation 2.7.3.4: Superharmonic oscillator's output voltage, imaginary values

Classic CMOS injection-locked frequency dividers have inefficient injection-locking due to being injected at the tail current source which results in a limited locking range. A typical classic complementary injection-locked frequency divider can be seen in Fig. 2.7.3.2. By injecting directly into the tank, the locking range can be made much wider. It was shown that the locking range is proportional to the injection current and inversely proportional to the Q-factor and tail current in (2.7.3.5). When using the direct injection method, the injection transistor(s) can be made very small, according to the desired injection strength[28].

$$\Delta \omega = \frac{I_{in} R_s}{I_{tail} \omega_0 L} = \frac{I_{in}}{I_{tail} Q}$$

Equation 2.7.3.5: Locking range equation

To further discuss the increase of locking range, the range can be increased by using an inductor with a larger value or by increasing the amplitude of the injected signal. Both methods of increasing the locking range are limited by phase and gain conditions of injection locking. Specifically, the phase condition requires that any excess phase introduced in the loop at the output frequency should be zero. If the system is excited at frequency ω_0 in an open loop and the amplitudes at v_o of the system and the summation output are the same, then the gain condition is satisfied. The locking range is dependent upon the free-running frequency and injection ratio. To enable a wider locking range, capacitors can be digitally switched into the output of the circuit, as done in the VCO. The locking range of the injection-locked frequency divider can be reduced if the free-running frequency of the injection-locked oscillator can scale with the output frequency of the VCO. For this reason, the VCO and injection-locked frequency divider can

benefit from sharing the same tuning control voltage and frequency tuning bits[26].

In tuning injection-locked frequency dividers, the frequency of the injected signal should be near the center of the pass band of the frequency divider. Varactors are used to tune the free-running frequency of the injection-locked frequency divider. When the input frequency enters the locking range of the N^{th} order injection-locked frequency divider, the output frequency becomes $(1/N)^{\text{th}}$ of the input frequency with a phase noise characteristic similar to that of the input signal.

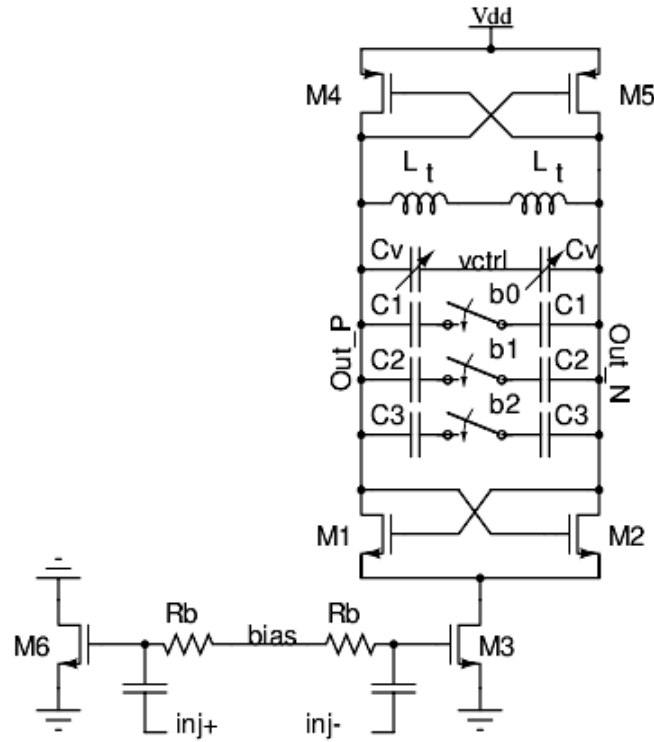


Fig. 2.7.3.2: Standard injection-locked frequency divider

Transistors M1, M2, M4, and M5 in Fig. 2.7.3.2 serve to generate the negative resistance required to keep the oscillation from decaying. C1, C2, and C3 are the coarse tuning capacitors while bits b2, b1, and b0 switch the capacitors in and out of the circuit for coarse tuning. C_v are varactors which are tuned by vctrl. Together, C_v and $C_{1,2,3}$ are used to tune the oscillator to the required pass-band. Transistors M4 and M5 are also sized for making a

symmetric output waveform. M3 is the tail current source which is biased by a circuit which is not shown. The actual injected signal here is capacitively coupled to the gate of the tail current source. M6 can serve as dummy loading for the positive injected signal.

2.7.4 Current Mode Latch

CML latches can be very attractive for high frequency RF division because they use a static current which will not disrupt the supply as much as digital dividers. Unfortunately, CML latches show a frequency selective characteristic which requires careful design so that the entire input frequency range may be met or the input amplitude must be raised. Otherwise, an input frequency outside of the input range will result in an input-to-output delay approaching half an input clock cycle and the latch will not have the output ready in time for the next latch to sample[3]. A division-by-N ratio is established when N latches are cascaded together with positive and negative clocks alternating to each block. The final negative differential output is connected to the positive differential input and the final positive differential is connected to the negative differential input. CML circuits are differential and generally consist of a pull up, pull down, and a static current source. A conventional CML latch consists of two branches- one for tracking and the other for holding (or latching), shown in Fig. 2.7.4.1. When the positive clock goes high, the circuit will track the input and pass it directly to the output. When the negative clock goes high, it will hold the current value at the output. The propagation delay is given by (2.7.4.1) where C_{total} is the total output capacitance and R_L is the load resistance. The maximum operating frequency is obtained by adding the setup time to (2.7.4.1). The bandwidth will also increase by reducing the load resistance[29].

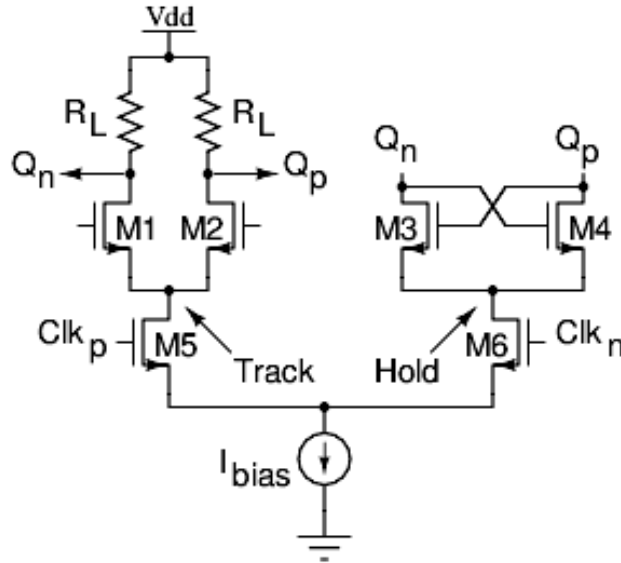


Fig. 2.7.4.1: Conventional CML Latch schematic

$$T_{DQ} = C_{total} * R_L$$

Equation 2.7.4.1: Propagation delay from input to output

If the circuit is latching, Q_n is logic 1, and Q_p is logic 0, then M_1 is off and $M_{2,5}$ are on. The maximum output voltage that can be seen is dependent upon the current through $M_{2,5}$ while they are ‘off’ and the resistance R_L . The same can be said of the minimum output voltage. Thus, the output voltage does not swing rail-to-rail, so the CML latch operates at a lower power[29]. Considering the maximum and minimum output voltage, the output of the CML latch is buffered to drive the downstream dividers.

Device overlap capacitance can allow for the output to couple back to the input and the clock to feed through toward the output. By using capacitive coupling to the gate of the switching transistors, the former problem can be eliminated. Additionally, clock feed through can be neutralized using the same method, however, excess capacitance should be avoided at the output in the interest of D-to-Q delay. A large resistive component is added in series to dampen, or, reduce the effect sharp spikes at high frequencies. These additions result in reduced setup time and dynamic power dissipation[29].

Conventional CML latches have a relatively high power dissipation at high frequencies. To combat this power dissipation issue, either inductive peaking or dynamic CML latches with modulated loads can be used. These

methods also can contribute to much larger operating frequencies, such as 70 GHz[30]. Inductive peaking, however, can contribute to design complexity and increased die area due to possibly large inductors needed.

Conventional latches will use the same transistor sizes for the sample and hold pair for complete current switching to take place in the circuit. Parasitic capacitances in the transistors require the tail current to be much higher than it needs to be to obtain a higher slew rate, and thus higher operating frequencies. This is wasteful because the hold transistors need not be so large since they do not need a large bias current to operate. The latch can be modified so that the track and hold branches use separate bias currents[31]. To achieve this, the sample and hold transistors can share a current source and the hold transistor sizes can limit the current through the hold branch. Thus, circuit complexity is reduced[29]. A diagram of this concept is shown in Fig. 2.7.4.2 where the R_L resistors are load resistors and the blocks are transistor pairs.

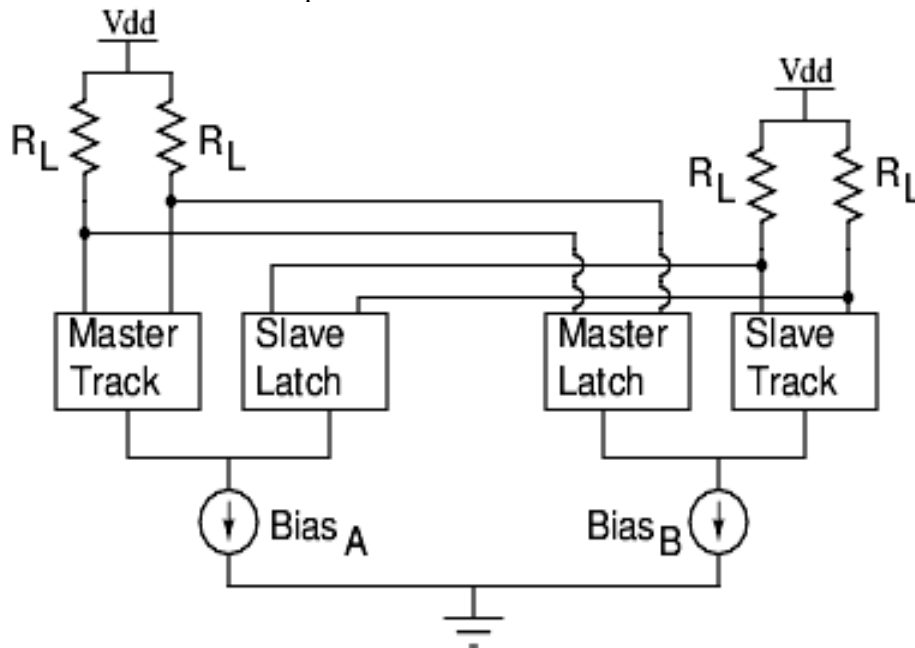


Fig. 2.7.4.2: Modified CML latch in divider configuration

2.7.5 D-Type Flip Flop Dividers

When the input frequency is low enough, D-type flip flops can divide the frequency further using less power consumption than the CML latches. These are typically in the final division stages toward the reference

frequency. A schematic of a D-flip flop and a D-flip flop in a divider configuration is shown in Fig. 2.7.5.1.

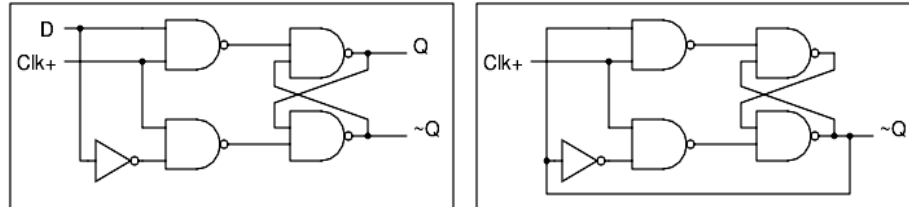


Fig. 2.7.5.1: D-FF (Left), Divider configuration (Right)

The flip flop inverted output is connected directly to the input while the divided frequency input signal connects to the clock input. In this connection, a feedback is formed which outputs a signal at exactly one half of the input clock frequency. At the first half of the input clock cycle, the output will be latched while, during the second half, the output stays at its last value until the next cycle. At higher frequencies, parasitic capacitances must be charged and discharged much faster than at lower frequencies which means the driving strength should be greater. However, as the driving strength increases, so does the size of the transistors, contributing excess parasitic capacitance. A trade off must be made between operating frequency, drive strength, and parasitic capacitance. The driving strength of the flip flops can be scaled down as the input frequency reduces to save power when using cascaded D-type flip flops for division.

CHAPTER 3

3 Design Process

A 30 GHz quadrature output PLL output was desired. To facilitate this, a frequency plan was developed where a 30 GHz QVCO with a 10 % tuning range would output a signal to be divided by 2 at the first stage. The following stages divide the 15 GHz signal down by 8 to realize the feedback signal, which feeds back to the phase-frequency detector. Good phase noise performance was desired with a minimum current consumption in each frequency divider block.

This section will discuss the design steps and considerations taken while constructing the PLL circuits. Starting with the VCO, the most important part, and moving on to the next lowest frequency circuits- the first stage divider and beyond. Finally, the phase-frequency detector and charge pump / loop filter designs are discussed.

3.1 Quadrature Voltage-Controlled Oscillator

The VCO is required to output a 30 GHz quadrature signal according to the specifications of the project. The tuning range is expected to be 10%, or 3 GHz, to account for process variation. A phase noise and a target current consumption of a few milliwatts was targeted. A table of similar VCOs is shown in table 3.1 which shows a comparison of DC power, phase noise, and frequency range. This was used as a reference for how much phase noise and power this project will target.

Reference	Output Frequency (GHz)	Phase Noise (dBc/Hz)	P _{DC} (mW)
[32]	26.8-30.3	-114.3 @ 1 MHz	7.8
[33]	29.24-31.56	-128 @ 10 MHz	4.56
[34]	27.36-41.04	-100.4 @ 1 MHz	11
[35]	29.98-31.01	-108.5 @ 1 MHz	9.2
[35]	29.617732-30.42	-104.1 @ 1 MHz	2.3

Table 3.1: VCO Comparison

A realistic Q-factor value of 15 was chosen along with an inductor value of 382 pH. Using the function shown in (3.1.1), the equivalent series resistance of the inductor was found to be about 4.8 Ω and the parallel resistance is 1.1 K Ω using (3.1.4).

$$R_s = \frac{(2\pi\omega_0 L)}{Q}$$

Equation 3.1.1: Inductor series resistance given Q-factor

A voltage swing of nearly 1.2 V is desired, maximizing the voltage that the technology can electrically handle. The current needed for this voltage is about 1.1 mA, as calculated from (3.1.2).

$$V_{\text{tank}} = I_{\text{bias}} R_p = I_{\text{bias}} \omega_0 L Q_L$$

Equation 3.1.2: Tank voltage swing

A power dissipation of about 1 mW can be expected, as calculated in (3.1.3).

$$P_{\text{DC}} = I_{\text{bias}} \times V_{\text{supply}}$$

Equation 3.1.3: Dissipated power

The cross-coupled NMOS transistors must have a g_m that is enough to cancel the loss of the tank. In other words, (2.6.1.5) must be satisfied. Thus, a g_m of at least 921 μS is needed. To account for process, voltage, and temperature variations, the target g_m is roughly 2.1 mS. Ideally, the width of the cross-coupled NMOS (M1 and M2 of Fig. 3.1.1) should be a minimal size which results in minimum up-conversion of 1/f noise while still satisfying (2.6.1.5) with margin[9].

$$R_p = R_s (Q^2 + 1)$$

Equation 3.1.4: Equivalent parallel resistance equation (inductor)

Given the previously chosen topology of QVCO, the total bias current will be double that of the VCO. The current was selected so that a minimum phase noise was obtained without wasting current or resulting in too large of a voltage swing. Since quadrature outputs are necessary, two extra transistors (M4 and M5 of Fig. 3.1.1) were added to the design to accept differential inputs from the second VCO's tank output at nodes A and B. The optimum width-to-length for these transistors is determined to be $5 \cdot (W/L)_{M1,M2}$ for achieving the best phase noise performance while understanding that the phase error is almost independent of this variable[14].

A tuning range of 10% is required. Thus, the VCO should operate between 28.5 GHz and 31.5 GHz. Digital tuning of the frequency band was implemented to reduce the VCO gain, and thus total phase noise. Three bits were used in digital tuning to provide eight discrete frequency steps throughout the tuning range. Due to non-linear components, the switched in capacitor values were manually set so that frequency steps between 28.5 GHz and 31.5 GHz were obtained with roughly a 25% frequency overlap in each band. The same was done for the varactor capacitance to ensure the entire frequency range can be swept while using codes 000 to 111. The switched capacitors C1, C2, and C3 were set to 2.8 fF, 4.9 fF, and 8.7 fF, respectively, to meet the tuning range requirement. The varactors were designed with minimum lengths to maximize their Q-factor. The maximum gain of the VCO is shown to be 1.211 GHz / V.

After optimization, a DC current of 1.6 mA was used in the VCO, thus, the QVCO used a total of roughly 3.2 mA, consuming 3.8 mW of power. In practice, automatic control of the bias current can be implemented over the tuning range as well as to optimize the g_m for start-up improvements. This is accomplished using an automatic gain control (AGC) circuit to keep a stable amplitude over the frequency range. Both VCOs share the same current source, but the current source's drain is isolated from each VCO using inductors L_{filt} .

A capacitor, C_d , capacitively couples the VCO's output to the buffer. The self-biased inverter (using resistor R_o) buffers the output of the VCO. In this way, the output can be made to be rail-to-rail. Resistor R_o can contribute to isolation issues if it is not large enough. In the design, R_o was chosen to be 30 K Ω . In the case of isolation issues with downstream circuitry, another inverter that is not self-biased can be placed at the output of the self-biased inverter.

A filtering technique to reduce the second harmonic seen at the tail current source was adopted to reduce phase noise. Inductor L_{filt} was placed in series with the source of the cross-coupled transistors and the tail current source. The inductance was chosen to resonate with the parasitic capacitance at M1 and M2 at the second harmonic frequency. Additionally, a large capacitor C_{filt} was placed at the drain of M3 to set a pole for high frequency signals. Inductor L_{filt} was optimal at around 600 pH near the second harmonic and a C_{filt} value of 1.3 pF was selected.

The schematic diagram illustrates a 1T1C 1T1C crossbar array with a differential readout circuit. The array consists of two rows of access transistors (M1, M2) and two columns of storage capacitors (C1, C2, C3). The word lines are controlled by a differential pair of access transistors (M4, M5) driven by a differential readout circuit. The readout circuit includes two inverters with feedback resistors (Ro) and capacitors (Cd). The array is biased by a common-mode bias circuit (M3, Cfilt) connected to the word lines. The output signals are Out_P and Out_N.

[illegible]

For the best results in the on-state, the voltage at the drain and source of the transistor in Fig. 3.1.2 should be 0 volts which achieves the lowest channel resistance. In the off-state, the drain and source voltage should be the highest to prevent the transistor from switching on twice per period, affecting the phase noise. To accomplish this, the input bX is the inverse of tune_bX, however, tune_bX is at a 1.8 volt level and bX is at a 1.2V level. The two resistors are in place so as not to decrease the tank Q-factor during

the off-state. This method creates an RC time constant from the bias resistors and drain/source parasitic capacitance. It can be reduced by using transistors between the bias voltage and drain/source to temporarily reduce the resistance between the two and quickly transfer the bias voltage to the drain/source. This may be necessary for the circuitry which provides the codes for course / fine tuning of the PLL not to give an incorrect code and lose the lock condition[36].

The VCO must operate in quadrature and the TS-QVCO topology was selected and implemented. Transistors were placed in series with the cross-coupled negative g_m transistors. The transistors must be sized so that sufficient negative g_m is provided and not too much parasitic capacitance is contributed to the tank. The quadrature transistors (M4, M5) were sized about 5 times larger than the cross-coupled transistors (M1, M2) for optimum phase noise. Design iterations to correct or ensure correctness of the tuning range and phase noise were made since the tank capacitance was changed as the optimum sizes were selected.

Table 3.2 shows the size of transistors and passive components used throughout the QVCO design.

Component	Size (W/L) (μm) unless specified
M1, M2	3 / 0.15
M4, M5	5 / 0.06
M3	94.5 / 0.06
M_{varactor} (not shown)	68 / 0.06
C1	2.8 fF
C2	4.9 fF
C3	8.7 fF
C_{filt}	1.3 pF
L1	382 pH
L_{filt}	600 pH
Cd	5 fF
Ro	30 K Ω

Table 3.2: QVCO Component Sizes

The QVCO tuning range results are shown in Fig. 3.1.3, where the 10% requirement has been met using a control voltage between 200 mV and 800 mV and 3-bit discrete tuning. The QVCO gain results at each discrete step are shown in Fig. 3.1.4.

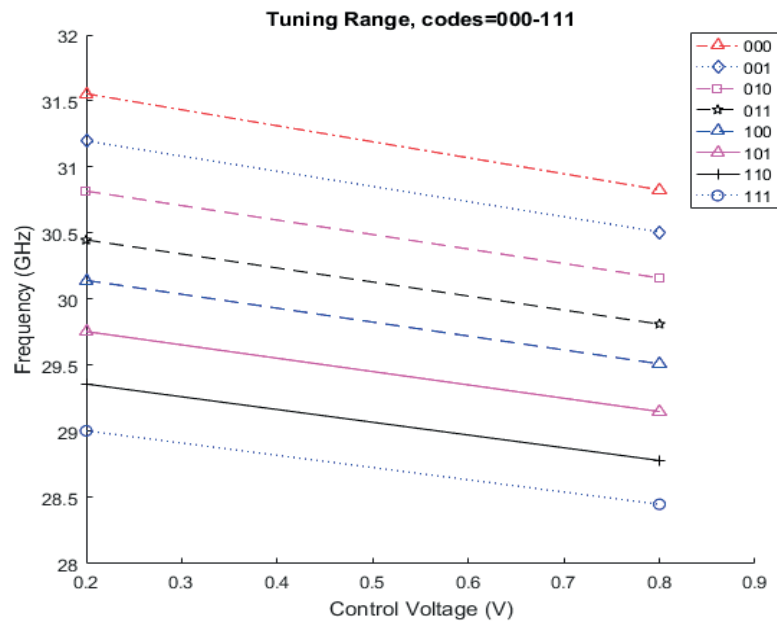


Fig. 3.1.3: QVCO tuning range

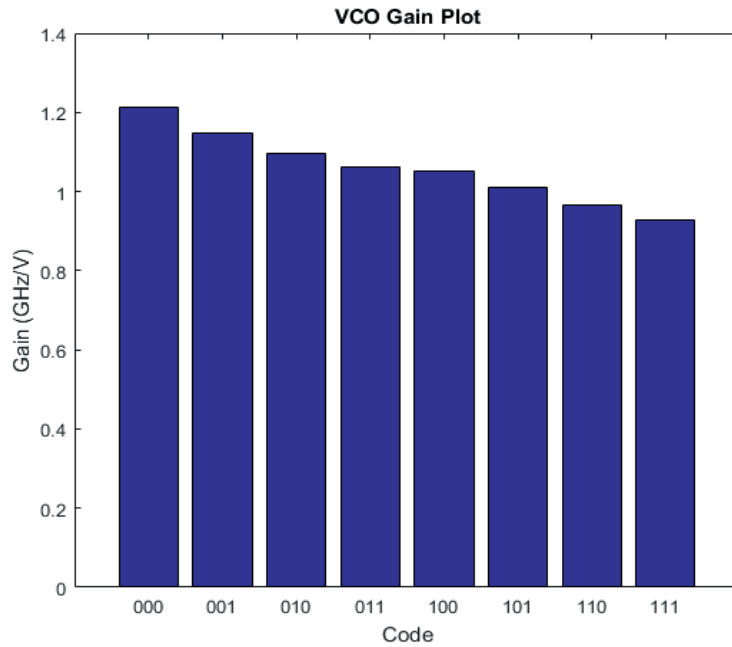


Fig. 3.1.4: QVCO Gain vs Control Code

The QVCO's steady-state current consumption as a function of tuning code and control voltage is shown in Fig. 3.1.5. The figure shows that the current consumption ranges between 3.594 mA and 3.196 mA.

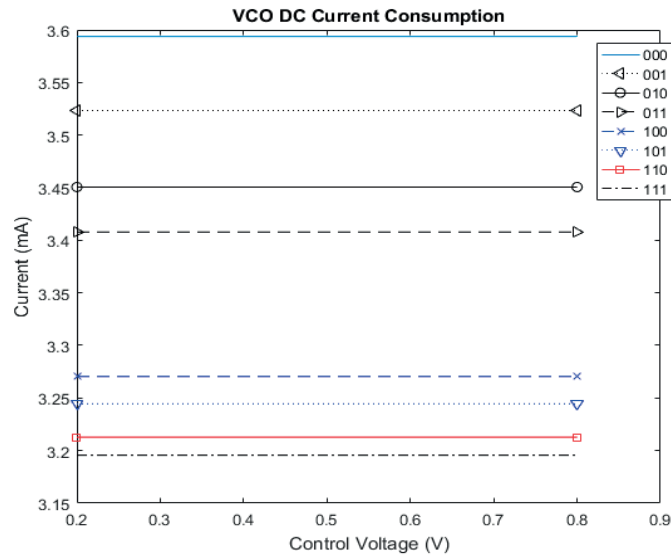


Fig. 3.1.5: QVCO DC Current Consumption

The VCO phase noise is shown in Fig. 3.1.7 where the minimum phase noise at 100 kHz, 1 MHz, and 10 MHz offsets are -74.12, -102.2, and -125.8 dBc/Hz. The plot shows the phase noise at each discrete tuning step while the control voltage is arbitrarily set to 600 mV. The achieved figure of merit for the VCO is shown in Fig. 3.1.6.

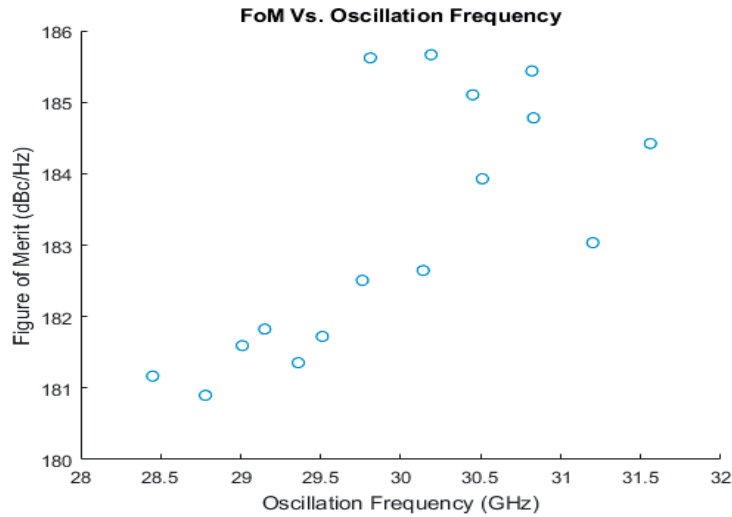
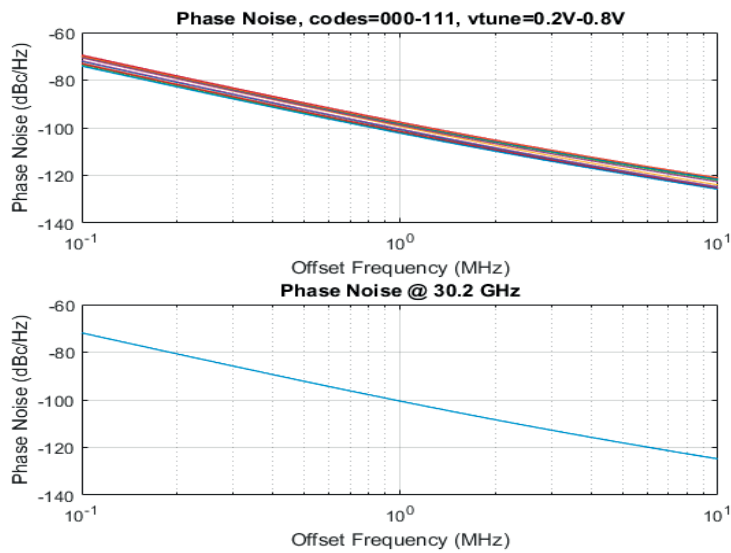


Fig. 3.1.6: QVCO figure of merit



3.1.7: QVCO phase noise plot

Fig.

The transient signals in Fig. 3.1.8 show the quadrature outputs at roughly 30 GHz before buffering.

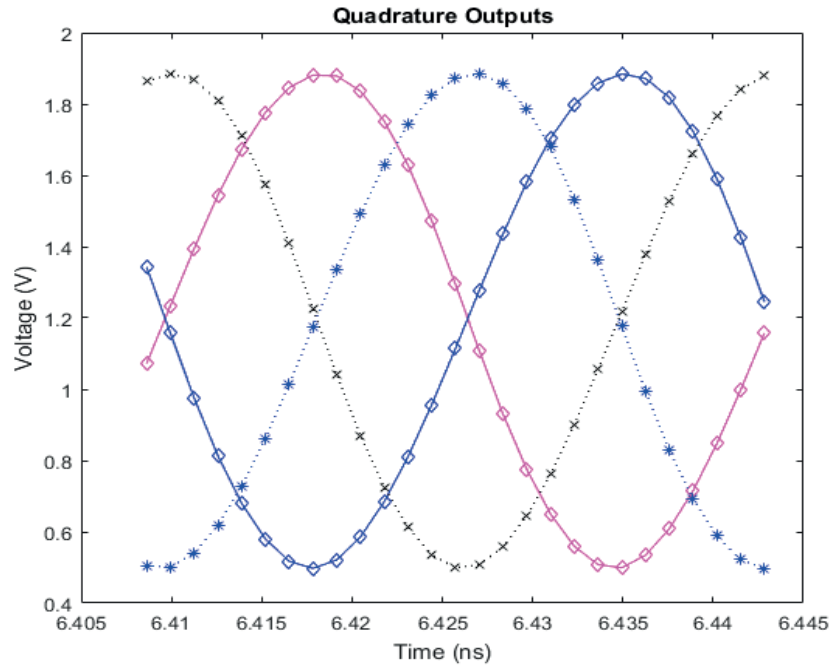


Fig. 3.1.8: Quadrature VCO transient outputs

Specification	Result
DC Current Consumption	3.19 mA to 3.52 mA
Tuning Range	10.06 %
Phase Noise:	
@ 100 kHz offset	-69.35 to -74.08 dBc/Hz
@ 1 MHz offset	-97.58 to -102.2 dBc/Hz
@ 10 MHz offset	-121 to -125 dBc/Hz
Oscillation Amplitude	Approx. 1.3 V to 1.1 V
FoM	184 to 186.6 dBc/Hz
Gain	0.926 GHz/V to 1.21 GHz/V
Phase Error	0.726 degrees

Table 3.3: QVCO Results Summary

3.2 Current Mode Latch Divider

Injection-locked frequency dividers are a very good choice for the first divider of the divider chain of this project due to their acceptable phase noise, locking range, and power consumption. They do, however, consume a large chip area due to the tank inductor. In this design, the current mode latch divider was evaluated as the first divider stage due to its low power consumption, chip area consumption, and phase noise performance.

A robust divider was targeted so that, throughout the VCO's signal swing and frequency range, a divided signal would be obtained. At the same time minimal power should be consumed, so as not to waste power. The latching circuitry has its current limited by the switching transistors instead of the current source since the current source is shared by the tracking and latching circuitry. The circuit was designed so that the current mode latch has a large enough signal swing for robust operation over the frequency range and so that the output buffers can reliably recover the signal with a rail-to-rail output for the downstream divider inputs.

Sufficient current was needed to be present to charge the parasitic capacitances throughout the operating frequency and a large enough voltage drop needed to be obtained to generously meet input voltage requirements for downstream circuitry. As the load resistors become smaller in resistance, the track and hold pairs need to become larger in width to keep a high signal swing- but not too large so that they contribute too much parasitic capacitance.

The finalized current mode latch configured in divide-by-two is shown in Fig. 3.2.1.

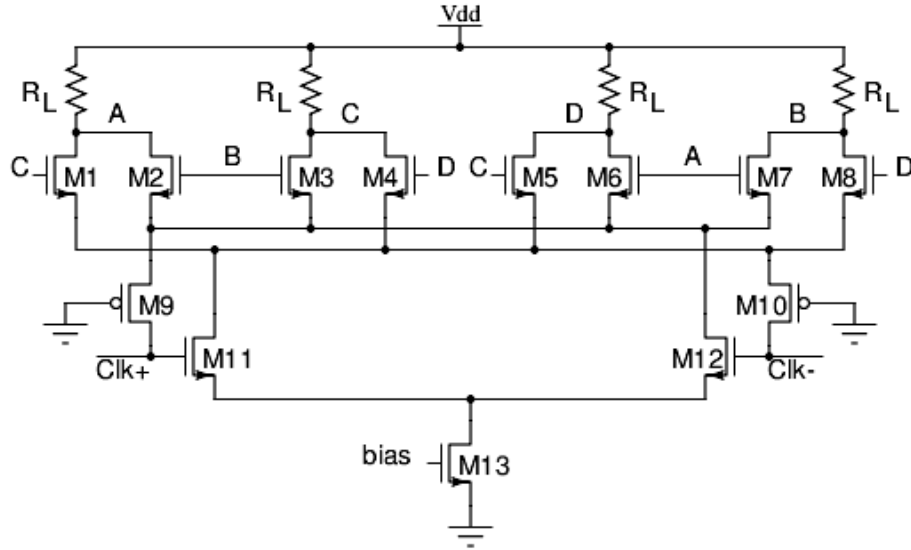


Fig. 3.2.1: CML Latch in divide-by-two configuration

As a starting point, the voltage swing was designed using the equation in (3.2.1). Assuming each branch uses the same current, using a target voltage swing of roughly 600 mV (from 300 mV to 900 mV), and a targeted total current of roughly 550 μ A, the load resistor should be about 6.5 K Ω .

$$V_{out_{min}} = V_{DD} - (I_{on} * R_L)$$

Equation 3.2.1: Minimum output voltage

The hold branch does not require as much current as the tracking branch so the transistors (M2, M3, M6, and M7) were sized $\frac{3}{4}$ as much as the tracking branch transistors (M1, M4, M5, and M8). After optimizations, a load resistance, R_L , of 5K Ω was chosen for larger operating frequencies. Transistors M9 and M10 neutralize clock feed-through, as discussed in section 2.7.4.

The biasing circuitry is shown in Fig. 3.2.2. An RC filter is used to filter out noise leading to the gate of the tail current source.

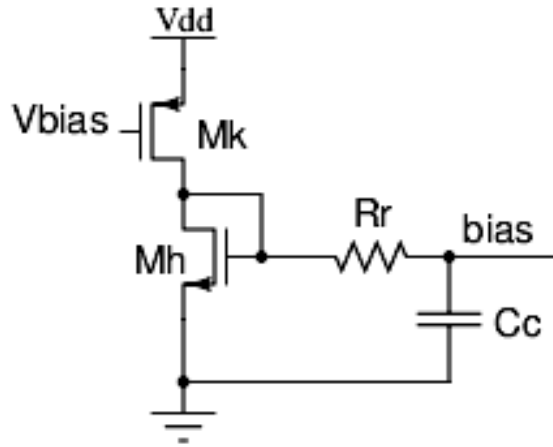


Fig. 3.2.2: Bias circuitry

Transistor sizes are given in table 3.4.

Component	Size (W/ L) (um)
M1, M4, M5, M8	1.2 / 0.06
M2, M3, M6, M7	0.8 / 0.06
M9, M10	0.135 / 0.180
M11, M12	2 / 0.06
M13	4 / 0.06
Mk	2.1 / 0.25
Mh	0.405 / 0.240
R_L	5 K Ω

Table 3.4: CML divider transistor sizes

Fig. 3.2.3 shows that the CML latch has excellent phase noise characteristics over the input frequency range. It is also important for the CML latch to work over a wide range of input powers. Fig. 3.2.4 shows operation at -25 dBm input. The current consumption at an input frequency of 31.5 GHz is also shown as the input power varies from 0 to -25 dBm. In particular, between 566 uA to 584 uA are consumed over the input power range.

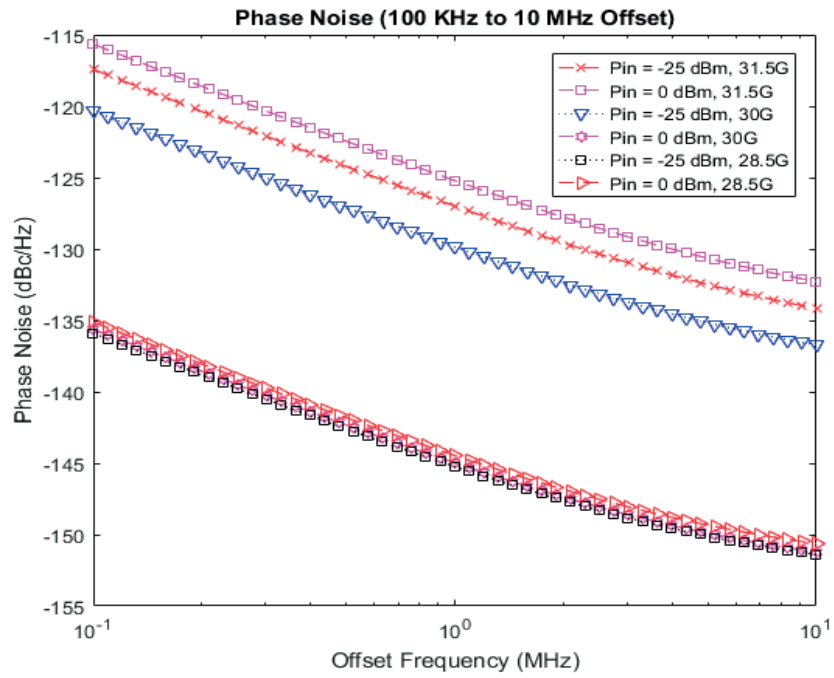


Fig. 3.2.3: CML latch phase noise

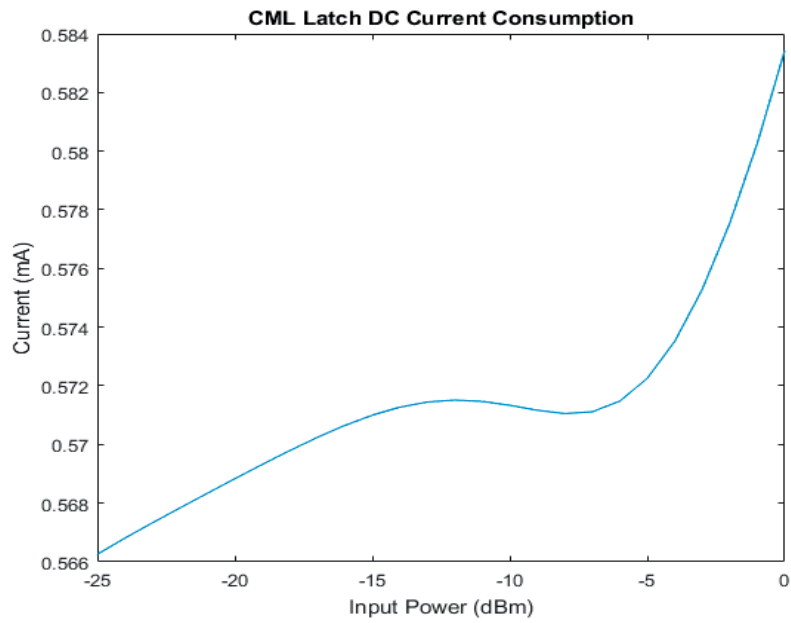


Fig. 3.2.4: CML latch current consumption

Table 3.5 summarizes the CML latch results.

Specification	Result
DC Current Consumption	566 uA to 583 uA
Output Voltage Swing	602.1 mV
Frequency Range	At least 28.5 GHz to 31.5 GHz
Phase Noise ($P_{IN} = 0$ dBm)	-135.1 dBc/Hz to -151.4 dBc/Hz

Table 3.5: CML divider results

3.3 Injection-Locked Frequency Divider

An injection locked frequency divider was explored to be the first divider in the divider chain due to its low phase noise, acceptable locking range, and relatively low power consumption at the operating frequency required. The choice comes at the cost of, primarily, a large chip area due to the large tank inductor. The injection-locked frequency divider operates similarly to the LC-type VCO, however, the input is differentially directly injected into the tank nodes. Thanks to the resonant components, some energy is re-circulated instead of thrown away each cycle compared to conventional flip-flop divider circuits.

In designing the injection locked frequency divider, a differential direct injection topology was used to enhance the locking range. The tank was intentionally de-Q'd for a larger locking range as well. A free-running frequency of roughly 15 GHz is desired while, when utilizing the binary weighted capacitors and tuning varactor, the free-running frequency should be able to be tuned from 14.25 GHz to 15.75 GHz. The designed injection-locked frequency divider is shown in Fig. 3.3.1.

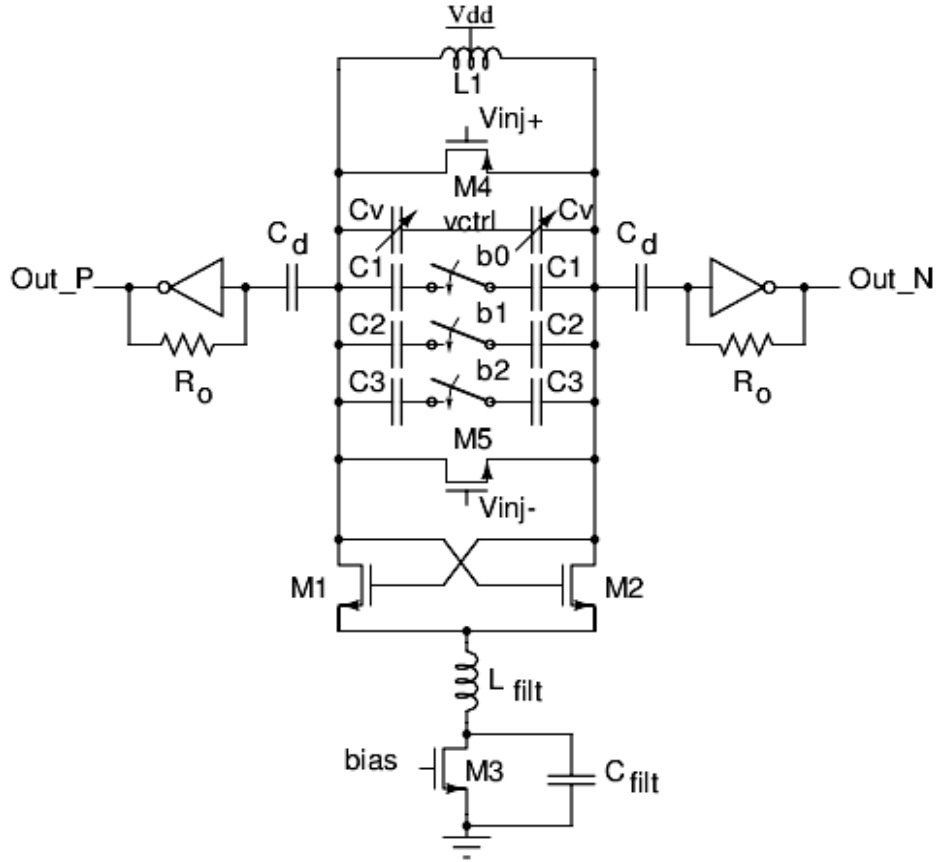


Fig. 3.3.1: Designed injection-locked frequency divider

An inductor value of 2.27 nH was selected and a Q-factor of 3 was used to realize a series tank resistance of roughly 71 Ω and a parallel resistance of 713 Ω . For a tank voltage of 1.2 volts, a bias current of about 1.9 mA would be necessary, corresponding to a DC power consumption of 2.2 mW. The necessary g_m for oscillation conditions to be met is 1.4 mS, and at least a g_m of 2.8 mS should be used for operation over process variation, voltage, and temperature variations.

To save in power consumption, a larger inductor can be used and the tank capacitance can be reduced. A complementary architecture could have been used for less current consumption with similar, but higher, phase noise. Additionally, a higher Q-factor can be used if the degradation of the tuning range still meets specifications. Additionally, a class C topology could be chosen to increase efficiency by upwards of 36%[25].

Capacitors C1, C2, and C3 are switched capacitors to reduce the size of the varactor needed for the tuning range. C1, C2, and C3 were chosen to be 1.6 fF, 3.1 fF, and 6.1 fF, respectively. These values were chosen using only transient analysis to match the tuning range with that of the VCO's tuning range, but at half of the frequency. More accuracy could be achieved using the PSS analysis.

Similar design strategies are implemented, as in the VCO, where tail filtering, a switching mechanism for discrete tuning capacitors, and self-biased inverters for output buffering were used. Circuit components and sizes are shown in table 3.6.

Component	Size (W/L) (μm) unless specified
M1, M2	3.848 / 0.12
M3	6.75 / 0.06
M4	0.42 / 0.06
M5	0.3 / 0.06
M _{varactor} (not shown)	33 / 0.06
C1	1.6 fF
C2	3.1 fF
C3	6.1 fF
C _d	5 fF
R _o	30 K Ω
L1	2.27 nH

Table 3.6: ILFD component sizes

The injection-locked frequency divider's transient outputs are plotted in Fig. 3.3.2 using both the VCO's buffered output and an ideal sinusoid as inputs as inputs.

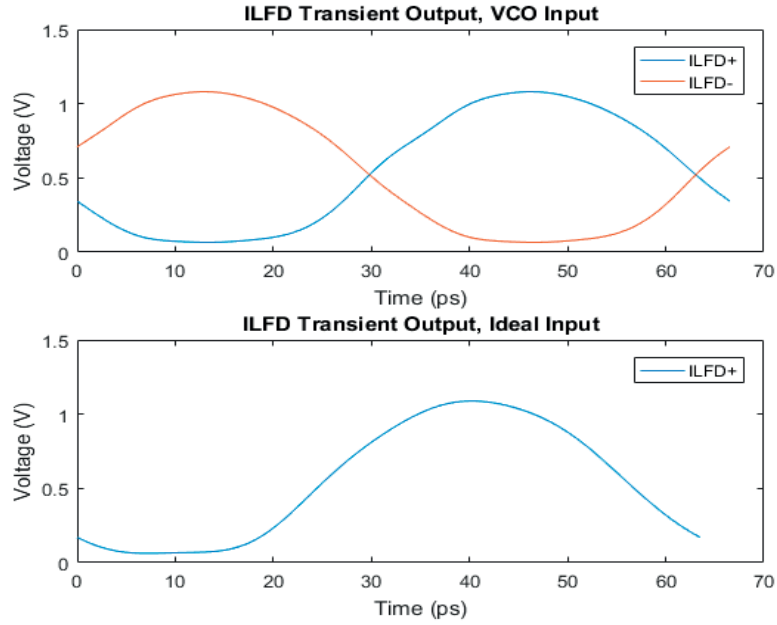


Fig. 3.3.2: ILFD Transient Outputs w. VCO (top) and Ideal (bottom) inputs

The plot in Fig. 3.3.3 shows a DC current consumption of 2.63 mA, 2.56 mA, and 2.52 mA for the operating frequencies of 28.5 GHz, 30 GHz, and 31.5 GHz, respectively. By comparing the phase noise and the steady state DC current consumption of the injection-locked frequency divider and the CML latch, some insight into what to use as the first stage of the divider for the system can be found. The phase noise of the injection-locked frequency divider can be seen in Fig. 3.3.4. It is obvious that the phase noise of the injection-locked frequency divider strongly follows that of the input signal. The tuning range of the injection locked frequency divider was proven using transient and periodic steady-state analysis. The periodic steady-state analysis signal amplitude versus frequency plot is shown in Fig. 3.3.5. The injection locked frequency divider outputs a strong signal over the tuning range, which can serve as proof that the injection-locked frequency divider can track and divide the input signal from 28.5 GHz to 31.5 GHz.

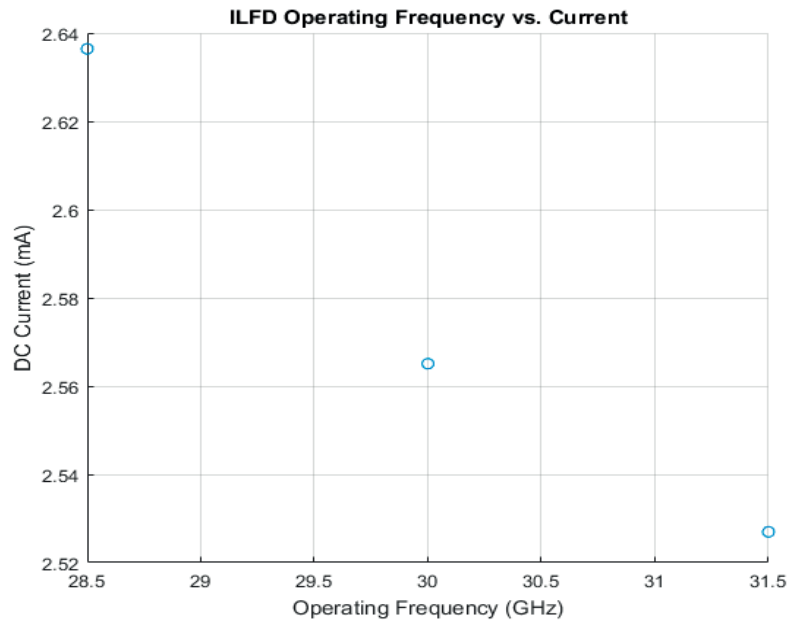


Fig. 3.3.3: ILFD DC current consumption

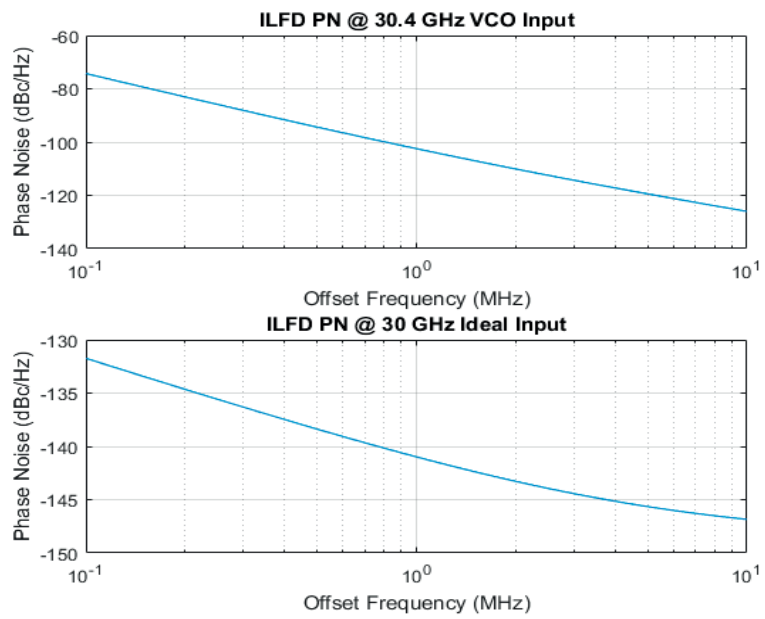


Fig. 3.3.4: Phase noise of ILFD with VCO (top) and Ideal (bottom) inputs

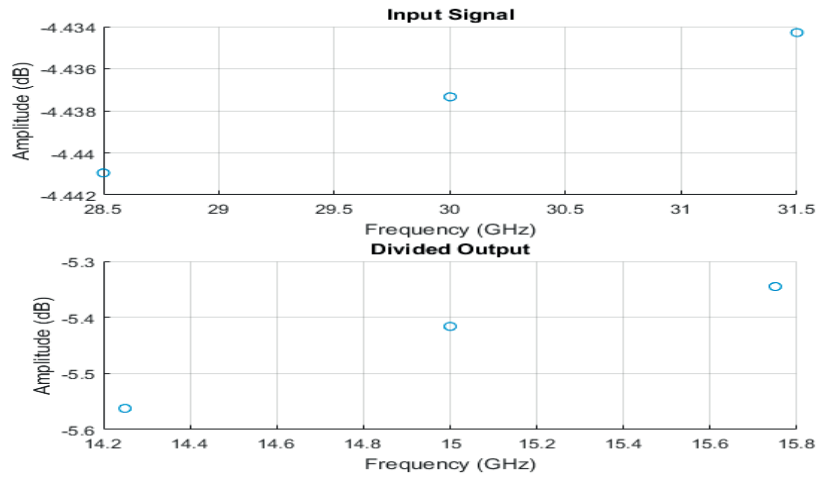


Fig. 3.3.5: Amplitude vs Frequency of ILFD outputs and inputs

In a comparison between power consumption, phase noise, area consumption, frequency range, and complexity, the current mode latch was chosen to be the first stage divider of the PLL.

3.4 D-flip Flop Dividers

The digital dividers are easy to implement and result in a nicely divided rail-to-rail signal. The output of the current mode latch has a maximum frequency of 15.75 GHz and if a digital divider is going to be used, it must be able to operate up to that frequency. The technology minimum-sized standard cells were used in implementing the digital dividers. In deciding the next dividers to use after the first stage, a phase noise and current versus operating frequency comparison was completed. The results are shown in Fig. 3.4.1 and Fig. 3.4.2.

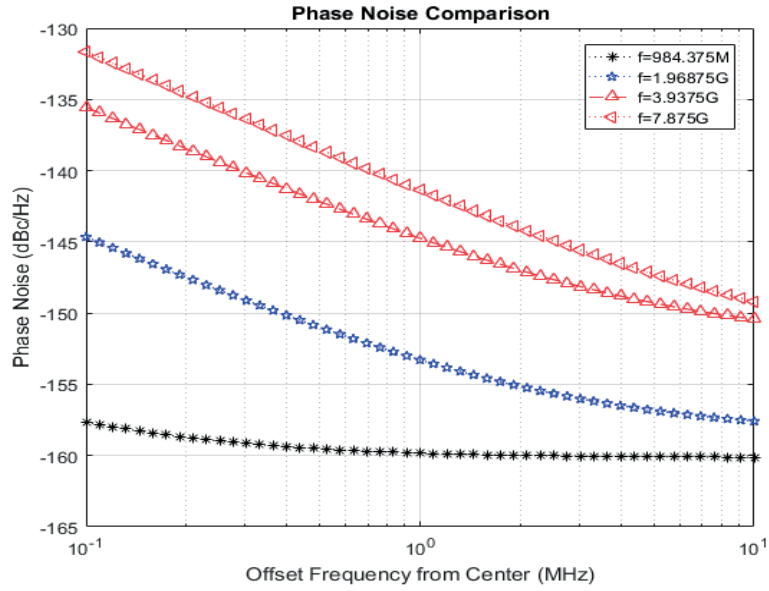


Fig. 3.4.1: DFF phase noise comparison

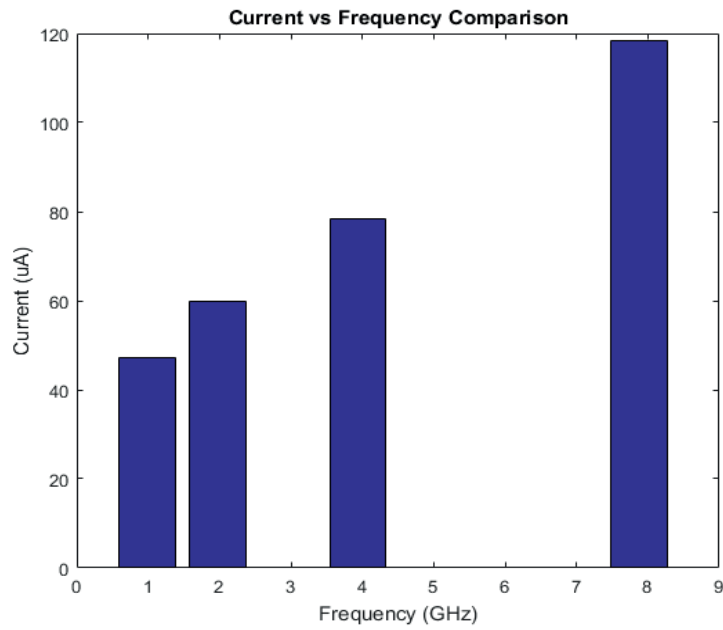


Fig. 3.4.2: Comparison of DFF current vs frequency

The D-flip flop divider presents an excellent phase noise at a current consumption much less than the current-mode latch divider. Due to the relatively low current consumption over the required frequency range the d-

flip flop works as a frequency divider for the remaining stages of the divider.

The divide-by-8 circuit is shown in Fig. 3.4.3.

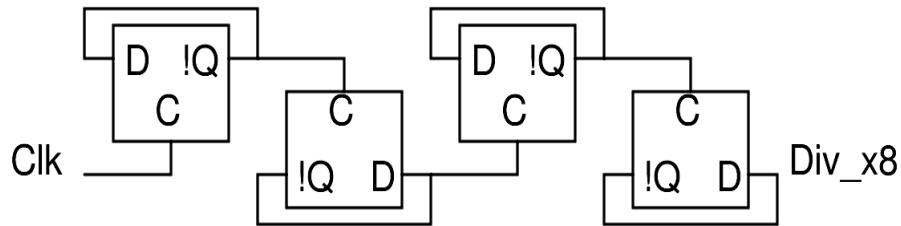


Fig. 3.4.3: Divide by 8 circuitry

3.5 Phase-Frequency Detector

In this design, the UP signal will increase the frequency and the DN signal will decrease the frequency. When the reference signal goes high, the phase-frequency detector's UP signal must go active. Similarly, when the feedback signal goes high, the phase-frequency detector's DN signal must go active. When both the UP and DN signals are high, the reset signal will go active and put the UP and DN signals in their reset state.

The phase-frequency detector was designed using slightly modified minimum-size standard cells so that the outputs, while in reset, are correct for the operation as described. Specifically, the circuitry was implemented using two inverted output D-flip flops with a reset input and a NAND gate with one inverted input. The phase-frequency detector schematic is described in Fig. 3.5.1.

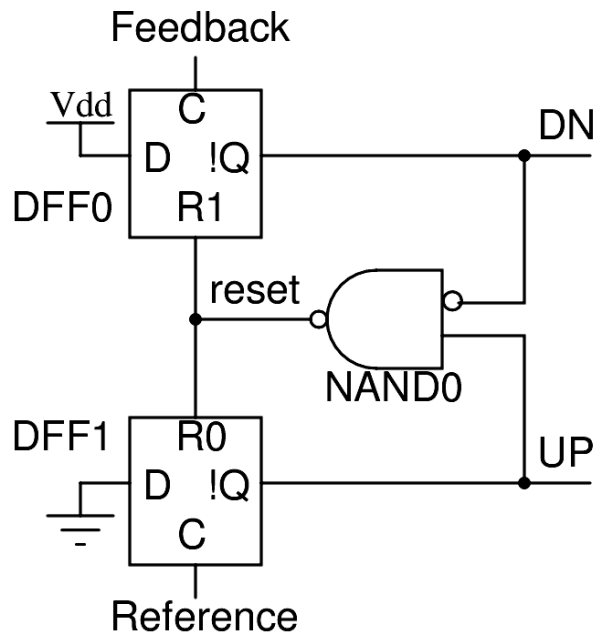


Fig. 3.5.1: PFD Implementation

The PLL must maintain negative feedback to work properly. The VCO uses P-type MOSFETS for varactors and, as such, the frequency decreases as the control voltage increases. Thus, the charge pump's PMOS path will increase the control voltage and decrease the VCO frequency. To turn the PMOS off (reset state), a logic '1' should be applied to the PMOS gate. Similarly the NMOS gate, in reset state, should have a logic '0' applied. When 'reset' is logic '0', the D-flip flops will be placed in the reset state.

The timing diagram from a transient simulation of the phase-frequency detector is shown in Fig. 3.5.2 and Fig. 3.5.3 while summarized in table 3.7.

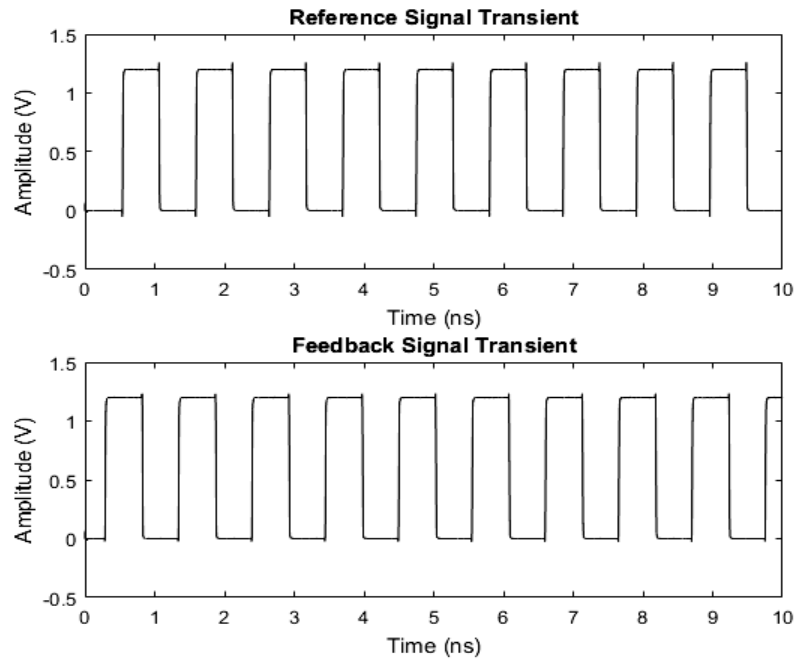


Fig. 3.5.2: PFD REF and DIV signals

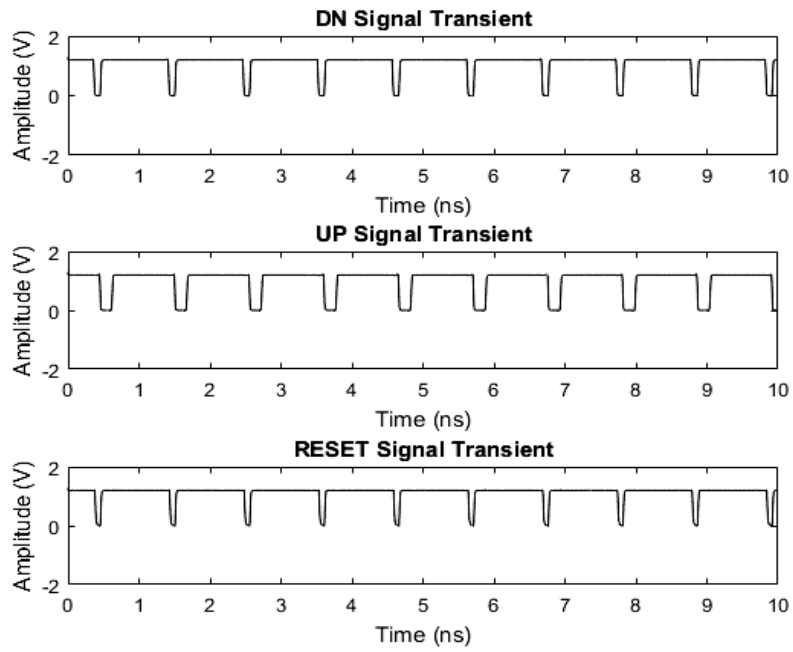


Fig. 3.5.3: PFD UP, DN, and RESET signals

Signal	Timing (ps)
$T_{D-Q, DFF0}$	75
$T_{D-Q, DFF1}$	80
$T_{D-Q, NAND0}$	20
T_{reset}	75
$T_{fall, DFF(80\%-20\%)}$	11
$T_{rise, DFF(20\%-80\%)}$	10

Table 3.7: PFD timing table

The approximate blind zone time was found using (2.3.1.1) and resulted in a value of 195 ps. The max phase error detection range is calculated using (2.3.1.2) and has a worst case result of 3.84π .

3.6 Charge-Pump and Loop Filter

The charge pump design features cascoded transistors for minimizing leakage and has two external bias voltages- one for the PMOS and one for the NMOS transistors. Circuitry was added for 7-bit phase tuning. The charge pump schematic is shown in Fig. 3.6.1.

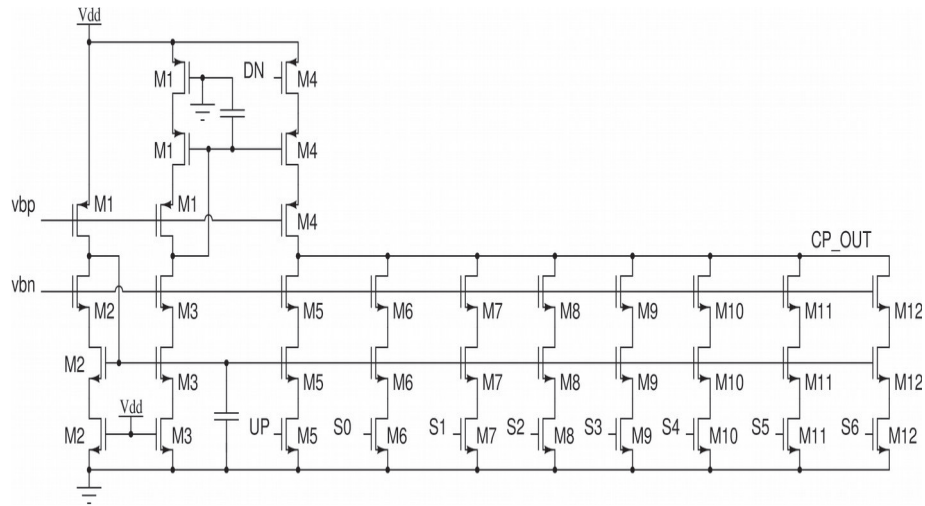


Fig. 3.6.1: Charge pump schematic

The transistors in cascode with the DN and UP transistors provide a larger output impedance as well as to reduce clock feed-through to the output of the charge pump. Transistors M6 to M12 provide a 7-bit tunable phase

offset, which will be used to compensate for phase offsets due to clock routing in the phased-array. Transistors M1, M2, and M3 provide current mirroring. To minimize mismatch, transistors M4 and M5 were sized so that the up and down drain currents are equal to each other. Transistors M6 to M12 were sized so that their current contribution is obtains steps in 6 degrees of phase offset for each digital word increase. Additionally, the lengths of the transistors meeting CP_OUT are increased to minimize leakage. The total leakage was simulated to be roughly 618 pA and was found by accumulating the current from transistors M5 to M12 while in the ‘off’ state. The total injection current is 1 mA, while the phase tuning transistors have their drain currents scaled for 6 degree phase offsets according to (3.6.1). Here, N is 32- the division ratio, I_{Δ} is the excess current needed to be injected to obtain a phase shift of $\Delta\Phi$, and I_{injected} is the injected current I_{UP} and I_{DN} .

$$\Delta\phi = \frac{N * 360 * I_{\Delta}}{I_{\text{injected}}}$$

Equation 3.6.1: Phase offset equation

The loop filter schematic is a 3rd order passive loop filter and the schematic is shown in Fig. 2.5.1. In designing the loop filter, a phase margin of 45 degrees was targeted. The filter values are shown in table 3.8.

Component	Value
R_0	15.873 K Ω
C_0	4.4238 fF
R_x	4.68 K Ω
C_x	680.589 fF
C_A	680.589 fF

Table 3.8: Loop filter component values

3.7 Design Bottlenecks

It is known that, as the operating frequency of an LC-type VCO increases, a phase noise penalty results, as the quality factor of inductors and varactors do not scale with frequency, which is attributed to substrate losses. There comes a trade-off between frequency, tuning range, power dissipation, and phase noise[37]. To compound the problem, the 16-QAM signaling required for high spectral efficiency requires a high carrier-to-noise ratio[38]. With respect to the area and power consumption of the PLL, it is better to use direct-conversion techniques[37]. Thus, the VCO itself (and

first stages of high frequency division) pose the most difficulties in achieving a PLL operating at high frequencies, when using a direct-conversion architecture. As the tuning range is increased, the tank Q-factor degrades, thus making it more difficult to design a spectrally pure PLL with a wide tuning range.

CHAPTER 6

4 Results

The PLL was simulated in a test-bench with a non-ideal reference clock designed as an LC-type VCO with an output frequency of roughly 946 MHz and a phase noise of roughly -130 dBc/Hz at a 1 MHz offset. Ideal voltage sources were used for biasing and supply voltages. The system test bench block diagram is shown in Fig. 4.1 below.

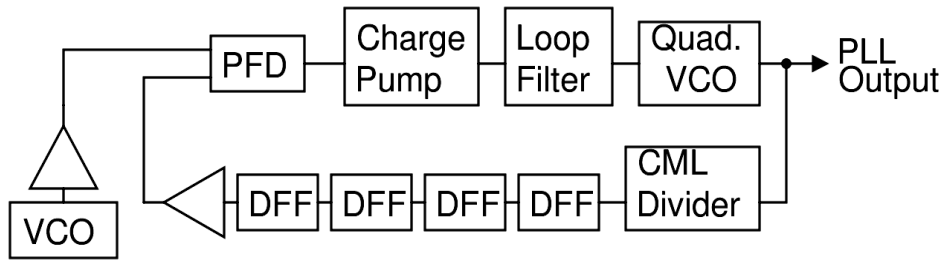


Fig. 4.1: System test bench / block diagram

Fig. 4.2 shows the steady state phase noise spectrum of the PLL output. Phase noise results of -90 dBc/Hz, -101.1 dBc/Hz, and -120.2 dBc/Hz can be seen at a 100 kHz, 1 MHz, and 10 MHz offset from the carrier, respectively. Fig. 4.3 shows the DC current consumption of each block in the system with an output frequency around 30.2 GHz. It is obvious that the QVCO consumes the most current followed by the dividers and buffers. The buffer current is an accumulation of all of the buffers used throughout the circuit. Table 4.1 shows the consumption values of each block along with the total current consumption and power dissipation.

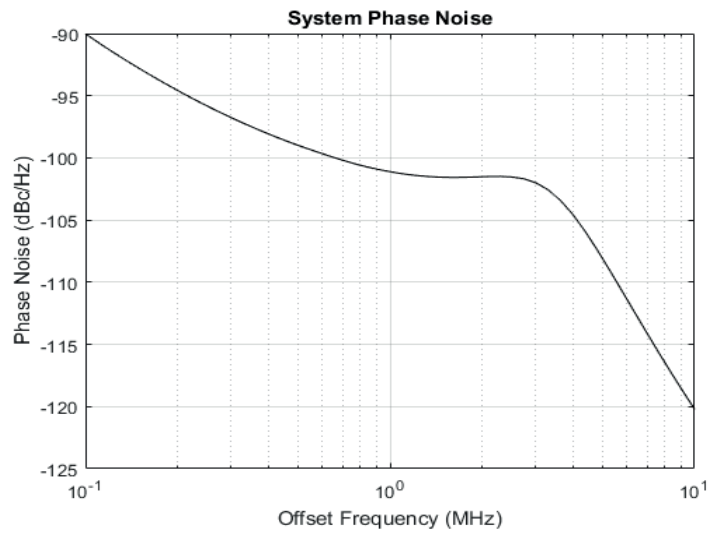


Fig. 4.2: PLL phase noise spectrum

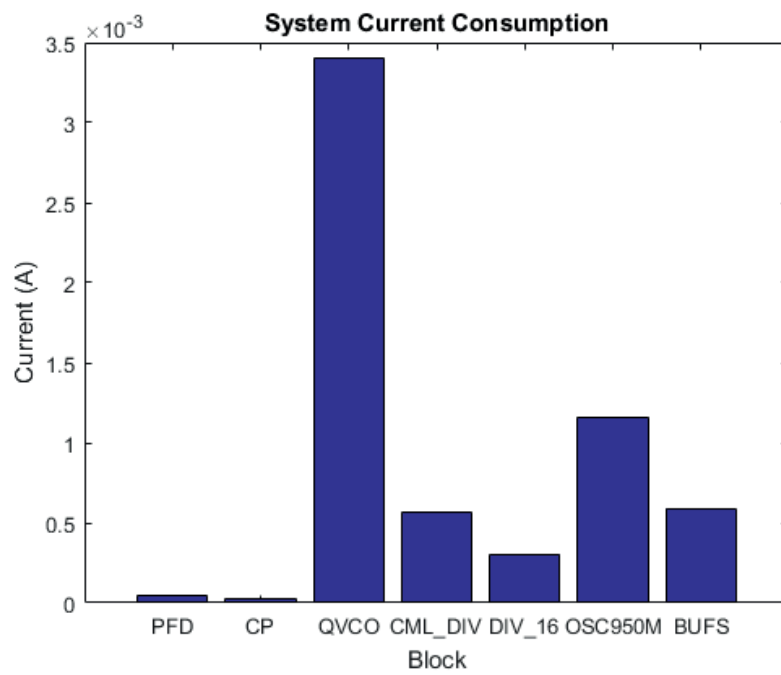


Fig. 4.3: PLL current consumption

Block	Consumption (At 30.2 GHz output)
Phase-Frequency Detector	47.2 μ A
Charge Pump	30.2 μ A
Quadrature VCO	3.4 mA
CML Divider	566.3 μ A
Divide-By-16 Chain	303.9 μ A
Buffers	588.5 μ A
Total	4.93 mA (5.92 mW)

Table 4.1: PLL current consumption

The output spectrum of the QVCO is shown in Fig. 4.4. Here, the fundamental is located at 30.27 GHz with an amplitude of -2.2 dB. Some cycles of the quadrature output are shown in Fig. 4.5.

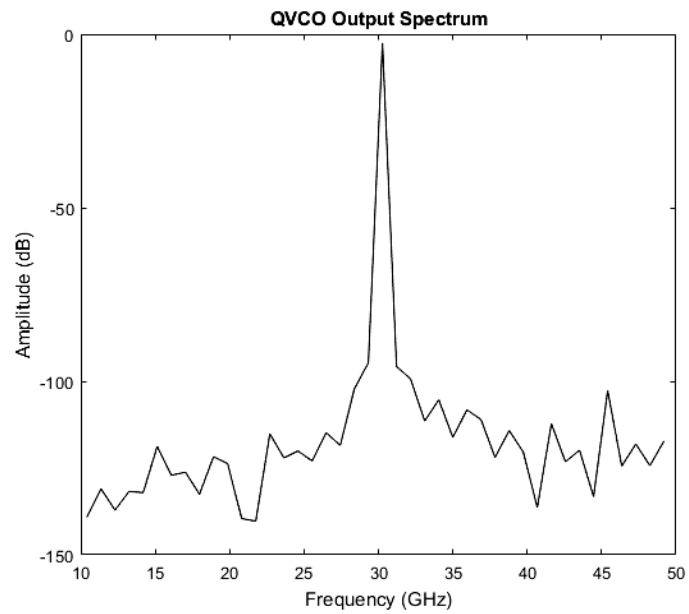


Fig. 4.4: QVCO output, system simulation

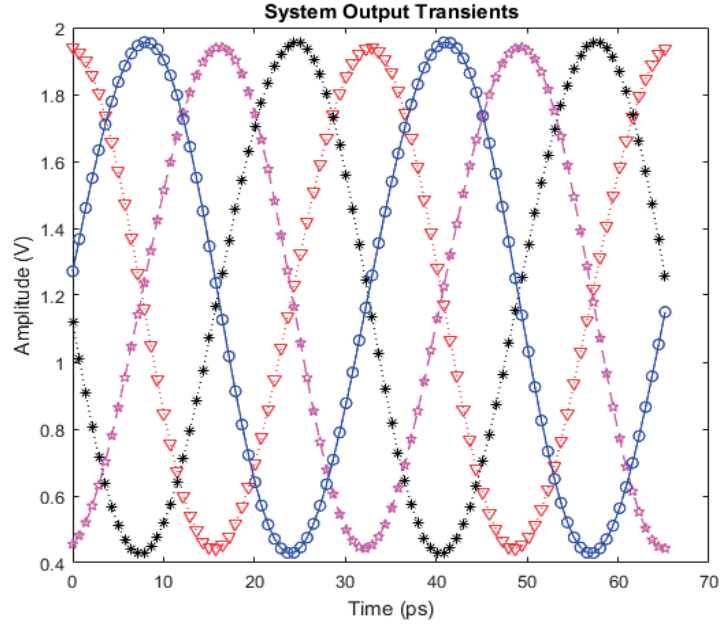


Fig. 4.5: QVCO transient, system simulation

The system response during start-up and a frequency step is shown in Fig. 4.6. Here, the reference frequency, at start-up, is 943 MHz and the frequency of the divided signal crosses the reference frequency around 500 ns. After 714 ns, the divided signal frequency stays within 0.05% of the reference frequency. After 2.5 μ s, the reference frequency changes to 956 MHz. The divided PLL output crosses the reference frequency around 700 ns after the frequency step (at 3.29 μ s). The divided signal stays within 0.05% of the reference frequency after 3.22 μ s, thus, it takes 720 ns to reach this point. The last cycle skip occurs at 2.98 μ s, which is roughly 480 ns after the frequency step.

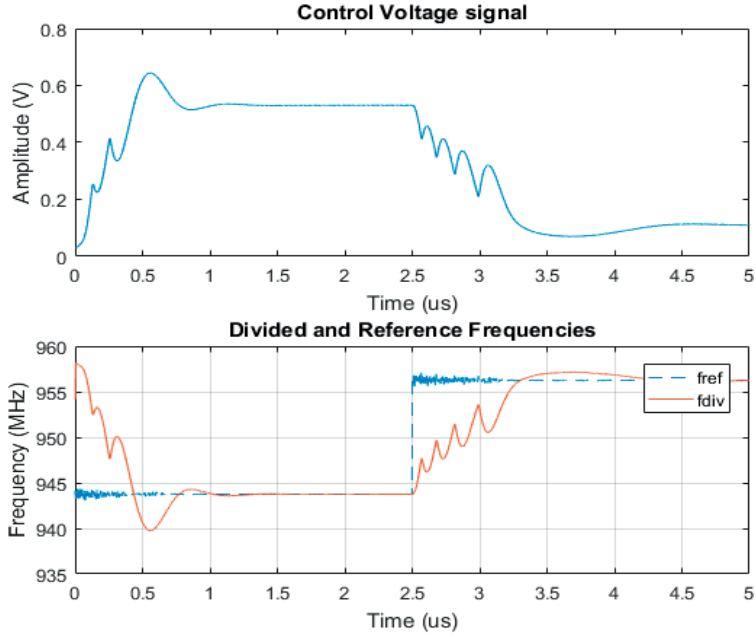


Fig. 4.6: System transients

The system was verified so that a lock will be obtained over the tuning range by running transient simulations from the minimum to maximum frequencies of the system. Due to long simulations creating a file which is too large, the simulation could not be done continuously and thus needed to be broken up over each frequency band. Seven simulations were completed and the transient results were concatenated together and time shifted accordingly. This result can be found in Fig. 4.7, where the reference and divided signal frequencies are shown on top of each other. Through this plot, we can assert that the performance is maintained throughout the tuning range.

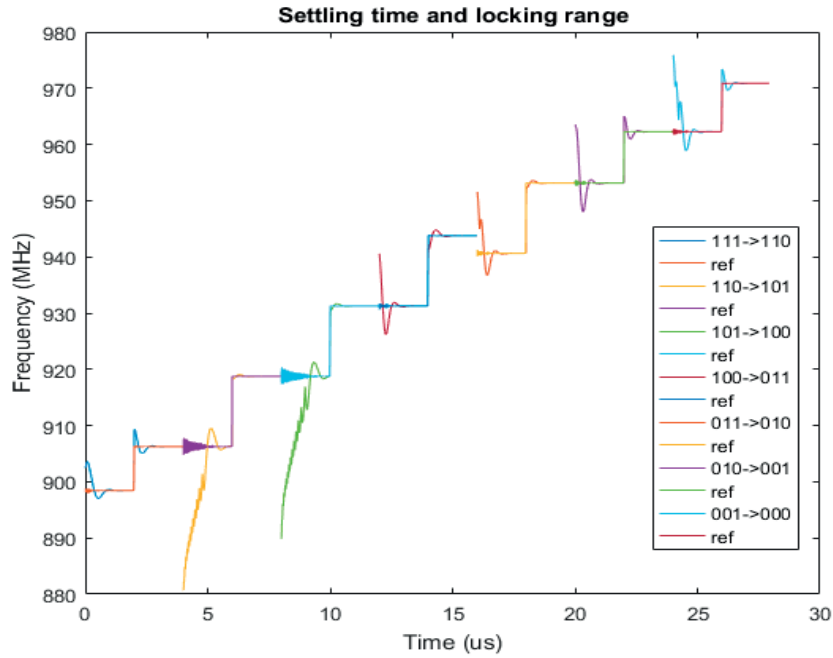


Fig. 4.7: Obtaining a lock throughout the tuning range

The system loop gain and phase are shown in Fig. 4.8. A phase margin of roughly 35 degrees was obtained. This value is lower than what was targeted, however, the loop filter can be altered to improve phase margin as well as optimize the loop bandwidth. The crossover frequency is found in the figure and has a value of roughly 1.84 MHz. The loop bandwidth has an influence on the overall phase noise depending on the phase noise of the input clock. The input clock has a better phase noise than the QVCO. Knowing this, the loop filter can be tweaked more to obtain a higher loop bandwidth such that the low phase noise of the reference clock is taken advantage of at frequencies close to the carrier. However, care is taken so that the noise attributed to the PLL output by the input clock is minimized.

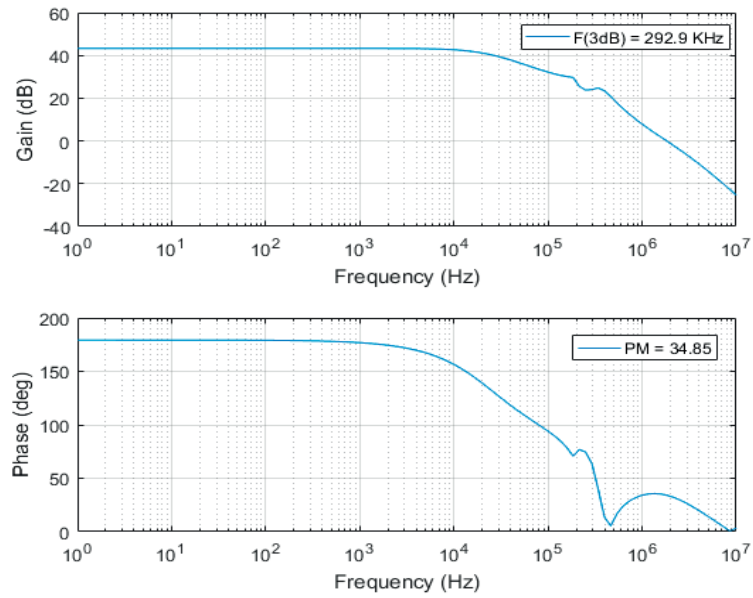


Fig. 4.8: System loop gain and phase

The system has a tunable phase thanks to an addition of the charge pump circuitry. The range of this tunable phase is shown in Fig. 4.9.

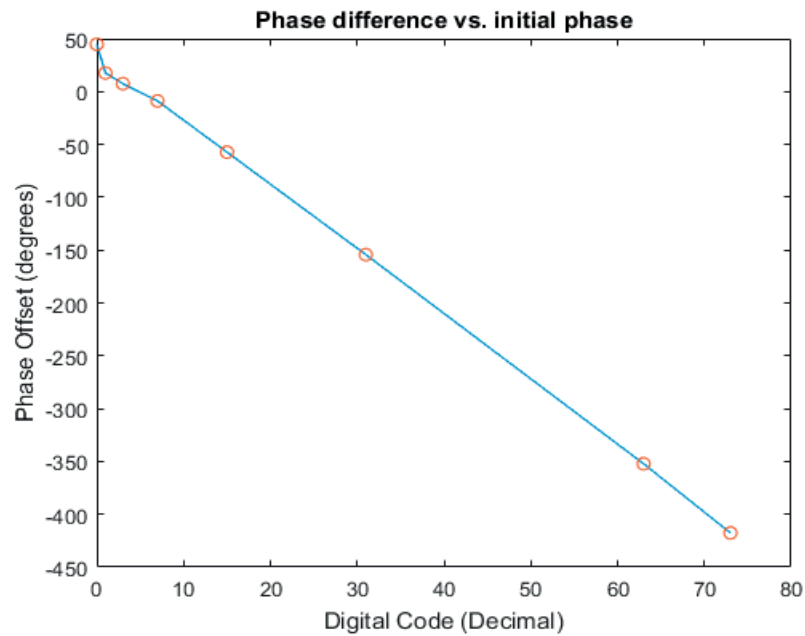


Fig. 4.9. Phase tuning range

The minimum step phase tuning step observed was 10 degrees. Table 4.2 shows the results from similar PLLs some kind of comparison can be made on the performance of this PLL and others.

Reference	Reference Frequency	Operating Range (GHz)	Phase Noise (dBc/Hz)	Power (mW)
[39]	125 MHz	28.5 to 32	-82 @ 600 kHz	287.5
[40]	125 MHz	21 to 32	-91 @ 1 MHz	30
[41]	100 MHz	21 to 48	-108 @ 1 MHz	148
[42]	194.4 MHz	23.8 to 30.2	-86 @ 1 MHz	31
[43]	-	20.1 to 26.7	-126.5 @ 10 MHz	33
[44]	-	16.45 to 30.55	-124.2 @ 10 MHz	27.2
This Work	943.7 MHz	28.5 to 31.5	-101.1 @ 1 MHz	6

Table 4.2: Results from similar PLLs

Parameter	Result
DC current consumption	4.9 mA
Power consumption	6 mW
Operating frequency	30.2 GHz
Tuning range	10 %
PLL Phase noise:	
At 100 kHz	-90 dBc/Hz
At 1 MHz	-101.1 dBc/Hz
At 10 MHz	-120.2 dBc/Hz
PLL quadrature phase error	0.726 degrees
Settling time	700 ns
Loop bandwidth	300 kHz
Phase tuning range	417 degrees

Table 4.3: PLL system results summarized

CHAPTER 7

5 Conclusions

A look into the application of a PLL for frequency synthesis in phased arrays was presented. Various architectures of each block were analyzed for use in the final phase-lock loop design. A system block diagram, models, and calculations for the blocks are presented and analyzed for a good understanding of their operation. Verilog-A modules and MATLAB code were used to model the operation of each block and come to a better understanding of how they operate. Finally, a 30 GHz PLL was designed and simulated using Cadence Virtuoso tools to illustrate the performance of each block while mathematical equations for each block in the system, design trade-offs, and architectures were analyzed for the best performance. A tuning range specification of 10% and 417 degrees of phase tuning capability with 10 degree resolution were added to the design to account for process, voltage, and temperature variations as well as mismatch due to routing and LO beamforming capability. A top-series QVCO, injection-locked frequency divider, current-mode latch, divide-by-8 circuit, phase-frequency divider, charge pump, loop filter, and buffers were all designed and their performance results are presented. Additionally, design bottlenecks in achieving a PLL that can operate at a higher frequency are discussed. Finally, the individual and system results were presented and briefly discussed.

The project was a success since the PC-PLL has a good phase noise, an exceptionally low power consumption, decent phase tuning resolution, and meets the 360 degree phase tuning range required by a PLL for use in LO beamforming applications. The phase tuning resolution can be increased easily by either adding more bits to the phase tuning circuitry in the charge pump or by decreasing the minimum phase step and taking a penalty in the total phase tuning range. While spending a long time on QVCO optimizations, a deep understanding of the QVCO circuitry and noise was obtained. This allowed for an intuitive understanding of the effects of increasing the PLL frequency. The low power consumption can be attributed to the low-power 65 nm CMOS technology, low PLL tuning range, low power CML divider, and high reference clock frequency.

Otherwise, the power consumption would be increased due to the need for higher power consumption in the feedback path for frequency division. The quadrature phase error result personally impressive thanks to the SQVCO topology. It should be noted that, by not increasing the tuning range of the QVCO further than 10%, excessive phase noise degradation was avoided.

Some issues were faced in the simulation of the complete PLL, since it is hard to obtain a convergence for the PLL in a periodic steady state analysis (PSS). For instance, simulating the phase tuning range of the closed loop circuit in a PSS simulation was difficult since convergence is needed for every digital code. One non-convergence would cause the entire simulation to fail. Each PSS simulation took around 6 hours to run. To compound the issue, in finding the phase tuning range for each of the seven bits (assuming no convergence issues), a total of 128 simulations would need to be ran, or roughly 33 days. To work around convergence issues in the PSS simulation, a transient analysis was ran while each bit of the phase tuning code was flipped from low to high. This way, 7 coarse tuning steps were able to be recorded in just 6 hours.

The system phase noise is partially dependent upon the reference phase noise and, as such, the loop filter is as well. The reference signal and its phase noise was arbitrarily generated. The loop filter can be optimized for a given reference PPSD to optimize the system phase noise. Additionally, an AGC circuit can be used to help optimize the QVCO over the complete tuning range. Specifically, the FoM of the QVCO could be made more flat over the frequency range. Other techniques, such as a class-C QVCO or using transformers, can be implemented to improve the efficiency of the QVCO.

The knowledge obtained from designing the PC-PLL and its components can be useful in many aspects, such as telecommunications, frequency synthesis, clock recovery, modulation and demodulation, and frequency multiplication and division. Knowledge of designing charge pumps can be applied in level shifting, LCD or LED drivers, memories and processors, and more. Voltage-controlled oscillators are a necessity to modern circuits, and knowledge of them can be applied in many applications.

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Appendix 1

Extended Material

A.1 Voltage-Controlled Oscillator VerilogA Model

```
`include "constants.vams"
`include "disciplines.vams"

module VCO_VLA(vin, vp, vn);
input vin;
output vp, vn;
electrical vin, vp, vn;
parameter real amp = 0.6;
parameter real center_freq = 16.05G;
parameter real vco_gain = -1.5G;
parameter integer steps_per_period = 32;

real phase;
real inst_freq;
integer resetph;

analog
begin
    inst_freq = center_freq + vco_gain * V(vin);
    $bound_step (1.0 / (steps_per_period*inst_freq));
    phase = idtmod(inst_freq,0,1,0);
    V(vp) <+ 0.6+amp * sin (2 * `M_PI * phase);
    V(vn) <+ 0.6+amp * -sin (2 * `M_PI * phase);
end
endmodule
```

A.2 Phase-Frequency VerilogA Model

```
`include "constants.vams"
`include "disciplines.vams"

module PFD_VLA(vdd,gnd,clkr, clkd, up, dn, rst);
inout clkr, clkd, up, dn, vdd, gnd, rst;
electrical clkr, clkd, up,dn, vdd,gnd, rst;

parameter real trise = 10e-12 ;
parameter real tdel = 75e-12 ;
parameter real tfall = 10e-12 ;
parameter real vth = 600m;

integer up1, dn1, rst1;

analog begin
  @(initial_step)
  begin
    dn1 = 1;
    up1 = 0;
    rst1 = 1;
  end

  if (up1 == 1 && dn1 == 0)
  begin
    rst1 = 0;
  end

  @(cross(V(rst) - vth, -1))
  begin
    rst1 = 1;
    dn1 = 1;
    up1 = 0;
  end

  @(cross(V(clkr) - vth, +1))
  begin
    up1 = 1;
  end
end
```

```

@(cross(V(clkd) - vth, +1))
begin
    dn1 = 0;
end

V(rst) <+ transition(V(vdd)*rst1, 20e-12, trise, tfall);
V(dn) <+ transition(V(vdd)*dn1, tdel, trise, tfall);
V(up) <+ transition(V(vdd)*up1, tdel, trise, tfall);

end

endmodule

```

A.3 D-Flip Flop VerilogA Model

```
`include "constants.vams"
`include "disciplines.vams"

module DFF_VLA(q, qbar, clk, d);
  input clk,d;
  output q,qbar;
  voltage q, qbar, clk, d;
  parameter real tdel  = 5p from [0:inf),
               trise = 5p from [0:inf),
               tfall = 5p from [0:inf),
               vdd = 1.2, from [0:inf),
               vgnd = 0;

  real vth;
  integer x;

  analog
  begin
    vth = vdd/2;
    @(initial_step) x = 0;

    @(cross(V(clk) - vth, +1 ))
    begin
      x = (V(d) > vth);
    end

    V(q)  <+ transition( vdd*x + vgnd*!x, tdel, trise, tfall );
    V(qbar) <+ transition( vdd*!x + vgnd*x, tdel, trise, tfall );
  end

endmodule
```




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