Vertical Heterostructure III-V Nanowire MOSFETs

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If cars had developed as fast as processors they would go at 470,000 mph, get 100,000 miles to the gallon, and cost 3 cents” claims Paul Ottelini, Intel CEO 2005-2013. This serves as a reminder of how fast the field of nanoelectronics is developing due to constant demand for faster and more energy efficient integrated circuits. The still ongoing electronics revolution was accelerated by the innovation of one simple and elegant device, namely the Si-based metal-oxide-semiconductor-field-effect-transistor MOSFET in 1959. The pillar of economic growth has since been based on downscaling the MOSFET and increasing the density of transistor per chip area. Downscaling of the transistor has favourably led to more efficient and faster devices. MOSFETs today are approaching sizes which only include few monolayers of atoms, basically dimensions of a few nanometer. Conventional electronics has thus been pushed into the quantum realm forcing future improvements to be based on innovation rather than simply downscaling. To win the battle against Heisenberg’s uncertainty leading to leakage currents and various other effect due to reduced size, new 3d geometries has been introduced. Amongst these new geometries is the bottom up approach utilizing vertical nanowires. The vertical geometry also enables easier integration of alternative high mobility semiconductor materials on a Si substrate. A potential candidate for integration on Si is the III-V compound semiconductors due improvements in charge carrier transport capabilities.

To further motivate a switch in transistor geometry the full infrastructure of devices need to be present, not only satisfying the logical domain. Therefore, in parallel to the digital branch, a wish for developing better analog RF-transistors is present. The requirements for an RF-transistor are quite different where stability and high frequency signal gain is of importance. In an RF circuit power dissipation can be sacrificed for increased performance, lending more room for new innovations.

In this thesis the use of the vertical nanowire geometry for MOSFET is further investigated by implementing a III-V, InAs/InGaAs, graded heterostructure, inside the channel, optimized for increased stability and low resistance ohmic-contacts. A Si-substrate with grown III-V nanowires, on top of a InAs buffer layer, is provided and afterwards processed into a complete set of devices. The orientation of the grading is chosen with an abrupt junction from the InAs buffer layer to InGaAs slowly graded back to InAs at the top, by implementing 550
nm long nanowires. The measured DC-characteristics indicates a presence of the heterostructure due to good saturation, low output conductance $g_d \approx 2 \, \mu S/\mu m$ at $V_{ds} = 0.5V$ and $V_{gs} = 0.5V$. Amplification and current does not reach intended values because of large access resistance, $R_c \approx 1500 \, \Omega \mu m$, with transconductance $g_{m,max} = 280 \, \mu S/\mu m$. Good gate control is indicated with devices showcasing low sub-threshold swing $SS$ down to 80 mV/dec.

Motivation of introducing a heterostructure is clear due to higher breakdown and increased linearity but the choice of the grading orientation is not. Contact resistance is mostly originating from the source side, which means that there is large room for improvement by tweaking the process. The nanowires also had a tendency to collapse which decreased the performance. In other words the theory of implementing a heterostructure with abrupt junction for larger breakdown voltage and increased linearity is promising and cannot yet be disregarded.
"Om bilar hade utvecklats så snabbt som processorer skulle de färdas i en hastighet på 760,000 km/h, gå 42 000 km per liter och kosta 25 öre" hävdar Paul Ottelini, Intel VD mellan 2005-2013. Detta påminner oss om vilken rasande fart utvecklingen har inom nanoelektronik branschen där elektroniska kretsar ständig blivit billigare samt mindre under det senaste halv seklet. Miniatyriseringen har fördelaktigt gått hand i hand med ökad prestanda. Den huvudsakliga beståndsdelen som används i dessa kretsar, som exempelvis en processor, är en transistor. Uppgiften för en transistor är att styra strömmar på så satt att de kan stängas av eller på.


För analoga applikationer däremot, i till exempel radiosändare och mottagare, ställs andra krav. Här kan det räcka med endast ett fåtal transistorer som effektivt kan tolka och förstärka en signal som varierar över tiden. När frekvensen på signalen som ska sändas, eller mottagas, ökar kan även mer information transporteras. I framtiden krävs därmed pålitliga transistorer som hinner tolka snabba strömförråningar på grund av signal-frekvenser på flera 100 GHz.

I den digitala världen har den pågående miniatyriseringen av de logiska kretsarna lett till att många dimensioner endast är tiotals atomer. Därmed uppkommer flera utmaningar vid vidare miniatyrisering av kretsarna som leder till att man fullkomligt förlorar kontrollen över gaten. För fortsatt utveckling tittar man då på alternativa material samt andra utformningar av transistorer. Det tål att nämnas att det som sker i den digitala världen självtillverka påverkar den analoga sfären.

I detta arbete har möjligheten att skapa transistorer av stående cylindriska pelare, även kallade nanotrådar, undersökt. På dessa nanotrådar kan gaten lin-
"Now this is not the end. It is not even the beginning. 
But it is perhaps the end of the beginning."

Sir Winston Leonard Spencer-Churchill

My time as a student at Lunds University is coming to an end, or perhaps, a new beginning. When my interests of continuing on the academic path where flailing, a few people made me realise my potential. Among these people there are two professors in particular, namely Dan Hessman and Lars-Erik Wernersson. The pursuit itself is priceless and the end result is necessarily not the most important. This is the way of the researcher. So from the bottom of my heart I would like to thank you for all your support.

I would also like to extend my gratitude to my practical coach Olli-Pekka, who tirelessly taught me a very long and complicated process, and Johannes Svensson, who had to develop an all new nanowire growth recipe. I am greatly humbled by the skill level possessed by these individuals.

My family has always been a source for inspiration and pushing me to pursue my dreams, therefore I thank Lars, Charita and Max.
## Abbreviations & symbols

### Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
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<tbody>
<tr>
<td>ADC</td>
<td>analogue-to-digital converter</td>
</tr>
<tr>
<td>ALD</td>
<td>atomic layer deposition</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>aluminium oxide</td>
</tr>
<tr>
<td>Ar</td>
<td>argon</td>
</tr>
<tr>
<td>As</td>
<td>arsenic</td>
</tr>
<tr>
<td>AsH₃</td>
<td>arsine</td>
</tr>
<tr>
<td>Au</td>
<td>gold</td>
</tr>
<tr>
<td>BOE</td>
<td>buffered oxide etch</td>
</tr>
<tr>
<td>BTBT</td>
<td>band-to-band tunneling</td>
</tr>
<tr>
<td>C</td>
<td>carbon</td>
</tr>
<tr>
<td>DR</td>
<td>double row array</td>
</tr>
<tr>
<td>EBL</td>
<td>electron beam lithography</td>
</tr>
<tr>
<td>GAA</td>
<td>gate all-around</td>
</tr>
<tr>
<td>GaAs</td>
<td>gallium arsenide</td>
</tr>
<tr>
<td>GaN</td>
<td>gallium nitride</td>
</tr>
<tr>
<td>GaSb</td>
<td>gallium antimonide</td>
</tr>
<tr>
<td>Ge</td>
<td>germanium</td>
</tr>
<tr>
<td>HBT</td>
<td>heterojunction bipolar transistor</td>
</tr>
<tr>
<td>HEMT</td>
<td>high electron mobility transistor</td>
</tr>
<tr>
<td>HF</td>
<td>hydro fluoride</td>
</tr>
<tr>
<td>HfO₂</td>
<td>hafnium dioxide</td>
</tr>
<tr>
<td>HSQ</td>
<td>hydrogen silsesquioxane</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
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<tr>
<td>------------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>ICP-RIE</td>
<td>inductively coupled plasma reactive-ion etching</td>
</tr>
<tr>
<td>In</td>
<td>indium</td>
</tr>
<tr>
<td>InAs</td>
<td>indium arsenide</td>
</tr>
<tr>
<td>InGaAs</td>
<td>indium gallium arsenide</td>
</tr>
<tr>
<td>InP</td>
<td>indium phosphide</td>
</tr>
<tr>
<td>InSb</td>
<td>indium antimonide</td>
</tr>
<tr>
<td>IPA</td>
<td>2-propanol</td>
</tr>
<tr>
<td>MESFET</td>
<td>metal-semiconductor field effect transistor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>metal-oxide-semiconductor field effect transistor</td>
</tr>
<tr>
<td>MOVPE</td>
<td>metalorganic vapour phase epitaxy</td>
</tr>
<tr>
<td>N₂</td>
<td>nitrogen</td>
</tr>
<tr>
<td>Ni</td>
<td>nickel</td>
</tr>
<tr>
<td>NW</td>
<td>nanowire</td>
</tr>
<tr>
<td>NWFET</td>
<td>nanowire field effect transistor</td>
</tr>
<tr>
<td>O</td>
<td>oxygen</td>
</tr>
<tr>
<td>PMMA</td>
<td>poly(methyl methacrylate)</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>RIE</td>
<td>reactive-ion etcher</td>
</tr>
<tr>
<td>SEM</td>
<td>scanning electron microscopy</td>
</tr>
<tr>
<td>Si</td>
<td>silicon</td>
</tr>
<tr>
<td>SiO₂</td>
<td>silicon dioxide</td>
</tr>
<tr>
<td>SiO</td>
<td>silicon monoxide</td>
</tr>
<tr>
<td>Sn</td>
<td>tin</td>
</tr>
<tr>
<td>TESn</td>
<td>tetraethylin</td>
</tr>
<tr>
<td>TFET</td>
<td>tunnel field effect transistor</td>
</tr>
<tr>
<td>TiN</td>
<td>titanium nitride</td>
</tr>
<tr>
<td>TMAH</td>
<td>tetramethylammonium hydroxide</td>
</tr>
<tr>
<td>TMGa</td>
<td>tetramethylgallium</td>
</tr>
<tr>
<td>TMIn</td>
<td>tetramethylindium</td>
</tr>
<tr>
<td>UV</td>
<td>ultraviolet</td>
</tr>
<tr>
<td>UVL</td>
<td>ultraviolet litography</td>
</tr>
<tr>
<td>VLS</td>
<td>vapor-liquid-solid</td>
</tr>
<tr>
<td>W</td>
<td>tungsten</td>
</tr>
</tbody>
</table>
Physical constants

\( \varepsilon_0 \) vacuum permittivity \( 8.854 \times 10^{-12} \text{ F/m} \)
\( k_B \) boltzmanns constant \( 8.617 \times 10^{-5} \text{ eV/K} \)
\( e \) euler's number \( 2.718 \)
\( q \) elementary charge \( 1.602 \times 10^{-19} \text{ C} \)

Symbols

\( a \) lattice constant m
\( A \) area \( \text{m}^2 \)
\( A_o \) open circuit amplification -
\( C_{ox} \) intrinsic oxide capacitance \( \text{F/m}^2 \)
\( C_{gd} \) gate-drain capacitance \( \text{F/m}^2 \)
\( C_{gs} \) gate-source capacitance \( \text{F/m}^2 \)
\( d \) distance m
\( D_{it} \) density of interface traps \( \text{m}^{-3} \)
\( E_C \) conduction band energy eV
\( E_F \) fermi-level eV
\( E_g \) band gap eV
\( E_V \) valence band energy eV
\( f_t \) cut-off frequency \( \text{Hz} \)
\( g_d \) output conductance S
\( g_m \) transconductance S
\( I_{ds} \) drain-source current A
\( I_{on} \) on-state current A
\( I_{off} \) off-state current A
\( N_d \) donors \( \text{m}^{-3} \)
\( N_a \) acceptors \( \text{m}^{-3} \)
\( V_{ds} \) drain-source voltage V
\( V_{gs} \) gate-source voltage V
\( V_t \) threshold voltage V
\( R_{dh} \) channel resistance \( \Omega \text{m} \)
\( R_d \) drain resistance \( \Omega \text{m} \)
\( R_c \) access resistance \( \Omega \text{m} \)
\( R_{on} \) on-resistance \( \Omega \text{m} \)
\( R_s \) source resistance \( \Omega \text{m} \)
\( SS \) sub-threshold slope mV/dec
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\varepsilon_r$</td>
<td>relative permittivity</td>
<td>-</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>dielectric constant</td>
<td>F/m</td>
</tr>
<tr>
<td>$\mu_e$</td>
<td>electron mobility</td>
<td>cm$^2$V$^{-1}$s$^{-1}$</td>
</tr>
<tr>
<td>$\mu_h$</td>
<td>hole mobility</td>
<td>cm$^2$V$^{-1}$s$^{-1}$</td>
</tr>
<tr>
<td>$\phi_B$</td>
<td>Schottky barrier potential</td>
<td>V</td>
</tr>
<tr>
<td>$\phi_M$</td>
<td>metal work function</td>
<td>V</td>
</tr>
<tr>
<td>$\phi_s$</td>
<td>semiconductor work function</td>
<td>V</td>
</tr>
<tr>
<td>$\chi_s$</td>
<td>semiconductor electron affinity</td>
<td>V</td>
</tr>
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A.1 Outlining all metrics for the best device in batch #1. Values are extracted from SEM inspections. All data is normalized to the total circumference of the nanowires. A mean value has been extracted from SEM inspections of other pads. Bias conditions are chosen in active region of the transistor at $V_g = 0.5$ and $V_{ds} = 0.6\,\text{V}$. 
Introduction

In the year 1925 Julius Edgar Lilienfeld filed a patent for the field effect transistor FET, describing the basics of what later would be known as the metal-oxide-semiconductor field effect transistor MOSFET [1]. Due to high purity semiconductors not being available the concept was experimentally confirmed decades later by Bell Labs in 1948. Further development was, at the time, not pursued due to problems connected to the surface of the semiconductor. Instead the germanium based point-contact transistor, invented in 1947, stole the show and became commercially available for use in the early pocket radios, replacing the bulky vacuum tubes [2]. Connected to improvement in semiconductor quality and advent of integrated circuits (ICs) based on silicon in the 1960s the dreams of the MOSFET once again resurfaced. At this point the interface problems had been resolved by means of taming the strong native oxide found in silicon. The emergence of the computer industry further pushed the revolution with constant demands for faster and more energy efficient circuits.

Gordon E. Moore released his predictions (Moore’s law) in 1965 stating that the number of transistors per chip area will roughly double every 24 months via geometrical downscaling [3]. The predictions was based on the fact that increased packing density leads to exponential increase in performance as well as lower power dissipation of the circuits. Moore’s law was followed strictly up until 2002 when the downscaling became constricted by power dissipation of 100 W/cm² [4]. To avoid overheating increase of performance was now pursued with multi-core systems and parallelization of computer tasks rather than speed.

Today the industry is in a place where things are shaken up with uncertainty. Improvements in transistor technology is now heavily dependent on innovations rather than downscaling. The technology demands has also changed with the upcoming era of IoT (Internet of things) setting up new standards for RF-transistors used in wireless communications [5]. A potential candidate for meeting the demands is to integrate III-V high speed material, on silicon substrates, utilizing a nanowire geometry with gate all-around (GAA) configuration. This alternative is further examined in this thesis. The needed background for absorbing and understanding the benefits of the work in this thesis is given in this chapter.
1.1 Semiconductor Physics

To grasp the concept of transistor technology it is important to have a fundamental understanding of its building blocks, namely the semiconductor. Normally a semiconductor consists of a solid chemical element or compound, for example III-V semiconductors, and is used for integrated circuits due to its ability to conduct electricity during some circumstances but not others. To explain this behaviour concepts of chemical potential and band gap are introduced. An intrinsic semiconductor has its chemical potential, described by Fermi-Dirac statistics, placed inside the band gap typically ranging from 0.5 up to 8 eV. Few charge carriers are typically available in a semiconductor leading to poor conductance. To circumvent this issue doping is introduced increasing the amount of charge carriers inside the conduction band. The concepts are further explained in this chapter.

1.1.1 The Origin of Band Structure

In a single atom the energy levels for orbiting electrons (fermions) are quantized maintaining a unique quantum number, described by the Pauli Principle [6]. Charge of the nucleus determines the amount of orbiting electrons, and size of the electron cloud, which controls the properties of the atom. In case of a semiconductor the atoms align in form of a crystal. When the atoms become tightly packed (lattice constant order of magnitude $a \sim \text{Å}$) hybridization occurs, wave functions overlap and mutual orbits for electrons are created. Pauli principle still applies, therefore the orbits spread in energy, see Fig 1.1. Two electrons can still have the same relative energy but will not share the same spin. The size of the bands depend on the energy of the bound states where the electrons originated from. To decide if a solid is in fact a semiconductor, metal or even an insulator the concept of a chemical potential, Fermi-level $E_F$, is introduced showing the statistical energy of the free charge carriers inside the crystal. Definitions of conduction and valence band are also introduced, with the valence band being the last filled energy band and conduction band being the next band with higher energy. Thus a metal has a Fermi level placed inside the conduction band and a semiconductor has its potential placed inside a band gap, meaning that there are no free carriers inside the conduction band at absolute zero temperature 0 K. In reality there is always carriers inside the conduction band due to thermal excitation.

A general concept is that the crystal structure shares electrons that can move "freely" inside the crystal lattice [7]. But since the electrons are moving inside a cluster of charge this is modelled by introducing a different effective mass $m^*$ for the charge carriers, see Fig 1.1 (free electron model). The potential of each atomic nucleus can be seen as a periodic perturbation in the free electron model, thus at certain wave vectors $\mathbf{k} = n\pi/a$ ($n \in \mathbb{Z}$) the periodicity of the carriers will resonate with the perturbation effectively shifting the kinetic energy of the carriers creating a band gap (nearly free electron model).
Fig 1.1: A simplified sodium crystal containing only three atoms to model the total potential seen by the charge carriers. The valence electrons in the structure are shared, and can move between atoms. (a) The potential for the free charge carriers can be modelled by a simple square potential where local potential shift originating from the atomic nucleus is neglected. This modelling is sufficient to introduce the concept of effective mass. (b) Another layer is added to the model where a periodic perturbation, depending on lattice constant $a$, is added. Crucial for the derivation of energy band gap seen by free charge carriers.

Fig 1.2: A typical shift in fermi-level $E_F$ during different doping. The intrinsic Fermi level $E_F$, resides in the middle of the band gap meaning that few free carriers are available and the material is highly resistive. The amount of free carriers $n$ or $p$ at room temperature is inversely dependant on the band gap $\frac{1}{E_g}$. When adding donors $N_d$ to the semiconductor the fermi level is shifted upwards to $E_{F,n}$ and in this case reaches above degenerate limit meaning that chemical potential is inside the conduction band. The same shift occurs downwards in energy when adding acceptors $N_a$ and the potential ends up at $E_{F,p}$. 
1.1.2 Doping

To manipulate the placement of the chemical potential, thus changing the electrical properties of the semiconductor, impurities are introduced effectively doping the crystal, see Fig. 1.2 [8]. Doping means that few atoms inside the crystal lattice of a semiconductor is substituted with compatible atoms from another material to create an abundance (n-type) or absence (p-type) of electrons. Absence of electrons can be modelled as quasi-particles called holes, normally with higher effective mass $m^*$ compared to electrons. Substituted atoms lending extra electrons are called donor states $N_d$ and respectively when removing electrons they are called acceptor states $N_A$.

In this work a n-doping is used in the order of $N_d \approx 10^{18} \text{ cm}^{-3}$, for comparison the concentration of atoms in a crystal is approximately $1/a^3 \approx 10^{21} \text{ cm}^{-3}$. III-V compounds, in many cases, have quite large lattice constant, small atom density, compared to Si which means that relatively small doping leads to degenerate Fermi-level [9]. A semiconductor overview and comparison is given in Table 1.2.

Fig 1.3: Dense version of the periodic table with atoms involved in high speed electronic devices. III-V compounds with typical dopants Sn or Si can give both p and n-doping. Source: Wikimedia Commons

In this thesis III-V compound InGaAs are doped during epitaxial growth, called in-situ doping, with Sn to add donors $N_d$. Seen from Fig.1.3 the gallium(Ga) or indium(In) atoms in InGaAs compound need to be substituted with impurities in order to achieve n-doping.

1.1.3 Schottky Barrier

Necessary for further understanding of transistor device physics is the formation of Schottky barriers in metal-semiconductor junctions, see Fig. 1.4. In early studies it was believed that the height $\phi_B$ of the formed potential barrier was only dependent on the difference between metal work function $\phi_M$ and electron affinity $\chi_s$ of the semiconductor, described by the Schottky-Mott rule [10]

$$q\phi_B \approx q(\phi_M - \chi_s)$$

(1.1)

where $q$ is the elementary charge. The length of the depletion region $W$, inside the semiconductor, can be reduced with higher doping according to

$$W \approx \frac{1}{\sqrt{N_d}}.$$ 

(1.2)
A thinner barrier allows higher chance of tunneling events which translates to less resistance in the junction [36].

Fig 1.4: The formed Schottky barrier, according to Schottky-Mott rule, in a metal-semiconductor junction. The height of the barrier is determined by the difference between metal work function $\phi_M$ and electron affinity of the semiconductor $\chi_s$, see equation [1]. Work function of the semiconductor $\phi_s$ is also given. Notice that $W$ depicts the width of the depletion region in the semiconductor in which the band bending takes place.

In practice the characterisation of the junction is much more complex because the height of the Schottky barrier is heavily dependent on surface states, known as metal induced gap states (MIGS), formed at the surface in between materials [11]. Therefore certain semiconductors exhibit different degrees of Fermi level pinning, meaning that the Fermi level of the semiconductor pins to certain positions relative to the chemical potential of the metal. Basically the gap states get charged and drive the band lineup to a new equilibrium state. The Fermi level pinning needs to be taken into account when choosing transistor material.

1.2 Background & Future of MOSFET

MOSFET uses manipulation of energy-barriers to either quench or conduct a current, toggling between on- and off-state [13]. The transistor is comprised of normally four different terminals; gate(G), drain(D), source(S) and body(B). The body terminal consists of the substrate itself in planar cases but when utilising the geometry of a NWFET the substrate is not a part of the active region effectively making it into a three terminal device. Active region of the MOSFET is called channel which is controlled via the gate terminal through a metal-oxide-semiconductor MOS interface, using an oxide as insulator. The MOS structure gives rise to a capacitance that makes it possible to control the potential of the free charge carriers inside the semiconductor channel. Different regimes are therefore defined to further describe the state of the charge carriers in the channel under different bias conditions applied to the gate electrode $V_{gs}$, namely accumulation, depletion and inversion. During accumulation the charge carriers, that constitutes the majority, are attracted to the semiconductor surface, along the oxide interface,
and in depletion these carriers are instead greatly reduced. When increasing the
degree of depletion, by modulating the gate bias above a certain threshold voltage
\( V_{gs} > V_t \), new minority charge carriers are being generated effectively inverting
the channel, thus inversion is achieved.

![Fig 1.5: Overview of how a MOSFET typically works. Depicting a planar n-transistor with no gate overlap (a) with the symbol describing a MOS transistor (b) in a circuit schematic. The schematic is used here to highlight relative position of terminals gate, drain and source in the band diagrams. The band simulations shows both off- (c) and on-state (d). Below threshold voltage \( V_{gs} < V_t \) the biasing is insufficient for creating an n-channel and the potential barrier quenches the thermionic emission of electrons. Above threshold \( V_{gs} > V_t \) the charge carriers can move past the potential barrier.](image)

At the two ends of the channel the source and drain terminals are situated
and used to control the electric field, by \( V_{ds} \), in the direction of the channel, hence
controlling the passing current \( I_{ds} \). If there is an energy barrier present inside
the channel, due to difference in doping levels between channel and source/drain
terminals, the current will not be able to flow from D- to S-terminal without
external bias, called an enhancement mode device [14]. An example of a n-type
enhancement mode device is depicted in Fig 1.5, where accumulation of electrons
inside the channel turns the device on [15].

Compared to other transistors the MOSFET offers low leakage current from the
gate electrode due to the insulating oxide in the MOS interface [16]. Maintaining
a low off-state leakage is key for reaching higher energy-efficiency in logical cir-
cuits where the amount of transistors is correlated to increased processing power.
Available field effect transistor without the metal-oxide-semiconductor interface
is for example high-electron-mobility-transistor HEMT or metal-semiconductor-
field-effect-transistor MESFET. A HEMT uses a wide bandgap material, as sub-
stitute for a dielectric, between metal and channel which leads to good quality
semiconductor interfaces sacrificing energy-efficiency for improved carrier trans-
port properties [17]. These characteristics are beneficial for transistors used in RF
applications.

1.2.1 Importance of High-\(\kappa\) Oxides

The on-going down scaling outlined by Moore’s Law has started to reach a certain limit where several quantum effects cannot be disregarded \[12\]. Amongst these effects are quantum tunneling, through the gate, which means that the oxide insulator inside the MOS structure is so thin that the wave-function of the charge carriers start to reach beyond the oxide, leading to an unwanted gate-leakage current \[36\]. In industry today silicon (Si) is widely used due to its availability, but also its native oxide SiO\(_2\). Due to silicon having a strong native oxide (SiO\(_2\)), the interface created between the materials has low density of interface traps \(D_{it}\) \[19\]. SiO\(_2\) also acts as a good insulator with sufficiently high permittivity \(\varepsilon_r\varepsilon_0 \equiv \kappa\).

A simple expression for the oxide capacitance \(C_{ox} [F/m^2]\) is given as

\[
C_{ox} = \frac{\varepsilon_r\varepsilon_0}{d} \equiv \frac{\kappa}{t_{ox}}
\]

with \(t_{ox}\) as the thickness of the dielectric. According to this simple formula tunneling effects, gate leakage, can be circumvented by keeping a thick oxide (\(\sim\) nm) and change to another dielectric material with higher \(\kappa\) to preserve electrostatics, see Table \[1.1\]. A typical oxide with high \(\kappa\)-value is HfO\(_2\) and is presently used by Intel instead of SiO\(_2\) see Fig \[1.6\] \[22\]. When introducing new oxide materials, issues regarding interface traps \(D_{it}\) are more prominent due to dangling bonds and point defects \[23\]. In this work III-V semiconductors are utilized which lacks
good native oxides. Implementing a high-κ oxide on III-Vs can hence lead to insufficient electrostatic control \[20\]. To minimize interface states, bi-layers can be utilized with for example Al₂O₃ as a buffer layer between semiconductor and HfO₂. Another source of \(D_i\) is doping of the semiconductor, where in-situ doping can degrade the crystal quality and therefore also the high-κ interface \[21\].

Table 1.1: Comparing dielectrics materials that are generally used for MOSFET. Both large offset \(\Delta E_{c,InAs}\) and bandgap is crucial for reduction of leakage. \[24\]

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>(\kappa/\varepsilon_0)</th>
<th>Bandgap [eV]</th>
<th>(\Delta E_{c,InAs}) [eV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon dioxide SiO₂</td>
<td>3.9</td>
<td>9</td>
<td>4.1</td>
</tr>
<tr>
<td>Silicon Nitride Si₃N₄</td>
<td>7</td>
<td>5.3</td>
<td>2.7</td>
</tr>
<tr>
<td>Hafnium dioxide HfO₂</td>
<td>25</td>
<td>5.8</td>
<td>2.5</td>
</tr>
<tr>
<td>Aluminium oxide Al₂O₃</td>
<td>9</td>
<td>8.8</td>
<td>3.6</td>
</tr>
<tr>
<td>Zirconium oxide ZrO₂</td>
<td>25</td>
<td>5.8</td>
<td>-</td>
</tr>
</tbody>
</table>

1.2.2 Benefits of NWFET and III-Vs

Due to the nature of the vertical nanowire geometry, strain between different crystal planes (lattice mismatch) can more easily be relaxed \[26\]. This creates vast opportunities of mixing different materials in so called heterojunctions to improve transistor performance. III-V nanowires can thus be integrated on top of a Si-substrate creating a more industry compatible and sustainable process \[28\]. Predictions have already been made stating that III-V compounds will be integrated on Si in commercial CMOS to benefit from the good transport properties, see Table 1.2, in order to improve energy efficiency and speed. The vertical geometry leads to increased packing density with the footprint area decoupled from the gate length \(L_g\) with corresponding metal contacts \[27\]. III-V wafers are small, brittle and expensive compared to Si-wafers, III-V materials are also less abundant in the earth’s crust making it crucial to still use Si-wafers \[25\].

Main benefit of changing to a more complex 3D structure is to improve electrostatic control with wrap-around gate configurations such as tri-gate (Fig 1.6) and gate-all around (GAA). This means that ratio between cross-sectional area of the channel and gate width is large, compared to its planar counterpart, maximizing gate control, see Fig 1.7. Continued downscaling of MOSFET devices has increased packing density and reduced drive voltage, in other words overall improvement of performance and cost per device. However, in the last decade, shrinking dimensions has also lead to undesirable short channel effects (SCE) such as drain induced barrier lowering DIBL and increased subthreshold swing \(SS\), especially at \(L_g \leq 30\) nm \[29\]. Switching from Si to III-V semiconductors will mean that drive voltage can be lowered without further downscaling of the gate length \(L_g\), due to superior mobility \[30\]. With better transport properties, the mean free path for charge carriers is increased which can potentially make the device oper-
Fig 1.7: Cross-sectional illustration of different gate geometries including planar, tri-gate and gate-all-around (GAA). (a) Side view of the conventional planar layout creating a sandwich of layers. (b) 3d implementation of lateral nanowires by tri-gate leading to better gate coverage, thus increased electrostatics compared to planar. (c) Complete overview of a GAA geometry, created with vertical nanowires, where ratio between gate width and cross-sectional channel area is maximized optimizing electrostatic control.

ate in the ballistic regime, with no scattering events occurring inside the channel. Intel has already improved transport properties (≈ 70%) by implementation of strained silicon as channel material, see Fig 1.6 [31].

Table 1.2 shows material parameters for selected semiconductors. III-V compounds has in several cases better mobility $\mu_n$ compared to silicon (Si), but this is not the case for hole mobility $\mu_p$. Having overall good performance for both holes and electrons is necessary for CMOS implementation in logic circuits. In this work however the processed MOSFET devices will be optimised for high frequency RF application, meaning that electron mobility (n-doping) is of importance. Observe that there is a fundamental correlation between lattice constant $a_0$ and bandgap $E_g$ as $a_0 \sim 1/E_g$. Implementing materials with a small bandgap might seem beneficial due to high mobility, but will lead to sensitivity such as thermal instability and low breakdown voltage. Notice that Si suffers from indirect bandgap which degrades the effective mass. Therefore III-V materials has been the first choice for optoelectronic devices, such as light-emitting-diode LED [32]. The currents are necessarily not higher in a MOSFET utilizing a high mobility III-V compound due to larger crystal lattice constant $a_0$, which translates to reduced density of states. The main benefit is that the ballistic regime, with no scattering inside the channel, can be reached at larger gate lengths ($L_g \leq 30$ nm) due to longer mean free path. The performance of a ballistic transistor is dependent on the injection velocity $v_{inj}$ of the charge carriers, which scales inversely with effective mass $v_{inj} \sim 1/m^*$. [33].
Table 1.2: Outlining important material parameters for selected IV and III-V semiconductors. Superior transport $\mu_n$ is shown for the III-V compounds compared to silicon. Parameters taken from [37]. Notice that the injection velocity for electrons $v_{inj,e}$ is extracted from virtual source modelling with $L_g = 30\text{nm}$ [34].

<table>
<thead>
<tr>
<th>Semi-conductor</th>
<th>$\mu_n$ [cm$^2$/Vs]</th>
<th>$\mu_p$ [cm$^2$/Vs]</th>
<th>$E_g$ [eV]</th>
<th>$a_0$ [Å]</th>
<th>$m^*/m_e$</th>
<th>$v_{inj,e}$ [cm/s]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1400</td>
<td>450</td>
<td>1.12</td>
<td>5.43</td>
<td>0.36</td>
<td>1.2\times10^7</td>
</tr>
<tr>
<td>Ge</td>
<td>3900</td>
<td>1900</td>
<td>0.66</td>
<td>5.66</td>
<td>0.22</td>
<td></td>
</tr>
<tr>
<td>GaAs</td>
<td>8500</td>
<td>400</td>
<td>1.42</td>
<td>5.65</td>
<td>0.063</td>
<td></td>
</tr>
<tr>
<td>InAs</td>
<td>40000</td>
<td>500</td>
<td>0.354</td>
<td>6.06</td>
<td>0.023</td>
<td>3.7\times10^7</td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>12000</td>
<td>300</td>
<td>0.74</td>
<td>5.87</td>
<td>0.041</td>
<td>2.8\times10^7</td>
</tr>
<tr>
<td>InSb</td>
<td>77000</td>
<td>850</td>
<td>0.17</td>
<td>6.48</td>
<td>0.014</td>
<td></td>
</tr>
<tr>
<td>GaSb</td>
<td>3000</td>
<td>1000</td>
<td>0.73</td>
<td>6.10</td>
<td>0.041</td>
<td></td>
</tr>
</tbody>
</table>

1.2.3 Design of RF Transistors

Radio frequency (RF) transistors are designed to handle high frequencies, well above 100 GHz, and still maintain both current and power gain. Emphasis is also put on the transistors ability to showcase high breakdown and stable saturation of the output conductance $g_d$. Further discussion of important metrics for high frequency performance are given in Chapter 2. Breakdown is the ability of the device to handle large currents during significant voltage bias ($V_{ds} \geq 4$ V) and is quantified by the destructive breakdown voltage $V_B$ at which the device physically breaks.

Effects leading to poor saturation and low $V_B$, when disregarding short channel effects (SCE), are impact ionization and band-to-band tunneling (BTBT), see Fig. 1.3. Both effects are inversely dependent on the band gap, $\sim 1/E_g$, of the active material that constitutes the MOSFET channel area [39, 42]. Impact ionization occurs when the kinetic energy of the charge carriers surpass the energy needed for excitation of extra electrons over the band gap. Thus when energy is lost via scattering events the probability of creating new electron-hole pairs is high [40]. This leads to a chain of events where the amount of free charge carriers are greatly accelerated. In a MOSFET impact ionization effects will lead to a sudden increase of the output current that can damage and ultimately lead to destructive breakdown of the device. The band-to-band tunneling effect, on the other hand, is dependent on the distortion of the potential seen by the charge carriers. When the potential barrier shrinks, under certain bias conditions, quantum tunneling is enabled through the band gap itself and new electron-hole-pairs can be generated [36]. These different effects likely occur if the provided energy, by a certain voltage drop $V_{bias}$, is significantly larger than the band gap, $qV_{bias} >> E_g$ with $q$ as the elementary charge, inside a segment of the channel material.
Fig 1.8: Effects during high bias conditions. In impact ionization electrons in the conduction band gain enough energy, due to an external electric field, to create extra electron-hole pairs during a scattering event. With BTBT (band-to-band-tunneling) the potential barrier is sufficiently thin to allow quantum tunneling, also generating extra electron hole-pairs.

Larger band gap leads to degraded carrier mobility, see Table 1.2. Notice that the amount of free charge carriers, density of states, is greatly sacrificed when aiming for higher mobility. Therefore when designing the channel there will be a trade off between speed and reliability of the transistor. Smart use of heterostructures can be employed to combine benefits of different semiconductors, ranging from large band gap or good transport to low $D_\text{it}$. Benefits when mixing materials has already been demonstrated in modern HBT (heterojunction bipolar transistor) for increasing the performance at high frequencies [35]. Wide band gap materials such as GaN, with $E_g = 3.4$ eV and $\mu_n = 440$ cm$^2$/Vs, has attracted increased attention due to its relatively high mobility for future integration in high power amplifiers [41].
Introduction
Chapter 2

MOSFET Performance Metrics

When benchmarking a functioning MOSFET device certain standardized metrics has been established. In this chapter the definitions for quantifying the performance of the transistors are outlined. Extracting these metrics is crucial for making accurate models which leads to greater understanding of the device and its use in circuit integration. Parasitic elements, unwanted resistance and capacitance, in a MOSFET can greatly limit the performance and can also be extracted by device modelling. Definitions covered are mainly DC metrics acquired with an input signal constant over time.

![Schematic of a MOSFET](image)

**Fig 2.1:** A schematic of a MOSFET indicating the biasing points for an intrinsic device with added series resistance. Source is normally connected to ground as a reference which means that biasing is controlled through the gate $V_{gs}$ and drain $V_{ds}$ electrodes. Biasing results in pulling a current from drain to source $I_{ds}$.

When measuring on a transistor all the metrics are extracted by sweeping either the gate voltage $V_{gs}$, at constant $V_{ds}$, or the drain voltage $V_{ds}$, at constant $V_{gs}$, and studying the change in the drain-current $I_{ds}$, see Fig 2.1. A transistor for radio frequency (RF) applications needs to have a certain bias in order to be in its active mode (saturation). The input signal will then be applied and modelled as...
a small signal shift of the voltage. To evaluate the small signal response different parameters describing the shapes of the DC curves are defined.

Fig 2.2: Output conductance of an actual MOSFET, illustrating extraction of $g_d$ and $R_{on}$. Notice that on-resistance $R_{on}$ is extracted below the saturation region and given as the inverse of the derivative.

2.1 On-resistance

Regarding output characteristics shown in Fig 2.2, inside the linear, non-saturated, region of the characteristics the on resistance $R_{on}$ can be extracted as the inverse of the slope $\frac{\partial I_{ds}}{\partial V_{ds}}$ when $V_{ds} \to 0$ V. The on resistance is comprised of mainly three different sources of resistance originating from source $R_s$, drain $R_d$ and the channel $R_{ch}$, see Fig 2.1. The source and drain resistance can be greatly reduced by making good contacts and decreasing series resistance of the MOSFET.

$$R_{on} = R_s + R_d + R_{ch} \quad (2.1)$$

The resistance originating from both source and drain, $R_s + R_d$, is referred to as access resistance $R_a$.

2.2 Output Conductance

Compared to transconductance, output conductance $g_d$ is instead the response of the drain current when changing source drain biasing $V_{ds}$. The definition is therefore defined as partial derivative of drain current with respect to source-drain voltage

$$g_d = \frac{\partial I_d}{\partial V_{ds}}. \quad (2.2)$$
Fig 2.3: A typical example of transfer characteristics for an enhancement mode MOSFET, in linear (a) and logarithmic scale (b). Example extracted from an actual measured transistor. \( g_m \) represents the derivative of the \( I_d-V_{ds} \) characteristics. \( V_t \) extrapolation carried out with the tangent of the voltage that yields maximum \( g_m \). SS is given by the slope of the exponentially increasing sub-threshold, \( V_{gs} < V_t \), segment. \( I_{on} \) is defined as one drive voltage \( V_{dd} = 0.5V \) above a fixed \( I_{off} \) current of 100 nA/µm.

An ideal MOSFET has zero \( g_d \) in saturation, meaning that channel length modulation has no effect on the resistance of the active area.

### 2.3 Transconductance

A transistor metric important for transistor in RF application is transconductance \( g_m \), defined as the partial derivative of the drain current with respect to gate voltage

\[
g_m \equiv \frac{\partial I_d}{\partial V_{gs}}
\] (2.3)

When applying a small signal input at the gate electrode the given response at the drain current is quantified by this metric.

### 2.4 Threshold Voltage

At a certain threshold voltage \( V_t \) the transistor switches from ON to OFF-state, see Fig 1.5. Typically defined as the gate voltage needed to initiate inversion of the channel. To register the threshold voltage via the \( I_{ds}-V_{gs} \) curve the tangent from the \( V_{gs} \) point, corresponding to the peak value of transconductance \( g_{m,\text{max}} \), is extrapolated down to zero drain current, see Fig 2.3. The threshold voltage is in reality not well defined which makes extraction of this metric quite arbitrary.
2.5 Voltage Gain

With transconductance $g_m$ and output conductance $g_d$ given the small signal voltage gain of the transistor, in CS configuration, can be derived from

$$A_v = \frac{\partial V_{ds}}{\partial V_{gs}} = \frac{g_m}{g_d}. \tag{2.4}$$

Notice that the given voltage gain $A_v$ is for a transistor in open circuit configuration.

2.6 Subthreshold Swing

Thermionic emission will always be limited by the amount of available free carriers above a certain potential barrier. When heat is applied to a system the carriers are redistributed according to Fermi-distribution. At high enough temperature, such as room temperature ($\sim 300 \text{ K}$), the distribution can be referred to as a Fermi-tail (similar to Boltzmann distribution) that is decaying exponentially when moving to higher energies compared to the conduction band, see Fig 1.2. The theoretical limit is hence naturally dependent on the distribution described by the Fermi-function and referred to as subthreshold slope $SS = \frac{1}{\log_{10}(e)} \frac{k_B T}{q}$. \tag{2.5}

$q$ represents the elementary charge, $k_B$ Boltzmann's constant and $e$ Euler’s number. $SS$ is identified from the transfer characteristics, in logarithmic scale, as the linear increase in the sub-threshold region, see Fig 2.3.

For logic circuits $SS$ is an essential parameter since a logic device is systematically switched between ON and OFF-state. In other words $SS$ describes how well a MOSFET works as a relay switch.

2.7 Cut-off Frequency

The only AC-metric covered in this chapter, quantifying at what frequency $f_t$ of the input signal, applied to the gate, the MOSFET showcases gain. Mentioned to underline the importance of $g_m$ and is described as

$$f_t \approx \frac{g_{m,i}}{2\pi(C_{gd} + C_{gs})} \tag{2.6}$$

with intrinsic transconductance $g_{m,i}$. Notice that extrinsic capacitances are approximated as the dominant source of parasitics and also access resistance, $R_s$ & $R_d$, are disregarded. In other words the $f_t$ scales linearly with $g_m$. 
MOSFET Evolution

Fig 3.1: a) The conventional "drain last" process developed by Sofia Johansson. b) Comparison done with self aligned gate process, "drain first", outlined by Martin Berg [46][47]. Schematic used, with permission, from doctoral thesis by Martin Berg.

The process used for manufacturing vertical nanowire MOSFET in this thesis was developed by Martin Berg and Karl-Magnus Persson [47]. Vertical processing require high precision tools optimized for an all new direction, namely normal to the substrate. Since lateral processing is utilized in industry and refined for more than half a century switching to vertical is challenging [43]. This type of processing is still in its cradle and is facing some of the challenges that was eventually resolved for the planar architecture. However vertical processing is fundamentally different from lateral due to the device being built from bottom to the top in a "bottom-up" fashion. In the bottom-up approach a system is pieced together to add up to a bigger and more complex system.

Previous processes optimized for RF-performance has included sub-sequentially adding all the pieces from bottom to the top. Starting with a wafer containing nanowires a first spacer is deposited followed by a gate and afterwards the second
spacer is added followed by the top contact. This method of conventionally depositing the top contact last was spearheaded by Sofia Johansson who developed vertical transistor that showcased gain at high frequency input, $f_t = 140$ GHz, see Figure 3.1[44]. In this thesis however the process starts with deposition of the top contact which enables a self-aligned gate process and also lends more margins in the high precision alignment steps.

A self-aligned process is crucial for increased performance due to complete gate coverage of the channel which enables lower series resistance. With larger currents, high amplification $g_m$ is possible which is fundamental for high RF-performance. The downside of tighter dimensions is larger parasitic which puts more emphasis on low-$\kappa$ integration, possibly with the use of air spacers.

The first generation of the gate last process consisted of pure InAs nanowires to accommodate both the digital and RF domain, see Fig 3.1. Growth techniques where adapted to decrease the resistance of the wire including a highly doped InAs overgrowth creating a shell for good ohmic contact. In later steps the shell could be selectively etched revealing the intrinsic or lowly doped gate area for high-$\kappa$ and metal deposition. The first generation transistors showcased instability, with high output conductance $g_d$ and low breakdown, due to the narrow bandgap of InAs.

In the second generation of NWFET these issues where addressed by incorporating a heterostructure featuring InAs and InGaAs, see Figure 3.2. Where the composition of the nanowire is gradually changed from InAs to InGaAs when moving from bottom to the top [49]. The overgrown shell, in this case, consisted of highly doped InGaAs. The result of this update in the NWFET remains unpublished.

Parallel to the second generation of devices a test is carried out, in this thesis, where the heterostructure is inverted, see Fig 3.3. Instead of gradually grading from InAs to InGaAs, the InGaAs is abruptly incorporated in the bottom
and graded back to InAs at the top. An abrupt junction creates an unwanted hetero-barrier, but the concept has possibilities of showcasing greater breakdown performance with the help of decoupling the ohmic contact performance from the Ga concentration, since InAs has better fermi-level pinning \[45\]. Low resistance in all ungated areas is crucial for high performance, thus the top and bottom segments are highly doped with \( N_d \geq 10^{18} \text{ cm}^{-3} \) to reduce contact resistance \( R_c \). A degenerate semiconductor at the bottom can compensate for the presence of a Schottky barrier. The placement of the gate is designed to cover the graded segment to benefit from the larger bandgap of In\(_{0.5}\)Ga\(_{0.5}\)As \( (E_g \approx 0.75\text{eV}) \). This configuration is optimized for the top segment acting as ground and the InAs buffer layer as drain. Notice that the final composition of the nanowire changed compared to the target sketch due to limitations during growth, see Fig 3.4.
Fig 3.4: A sketch for composition of the nanowires processed in this thesis. Due to limitations and variations during growth there is a difference between the target composition and final batch.
MOSFET Fabrication

Fig 4.1: An overview of the finished transistor in top ground configuration. The structure can also be bottom grounded meaning that the source and drain contacts, in this case, are switched. The choice of the optimal configuration, top ground, is motivated by band-simulations, see Fig 3.3.

The fabrication of the vertical MOSFET is a complex and involves many steps in order to deposit the top metal first for creating sufficient gate-overlap and, in the end, realize the final structure, see Fig 4.1. All the steps are thoroughly covered, in this chapter, combined with theory needed for greater understanding of process sensitivity.
4.1 Nanowire Growth

The device performance will always be limited by the quality of the nanowires making up the final transistor. The growth of the nanowires was therefore outsourced to an experienced researcher, namely Dr. Johannes Svensson at EIT department, Lund University. Therefore the growth process is described mostly qualitatively.

To alleviate lattice stress and enable growth of good quality III-V nanowires, on top of a silicon substrate, a 260 nm thick InAs layer is grown by metal organic vapor phase epitaxy MOVPE. In this epitaxy technique the sample is placed inside a chamber and flooded with precursor gases (TMIn, AsH$_3$), at elevated temperature, which reacts on top of the substrate surface to form the final crystalline InAs buffer layer. The silicon substrate, now covered with InAs, is later patterned with gold dots by an EBL defined lift off process using a PMMA film. The gold dots will act as catalysts in the vapor-liquid-solid (VLS) process. In this mechanism, the catalyst dots create liquid alloy droplets at high temperature (420° C-470° C) by adsorbing the vapors inside the MOVPE chamber [51]. Thus local supersaturation of the alloy occurs, which means that the concentration of components exceed its equilibrium. The system then strives to lower its energy which in turn enables 1D growth that continues as long as precursor gases are supplied, creating nanowires. By controlling the supply of precursor gases (TMIn, AsH$_3$, TMGa), during the process, InGaAs composition of the nanowire can be controlled along the growth direction [49].

Different patterns are defined by the EBL process including double row arrays, pads and single nanowire structures. The growth is thus optimized for the most
reoccuring structure, namely the zigzag double row array, see Fig 4.2.

Doping of the wires are carried out in-situ, meaning that they are doped in conjunction with deposition [52]. The dopants are added by another precursor gas, namely TESn, which adds n-doping by substitution with Sn atoms. The precision of the in-situ doping is limited by diffusion mechanisms leading to dopant atoms relocating and spreading at elevated temperatures to reduce induced strain. These effects amounted to a slightly different outcome in doping concentration and length in the final batch compared to target composition, see Fig 3.4.

4.2 Top Metal Deposition

The top contact is deposited by sputtering of 20 nm tungsten (W) and ALD of 3 nm of titanium-nitride (TiN) by utilizing a sacrificial spacer, see Fig 4.3. Sputtering amounts to good step coverage with thickness of approximately 1/3 on the sidewalls compared to the planar surface. This ratio will vary depending on nanowire spacing due to shadowing effects. The ALD process, on the other hand, leads to complete uniform step coverage independent of spacing, therefore the thin TiN film will serve as extra protection for the inner metal shell, on the nanowire sidewalls, in later etching steps. The metal film on the planar surface is specifically targeted with anisotropic dry etching in an ICP-RIE using SF₆ and CF₄F₈ gas supported by argon ions (Ar⁺). The etch time (85 s) is calibrated to completely remove metal on the planar surface and reveal the gold particles situated on the tip of the wires. The final result is given with SEM in Fig 4.4.

Fig 4.3: A schematic image depicting the top contact deposited by sputtering and ALD.
4.3 Drain Pad and Bottom Spacer

The 260 nm InAs buffer layer covering the silicon substrate is highly doped \(N_D = 5 \cdot 10^{19} \text{ cm}^{-3}\) and is therefore highly conductive. To further isolate the different devices, present on a single sample, from each other, a mesa etch has to be carried out. The etch removes the excess of the InAs layer which is crucial for good RF-performance by minimizing overlapping parasitic capacitance. The material left on the surface creates a pad that acts as the bottom contact and constitutes the drain. The pad is defined via optical lithography utilizing, spun on and baked, S1813 photoresist at 4000 rpm, resulting in a thickness of 1300 nm. The pattern is defined via a mask aligner (soft UV) later developed with MF 319 containing highly diluted TMAH 2.2 % \([55]\). Unwanted resist residues are thoroughly removed via an oxygen plasma. The resist acts as an etch mask when using InAs wet etch consisting of \(\text{H}_3\text{PO}_4: \text{H}_2\text{O}_2: \text{H}_2\text{O}(1:1:25)\) and can afterwards easily be removed with an acetone and IPA rinse.

To fabricate the bottom spacer a 50 nm thick \(\text{SiO}_2\) layer is deposited via ALD and etched with the help of a resist mask using a "etch-back" process, see Fig. 4.5. In this method the resist (S1813) is deposited on top of the \(\text{SiO}_2\) layer, by spinning and baking, and thinned by RIE with oxygen plasma until the top of the nanowires are visible. Desired resist thickness is around 200 nm ensuring step coverage of the mesa etch. Diluted HF (1:100) is used for controllable wet etch to remove the \(\text{SiO}_2\) from the nanowire sidewalls until only the desired spacer is left. The resist mask is then completely removed via acetone and IPA rinse.
Fig 4.5: The creation of the first spacer. 1 A SiO$_2$ spacer is first applied via ALD. Organic resist is later spun onto the sample and thinned down via O$_2$ dry etching. 2 The SiO$_2$ spacer is etched via HF (1:100 H$_2$O) wet etch with the organic spacer acting as a etch mask. 3 The resist spacer is removed with acetone leaving only the finished first spacer.

4.4 Gate Deposition

Schematic illustrations for the gate deposition process is given in Fig 4.6. To increase electrostatic control, of the channel, sidewall etching is performed targeting the exposed part of the nanowire, later acting as the gate area. A long nanowire will be subject to more capillary force during H$_2$O or IPA rinsing steps, specifically during drying. Based on previous calibrations the etching is used to reach a diameter slightly above 25 nm with a nanowires around 550 nm long.

After sufficient reduction of the gate diameter the high-κ dielectric can be deposited via ALD, see Fig 4.7. Chosen dielectric consist of a bilayer with hafnia HfO$_2$ and sapphire Al$_2$O$_3$. Sapphire is known to create a good interface and is therefore used as a thin 1 nm buffer layer while the 4 nm HfO$_2$ layer, with higher κ-value, contributes to greater electrostatics. The deposition is in the end carried out with 10 cycles of Al$_2$O$_3$ and 40 cycles of HfO$_2$ leading to an approximate high-κ thickness of approximately 45 Å.
Fig 4.6: Deposition of the gate contact.  
1. Etching is performed targeting the exposed semiconductor effectively thinning it below 30 nm of diameter. 
2. 60 nm of tungsten is sputtered onto the sample. A organic spacer is created via spun on resist and dry etching. 
3. The exposed tungsten is removed via SF6 dry etch. The organic spacer is afterwards removed via aceton.

60 nm gate metal, of tungsten (W), is applied via sputtering, completely covering the nanowires as well as the planar surface. A resist (S1813) is spun on, baked and thinned down with oxygen plasma in a RIE until desired gate-length is reached. High precision is needed for sufficient overlap as well as leaving margins for the second organic spacer. Minimizing the overlap is further important to reduce parasitic capacitance, but its presence is necessary to ensure good DC-performance. Exposed tungsten can be removed via dry etching utilizing SF6 gas in a RIE process, see Fig 4.7(b). The S1813 is removed, with a usual acetone and IPA rinse, in order to spin on a new resist for use in UV-litography to define the gate pad. After the pattern is exposed in a mask aligner (soft UV) and removed via MF319 the excess tungsten is removed with dry etching (SF6).
4.5 Via Holes and Top Contact

A second organic spacer is fabricated with spun on S1813, now permanently baked and thinned down until 50-100 nm of the top metal is visible, see Fig 4.8. To enable metal-to-metal connection of the top contact the high-κ is removed with a BOE (HF) wet etch. All terminals must further be available for connection via the top metal, thus via holes for both the gate and drain has to be etched. A resist etch mask (S1813) is spun on and baked, and via holes are exposed, one at a time, with mask alignment (soft UV) and development. The gate via is completely cleaned out with oxygen plasma, locally removing the organic spacer, in a RIE. The drain via is also cleaned out with a oxygen plasma followed by a BOE etch for high-κ and bottom spacer removal. Sputtering is used to deposit the top contact consisting of 15 nm nickel (Ni), 30 nm tungsten (W) and 200 nm gold (Au). With the tungsten acting as a diffusion barrier and Ni for creating a good metal-to-metal interface.

The top metal layout, shown in Fig 4.9, is designed to isolate the gate, source and drain terminals from each other and is defined with a UV patterned resist (S1813) mask followed by three individual etch steps. The gold is wet etched using potassium-iodine (KI), the tungsten via SF₆ dry etching and Ni with H₂O:H₂SO₄:HNO₃:CH₃COOH (10:5:5:2) wet etching.
Fig 4.8: Deposition of the second spacer and top contact. 1. An organic spacer is spun onto the sample, permanently baked and thinned down via O₂ dry etching. 2. Via holes are etched with sacrificial resist layer acting as etch mask where via holes are exposed, one at a time, via UV lithography. 3. Top contact is sputtered consisting of Ni, W and Au.

Fig 4.9: Showing the finished top metal layout in top grounded configuration.
Two batches were finalized during this diploma work, with each batch containing two full-scale samples. The first processed batch only resulted in one device with transistor DC-characteristics and the second one showcased promising results with a high yield of approximately 20, of 110 in total, working transistors on each sample. Techniques for RF-optimization were not employed, such as minimizing overlap capacitance with finger contacts, thus only DC-characteristics were measured. To further reach sufficient results with high RF-performance, the $g_m$ is crucial and scales linearly with cut off frequency $f_t$ (equation 2.6), but also high breakdown ($V_{ds} \geq 4$ V) is essential as proof-of-concept. The measurements of the devices were carried out in a probe station.

5.1 Processing

This section serves to highlight differences between the processed samples and also discuss challenges during certain processing steps. Many of the used machines such as the ICP-RIE and RIE are not dedicated for a certain set of materials. Thus the chambers are constantly contaminated with many different substances during their life cycles. For this process it has meant that the etch rates were constantly varying which required extra caution and frequent SEM inspections. Bear in mind that many machines are not optimized for vertical processing making it even more tedious when high precision alignment is required.

Chamber conditions and bad calibration of the anisotropic dry etching steps led to the first batch showcasing extra roughness of the fabricated top contact. In many instances the gold particle was completely etched away including the semiconductor material underneath leaving a hollow top metal contact, see Fig 5.1(a). The majority of devices where therefore completely destroyed during the many processing steps ahead. Fig 5.2 shows the severity of damage to one of the few surviving double row arrays.

During the second batch the ICP-RIE was correctly calibrated but the chamber was not sufficiently cleaned. A residual film was therefore left on the surface after anisotropic etching and removal of the HSQ spacer, see Fig 5.1(b). The origin and composition of the film could not be confirmed due to the lack of proper tools for analysis. Sample B, in the second batch, was heavily damaged by the
residual film and therefore extra wet etching steps were tested for removing the film. The sample was, after top metal fabrication, put in extended BOE(HF) etch followed by hydrogen passivation in H$_2$SO$_4$, both steps had limited effect and mostly etched the exposed nanowire sidewalls. Sample A was also covered by the residual film but to less extent so no extra etching steps were performed. Notice that many nanowire arrays, especially in Sample B, were completely collapsed after the top contact fabrication. Most likely due to residues ripping away from the planar surface during the HSQ removal. In contrast to the first batch the quality of the top contact was greatly improved for batch #2. A fair comparison between the top contacts of single nanowire structures are performed in Fig 5.1.

Extra caution for further collapse had to be taken during the targeted sidewall etching. Therefore etching was only performed on Sample A and not on Sample B. Therefore the diameter was significantly smaller on Sample A potentially leading to better electrostatic control of the gate. The difference is given in Fig 5.3 showing nanowire arrays, with the same relative position, on each sample. Table 5.1 states the important differences between the processed batches later necessary for understanding of measurement data.

Table 5.1: A quick comparison between processed samples. ¹Top contact quality and gate alignment greatly improved between batches, with the first batch having ~ 20 nm of ungated channel area. ²All processing was optimized for the double row (DR) arrays in the second batch. The gate length is varying between devices due to both the bottom spacer and position of the top contact.

<table>
<thead>
<tr>
<th>type</th>
<th>state</th>
<th>remarks</th>
<th>Fig.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Batch #1</td>
<td>top contact quality</td>
<td>visibly bad</td>
<td>pads &amp; singles DR arrays</td>
</tr>
<tr>
<td></td>
<td>bottom spacer</td>
<td>50-100 nm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>gate coverage</td>
<td>insufficient¹</td>
<td></td>
</tr>
<tr>
<td>Batch #2</td>
<td>top contact quality</td>
<td>OK¹</td>
<td>5.1(b)</td>
</tr>
<tr>
<td>Sample A</td>
<td>bottom spacer</td>
<td>50-200 nm</td>
<td>DR arrays²</td>
</tr>
<tr>
<td></td>
<td>sidewall etch</td>
<td>~ 3 nm etch</td>
<td>isotropically</td>
</tr>
<tr>
<td></td>
<td>diameter</td>
<td>31-37 nm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>gate coverage</td>
<td>complete¹</td>
<td>4.7(b)</td>
</tr>
<tr>
<td></td>
<td>gate length $L_g$</td>
<td>60-180 nm</td>
<td>DR arrays²</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5.3</td>
</tr>
<tr>
<td>Batch #2</td>
<td>top contact quality</td>
<td>OK¹</td>
<td>5.1</td>
</tr>
<tr>
<td>Sample B</td>
<td>bottom spacer</td>
<td>50-180 nm</td>
<td>DR arrays²</td>
</tr>
<tr>
<td></td>
<td>sidewall etch</td>
<td>none</td>
<td></td>
</tr>
<tr>
<td></td>
<td>diameter</td>
<td>29-33 nm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>gate coverage</td>
<td>complete¹</td>
<td>4.7(b)</td>
</tr>
<tr>
<td></td>
<td>gate length $L_g$</td>
<td>80-180 nm</td>
<td>DR arrays²</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5.3</td>
</tr>
</tbody>
</table>
Fig 5.1: Two single nanowire structures after removal of the temporary HSQ spacer. Highlighting the metal surface roughness for comparison,

Fig 5.2: The damage after fabricating the top metal in batch #1. Hollow top metals are visible and the metal surface roughness is clearly shown.

Fig 5.3: Nanowires after digital etch and high-κ deposition for both samples in batch #2. High-κ thickness is 4.5 nm according to SEM inspections, thus the mean diameter of the specific array in Sample A is 29 nm and 35 nm in Sample B.
5.2 Measurements

Approximately 100 devices where measured in this project with ~1% boasting good DC performance. A small summary of the best devices are given in Table 5.2. Batch #1 is included to highlight the importance of tweaking the process. The sample subject to digital etch (Table 5.1) shows overall improved $g_m$ as well as lower SS which is expected due to increased electrostatic control. Notice that the overall $g_m$ performance is low for all devices, see Table 5.4 for benchmarking, which indicates high resistance in the system.

Most devices, containing DR arrays, were subject to high rate of collapsed nanowires. The collapse can introduce inhomogeneous strain and degrade the crystal quality, which might lead to higher resistance and low $g_m$. No detailed study has been performed regarding degradation of the currents in collapsed nanowire structures, which means the influence is not taken into consideration when normalizing the currents.

<table>
<thead>
<tr>
<th>type</th>
<th>$L_g$ (nm)</th>
<th>Diam. (mS/µm)</th>
<th>$g_{m_{max}}$ (tg/bg)</th>
<th>$SS_{min}$ (tg/bg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>batch #1</td>
<td>pad</td>
<td>220</td>
<td>0.010/0.002</td>
<td>92/103</td>
</tr>
<tr>
<td>batch #2</td>
<td>DR</td>
<td>80</td>
<td>0.28/0.24</td>
<td>80/130</td>
</tr>
<tr>
<td>sample A</td>
<td>DR</td>
<td>120</td>
<td>0.24/0.21</td>
<td>71/122</td>
</tr>
<tr>
<td></td>
<td>DR</td>
<td>60</td>
<td>0.22/0.20</td>
<td>96/123</td>
</tr>
<tr>
<td></td>
<td>DR</td>
<td>120</td>
<td>0.19/0.15</td>
<td>152/135</td>
</tr>
<tr>
<td>batch #2</td>
<td>pad</td>
<td>200</td>
<td>0.18/0.30</td>
<td>99/104</td>
</tr>
<tr>
<td>sample B</td>
<td>single</td>
<td>220</td>
<td>0.13/0.17</td>
<td>182/114</td>
</tr>
<tr>
<td></td>
<td>DR</td>
<td>140</td>
<td>0.08/0.13</td>
<td>98/110</td>
</tr>
<tr>
<td></td>
<td>DR</td>
<td>140</td>
<td>0.07/0.12</td>
<td>110/106</td>
</tr>
</tbody>
</table>

Table 5.2 contains a complete overview of important metrics necessary for later benchmarking. Notice that the thick bottom spacer in the second batch leaves large ungated segments of the channel in the DR arrays. When a heterostructure is present (Fig. 3.3) the gate placement is important and will yield different results. For minimizing the resistance originating from the heterobarrier and large bandgap at the bottom contact, top ground (tg) configuration should be beneficial compared to bottom ground (bg). This holds true for sample A where both $g_{m_{max}}$ and SS is higher for tg. Sample B, that inherits the record $g_{m_{max}}$ only for bg, indicates that the improved performance in tg, for sample A, could be due to extra resistance originating from the ungated segment. Leaving an
ungated segment adds series resistance which lowers the effective voltage drop over the channel. However the $g_m$ of the record device is still too low for RF implementation, where the goal is at least $g_{m,\text{max}} \geq 1 \text{ mS/\mu m}$. The measurements in general narrows the main source of resistance down to the insufficient quality of the fabricated top contact for all processed samples. The deposition method and choice of tungsten (W) for the top contact can therefore be questioned.

![Graphs showing measurements](image)

**Fig 5.4:** Overview of all arrays in batch 2. No sidewall etch was performed on sample B, meaning that the effective diameter of the nanowires are smaller in sample A, see Table 5.1. (a)-(b) shows the correlation between extracted values $R_{on}$ and $g_{m,\text{max}}$, clearly showing the expected exponential trend when decreasing the total resistance. (c)-(d) Outlines SS dependence of $g_{m,\text{max}}$, showing no clear trend.
The importance of lowering the resistance of the system, quantified by $R_{on}$, is visually presented in Fig. 5.4 where measured $g_m$ is proven to be inversely proportional to $R_{on}$. Sample B has in general a boost in performance when switching from $tg$ to $bg$ configuration. The opposite is true for sample A where the highest $g_m$ devices are shifted downwards, but the trend is not consistent for all devices. An increase in gate control, quantified by $SS$, can be observed for sample A and for $tg$ in general. Increased gate control overall is not consistent with a boost in $g_m$.

The $SS$ dependence on $V_t$ is further explored in Fig 5.5 and the access resistance $R_c = R_s + R_d$ is extracted. Turning a device on at a faster rate could lower the threshold voltage, but no clear correlation can be seen. This is likely due to other effects being more prominent such as voltage division over the contacts. Therefore the access resistance is examined for the best sample and estimated to 1500 Ωµm. Due to collapsed structures leading to increased resistance all devices with $R_{on} > 2800$ Ωµm are discarded for a fair extrapolation. Notice that the extrapolated values are used as a rough estimate of the present access resistance. The slope of the extrapolation indicates that the resistance inside the channel is also large with a 1:1 ratio at $L_g = 180$ nm which is likely a combination of of potential barriers together with the higher bandgap of InGaAs. Compared to previous InAs devices fabricated with the same process the resistance was estimated to a lower value of $R_c = 750$ Ωµm [48]. These devices, on the other hand, had a highly doped overgrown InAs shell which likely decreased the resistance originating from the Schottky contacts. The short gate-length is a result of both long top metal but also a large bottom spacer, $\approx 120$ nm. This does not seem to influence on the contact resistance greatly, in $tg$, due to the clear reduction of $R_{on}$ for the short $L_g$ devices.

![Fig 5.5: Exhibiting the $SS-V_t$ and $R_{on}$-$L_g$ dependence. Attempts for extrapolating the access resistance, $R_c = R_s + R_d$, are performed with taking all values into account (#1) and a selected few (#2) that are highlighted. A smaller ratio of collapsed nanowires seem to be present in the highlighted devices. Note that the $L_g$ values are based on estimates from SEM pictures that, in this case, might be insufficient due to large thickness variation of the bottom spacer.](image-url)
5.2.1 Device Characteristics

One device with good characteristics have been hand picked to delve into all performance metrics. Many devices showed improved current levels in bottom ground configuration which is contrary to the band gap simulations, see Table 5.2. The greatest transistors broke the trend with slightly improved currents in top ground indicating that the $R_s$, originating from the top contact, for these devices were likely low. DC characteristics for the best, and most representative, device is seen in Fig 5.6 & 5.7 and metrics are compiled in Table 5.2.1.

The device shows promising off-state performance with low SS, of 80 mV/dec, being close to constant from $V_{gs} = -0.16$ V to $V_{gs} = 0.2$ V. The maximum $g_m$ hits the mark of 280 $\mu$S/µm, in top ground, and slightly lowered to 250 $\mu$S/µm when switching configuration. The off-state current is improved many orders of magnitude with $tg$. A promising metric is the low $g_d$ (at $V_{ds}, V_{gs} = 0.5$ V) which is 2 $\mu$S/µm. It is expected to get better saturation, low and consistent $g_d$, when the potential drop occur over the high band gap segments. This should be reflected in $tg$, which is not the case. This raises questions about the InAs present in the bottom, or gate-misalignment of the nanowire, see Fig 4.1. Overall the $R_{on}$ metric is large (1700 $\Omega$µm) and has to be reduced with better contacts in order to reach competitive values, see Table 5.4. The goal was to keep the channel intrinsic to ensure good crystal quality, but in reality the segment is unintentionally doped which can reduce the crystal quality, see Fig 3.4. Therefore the channel itself is also providing large resistance to the system.

![Fig 5.6](image-url) Transfer characteristics, plotted in logarithmic scale, for the hero device found batch #2. Metrics compiled in Table 5.2.1.
Fig 5.7: Output characteristics for the hero device found batch #2. Metrics compiled in Fig 5.2.1.

Table 5.3: Outlining all metrics for the best device in batch #1. Values are extracted from SEM inspections. All data is normalized to the total circumference of the nanowires. 1Bias conditions are chosen in active region of the transistor at $V_g = 0.5$ and $V_{ds} = 0.5V$.

<table>
<thead>
<tr>
<th>Batch #2</th>
<th>Metric</th>
<th>Value</th>
<th>Unit</th>
<th>remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>geometry</td>
<td>double row</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td># of nanowires</td>
<td>300</td>
<td>-</td>
<td>nm</td>
<td></td>
</tr>
<tr>
<td>diameter</td>
<td>30</td>
<td>30 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>high $\kappa$: Al$_2$O$_3$/HfO$_2$</td>
<td>10/40</td>
<td>cycles</td>
<td></td>
<td></td>
</tr>
<tr>
<td>high $\kappa$ thickness</td>
<td>4.5</td>
<td>4.5 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>gate length $L_g$</td>
<td>80</td>
<td>80 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>gate leakage $I_g$</td>
<td>$\sim$ 1</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bottom ground</td>
<td>$g_{m,\text{max}}$</td>
<td>250</td>
<td>$\mu$S/µm</td>
<td></td>
</tr>
<tr>
<td>SS</td>
<td>130</td>
<td>mV/dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$g_d$</td>
<td>2</td>
<td>$\mu$S/µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q$</td>
<td>1.9</td>
<td>kS-dec/Vm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{\text{DC}}$</td>
<td>25</td>
<td>125</td>
<td>bias$^1$</td>
<td></td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>1700</td>
<td>$\Omega \cdot \mu m$</td>
<td>bias$^1$</td>
<td></td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>54</td>
<td>$\mu A/\mu m$</td>
<td>bias$^1$</td>
<td></td>
</tr>
<tr>
<td>$V_t$</td>
<td>0.1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>top ground</td>
<td>$g_{m,\text{max}}$</td>
<td>280</td>
<td>$\mu$S/µm</td>
<td></td>
</tr>
<tr>
<td>SS</td>
<td>80</td>
<td>mV/dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$g_d$</td>
<td>2</td>
<td>$\mu$S/µm</td>
<td>bias$^1$</td>
<td></td>
</tr>
<tr>
<td>$Q$</td>
<td>3.5</td>
<td>kS-dec/Vm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{\text{DC}}$</td>
<td>140</td>
<td>-</td>
<td>bias$^1$</td>
<td></td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>1900</td>
<td>$\Omega \cdot \mu m$</td>
<td>bias$^1$</td>
<td></td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>84</td>
<td>$\mu A/\mu m$</td>
<td>bias$^1$</td>
<td></td>
</tr>
<tr>
<td>$V_t$</td>
<td>0.28</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.3 Benchmarking

To understand the possibilities and motivate key choices in processing it is crucial to do benchmarking, see Table 5.4. The general, and expected, trend is improved $g_m$ with decreased dimensions, specifically $L_g$. The off-state performance is also sacrificed to reach high $g_m$ with $SS$-values well above 60 mV/dec (theoretical limit) for the record devices. The first batch had catastrophic transconductance $g_{m,max}$ with only a single device with sufficient gate-control, $SS = 103$ mV/dec. In the second batch the current levels and $g_m$ were drastically improved but still low in comparison similar vertical devices. Previous generation utilized an overgrown highly doped InAs shell, covering the nanowires, which will improve the contact (Schottky) between semiconductor and metal [59]. This overgrowth is not present on the nanowires used in this thesis. To improve interface the semiconductor-metal interface alternative metals can be used such as nickel (Ni). The Ni metal has a tendency to react and form an alloy between the metal and semiconductor decreasing the resistance and transfer length [60].

Table 5.4: A comparison with mainly other work from the research group (Nanoelectronics Group), created in the same lab using mostly the same equipment. V highlight the vertical orientation of the device, other devices utilize a lateral geometry. Notice that all V-NW devices are integrated on silicon while the both the HEMT and record device are based on an InP(III-V) substrate.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Channel</th>
<th>$g_{m,max}$ mS/µm</th>
<th>$SS_{min}$ mV/dec</th>
<th>$L_g$ nm</th>
<th>reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>V-NW MOSFET</td>
<td>InGaAs/InAs</td>
<td>0.28</td>
<td>80</td>
<td>110</td>
<td>batch #2</td>
</tr>
<tr>
<td>V-NW MOSFET</td>
<td>InGaAs/InAs</td>
<td>0.01</td>
<td>103</td>
<td>220</td>
<td>batch #1</td>
</tr>
<tr>
<td>V-NW MOSFET</td>
<td>InAs</td>
<td>1.02</td>
<td>124</td>
<td>130</td>
<td>[47]</td>
</tr>
<tr>
<td>V-NW MOSFET</td>
<td>InAs</td>
<td>0.73</td>
<td>420</td>
<td>150</td>
<td>[44]</td>
</tr>
<tr>
<td>NW MOSFET</td>
<td>InGaAs</td>
<td>3.30</td>
<td>118</td>
<td>60</td>
<td>[57]</td>
</tr>
<tr>
<td>HEMT</td>
<td>InGaAs</td>
<td>2.5</td>
<td>115</td>
<td>40</td>
<td>[58]</td>
</tr>
</tbody>
</table>
5.4 Breakdown

A few devices, from batch #2, was chosen for testing the limit for destructive breakdown $V_B$ and is reported to occur slightly below $V_{ds} = 4V$ in the standard top ground configuration, see Fig 5.8. Different devices could be continually pushed to high bias conditions, with $V_{ds} \leq 3.5V$, and show repetition of largely the same output characteristics with no major sign of damage. Notice that the currents are still relatively low and the effective voltage over the gate is also reduced due to large contact resistance. Impact ionization can be spotted starting from 0.6 V and accelerating after 2.2 V. The impact ionization might not be the only effect leading to increased currents, also tunneling can be present, see Fig 1.8

![Fig 5.8: Output characteristics for a representative, double row, device at bias conditions close to its breakdown at 4 V. The device is found batch #2-sample A. The transistor can operate up to 3.5 V, but showcases bad saturation with high $g_d$. Different segments can be identified with (a) being well saturated and (b) showing impact ionization that accelerates further in (c).](image)

In top ground the voltage drop will occur in a high bandgap region unlike bottom ground where only InAs is present, see Fig 3.3. To study if this is actually translated to the processed devices, the destructive breakdown for both configurations is given in Fig 5.9. The theory can be clearly confirmed with the device breaking at 2.2 V in bg compared to 4 V when switching configuration. Surprisingly the trends of the curves are completely different with tg indicating some form of extra potential barriers suppressing the current which might be linked to the heterobarrier present in the nanowire structure.
Fig 5.9: Comparing output characteristics for top and bottom ground configuration in a representative, double row, device. The device is found batch #2-sample A. The transistor breaks at 2.2 V in bottom ground. Different segments can be identified with (a) being well saturated and (b) showing impact ionization that accelerates further in (c).
Conclusion & Outlook

The benefits of introducing an InGaAs/InAs heterostructure as channel material has proven necessary for improved stability of the transistors, with good saturation of $g_d$. In the end mixing of III-V materials is a great advantage and possibility when utilizing the bottom up approach with epitaxial growth of nanowires. Therefore this study has served to gain evidence of the quality and control of growth techniques. Initially the control of doping was questioned, if the in-situ doping would provide enough precision for doping of the short bottom segment present at the drain side while keeping the channel close to intrinsic (unintentionally doped). The typical characteristics of a junctionless transistor is bad modulation of current and a depletion type transistor (on-state by default). The processed transistors exhibit none of these behaviours with $V_t > 0$ V and $SS < 90$ mV/dec.

Quality of the bi-layer high-$\kappa$ is also surprisingly good (low $SS$ and gate leakage) and is likely connected to the state of the ALD chamber. Nonetheless it proves the presence of a good nanowire surface for the high-$\kappa$ interface and motivates further implementation of the bi-layer.

The created transistors are also commercially viable due to the III-V integration on top of silicon. The geometry itself has conceptually many benefits with its GAA configuration and decoupling of footprint area with the actual length of the device.

The DC characteristics are insufficient for further investigation of RF capabilities due to the high resistance of the structure $R_c \approx 1500\Omega \mu m$ and collapse of nanowires. Both of these problems can be addressed in the near future by utilizing shorter nanowires ($\sim 300$ nm), introducing annealing, better control of the ICP-RIE process and possibly using a highly doped overgrowth. The latter steps are necessary for improvement of the metal-semiconductor junction, notice that a change in top metal all together is also possible.

The orientation of the heterostructure lends itself to top grounded configuration with the drain pad situated at the bottom. Which might prove useful due to heat developing in the substrate rather than top contact. After creating matching networks and other necessary circuity, in addition to the devices, heat development in the substrate is convenient for efficient cooling.
References


   http://eceee.colorado.edu/~bart/book/moseb.htm/
   http://www0.cs.ucl.ac.uk/staff/ucadexq/projects/vlsi/report.pdf/ (2016-07-20)


[40] O. Triebl et al., "Reliability issues in High Voltage Semiconductors," Vienna University chapter 5.1, (2013)


The metrics for the first batch containing only one working transistor is included in this appendix.

Table A.1: Outlining all metrics for the best device in batch #1. Values are extracted from SEM inspections. All data is normalized to the total circumference of the nanowires. 1A mean value has been extracted from SEM inspections of other pads 2Bias conditions are chosen in active region of the transistor at $V_g = 0.5$ and $V_{ds} = 0.6V$.

<table>
<thead>
<tr>
<th>Batch #1 Metric</th>
<th>Value</th>
<th>Unit</th>
<th>remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>geometry pad</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td># of nanowires</td>
<td>107</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>diameter</td>
<td>31</td>
<td>nm</td>
<td>mean $^1$</td>
</tr>
<tr>
<td>high κ: Al$_2$O$_3$/HfO$_2$</td>
<td>10/40</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td>high κ thickness</td>
<td>4.5</td>
<td>nm</td>
<td>mean $^1$</td>
</tr>
<tr>
<td>gate length $L_g$</td>
<td>220</td>
<td>nm</td>
<td></td>
</tr>
</tbody>
</table>

| bottom ground $g_{m,peak}$ | 10 | mS/mm |
| SS                           | 103 | mV/dec |
| $g_d$                        | -  | mS/mm |
| $Q$                          | 0.097 | kS·dec/Vm |

| top ground $g_{m,peak}$ | 2.5 | mS/mm |
| SS                        | 92  | mV/dec |
| $g_d$                     | 0.10 | mS/mm |
| $Q$                       | 0.027 | kS·dec/Vm |
| $A_{V_{OC}}$              | 25  | - |
| $R_{ON}$                  | $940 \times 10^3$ | Ω·µm | bias $^2$ |