

Master's Thesis

# **Inductorless LNA and Harmonic-rejection Mixer for Wideband Direct-conversion Receiver**

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# Abstract

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In this master thesis, combinations of noise-canceling LNA and harmonic-rejection mixers are investigated and compared to find an optimal inductorless receiver front-end for low-band (600-960MHz) FDD LTE-A network. The work was carried out in a modem development project at Ericsson Modems, Lund. Three receiver versions with different harmonic rejection techniques are compared in terms of noise figure (NF) and power consumption and the receiver with 6 LO phases is selected for optimization. The LNA combines noise cancellation for matching stage and nonlinearity cancellation for output stages so both low noise figure and high linearity are achieved.

The final circuit show great potential for FDD LTE-A system with support up to 3 aggregated carriers for higher bandwidth. Low NF at 1.62 dB after the LNA and 1.75 dB after the mixer are observed from 0.4-1GHz. The LNA IIP2 is above 12 dBm and robust with process and temperature. Gain switching with possible reduction of 6 and 12 dB is integrated and the LNA linearity is not significantly suffered by low gain. Input return loss (S11) is better than -12dB regardless of gain, number of carriers and temperature (-30 – 110°C). Inductorless operation saves a lot of chip area and avoid dead package area, which then save cost and make the solution competitive.



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## Abbreviations

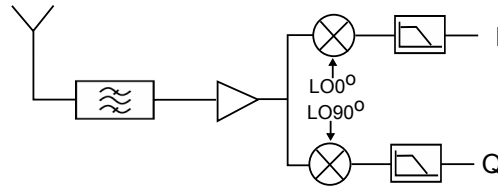
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DCR	Direct Conversion Receiver
IF	Intermediate Frequency
BER	Bit-error-rate
FDD	Frequency Division Duplex
LTE	Long Term Evolution
LTE-A	LTE-Advanced
WCDMA	Wideband Code-Division Multiple Access
LNA	Low Noise Amplifier
IM2	Second-order Intermodulation
IM3	Third-order Intermodulation
IIP2	Second-order Intercept Point
IIP3	Third-order Intercept Point
CA	Carrier Aggregation
LO	Local Oscillator
MIMO	Multiple Input Multiple Output
CMOS	Complementary Metal Oxide Silicon
TIA	Trans-impedance Amplifier
NC-LNA	Noise Canceling LNA
HRM	Harmonic Rejection Mixer
NF	Noise Figure
CP1	1dB Compression Point
CSFB	Common Source with Resistive Feedback
CG-CS	Common Gate Common Source
HR-Rx	Harmonic Rejection Receiver
VCO	Voltage-Controlled Oscillator



## 1.1 Cellular Direct-conversion Receiver Challenges

Direct-conversion receiver (DCR) has become the dominant receiver architecture for cellular terminals [1]. The composition of this architecture is depicted in Figure 1.1. The main advantage of DCR is the IF filter which is not required as in super-heterodyne architecture, which makes DCR easier to be fully integratable [1], [2]. The main drawback of DCR is from the second order nonlinearity which can intermodulate two adjacent input interferences and generate baseband component (IM2) at the difference frequency [2]. Since the wanted information signal after downconversion also resides at baseband, the signal spectrum is now altered which causes more errors (or higher bit-error-rate - BER) for subsequent processing. Another source of destructive baseband components is amplitude-modulated interferences, such as the strong leakage of transmitting signal (Tx leakage) in frequency-division duplex (FDD) systems (WCDMA, LTE FDD). Here the low-pass envelopes of the interferences appear at baseband due to the squaring of the interferences [2], [3] [4]. Since low-frequency components are easily removed at LNA-mixer interface by ac coupling, the mixer becomes the dominant nonlinear block, and a high input-referred intercept point (IIP2) is normally required for the mixer [2].



**Figure 1.1:** Direct-conversion receiver architecture.

IIP2 of LNA, however, is becoming more important with Carrier Aggregation (CA) technique [5] proposed for LTE-Advanced (LTE-A) networks. The user terminals can use (aggregate) up to 5 channels simultaneously to have wider bandwidth for data transmission rate up to 1Gb/s. The channels can be in the same band (intra-band CA) or in different bands (inter-band CA). In a simple use case,



the user terminal receives data in one band at  $f_{Rx1}$  and transceives data in another band at  $f_{Tx2}$  and  $f_{Rx2}$  and the two bands are far away enough from each other such that  $f_{Tx2} \approx 2f_{Rx1}$ , an interference which fulfills  $f_{int} = f_{Tx2} - f_{Rx1}$  can intermodulate with leakage of Tx2 and their IM2 product can fall directly on Rx1 channel. The interference is in-band with Rx1 channel so does not get attenuated by duplexer or RF filter. The IM2 product requires high IIP2 of the LNA to eliminate.

Another drawback of DCR is the LO self-mixing caused by LO signal mixing (multiplying) with its leakage at mixer's RF port [2]. The leaking is through mixer or substrate. The LO squared contains positive average dc level which can compress the baseband amplifier, hence making baseband processing impossible. The other drawbacks include mixer flicker noise and I/Q mismatch [2].

The DCR should be able to receive signals from as many bands as possible to be competitive and widely usable. As an example, to be fully functional for LTE networks, a frequency range from 450MHz to 3.8GHz must be supported [1], [6]. This opens the path for wideband front-end topologies, as integrating many narrowband front-ends into one chip is too area-consuming and complex (in routing, for instance), especially at low frequency bands where large inductors are often required. This fact is even more important in the context of Multiple-Input-Multiple-Output (MIMO) technique [7], in which multiple receiver chains are used and connected to separate antennas to exploit multipath propagation. The multiple number of receivers basically multiplies the area needed for receiver part in the modem chip.

Wideband operation, however, comes at the cost of wider spectrum for unwanted interferences and noise [8]. Besides nonlinearity, the front-end can produce in-band distortion through mechanisms such as harmonic mixing [8] and reciprocal mixing [9], [1]. Harmonic mixing is from LO signals which are preferably square wave to improve the switching time and linearity, hence consist of the fundamental sine wave LO and many higher order LO harmonics. The harmonics down-convert nearby interferences and noise floor to baseband. Noise floor at baseband rises up and the noise figure gets worse. This effect is also called noise folding.

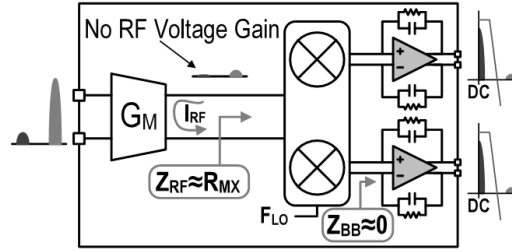
Reciprocal mixing, on the other hand, arises from phase noise of the fundamental LO, which manifests itself as noise sidebands in the left and right sides of the center fundamental LO tone. The phase noise down-converts interferences at its frequency to baseband, and the same issue of altering baseband signal spectrum occurs here.

Lastly, the challenges for DCR come from lower voltage supply in smaller CMOS technology [6]. For example, the supply reduces from 1.2V in 65nm technology to 1V in 28nm process. While moving down in device size helps improving the device cut-off frequency, the disadvantage is the lower voltage swing for amplifier stages. The amplifier is easy to be compressed and also the possible number of stacked transistor (in cascode stages, for example) is now reduced.

## 1.2 Recent Wideband Front-end Innovations

In recent years, a number of innovative techniques have been proposed to alleviate performance issues of the receiver front-end. Some of the key innovations are summarized below as they are used in this Thesis.

**Current-mode Front-end:** Recent developments in receiver architecture has led to the adoption of current-domain operation to replace the traditional voltage-domain operation [6], [8], [10], [11]. The LNA is replaced by an LNTA (transconductance stage) to obtain signal in current form, which then drives current-mode passive mixer. The advantage of passive mixer lies in its high linearity and low flicker noise [12]. The baseband signal current out of the mixer is converted back to voltage by a trans-impedance amplifier (TIA) stage. If the input impedance of the TIA is small, the voltage gain is really small throughout the signal path, and gain compression are alleviated. Figure 1.2 illustrates the concept of the current-domain receiver [12].



**Figure 1.2:** Current-domain receiver topology [12].

**Noise-canceling LNAs (NC-LNA):** The traditional wideband LNAs based on common-source (CS) or common-gate (CG) stages are theoretically limited at noise figure (NF) of 3dB due to  $g_m$ -constrained transistors for input matching [2]. Some improvement techniques such as feed-forward or feedback can lower NF of CG stage but require the use of large inductors at the output [2]. NC-LNAs were proposed [13], [14] to cancel noise of matching transistors without any inductors, so a much lower NF than 3dB were obtained.

**Harmonic-rejection Mixer (HRM):** This technique aims to alleviate harmonic mixing and noise folding by combining phase-shifted LO signals to obtain an effective LO close to sine wave. The higher odd LO harmonics are significantly rejected so the in-band distortion caused by them is reduced. The HRMs in [22], [15] cancel 3LO and 5LO harmonics while the HRM in [6] cancels 3LO.

## 1.3 Thesis Objectives and Organization

The thesis is focused on investigating inductorless direct-conversion receiver front-ends for low-band (600-960MHz) FDD LTE-A system. Besides reducing the chip area, inductorless front-ends avoid dead package area beneath an inductor so more package balls can be placed in case fan in wafer level packaging (FIWLP) is used

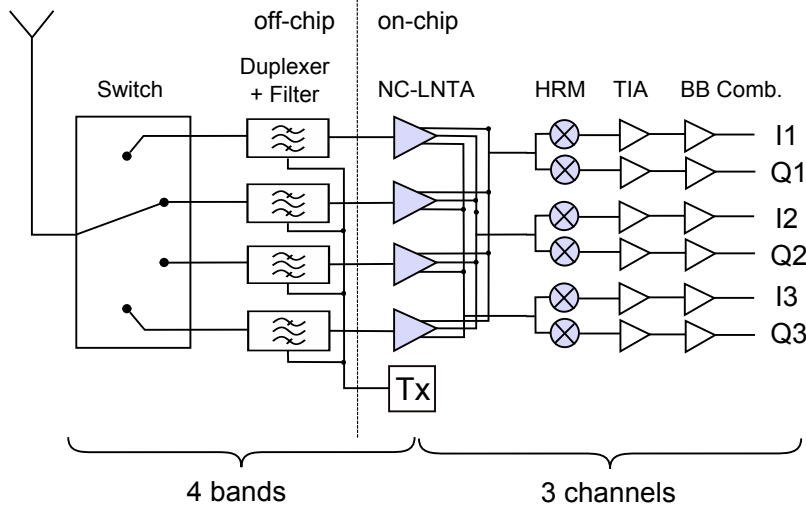
for the chip [16]. A simple carrier aggregation scenario with 1 Tx and 2 Rx is aimed, while 3 Rx option should be available with some degraded performance. The reason for aiming at 1 Tx is that the linearity requirements of LNA would be too stringent due to many strong Tx leakages in case multiple Tx are used. To fulfill the inductorless requirement, combination of NC-LNA and HRM is proposed. Also the front-ends should operate in current-domain to alleviate compression issue.

The rest of the thesis is organized as followed: Chapter 2 discusses the specifications for LNA and mixer and how the specifications should work for the given objectives. Chapter 3 reviews the literature of NC-LNA and HRM. Chapter 4 proposes LNA schematic and analyzes separate aspects of the circuit. Chapter 5 and 6 discuss the circuit design process and simulation results. Chapter 7 concludes the thesis and propose future work.

## Target Specifications and Explanation

### 2.1 Topology and Technology

The LNAs (LNTAs in fact) and mixers should work in topology shown in Figure 2.1, in which 4 identical LNTAs are muxed so that only one of them is active at a time for the desired band. To support aggregation of 3 carriers, the NC-LNTAs have 3 differential outputs to drive 3 separate mixers (HRM type). Output of each mixers is connected to a trans-impedance amplifier (TIA) so that voltage signal is obtained at baseband. The baseband combination blocks combine outputs from TIAs to obtain harmonic rejection.



**Figure 2.1:** Front-end Topology. The colored blocks are the focus of this Thesis.

The thesis is focused on implementing the LNAs and mixers. The rest of the front-end (LO, TIA, combination amplifiers) are ideal components. The design is aimed at schematic level and no layout is implemented. Due to the limit of time, the main focus is the LNAs and the mixers are implemented to compare noise

figure and power consumption of different harmonic rejection techniques. The mixer IIP2 is not simulated in the thesis.

The process choice is 28nm CMOS Bulk with 1V supply voltage.

## 2.2 LNA Specifications

The LNA specifications is shown in Table 2.1. Each specification is explained below.

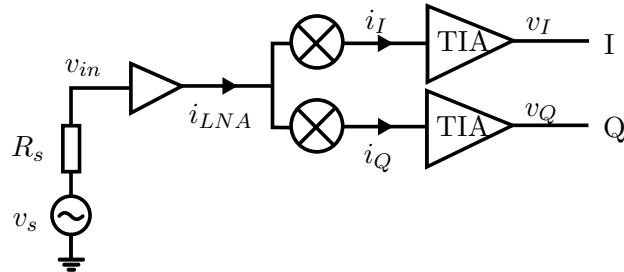
Parameters	Values
Type	Noise-canceling LNA
Supply Voltage	1V
Current Consumption	<20mA
Frequency Range	600-960 MHz
Temperature Range	-30-110°C
Transconductance to mixer output	17mS
Noise Figure	<1.5dB
CP1	>-15dBm
IIP3	>0dBm
IIP2	>15dBm
Source Impedance	50Ω
S11 (input return loss)	<-12dBm
Output Impedance	>1kΩ differential
Gain Control	0, -6 and -12 dB power gain reduction modes

**Table 2.1:** LNA Target Specifications.

**Transconductance:** The transconductance to mixer output is defined as:

$$g_{m\_total} = \frac{i_I}{v_{in}} = \frac{i_Q}{v_{in}} \quad (2.1)$$

where the quantities are illustrated in Figure 2.2.



**Figure 2.2:** Signal path in the receiver.

The  $g_{m\_total}$  depends on  $g_{m,LNA}$  and the mixer conversion gain, which is defined from the duty cycle of the LO signals (section 4.2.2).

**Noise Figure:** Noise performance is an important specification of RF blocks, as it directly limits the receiver sensitivity. The noise performance of a block is quantified by its noise figure (NF), which is the ratio of the signal-to-noise ratios at the input and output, as shown below:

$$NF = \frac{SNR_{input}}{SNR_{output}} = \frac{Total\ noise\ at\ output}{Noise\ at\ output\ due\ to\ source\ only} \quad (2.2)$$

The LNA noise and gain limit the noise figure of the whole receiver chain, as shown in Friis's equation for calculating noise figure of cascaded stages:

$$NF_{total} = NF_1 + \frac{NF_2}{G_1} + \frac{NF_3}{G_1 G_2} + \dots + \frac{NF_n}{G_1 G_2 \dots G_{n-1}} \quad (2.3)$$

In CMOS technology, the two dominant noisy devices are resistor and MOSFET. Resistor exhibits thermal noise represented as a white voltage noise source in series with an equivalent noiseless resistor. The power spectrum density of voltage noise is given as:

$$\overline{v_n^2} = 4kTR \quad (2.4)$$

Dominant noise sources in MOSFETs are thermal, gate-induced and flicker noise. The thermal noise arises from conducting channel and from gate resistor, in which the gate resistor noise can be made very small when a large number of gate fingers is used. The gate-induced noise is from the channel coupled capacitively to the gate, and is negligible if operating frequency is below the MOSFET cut-off frequency [2] (which is in range of 100 GHz [24]). Flicker noise power decreases with higher frequency, and is significant only at low frequency.

Since MOSFET in LNA works at high frequency, thermal noise is the most important noise source. The noise can be represented as a voltage source in series with the gate terminal, or a current source in parallel with the channel (Figure 2.3), and has a power spectrum density in saturation region given by [2]:

$$\overline{v_n^2} = \frac{4kT\gamma}{g_m} \quad (2.5)$$

or:

$$\overline{i_n^2} = 4kT\gamma g_m \quad (2.6)$$

where:

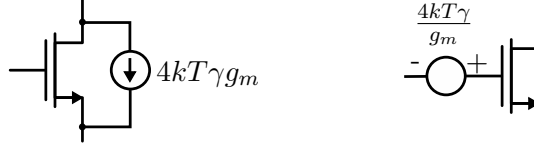
$k$  is the Boltzmann constant

$T$  is temperature (in Kelvin)

$\gamma$  is a process-dependent constant which is 2/3 for long channel transistor and is between 1-2 for short-channel device [2]

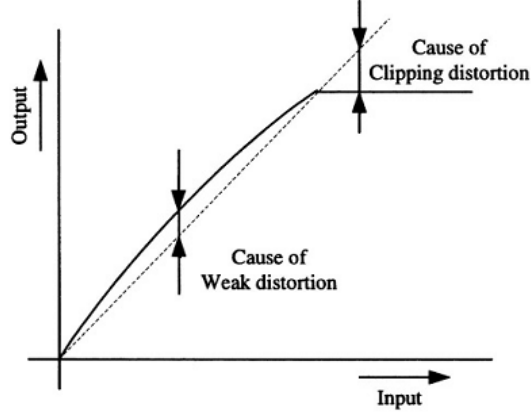
$g_m$  is transistor transconductance

The general way to reduce MOSFET noise is to increase its transconductance, and to use long channel to mitigate short-channel effect.



**Figure 2.3:** Representations of MOSFET thermal noise [2].

**Linearity:** Amplifiers are often assumed linear, in which the gain is constant with regard to the input level, so that powerful tools from linear model like transfer function can be used. However, due to the inherent nonlinearity of MOSFET, the amplifier linearity should be analyzed. The deviations from linear model are caused by clipping and by weak nonlinearity [19], as illustrated in Figure 2.4. Clipping occurs due to the limit in current and voltage of supply, which cause the flat response of output with increasing input level. The weak nonlinearity in long-channel transistor is mainly caused by nonlinear transconductance  $g_m$  with respect to  $V_{gs}$  and  $V_{ds}$ . In deep-submicron technology, the nonlinearity of output conductance  $g_{ds}$  becomes more prominent [20].



**Figure 2.4:** Deviations from linear model of amplifier [19].

Nonlinear characteristics cause many undesired effects for RF amplifiers. Due to clipping, gain compression occurs as the gain is reduced with high input level. The input level for the gain to reduce 1dB compared to the small-signal gain is called 1dB compression point (CP1). The second nonlinear effect is desensitization, or blocking, in which a large input interference can lower gain at wanted signal frequency, hence desensitize the amplifier. Harmonic distortion (HD) and intermodulation distortion (IMD) are other two important effects. If there are two tones at input with frequency  $f_1$  and  $f_2$ , the output spectrum includes all sum and difference of the input tone harmonics  $m.f_1 \pm n.f_2$ , where  $m$  and  $n$  are integer numbers. High order harmonics are normally weak and far from input tones so can be removed by filter. The 2nd and 3rd order intermodulation products (IM2 and IM3) at  $f_1 - f_2$ ,  $2f_1 - f_2$  and  $2f_2 - f_1$  may easily fall within the signal bandwidth and therefore alter the signal spectrum, leading to errors in demodulation.

In this thesis, 1dB cross compression point is used instead of the standard compression point. Suppose at the input there are small wanted signal and a large interference. The large interference cross modulates with the signal and produces distortion component at the signal frequency [4]. CP1 is defined as the power level of the interference to lower the signal gain by 1 dB.

Input-referred second-order and third-order intercept points (IIP2 and IIP3) are used to quantify intermodulation distortion in RF circuits. In this thesis, two-tone test is used to define IIP2 and IIP3. Suppose at LNA input, there are tones at receiving frequency ( $f_{Rx}$ ), leakage transmitting frequency ( $f_{Tx}$ ) and a blocker (interference) frequency ( $f_{Blc}$ ). The input tone powers are  $P_{Rx,in}$ ,  $P_{Tx,in}$  and  $P_{Blc,in}$ . The power of IM2 and IM3 products at output are denoted as  $P_{IM2}$  and  $P_{IM3}$ .  $G_{LNA}$  denotes LNA power gain with referred to  $50\Omega$  load at  $f_{Rx}$ . Table 2.2, equations 2.7 and 2.8 show conditions and calculation of IIP2. Table 2.3, equations 2.9 and 2.10 show conditions and calculation of IIP3.

Parameters	Values	Parameters	Values
$f_{Rx}$	729 MHz	$P_{Rx,in}$	-60 dBm
$f_{Tx}$	1428 MHz	$P_{Tx,in}$	-26 dBm
$f_{Blc}$	$f_{Tx} - f_{Rx}$	$P_{Blc,in}$	-30 dBm

**Table 2.2:** Conditions for measuring IIP2

$$f_{IM2} = f_{Tx} - f_{Blc} \quad (2.7)$$

$$IIP2 = P_{Tx,in} + P_{Blc,in} - P_{IM2} - G_{LNA} \quad (2.8)$$

Parameters	Values	Parameters	Values
$f_{Rx}$	729 MHz	$P_{Rx,in}$	-60 dBm
$f_{Tx}$	699 MHz	$P_{Tx,in}$	-26 dBm
$f_{Blc}$	$(f_{Tx} + f_{Rx})/2$	$P_{Blc,in}$	-30 dBm

**Table 2.3:** Conditions for measuring IIP3

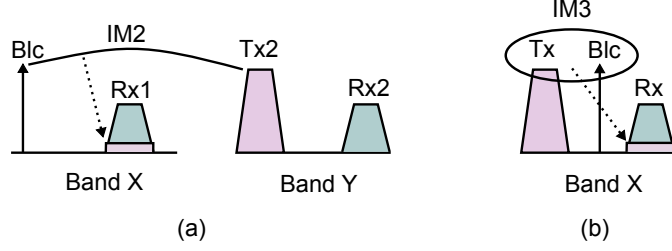
$$f_{IM3} = 2f_{Blc} - f_{Tx} \quad (2.9)$$

$$IIP3 = \frac{P_{Tx,in} + 2P_{Blc,in} - P_{IM3} - G_{LNA}}{2} \quad (2.10)$$

The IIP2 test case above illustrates a situation when 2 carriers at different bands are used for downlink data. The blocker is in-band with the Rx and can be strong. Figure 2.5(a) depicts the test case.

In the IIP3 test case, the blocker frequency is at the middle of receiving and transmitting frequencies (also called half duplex distance case). This scenario is not necessarily from carrier aggregation as it can happen for single carrier as well. Figure 2.5(b) depicts the test case.





**Figure 2.5:** (a) IM2 product when 2 carriers are aggregated.  
 (b) IM3 product in case of single carrier (half duplex distance case).

In cascaded RF stages, the total CP1, IIP2 and IIP3 can be calculated from individual CP1, IIP2 and IIP3 of each stage. Suppose two blocks A and B are cascaded, in which A is in front of B, equations 2.11, 2.12 and 2.13 show the calculation of total nonlinearity quantities [21].

$$\frac{1}{CP1_{total}} = \frac{1}{CP1_A} + \frac{A_{vA}^2}{CP1_B} \quad (2.11)$$

$$\frac{1}{\sqrt{IIP2_{total}}} = \frac{1}{\sqrt{IIP2_A}} + \frac{A_{vA}}{\sqrt{IIP2_B}} \quad (2.12)$$

$$\frac{1}{IIP3_{total}} = \frac{1}{IIP3_A} + \frac{A_{vA}^2}{IIP3_B} \quad (2.13)$$

where CP1, IIP2 and IIP3 are in power unit.

The above equations show the reduction of input-referred linearity from stage B due to the voltage gain  $A_{vA}$  of stage A. Comparing with Friis' formula (equation 2.3), it can be seen a trade-off between noise and linearity with respect to choosing voltage gain of first stages in RF front-end.

**Source Impedance and Input Matching:** The LNA input impedance is often desired to be  $50\Omega$  to reduce reflected power and to meet the standardized  $50\Omega$  load impedance of the band-pass filter [2]. Shown in Figure 2.6, the off-chip filter is connected to the LNA through a transmission line with characteristic impedance of  $Z_0 = 50\Omega$  and an unknown length. If the LNA input impedance is not  $50\Omega$ , the load impedance seen by the filter will deviate from its standard  $50\Omega$ , which affect the filter's return loss and ripple characteristics [2]. An input impedance of  $50\Omega$  of LNA also matches with the transmission line characteristic impedance, hence maximizes power transfer.

Input matching is quantified by the input return loss ( $S_{11}$ ), which is the ratio of reflected power and the incident power. The expression of  $S_{11}$  is given by [2]:

$$S_{11}(dB) = 10 \log_{10} \left| \frac{Z_{in,LNA} - Z_0}{Z_{in,LNA} + Z_0} \right|^2 \quad (2.14)$$

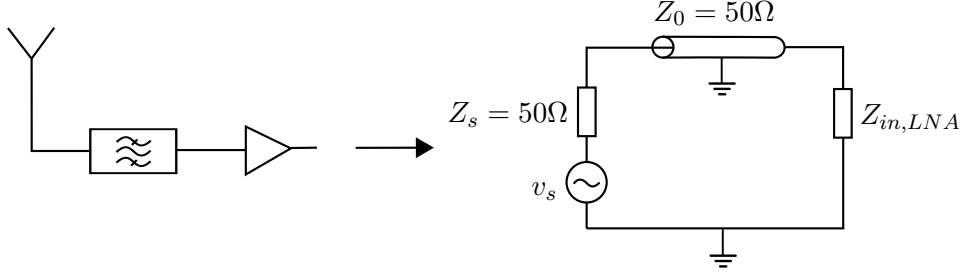


Figure 2.6: Input circuit of LNA.

**Output Impedance:** The LNA output impedance  $r_{out}$  needs to be large enough to not affect the current flowing to the LNA load. Figure 2.7 shows the signal equivalent circuit with the LNA driving load (input impedance of mixer and TIA  $Z_{in,Mixer}$ ) and  $r_{out}$ . The current flowing into the load is given by:

$$i_L = g_m v_{in} \frac{r_{out}}{r_{out} + Z_{in,Mixer}} = g_m v_{in} \frac{1}{1 + \frac{Z_{in,Mixer}}{r_{out}}} \quad (2.15)$$

The ratio  $Z_{in,Mixer}/r_{out}$  needs to be as small as possible, so that most of the LNA output current flows into the TIA and does not depend on  $Z_{in,Mixer}$ . In this thesis,  $Z_{in,Mixer}$  is estimated to be 30-50Ω differential and a value of 1kΩ differential is targeted for  $r_{out}$ .

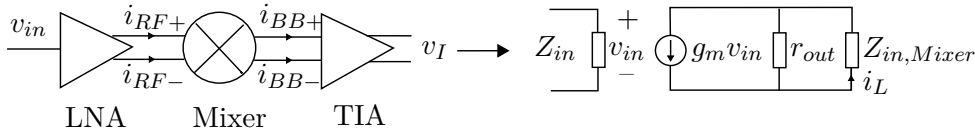


Figure 2.7: LNA output circuit.

**Gain Control:** During operation, the receiver can sense signal with power from weak to strong depending on the distance from the receiver to the base station. A dynamic range of 100dB can be possible for signal in cellular network [2]. The strong signal can easily drive the LNA into compression which is undesirable. To eliminate this problem, the LNA should be designed with several gain stages in parallel that can be turned on or off independently, so that the total gain can be reduced for strong input signal. In this thesis, 3 power gain reduction levels of 0dB (for weak signal), -6dB (for medium signal) and -12dB (for strong signal) are targeted. Equivalently, the LNA transconductance needs to reduce by 1, 2, and 4 times, respectively.

The gain reduction will lead to degraded performance of the LNA. Noise figure will increase as transconductance is decreased. However, the linearity should be the same or higher to tolerate stronger interferences from close base station. Current consumption should be reduced as smaller gain is needed.

## 2.3 Mixer Specifications

Parameters	Values
Type	Harmonic-Rejection Double-balanced Passive Mixer
3LO Rejection	>10dB
in-band IIP2	>70dBm

**Table 2.4:** Mixer Target Specifications

**LO Harmonic Rejection:** In the traditional double-balanced passive mixer with 25% duty cycle LO, the even-order LO harmonics are rejected but the odd-order ones still remain, which cause the LNA noise to be folded into baseband. Assume LNA noise floor is flat, the increase of noise figure due to noise-folding effect is given by (section 3.3.1):

$$NF_{penalty} = 10\log(1 + \frac{1}{9} + \frac{1}{25} + \dots) = 0.7dB \quad (2.16)$$

Here the terms  $1/9, 1/25, \dots$  are power of 3LO, 5LO and higher order odd harmonics divided by power of fundamental LO frequency.

In case harmonic rejection technique is applied for mixer, the harmonic power can be significantly reduced, hence the folded noise power is less. A minimum rejection of 10dB is targeted for the 3LO harmonic, which will improve the noise figure by 0.5dB, as shown below.

$$NF_{penalty} = 10\log(1 + \frac{1}{90} + \frac{1}{25} + \dots) = 0.2dB \quad (2.17)$$

**In-band IIP2:** The mixer intended to use in this thesis is of double-balanced type. In this mixer, the IIP2 depends on the mismatch between switch transistors and the mismatch between two differential LNA output branches [2]. IIP2 needs to be measured from Monte-Carlo simulation, in which transistor mismatch is taken into account. Due to the lack of time and the focus of mixers is for the harmonic rejection function, the IIP2 of mixers is not simulated in this Thesis.

This chapter reviews traditional wideband techniques for LNA and the recently proposed noise-canceling LNA (NC-LNA) topologies. The traditional LNAs have a lower limit for noise figure due to input matching, or require to use inductor to reach large voltage gain. The NC-LNAs relax the noise-matching trade-off so a much lower NF can be achieved, and inductor is not necessary.

The third part of the chapter explains the concept of harmonic-rejection mixer (HRM) to alleviate harmonic mixing and noise-folding effects. Two HRM topologies using 8 phase or 6 phase LO signals are described.

## 3.1 Traditional Wideband LNA Topologies

### 3.1.1 Common-Source Stage with Resistive Feedback

The CS stage with resistive feedback (CSFB) is shown in Figure 3.1. Here the input signal gets amplified by both PMOS and NMOS, so a higher transconductance  $g_m$  can be obtained compared to the case only one transistor is used, assumed that the same current is consumed. Also the noise figure is better for the former case [2].

Assume the output resistance of transistors and load resistance are infinite, the input resistance looking into the CS stage is given by [2]:

$$R_{in} = \frac{1}{g_{m1}} + \frac{1}{g_{m2}} \quad (3.1)$$

where  $g_{m1}$  and  $g_{m2}$  are transconductance of  $M_1$ ,  $M_2$ , respectively. The voltage gain is calculated by:

$$A_v = \frac{v_{out}}{v_{in}} = 1 - \frac{R_f}{R_s} \quad (3.2)$$

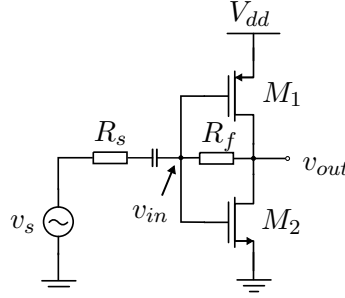
For the input to be matched,  $R_{in}$  must be equal to  $R_s$ . Since  $R_{in}$  does not depend on frequency (the gate capacitance of  $M_1$  and  $M_2$  will affect input impedance, but only at high frequency), the input matching is wideband.

The total transconductance of transistors is fixed, and so is the noise contribution from them. The feedback resistor also contributes to the total noise figure, which is expressed by [2]:

$$NF = 1 + \gamma + \frac{4R_s}{R_f} \quad (3.3)$$

For  $\gamma \approx 1$ ,  $NF > 3dB$  even if  $R_f$  is made much greater than  $R_s$ .

In reality, the finite output resistance and load modify the input resistance and lower the gain. Input matching is decreased and a higher transconductance from transistors is required to compensate. As a result, a lower NF can be obtained.



**Figure 3.1:** CS stage with resistive feedback. Load resistance is assumed infinite.

### 3.1.2 Common-Gate Stage

The common-gate stage schematic is shown in Figure 3.2 [2]. Here  $L_1$ - $C_1$  tank resonates at the desired channel frequency and acts as a channel-select filter.  $R_1$  is the equivalent resistor in parallel with  $L_1$ . The input resistance of the stage is  $R_{in} \approx 1/g_m$  and is wideband. Also the voltage gain and noise figure are given by:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{R_1}{R_s} \quad (3.4)$$

$$NF = 1 + \gamma + \frac{4R_s}{R_1} \quad (3.5)$$

As in the case of common-source stage,  $NF > 3dB$  for common-gate stage. This also comes from the required condition for input match  $g_m = 1/R_s$ .

Several techniques have been proposed to break the matching-noise trade-off of CG stages. Figure 3.3 show positive feedback and feedforward techniques [2].

The feedback path acts to increase the input resistance of CG stage, therefore a higher transconductance and a lower noise is allowed for the transistor.

$$R_{in,fb} = \frac{1}{g_m} + AR_1 \quad (3.6)$$

For input matching,  $R_{in,fb} = R_s$ , hence  $g_m$  can be calculated as:

$$g_m = \frac{1}{R_s - AR_1} \quad (3.7)$$

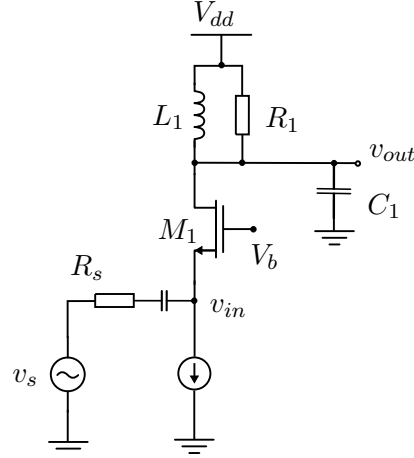


Figure 3.2: CG stage.

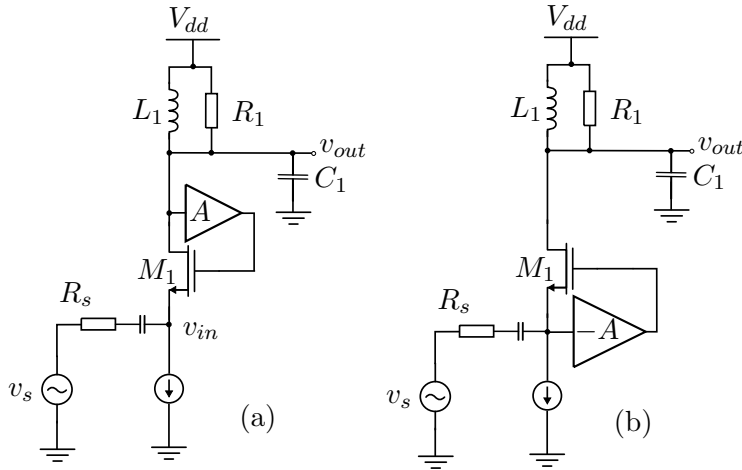


Figure 3.3: CG stage with (a) positive feedback (b) feedforward.

This value is higher than  $1/R_s$  as in case of normal CG stage, hence the transistor generates less thermal noise. The noise figure is given by Equation 3.8 [2], which show a lower NF can be obtained by raising  $g_m$ .

$$NF_{fb} = 1 + \frac{\gamma}{g_m R_s} + \frac{R_s}{R_1} \left(1 + \frac{1}{g_m R_s}\right)^2 \quad (3.8)$$

The feedforward technique is also called  $g_m$ -boosted technique as the input impedance is lowered by the feedforward gain [2]. The input-referred noise contribution of  $M_1$  is also reduced by the same factor, leading to lower noise figure.

$$R_{in,ff} = \frac{1}{g_m(1 + A)} \quad (3.9)$$

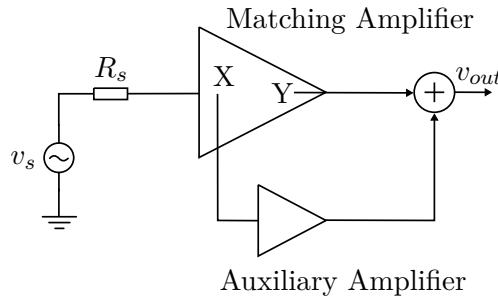
$$NF_{ff} = 1 + \frac{\gamma}{1 + A} + \frac{4R_s}{R_1} \quad (3.10)$$

In all above variants of CG stage, NF can be significantly reduced, but the inductive load is necessary to provide required high  $R_1$  for high voltage gain and to lower the noise. The inductor also resonates with the output capacitance at channel frequency to lower the amplifier noise floor at high frequency to mitigate noise folding. Inductor, on the other hand, is area-consuming, especially for low-band operation. Noise-canceling techniques combined with harmonic-rejection mixers can provide alternative approaches to settle the above mentioned issues without the use of inductors.

## 3.2 Noise-canceling Topologies

### 3.2.1 Noise-canceling Principle

The principle of noise-canceling LNAs (NC-LNA) is illustrated in Figure 3.4. The amplifier includes two amplifying stages in parallel, in which one stage is for input matching. Two nodes X and Y are selected inside the matching stage such that the signals there appear in-phase and the noise from matching active device appears there out of phase [2]. An auxiliary amplifier then amplifies both noise and signal from node X such that the noise level becomes the same with noise level at node Y. If a summation stage is placed at the output, the noise from X and Y will cancel each other, while the signals will add up. The noise from active device of matching stage is canceled, which means the  $\gamma$  terms in Equations 3.3 and 3.8 are now nulled.



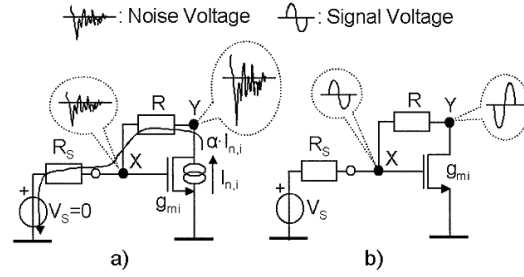
**Figure 3.4:** Conceptual schematic of noise-canceling LNAs [2]

The auxiliary amplifier also contributes noise, but since its gain and device transconductance can be set quite high, the noise can be small. Overall, the noise figure of LNA is significantly improved.

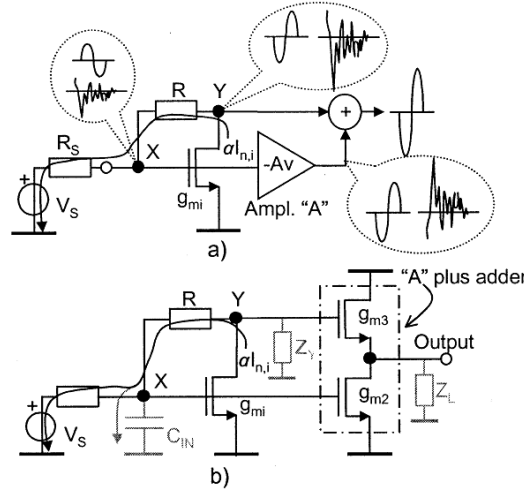
NC-LNA topologies has been published for both the basic CSRF and CG amplifiers (matching amplifiers). The resistive feedback NC-LNA was proposed in 2004 [13], and the common-gate-common-source LNA was introduced in 2008 [14]. The two topologies are summarized in the next sections.

### 3.2.2 CS Stage with Resistive Feedback

The X and Y nodes are identified for CSRF matching stage as shown in Figure 3.5. The thermal noise of NMOS is represented as a current source  $I_{n,i}$  in parallel with its channel. The noise current flows through the feedback resistor  $R$  and the source resistor  $R_s$  to ground, therefore the noise voltage at X and Y nodes are in-phase. On the other hand, the common-source stage provides a negative gain, so the signal voltages at X and Y nodes are out of phase.



**Figure 3.5:** Phase comparison of (a) matching transistor noise and (b) signal at nodes X and Y [13].



**Figure 3.6:** (a) Matching transistor noise is canceled at output (b) LNA schematic [13].

Figure 3.6(a) shows the noise-cancellation when an inverting auxiliary amplifier is added. The amplifier gain must be selected so the noise level at its output is equal to the noise level at the Y node. The value of gain is given by Equation 3.11 [13].

$$A_v = 1 + \frac{R}{R_s} \quad (3.11)$$



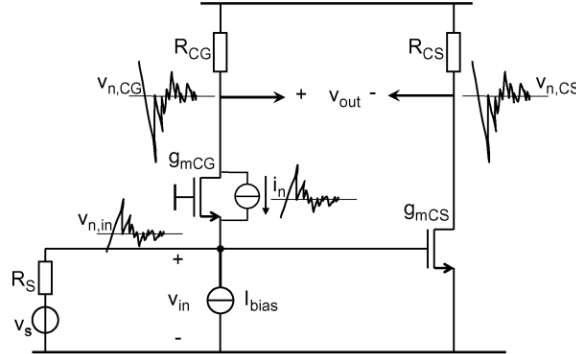
The noise figure of LNA now is limited by the feedback resistor and the noise from auxiliary gain stage, which are not constrained by matching requirement. A NF of 2dB was achieved in [13] for frequency range 250-1100 MHz.

The resistive feedback NC-LNA in [13] generates single-ended output, which is not favorable in RF design. Differential output is more preferred to reduce second-order distortion and power supply noise [14]. The topology can be modified so that differential signal is obtained at output by removing the summation stage and adding an inverting amplifier after the matching stage. However, the auxiliary gain required for balanced differential output is different from the gain for noise-canceling (see section 4.1.2), so if balanced output is desired, the noise from matching stage is not completely canceled.

The common-gate-common-source LNA (CG-CS) can provide both noise-canceling and balanced output simultaneously, which make it very attractive. The topology was proposed in 2008.

### 3.2.3 Common-Gate-Common-Source LNA

Figure 3.7 shows the schematic of this type of NC-LNA. Here the common-source stage provides inverting function to invert the noise polarity produced by the matching common-gate stage. With the condition that the voltage gains of CS and CG stages are equal in magnitude, both output balance and CG noise cancellation can be achieved [14]. The common voltage gain is given by equation 3.12.



**Figure 3.7:** Noise cancellation in CG-CS LNA [14].

$$A_{v,CS} = -A_{v,CG} = -\frac{R_{CG}}{R_S} \quad (3.12)$$

where:

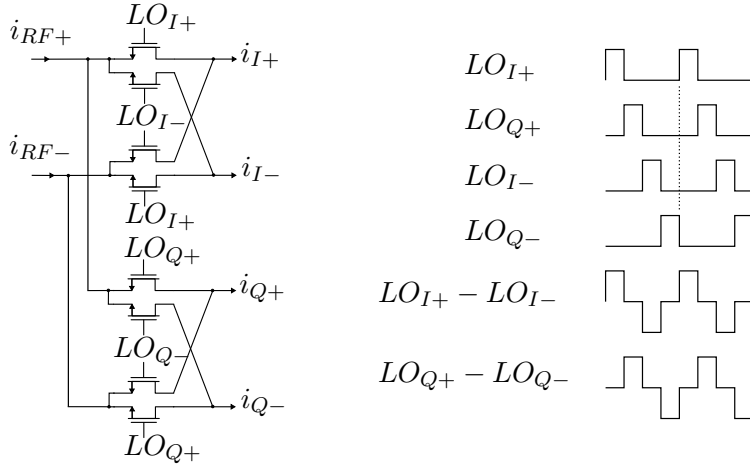
$$A_{v,CS} = -g_{m,CS}R_{CS} \quad (3.13)$$

The CS transconductance can be made large to reduce its thermal noise, provided that the resistor  $R_{CS}$  is scaled down to fulfill Equation 3.12. The LNA achieves noise figure of 3 dB in range 0.2-2 GHz.

### 3.3 Harmonic Rejection Mixer (HRM)

#### 3.3.1 Noise-folding Effect

The traditional receiver system uses passive double-balanced mixers, as shown in Figure 3.8. LO signals are 25% duty cycle non-overlapping square waves. The output current of the mixers is given by equation 3.14.



**Figure 3.8:** Passive double-balanced I-Q mixers with 25% duty cycle non-overlapping LO signals.

$$i_{I+} = i_{RF+} \text{sgn}(LO_{I+}) + i_{RF-} \text{sgn}(LO_{I-}) = i_{RF+} \text{sgn}(LO_{I+} - LO_{I-}) \quad (3.14)$$

where  $\text{sgn}()$  is the sign function. The *effective* LO waveform  $LO_{eff} = LO_{I+} - LO_{I-}$  is shown in Figure 3.8. Taking Fourier series expansion of the right side of equation 3.14 to get:

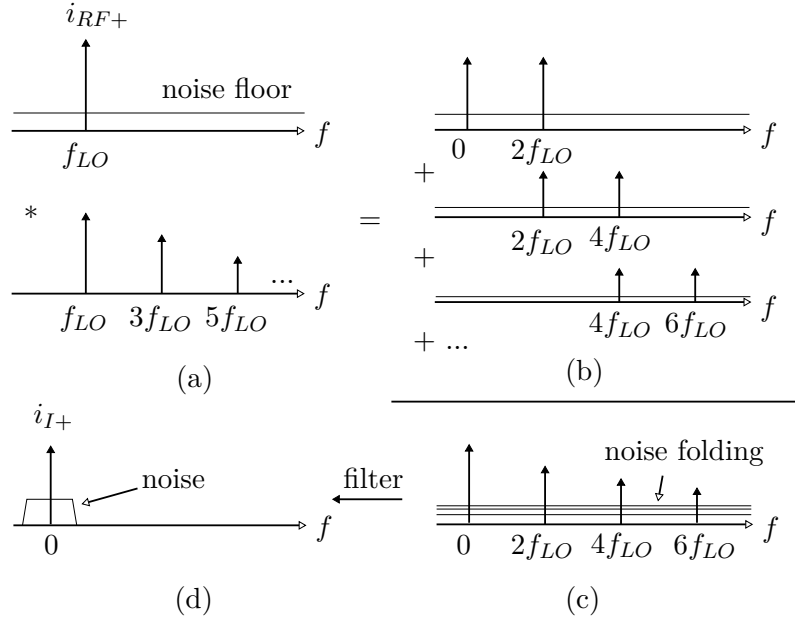
$$i_{I+} = \frac{2\sqrt{2}}{\pi} i_{RF+} \left[ \cos\left(\omega_{LO}t - \frac{\pi}{2}\right) + \frac{1}{3} \sin\left(3\omega_{LO}t - \frac{\pi}{2}\right) + \frac{1}{5} \cos\left(5\omega_{LO}t - \frac{\pi}{2}\right) + \dots \right] \quad (3.15)$$

The effective LO includes only the odd-order harmonics with decreasing magnitude. These LO harmonics down-convert noise at around their frequencies to baseband, so the total noise at baseband is increased. This noise-folding effect is illustrated in Figure 3.9. The noise figure increase due to noise folding is expressed by:

$$NF_{penalty} = 1 + \frac{1}{9} + \frac{1}{25} + \dots \approx 0.7dB \quad (3.16)$$

where  $1/9$ ,  $1/25$  are power ratios of 3LO, 5LO harmonics in  $LO_{eff}$  compared to the fundamental LO.

Several mixer architectures have been proposed to cancel odd order LO harmonics. The next sections examine two architectures which use LO with 8 phases and 6 phases.



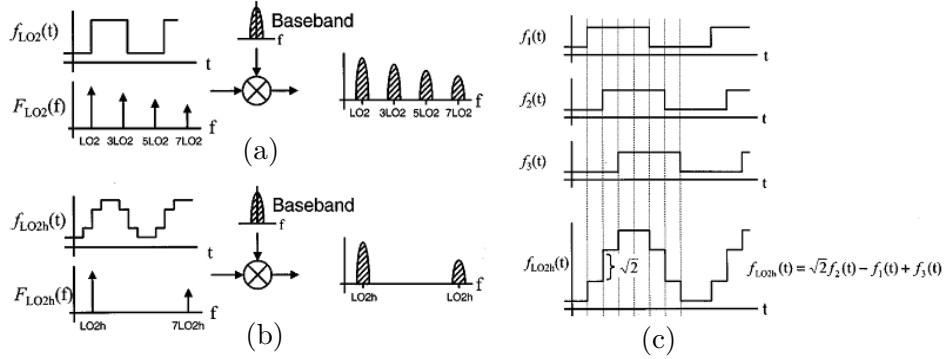
**Figure 3.9:** Noise folding effect: (a) Convolution of  $i_{RF+}$  and  $LO_{eff}$  (b) Sum of convoluted terms (c) Noise folding (d) Signal and noise after baseband filter.

### 3.3.2 8LO HRM

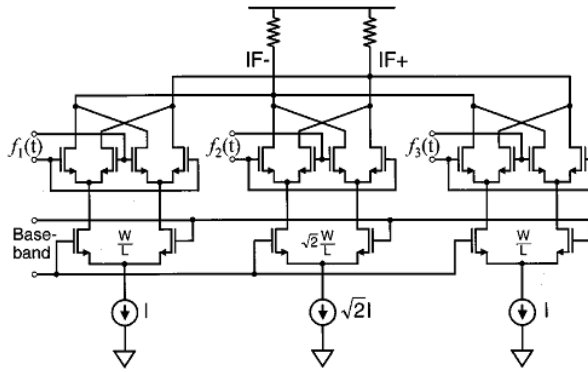
The first mixer architecture for rejecting LO odd harmonics was proposed by Weldon [22] and was aimed for up-conversion mixers in RF transmitter. The idea is to modify the waveform of  $LO_{eff}$  such that it is close to the fundamental LO sine wave. As shown in Figure 3.10 for I channel only, by summing three square-wave LOs which are  $45^\circ$  shifted from each other (equivalent to  $1/8$  period), and scaling the second LO by a factor of  $\sqrt{2}$ , an  $LO_{eff}$  is obtained which contains no 3LO and 5LO spectral components.

The mixer schematic includes three Gilbert multiplier cells (Figure 3.11), in which a tail current source of  $\sqrt{2}I$  is used for the second LO cell to increase  $g_m$  of its input transistors, so the  $\sqrt{2}$  ratio can be implemented.

The rejection efficiency is limited by the accuracy of implemented  $\sqrt{2}$  ratio, the gain mismatch of transistors and the phase error of LO signals. If a perfect  $\sqrt{2}$  is generated, and assume  $1^\circ$  phase error together with 1% matching error, approximately 35 dB of rejection is obtained for both 3LO and 5LO [22].



**Figure 3.10:** (a) Harmonic mixing with normal mixer, (b) rejection of 3LO and 5LO with modified  $LO_{eff}$ , (c) Generation of  $LO_{eff}$  [22].



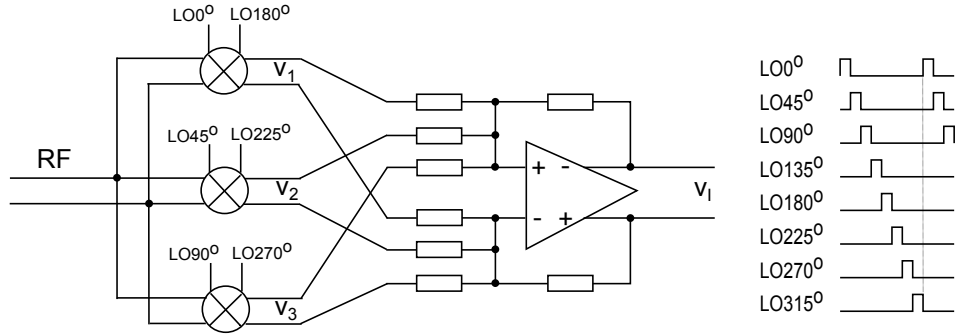
**Figure 3.11:** Harmonic-rejection mixer schematic [22].

Another approach to implement this HRM was introduced by Molnar [15], as shown in Figure 3.12. A 3-input differential amplifier sums up the baseband signals out of the 3 mixers. The gain ratio  $1 : \sqrt{2} : 1$  is implemented by scaling the input resistors of the amplifier. The output voltage can be written as:

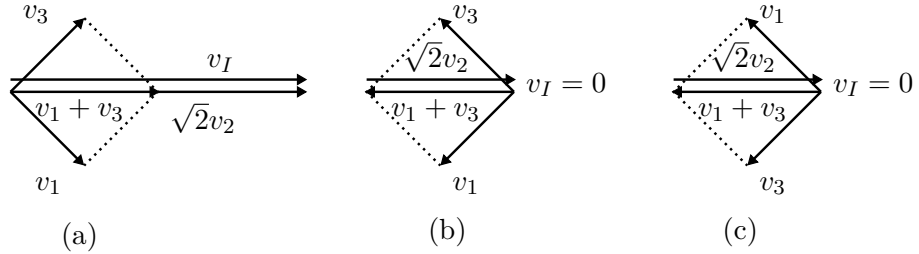
$$v_I = v_1 + \sqrt{2}v_2 + v_3 \quad (3.17)$$

Figure 3.13 shows the vector diagrams to understand the nature of harmonic rejection. At  $f_{RF} = f_{LO}$  the vectors  $v_1 + v_3$  and  $\sqrt{2}v_2$  are of same direction and the sum vector  $v_I$  is equal to  $2\sqrt{2}v_2$ . For  $f_{RF} = 3f_{LO}$  and  $f_{RF} = 5f_{LO}$ , the angles between  $v_1$ ,  $v_2$  and  $v_3$ ,  $v_2$  are now  $135^\circ$ , so  $v_1 + v_3$  is now opposing and cancels  $\sqrt{2}v_2$ , so the sum vector  $v_I$  is zero.

The 8LO HRM architectures has found wide applications in wireless receivers and wideband TV tuners.



**Figure 3.12:** (left) HRM proposed by Molnar (right) LO signals.



**Figure 3.13:** Vector diagram at (a)  $f_{RF} = f_{LO}$  (b)  $f_{RF} = 3f_{LO}$  (c)  $f_{RF} = 5f_{LO}$ . The 3LO and 5LO components are rejected.

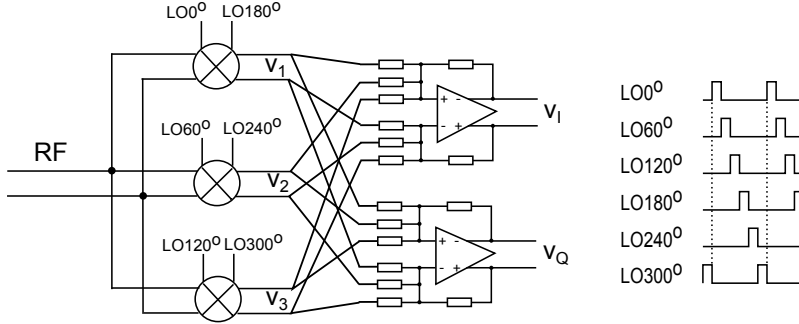
### 3.3.3 6LO HRM

To generate quadrature baseband signals, the 8LO HRM needs 8 LO phases to drive 4 mixers. For RF receivers, the 5th LO can be outside the frequency range of the system [6] and is already suppressed by LNA bandwidth. The 3rd LO harmonic is still harmful and needs to be rejected. The technique proposed in [6] aims to remove the 3LO only and 3 mixers need to be used instead of 4, so chip area is saved, and the mixer capacitance load for the VCO is reduced. Figure 3.14 shows the circuit in details.

The generation of I, Q signals includes 2 steps: First, a set of intermediate signals  $v'_1, v'_2, v'_3$  is established from  $v_1, v_2, v_3$  in such a way that they do not have 3LO components. Second, I, Q signals are built from intermediate signals so  $v_I$  and  $v_Q$  are 90° shifted from each other.

The following equations show calculations for each steps.

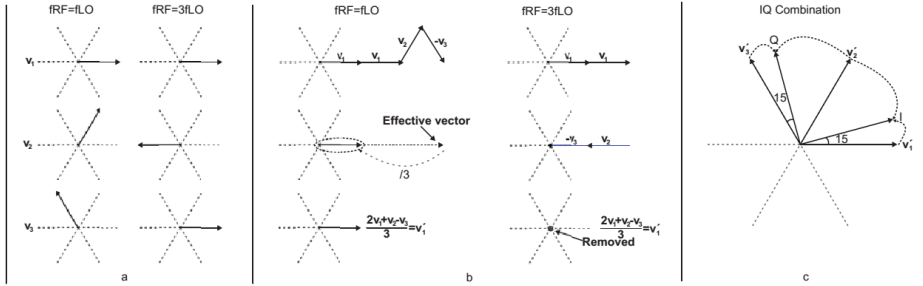
$$\begin{aligned} v'_1 &= (2v_1 + v_2 - v_3)/3 \\ v'_2 &= (2v_2 + v_1 + v_3)/3 \\ v'_3 &= (2v_3 - v_1 + v_2)/3 \end{aligned} \quad (3.18)$$



**Figure 3.14:** 6LO HRM proposed by Nejdel: (left) Schematic, (right) LO signals.

$$\begin{aligned} v_I &= (1 + \sqrt{3})v_1' + v_2' \\ v_Q &= (1 + \sqrt{3})v_3' + v_2' \end{aligned} \quad (3.19)$$

Figure 3.15 explains in vector diagram how intermediate signals are nulled around  $f_{RF} = 3f_{LO}$ , and the relative direction of I-Q signals with the intermediate ones.



**Figure 3.15:** 3LO rejection and quadrature generation [6]: (a) Relative direction of  $f_{LO}$  and  $3f_{LO}$  components of  $v_1, v_2, v_3$  (b) Generation of intermediate signals to preserve  $f_{LO}$  and reject  $3f_{LO}$  component (c) Generation of I-Q signals.

Combining equation 3.18 and 3.19 to obtain relation between I-Q signals and signals at mixer outputs. This relation is used to select values for resistors of the differential amplifier.

$$\begin{aligned} v_I &= \frac{(\sqrt{3} + 2)v_1 + (\sqrt{3} + 1)v_2 - v_3}{\sqrt{3}} \\ v_Q &= \frac{-v_1 + (\sqrt{3} + 1)v_2 + (\sqrt{3} + 2)v_3}{\sqrt{3}} \end{aligned} \quad (3.20)$$

The 6LO HRM achieved a 3LO rejection ratio of 40 to 50 dB up to signal frequency of 3.5 GHz and then reduces with higher frequency.

One possible problem is the 3LO components exist at the input of the differential amplifier and only get nulled after it. A strong interference at  $3f_{LO}$  can drive the amplifier to compression which is undesired. The author in [6] mentioned to use 33% duty-cycle LOs as an alternative to drive the mixers, as there is no 3LO component with 33% square wave and the interference can be canceled by the mixers. This alternative technique reached 30-40 dB rejection ratio over the frequency range.

# Circuit Analysis

This chapter is for a detailed analysis of circuit properties. The NC-LNA and HRM are investigated for important metrics, together with methods to improve those metrics. The circuit insight gained will be used in the next chapter on circuit designing.

## 4.1 LNA Analysis

### 4.1.1 Initial Schematic and Operation

The NC-LNA in this Thesis starts with the circuit shown in Figure 4.1. The matching stage is common-source with resistive feedback. Since current output are desired to drive the current mode mixers, a transconductance stage  $g_{mA}$  is added after the common-source. Another transconductance stage  $g_{mB}$  acts as the auxiliary stage. If  $g_{mA}$  and  $g_{mB}$  are both negative and properly selected, the noise from *inv* stage is canceled.

$g_{mA}$  and  $g_{mB}$  stages base on push-pull stage to combine transconductance of PMOS and NMOS. This configuration improves linearity, especially IIP2 to meet the IIP2 specification, as explained in section 4.1.4.

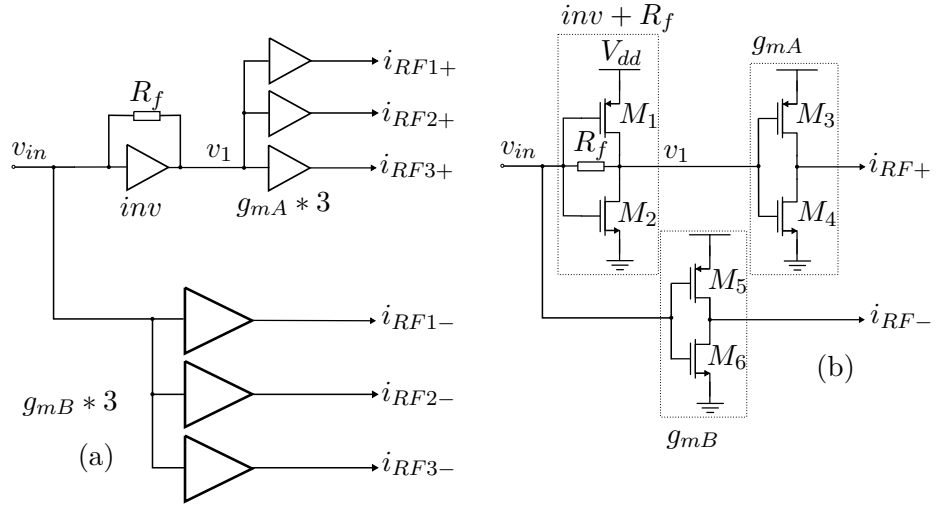
Most of the analysis in this chapter is for the LNA with 1 output port (Figure 4.1(a)). Some analysis involve the LNA with 3 output ports and will be clearly stated.

### 4.1.2 Input Matching

The input matching of the common-source stage was discussed in Section 3.1.1. The main difference when moving to noise-canceling is the large gate capacitance of the 3  $g_{mB}$  stages due to the required large transistors to provide high transconductance. The input matching is worse, especially at high frequency. Another source of input capacitance is from parasitic capacitance of coupling capacitors in front of  $g_{mB}$  stages.

The gate capacitance can be reduced by using shorter transistor while maintaining transconductance, but it may come at the cost of higher noise (higher  $\gamma$  factor in Equation 2.5 for short-channel device).





**Figure 4.1:** Initially proposed NC-LNA: (a) Block circuit with 3 output ports (b) Implementation of circuit with 1 output port (biasing not shown).

### 4.1.3 Noise

For the noise from  $inv$  stage to be canceled, the noise appears at the two LNA outputs must have equal magnitude. The small-signal circuit with noise from  $inv$  stage as a current source is shown in Figure 4.2. The output noise currents are given by:

$$i_{n+} = v_1 g_{mA} = i_2 (R_s + R_f) g_{mA} \quad (4.1)$$

$$i_{n-} = v_2 g_{mB} = i_2 R_s g_{mB} \quad (4.2)$$

For  $i_{n+} = i_{n-}$ , equating the right sides of 4.1 and 4.2 to get:

$$\frac{g_{mB}}{g_{mA}} = \frac{R_f}{R_s} + 1 \quad (4.3)$$

Equation 4.3 shows condition for noise cancellation. Note that it does not depend on the output resistance  $R_{out}$  of  $inv$  stage.

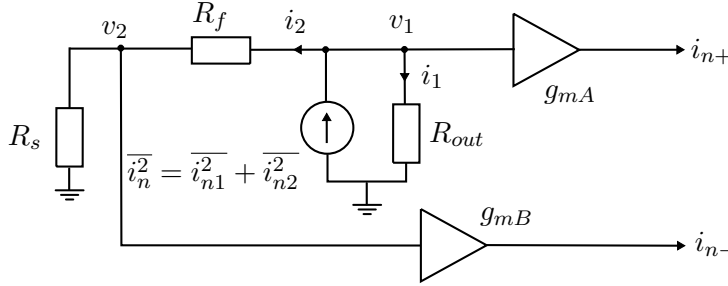
The condition for balanced output, however, is different from equation 4.3. For  $i_{RF+} = i_{RF-}$  the equation below is derived:

$$|A_v| g_{mA} = g_{mB} \quad (4.4)$$

Combining equation 4.4 with 3.2 to obtain:

$$\frac{g_{mB}}{g_{mA}} = \frac{R_f}{R_s} - 1 \quad (4.5)$$

Output balancing is more important than complete noise canceling, so equation 4.5 is used in design stage. Even though the noise is not perfectly canceled, if a high value is chosen for  $R_f/R_s$ , difference between 4.3 and 4.5 is quite small so a significant amount of noise is still be canceled.



**Figure 4.2:** Noise cancellation with proper transconductance stages.

The other noise sources of the LNA are now dominant. Noise from  $g_{mA}$  is suppressed by  $inv$  voltage gain. Noise from  $R_f$  is small if higher value is set for the resistor, with the cost of linearity at output of  $inv$  stage. The noise from  $g_{mB}$  is reduced with higher transconductance, and longer channels for its transistor.

The NC technique works well at low frequency but is shown to be less effective with high frequency [13]. The input capacitance of the LNA appears parallel with the source resistance so the *total* source impedance  $Z_s = R_s // Z_{Cin}$  is smaller with higher frequency. In the extreme case of infinitely high frequency,  $Z_s = 0$  and no portion of the noise voltage from matching stage is amplified by the  $g_{mB}$  stage, while the noise voltage is still amplified by  $g_{mA}$  stage. As a result, noise cancellation is not seen at the LNA output.

#### 4.1.4 Linearity

##### Clipping Analysis

The input voltage swing of the LNA is defined by CP1. The specification given is CP1>-15dBm, which translates into  $\approx 110\text{mV}_{pp}$  at input.

The clipping behavior is decided by the circuit node with largest voltage swing. Since  $g_{mA}$  and  $g_{mB}$  stages have current outputs driving low load impedance, the output voltage swing of these stages are quite small. For example, suppose  $g_{mB} = 70\text{mS}$ , mixer input impedance is  $R_{in,Mixer} = 25\Omega$ , the voltage swing at output of  $g_{mB}$  is:

$$V_{sw,out} = V_{sw,in} \cdot g_{mB} \cdot R_{in,Mixer} = 200\text{mV}_{pp} \quad (4.6)$$

which is much smaller than supply of 1V.

The  $inv$  stage is different since it does voltage amplification. Suppose its output swing is equal to supply (1V<sub>pp</sub>), its maximum voltage gain is given by:

$$A_{v,max} = 1\text{V}/110\text{mV} = 9 \quad (4.7)$$

Therefore, a gain of less than 9V/V should be selected for *inv* stage to prevent its output clipping.

The large voltage swing at *inv* output can also cause input clipping for  $g_{mA}$  stage. It is noted that this stage can handle large input as a characteristic of the basic push-pull stage. The following section will explain this point.

#### Weak-nonlinearity Analysis

One interesting property of NC-LNA is that the distortion of matching stage is canceled at the output [13]. The reason is that the nonlinear output current of this stage appears at the same position with the noise current source in Figure 4.2, therefore, get canceled at output as the noise current.

The nonlinearity of the LNA is decided by  $g_{mA}$  and  $g_{mB}$  stages, in which the  $g_{mA}$  linearity is worsened by the *inv* gain, as discussed in section 2.2.

The  $g_{mA}$  and  $g_{mB}$  stages base on the basic push-pull transconductance stage, which was claimed to have better IIP2 and IIP3 compared to individual transistors, provided that transconductance of PMOS and NMOS are equal [10]. To illustrate this point, a sample LNA with the following parameters is analyzed:

Parameters	Values
Output	Balanced
$A_{v,inv}$	7 V/V
$g_{mA}$	8 mS
$g_{mB}$	56 mS

**Table 4.1:** LNA sample parameters for linearity analysis.

Figure 4.3 shows the circuit of transconductance stages. PMOS and NMOS are biased so that their transconductance are approximately the same, here the bias voltages at the gates are both 0.5V. A bias resistor of 20k $\Omega$  is used to connect the gate and drain of PMOS, so the drain voltage at dc is fixed and less variable with process and temperature (PVT). The bias for NMOS is provided by an external NMOS current mirror (not shown).  $C_1, C_2, C_3$  are ac coupling capacitors which are in range of 3-5pF. The mixer input impedance is represented by a load resistor  $R_L$ .

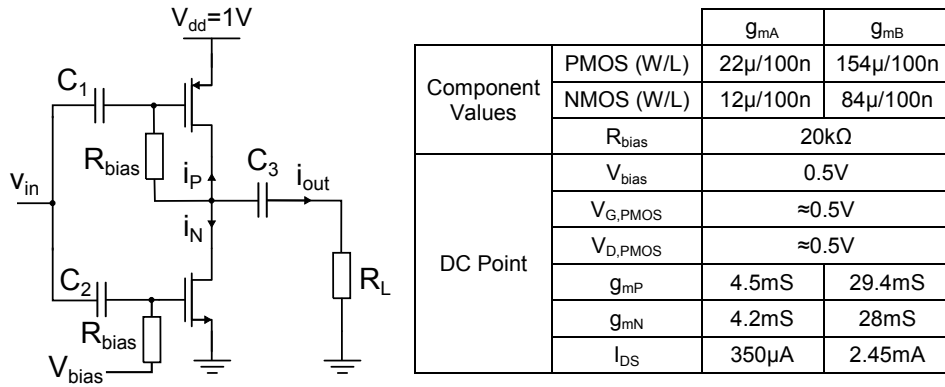
Suppose the composite and individual signal currents can be expressed by Taylor expansions, as below:

$$i_P = g_{mP}v_{in} + \frac{g_{m2P}}{2!}v_{in}^2 + \frac{g_{m3P}}{3!}v_{in}^3 + \dots \quad (4.8)$$

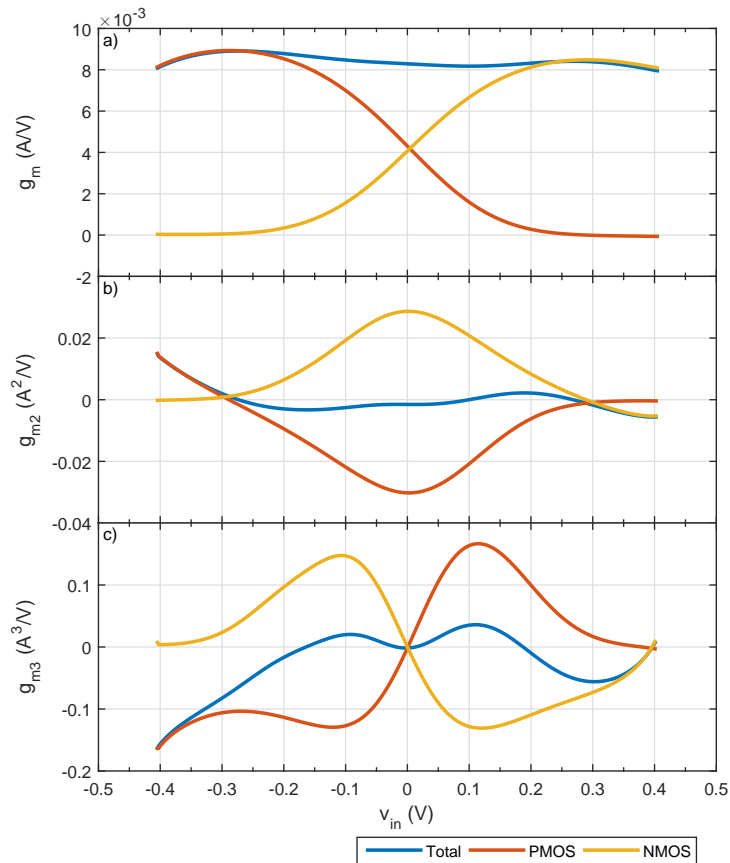
$$i_N = g_{mN}v_{in} + \frac{g_{m2N}}{2!}v_{in}^2 + \frac{g_{m3N}}{3!}v_{in}^3 + \dots \quad (4.9)$$

$$i_{out} = i_P + i_N = g_m v_{in} + \frac{g_{m2}}{2!}v_{in}^2 + \frac{g_{m3}}{3!}v_{in}^3 + \dots \quad (4.10)$$

Neglecting nonlinear terms with orders higher than 3, IIP2 is decided by second order terms and IIP3 is decided by third order terms [2]. Note that equations above include the effect of nonlinear  $g_{ds}$  on output currents since  $g_{ds}$  is a function of  $v_{ds}$ , which in turn is a function of  $v_{in}$ .



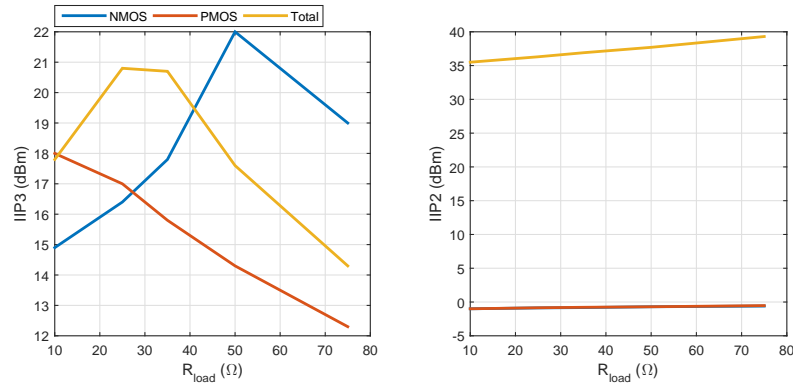
**Figure 4.3:** Detailed sample circuit for  $g_{mA}$  and  $g_{mB}$ .



**Figure 4.4:** Taylor expansion terms of  $g_{mA}$  stage ( $R_L = 35\Omega$ ).

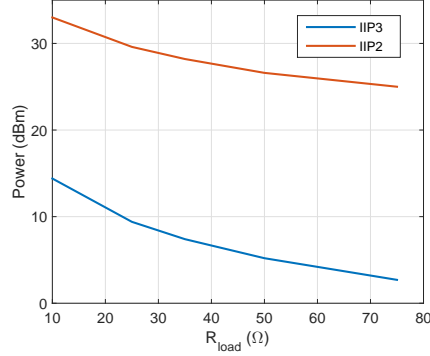
To include the effect of  $g_{ds}$ , transient simulations are used, together with derivation function inside Cadence (see Appendix A.2), so accurate values of the terms can be obtained. Figure 4.4 shows dependence of Taylor expansion terms on input voltage for  $g_{mA}$  stage loaded by  $R_L = 35\Omega$ . From graph (a), it can be seen that the composite  $g_m$  is almost flat in a wide range of input voltage. This suggests the ability to handle large input level and hence higher linearity and compression point compared to individual transistors. In graph (b), the composite  $g_{m2}$  shows much lower value (close to zero) as  $g_{m2P}$  and  $g_{m2N}$  hold opposite values and cancel each other. This suggests much higher total IIP2, compared to individual IIP2. The situation of third order terms is different as both  $g_{m2P}$  and  $g_{m3N}$  are already close to zero at  $v_{in} = 0$  so the cancellation here is much less effective than  $g_{m2}$  cancellation. In fact,  $g_{m3}$  cancellation is harder to achieve as it depends on  $R_L$  and needs careful adjustment of dimension and size of PMOS and NMOS so  $g_{m2P}$  and  $g_{m3N}$  hold opposite signs around  $v_{in} = 0$ . The necessary adjustments have been done here, and the final IIP2 and IIP3 depicted in Figure 4.5 show cancellation effectiveness.

Figure 4.5(right) shows that an increase of over 35dB is achieved for composite IIP2, compared to individual IIP2. Also the composite IIP2 is quite independent of load resistor, suggesting a robust cancellation. The IIP3 cancellation in the left graph is however less effective. The cancellation works only in a limited range of load resistor (here from 20-40 $\Omega$ , where composite IIP3 is higher than individual IIP3 plus 3dB to compensate for the doubled transconductance). For higher or lower load, the cancellation does not work well. The “good” range 20-40 $\Omega$  can be used to design input impedance of mixer and TIA.



**Figure 4.5:** Individual and composite IIP2 and IIP3 of  $g_{mA}$  stage.

For  $g_{mA}$  stage, the output resistance of PMOS and NMOS is high (in order of  $k\Omega$ ) so the effect of  $g_{ds}$  nonlinearity is small. In  $g_{mB}$  stage, the output resistance is much lower (7 times roughly) so  $g_{ds}$  nonlinearity becomes more important. Figure 4.6 depicts composite IIP2 and IIP3 of the stage. It can be seen that IIP2 cancellation still works effectively with above 25dBm IIP2 value for the whole range of load (10 – 75 $\Omega$ ). The IIP3 is quite lower than IIP3 of  $g_{mA}$  stage, and decreases with higher load.



**Figure 4.6:** IIP2 and IIP3 of  $g_{mB}$  stage.

For a rough calculation of IIP2 and IIP3 of the whole LNA, equations 2.12 and 2.13 are used with the note that nonlinearity of  $inv$  stage is canceled already. IIP2 and IIP3 of  $g_{mA}$  referred to LNA input is calculated as:

$$IIP3_{g_{mA},referred} = IIP3_{g_{mA}} - 17dB \quad (4.11)$$

$$IIP2_{g_{mA},referred} = IIP2_{g_{mA}} - 17dB \quad (4.12)$$

where 17dB is the power gain of  $inv$  stage ( $A_v = 7V/V$ ). For  $R_L = 35\Omega$ , input-referred IIP3 and IIP2 are  $21-17=4dBm$  and  $36-17=19dBm$ , respectively. Those values are quite lower than IIP3 and IIP2 of  $g_{mB}$  stage, which are 7dBm and 28dBm, respectively.

It is safe to conclude that nonlinearity of LNA is dominated by  $g_{mA}$  stage, and the LNA is theoretically able to achieve 4dBm for IIP3 and 19dBm for IIP2, which is better than the target specifications.

#### 4.1.5 Bandwidth

The bandwidth of the LNA is decided by parasitic capacitances at the LNA input and at the input of  $g_{mA}$  stage [13]. The input node capacitance is dominated by coupling capacitors (substrate capacitance) and gate capacitance of  $g_{mB}$  stages, as there are 3 such stages, and transistor dimensions of  $g_{mB}$  are large for a high transconductance. The same occurs for coupling capacitors and gate capacitance of  $g_{mA}$  dominating capacitance at input node of  $g_{mA}$ .

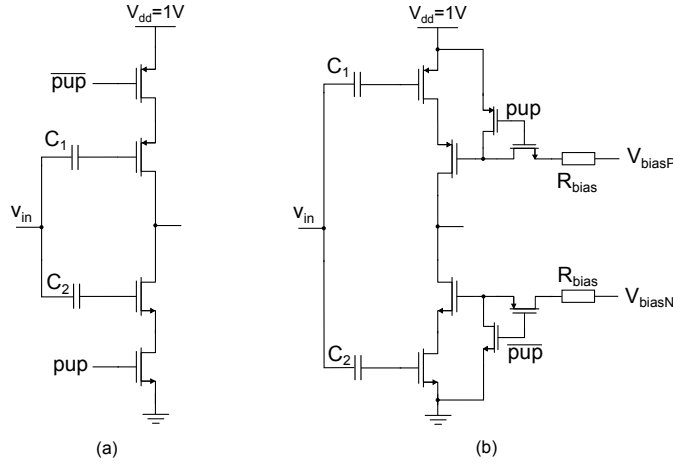
The gate capacitance can be reduced by using smaller transistors, with the risk of higher noise, and lower output impedance. The coupling capacitors can be reduced by a special arrangement so transconductance stages can share a same pair of coupling capacitors (will be detailed in Section 5.2).

#### 4.1.6 Gain Control

In order to support power gain reduction of -6 and -12dB, the LNA transconductance should be able to reduce to 2 and 4 times. One simple solution is to keep  $inv$

stage, and divide  $g_{mA}$  and  $g_{mB}$  stages into 4 identical sub-stages in parallel. The sub-stages should be able to switch on or off independently. Transistors working as switches (in triode region) must be added. The switches can be placed at 3 positions: In bias circuit, close to supply, or at the circuit output. The first method relates to bias network design and is not shown here, the other two are shown in Figure 4.7. Placing the switches close to supply does not require any bias network for them while the switches at output can be used as cascode devices to improve the output impedance. Here the cascode devices require separate bias network. This cascode+switch is beneficial for  $g_{mB}$  stage as its output impedance is quite low.

Another way to reduce gain is to keep  $g_{mA}$  stage and reduce feedback resistor of  $inv$  stage to reduce its voltage gain. The advantage is the LNA linearity is improved with lower  $inv$  gain, which is good to tolerate strong intermodulation products from input blockers. The difficulty is the voltage gain not proportionally increase with the feedback resistor so it is not easy to reduce the gain by exactly 2 and 4 times. It is also hard to match the voltage gain reduction with the transconductance reduction of  $g_{mB}$  stage in various process and temperature conditions. Gain reduction mismatch may arise and careful calibration is needed. This later challenge is easily ignored if  $g_{mA}$  transconductance reduction is used as matching between  $g_{mA}$  and  $g_{mB}$  can be better controlled in layout.



**Figure 4.7:** Transconductance stage with power-up switches: (a) Switches close to supply, (b) Switches at output. Biasing for gain devices is not shown.

#### 4.1.7 Robustness

As pointed out in [13], the noise cancellation is relatively robust to device parameter variation. The output resistance of  $inv$  stage and gate capacitance of  $g_{mA}$  stage does not affect the cancellation (see Section 4.1.3). The cancellation is sensitive with variations of  $R_s$  and  $A_v$ , but with low sensitivity only [13].

The LNA linearity is decided by linearity of  $g_{mA}$  stage and the  $inv$  gain. The

$g_{mA}$  linearity is found from simulation to be robust to process variation (shown by Table 4.2). To our surprise, the fs and sf corners show no noticeable degradation of IIP2 and IIP3 compared to other corners, even though the  $g_{mA}$  stage includes both PMOS and NMOS. This robustness is result of constant current source and NMOS current mirror used to provide bias for  $g_{mA}$  NMOS, and the use of bias resistor for PMOS self-biasing. In the real chip, a constant current source is always available [17]. The bias voltages for NMOS and PMOS are automatically adjusted according to corners, and nonlinearity cancellation is maintained.

The gain of  $inv$  stage is decided by its feedback resistor, whose value found in simulation may vary by 25% from nominal value due to process variation. The power gain, therefore, may vary by 2dB from the nominal value. This variation can be smaller if resistor calibration technique is used, for example by adopting an off-chip accurate resistor for reference [18].

The LNA linearity can be concluded to be robust to process.

	tt	ss	ff	fs	sf
IIP2 (dBm)	36.9	28.8	38.3	58.2	31.2
IIP3 (dBm)	20.7	21.1	17.9	22.4	17

**Table 4.2:** IIP2 and IIP3 of  $g_{mA}$  stage dependent on process corners ( $R_L = 35\Omega$ ).

## 4.2 Mixer Analysis

### 4.2.1 Mixer Circuits

In this Thesis, 4 types of mixers are analyzed and compared: The traditional mixer driven by 4 LO signals with 25% duty cycle (4LO 25% for short) for comparison reference, and 3 mixer types with harmonic rejection function: 4LO 33%, 6LO and 8LO. Figure 4.8 depicts the circuits of the mixers. Note that the 4LO 33% type requires two separate input ports as the LO signals overlap with each other. Also there are dummy mixers in parallel with the main I-Q mixers to direct  $i_{RF}$  to ground as the LO signals do not cover the full LO cycle. Dummy mixers are not shown in Figure 4.8 for simplicity.

### 4.2.2 Conversion Gain and Harmonic Rejection

The conversion gain of one mixer is defined as the ratio of baseband current at output and RF current at input  $i_{BB}/i_{RF}$ . Conversion gain depends on the LO duty cycle  $D$ , as shown in equation 4.13. The gain for the 4 mixer types are calculated as in Table 4.3.

$$Gain = \frac{2}{\pi} \sin \pi D \quad (4.13)$$



Table 4.3 also shows the harmonic rejection ratios  $HRR_3$  and  $HRR_5$  of each mixer type. The 4LO 25% mixer does not reject odd LO harmonics and is used here as the reference.  $HRR_3$  and  $HRR_5$  are defined as followed:

$$HRR_3 = \left( \frac{P_{3LO}}{P_{LO}} \right)_{ref} - \left( \frac{P_{3LO}}{P_{LO}} \right)_{measured} \quad (4.14)$$

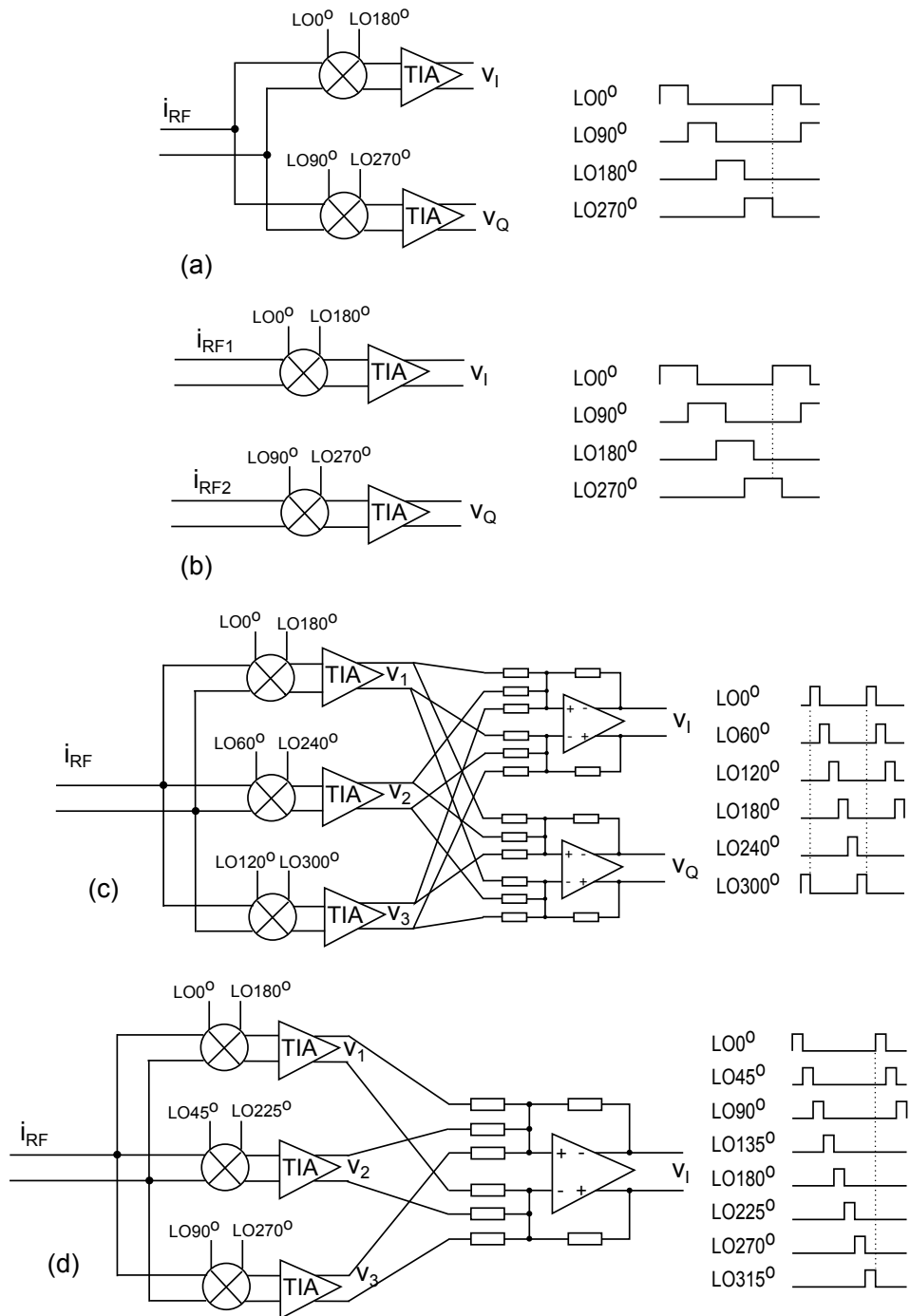
$$HRR_5 = \left( \frac{P_{5LO}}{P_{LO}} \right)_{ref} - \left( \frac{P_{5LO}}{P_{LO}} \right)_{measured} \quad (4.15)$$

where  $P_{LO}$ ,  $P_{3LO}$ ,  $P_{5LO}$  are power levels at frequency  $f_{LO}$ ,  $3f_{LO}$  and  $5f_{LO}$ , respectively. The power levels are measured from Cadence PXF (Periodic Transfer Function) simulations, in which ideal transconductance amplifiers (voltage-controlled current sources) are used instead of real LNAs to drive the mixers. The TIAs and LO signals used in the simulations are also ideal (voltage-controlled current sources and square waves with no phase errors). The baseband combination amplifiers in 6LO and 8LO mixers are ideal and the values of resistors are calculated from equations 3.20 and 3.17.

The simulated harmonic-rejection ratios are over-optimistic as the LO phase error, mixer gain mismatches and resistor mismatch are not taken into account. To obtain realistic figures, Monto-Carlo simulations should be done and real LO circuit is required to include all possible mismatches. The numbers in Table 4.3, however, show that the target  $HRR_3 > 10dB$  can be easily achieved in real circuits for all analyzed harmonic-rejection mixers.

Mixer	$D$	Gain	$\frac{P_{3LO}}{P_{LO}}$	$HRR_3$	$\frac{P_{5LO}}{P_{LO}}$	$HRR_5$
4LO	25%	$\sqrt{2}/\pi = 0.551$	-9.5dB	0	-14dB	0
4LO	33%	$\sqrt{3}/\pi = 0.45$	-58dB	48.5dB		
6LO	16.7%	$1/\pi = 0.318$	-76dB	66.5dB		
8LO	12.5%	0.244	-75dB	65.5dB	-78dB	68dB

**Table 4.3:** Conversion gain and harmonic rejection ratios for different mixers.



**Figure 4.8:** Mixer types: (a) 4LO 25% (b) 4LO 33% (dummy mixers not shown) (c) 6LO (d) 8LO (Q branch not shown).



# Circuit Design

This chapter explains in details the design process adopted for the inductorless harmonic-rejection receiver. From circuit analysis (chapter 4), the following insight of circuit properties were observed:

- The noise figure is decided by feedback resistor and  $g_{mB}$  stage. Noise contribution of matching and  $g_{mA}$  stages are small.
- Input matching is affected by output resistance of *inv* stage and gate capacitance of  $g_{mB}$  stage.
- Weak nonlinearity is decided by  $g_{mA}$  stage.
- Clipping is decided by *inv* stage and a gain of  $A_v < 9V/V$  should be used to meet the target CP1.
- The output resistance of  $g_{mB}$  is potentially small and need cascode to improve.
- Bandwidth is affected by gate capacitance of  $g_{mB}$  and  $g_{mA}$  stages.
- Gain control can be obtained by adding switches.
- Harmonic rejection ratio is good enough for the target specification.

The following procedure is used for the circuit design:

- Step 1: Combine the NC-LNA with HRMs. The LNAs' transconductance are calculated from mixers' conversion gain and the required transconductance at TIA input. The LNAs then are designed so that lowest possible noise figures can be obtained. To do this, the feedback resistors are selected as high as possible without suffering compression and input matching too much. Here other parameters of the LNA such as linearity, bandwidth, output resistance are not accounted. The LNA-HRM combinations are then compared in terms of potential noise figure and power consumption. The most promising combination is selected for further optimization.

- Step 2: Adding cascode for  $g_{mB}$  stage to improve its output resistance.
- Step 3: Optimize input matching and bandwidth.
- Step 4: Weak nonlinearity optimization: Adjusting  $g_{mA}$  transistor sizes and bias to obtain  $g_{m2}$  and  $g_{m3}$  cancellation.
- Step 5: Gain switching: Break transconductance stages into sub-stages in parallel and add power-up switches for each sub-stages.

Step 1 is explained in Section 5.1. Section 5.2 discusses the remained steps.

## 5.1 Comparing Harmonic Rejection Receivers

The 3 harmonic-rejection mixers were integrated with NC-LNA to form harmonic-rejection receivers (HR-Rx). In this step the receivers are compared in terms of noise figure and current consumption. NF is the sum of NF after LNA and the  $NF_{penalty}$  caused by noise folding.  $NF_{LNA}$  depends on the LNA transconductance and the feedback resistor. In all analyzed receivers, the resistors are selected to be  $800\Omega$ , which provide a gain of  $A_v = 10V/V$  for the *inv* stage (the gain is reduced compared to the ideal gain  $R_f/R_s - 1$  due to the output impedance of *inv* stage, as discussed in Section 4.1.2). Such a high gain is used so a better noise figure is obtained, though compression point is suffered. The LNA transconductance is calculated from target transconductance after the mixer (17mS) and the mixer gain, as followed:

$$g_{m,LNA} = \frac{17mS}{Gain_{mixer}} \quad (5.1)$$

Combining equation 5.1 and Table 4.3 to obtain required transconductance for LNA in each receivers. The circuit and LNA transconductance for each HR-Rx are shown in Figure 5.1. Note that the receivers here are for one channel only. To fulfill the specification of supporting 3 channels (3 carriers aggregated) the number of  $g_{mA}$ ,  $g_{mB}$ , mixer, TIA and combination amplifier stages should be tripled.

Noise figure analysis were done for each HR-Rx. Normal noise analysis was used to measure NF after LNA. Periodic noise (PNOISE) analysis was used to measure NF after mixer. The results are shown in Table 6.1. 8LO HR-Rx performs lowest  $NF_{LNA}$  and  $NF_{penalty}$  as the LNA transconductance is highest and harmonic rejection works for both 3LO and 5LO. The 4LO HR-Rx has highest NF due to the lowest LNA transconductance.

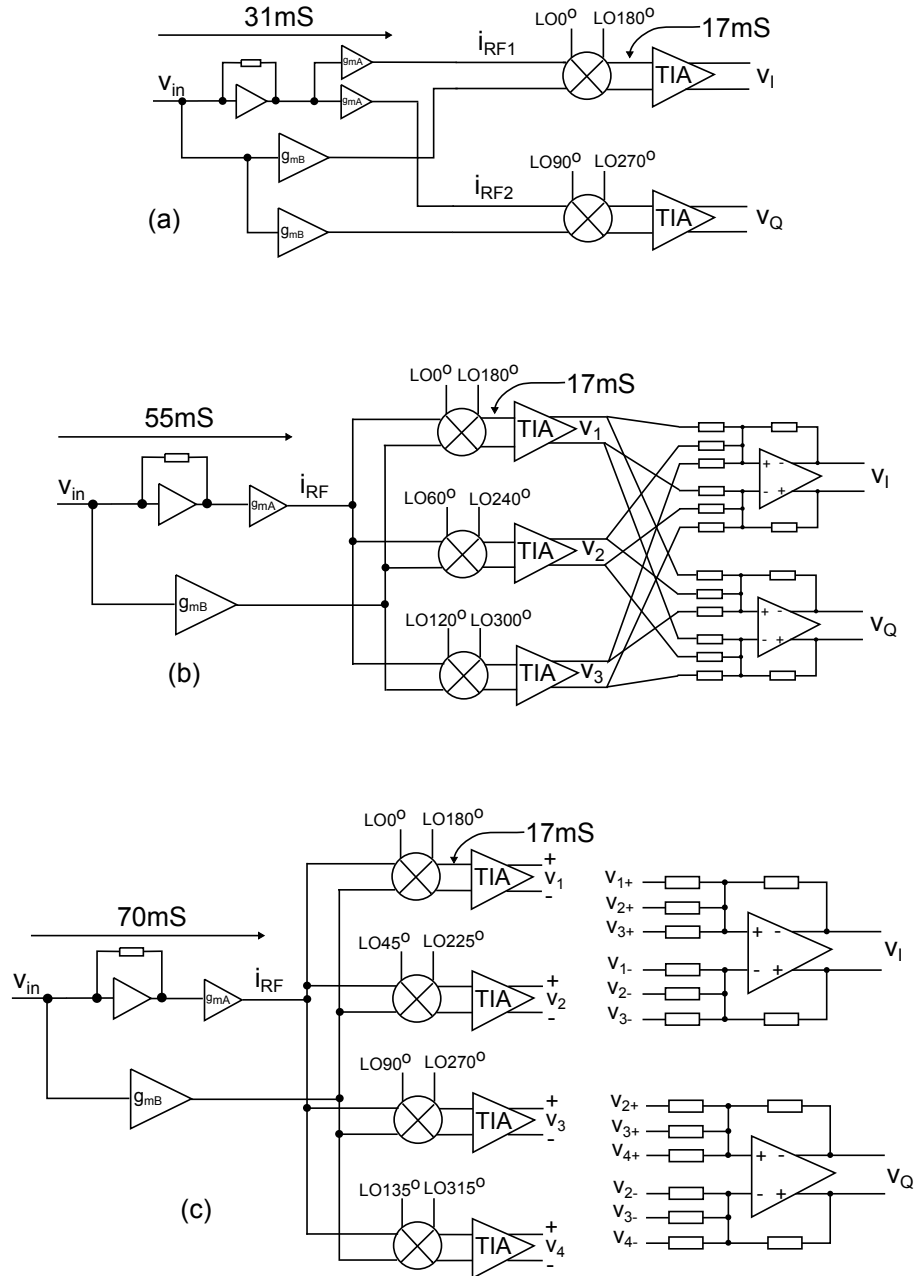
Current consumption of the HR-Rx is shown in Table 6.2. Here the mixer current is measured to be 0.4mA at 1GHz in a separate transient simulation (includes a double-balanced passive mixer driven by 1GHz LO signals). The TIAs and combination amplifiers are assumed to use the same kind of differential amplifier with current consumption of 2mA (suggested by the thesis advisors). The current given in Table 6.2 is for the case where 2 channels are working simultaneously and 1 channel is off.

It can be seen that the 8LO HR-Rx consumes current twice as much as that of the 4LO HR-Rx, and about 40% higher than that of the 6LO HR-Rx. This is considered as the cost for better noise figure.

The target noise figure after mixer is  $NF_{LNA} + NF_{penalty} = 1.5 + 0.2 = 1.7dB$  which is in range of the 6LO HR-Rx. This topology also consumes reasonable current, therefore was selected for further optimization.

One point to note is the comparison above bases on the assumption that the transconductance to the TIA input is the same for all HR-Rx. This comparison may be seen as unfair as the 8LO HR-Rx has mixers with highest conversion loss so the LNA transconductance is highest and LNA noise figure is already lowest. In other words, the lowest NF of 8LO HR-Rx is not only due to harmonic rejection function but also from LNA. Since the purpose of the comparison is to find out lowest possible NF from each receivers, the method was still used. Alternatively,

the comparison may base on the same LNA transconductance ground, so the NF differences between the receivers are from harmonic rejection only. This method was not used as NF is higher and not good enough for the target specification.



**Figure 5.1:** Harmonic-rejection receivers (1 channel): (a) 4LO 33% (dummy mixers not shown) (b) 6LO (d) 8LO.

## 5.2 LNA Design

### 5.2.1 Step 2: Output Resistance

The target output resistance is  $1\text{k}\Omega$  differential, which means each of  $g_{mA}$  and  $g_{mB}$  stages should obtain an  $r_{out} = 500\Omega$ . From simulations,  $r_{out,gmA} \approx 700\Omega$  and  $r_{out,gmB} \approx 200\Omega$ , which is not good enough. Cascode transistors were added to  $g_{mB}$  stage to improve the output resistance. The circuit of  $g_{mB}$  stage is shown in Figure 5.2.  $r_{out,gmB}$  is improved to  $1.3\text{k}\Omega$ .

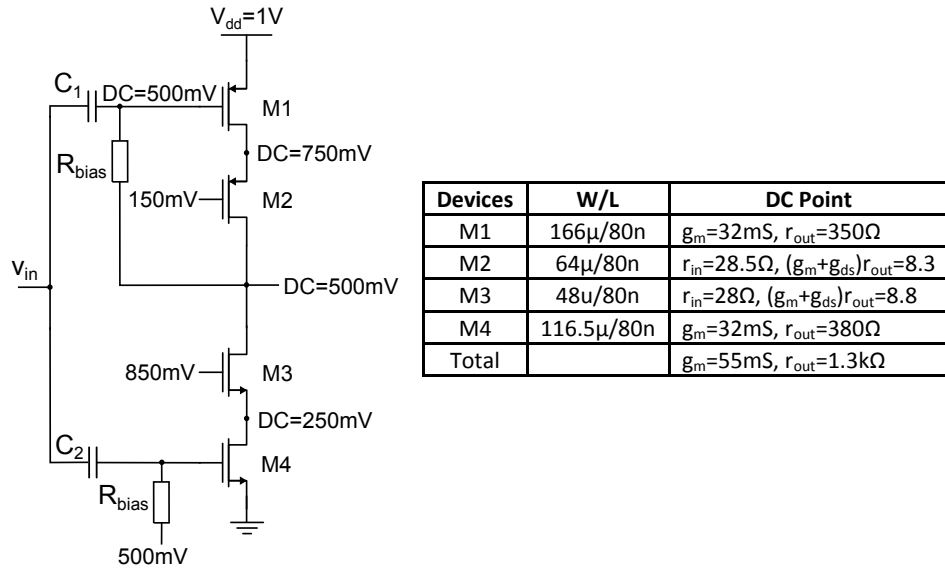


Figure 5.2:  $g_{mB}$  stage with cascode.

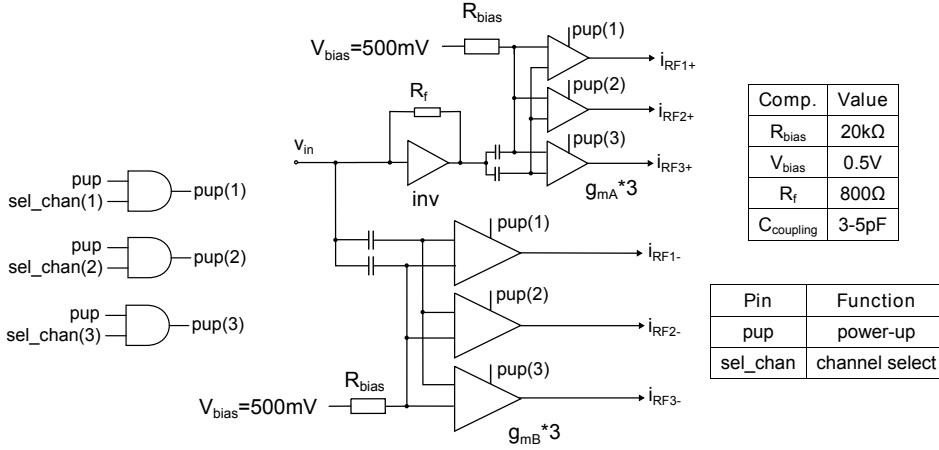
### 5.2.2 Step 3: Input Matching and Bandwidth

The input matching and bandwidth need to improve by reducing parasitic capacitance at LNA input and at output of  $inv$  stage. Some methods were tried as followed:

- Reducing coupling capacitors of  $g_{mA}$  and  $g_{mB}$  stages (as there are 3 copies of each stage). The 3  $g_{mB}$  stages now are dc-coupled with each other at input. As they need to be turned on or off independently, their cascode devices are used as switches (as discussed in Section 4.1.6). The same solution is used for the three  $g_{mA}$  stages, here the transistor switches are placed close to supply. Figure 5.3 shows the LNA block circuit with reduced coupling capacitors. The  $pup$  pin is for powering up the whole LNA and the  $sel\_chan$  pins are for selecting channels independently. 3 AND gates are used to generate internal power-up control signals for each channel.

- Try scaling down transistors of  $g_{mA}$  and  $g_{mB}$  stages to reduce their gate capacitance. It was found out that the noise suffers a lot if the transistor channel

gets shorter than 80nm. The transistor channel length was selected to be 80nm for all the gain devices.



**Figure 5.3:** LNA block circuit.

### 5.2.3 Step 4: Distortion

The mixer on-resistance was measured to be 17 $\Omega$ . Since the TIA input impedance is estimated to be 25 $\Omega$ , the load of the LNA is 42 $\Omega$  single-ended, or 84 $\Omega$  differential. This load value is used to adjust  $g_{mA}$  stage inside LNA so that nonlinearity cancellation can be obtained (as described in Appendix A.2). It is noted that due to the multiplexing of 4 LNAs in the target receiver topology, the parasitic capacitance at each LNA's output is quite a lot and the IIP3 is suffered compared to the case only one LNA exists. An IIP3 of -4.3dBm is achieved for the full topology.

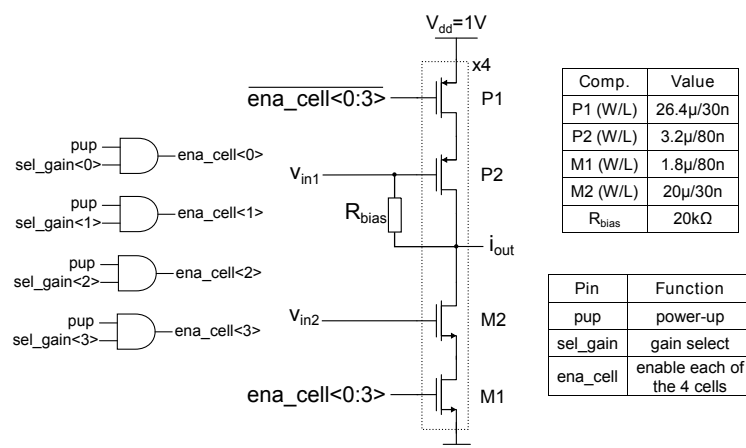
### 5.2.4 Step 5: Gain Switching

There are two sub-steps to be done:

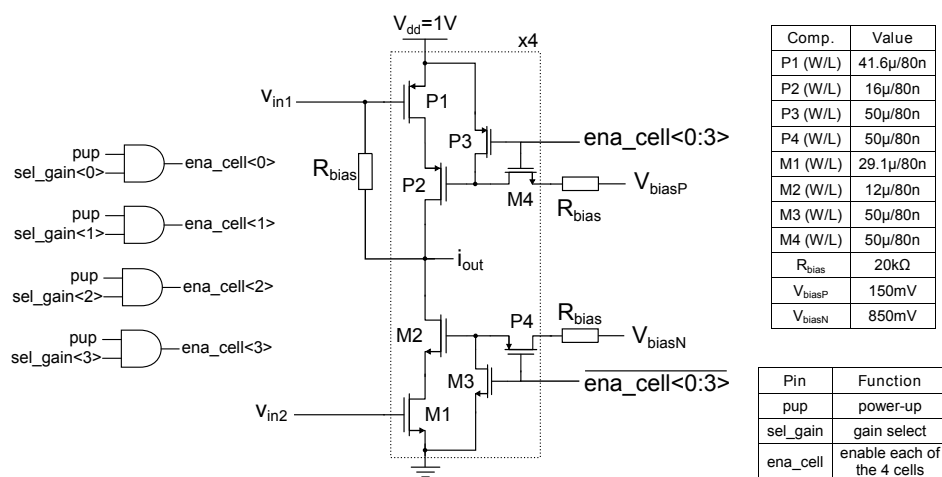
- Divide  $g_{mA}$  and  $g_{mB}$  stages into 4 sub-stages in parallel.
- Add power-up switches for each sub-stages.

The schematics of transconductance stages with power-up switch added are shown in Figure 5.4 and 5.5.





**Figure 5.4:**  $g_{mA}$  stage circuit for gain switching.



**Figure 5.5:**  $g_{mB}$  stage circuit with gain switching.

## Simulation Results

### 6.1 Comparison of Harmonic Rejection Receivers

The three HR-Rx are compared in terms of NF and current consumption. The receiver schematics are shown in Figure 5.1. All feedback resistors inside LNAs are  $800\Omega$ . Simulation results are discussed in Section 5.1.

HR-Rx	NF @ 500MHz (dB)		NF @ 1GHz (dB)	
	After LNA	After Mixer	After LNA	After Mixer
4LO 33%	2.15	2.32 (+0.17)	2.4	2.6 (+0.2)
6LO 16.7%	1.63	1.78 (+0.15)	1.68	1.8 (+0.12)
8LO 12.5%	1.46	1.49 (+0.03)	1.48	1.52 (+0.04)

**Table 6.1:** Noise figure comparison of different HR-Rx. Numbers in brackets are  $NF_{penalty}$  caused by noise folding.

Blocks		4LO 33%	6LO 16.7%	8LO 12.5%
LNA	<i>inv</i>	1.77	1.77	1.77
	$g_{mA}$	$0.25*2*2^1$	$0.41*2^1$	$0.8*2^1$
	$g_{mB}$	$1.52*2*2^1$	$3*2^1$	$6.3*2^1$
	<b>Total</b>	<b>8.85</b>	<b>8.6</b>	<b>16</b>
Mixer (@1GHz)		$0.4*4*2=3.2^{1,2}$	$0.4*3*2=2.4^1$	$0.4*4*2=3.2^1$
TIA		$2*2*2=8^1$	$2*3*2=12^1$	$2*4*2=16^1$
Comb. Amps		0	$2*2*2=8^1$	$2*2*2=8^1$
<b>Total (@1GHz)</b>		<b>20mA</b>	<b>31mA</b>	<b>43.2mA</b>

<sup>1</sup> \*2 due to 2 channels.

<sup>2</sup> \*4 due to 2 additional dummy mixers.

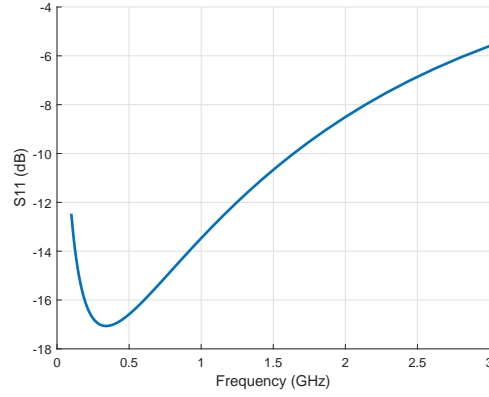
**Table 6.2:** Current consumption comparison of different HR-Rx.

## 6.2 LNA Simulations

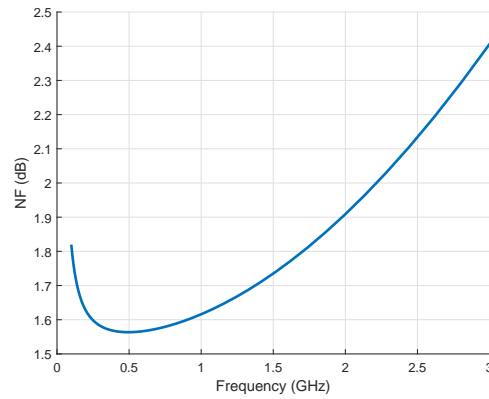
The following simulation results are for LNA inside the 6LO HR-Rx after optimization. The LNA transconductance is 55mS.  $R_{fb}$  is chosen to be 700 Ohm which gives a voltage gain of  $A_v = 9.6V/V$  for the *inv* stage. This high gain affects CP1 and linearity but was chosen for low NF. The LNA were tested in different conditions: Nominal condition, reduced gain, number of aggregated carriers and temperature variations.

### 6.2.1 Nominal Condition

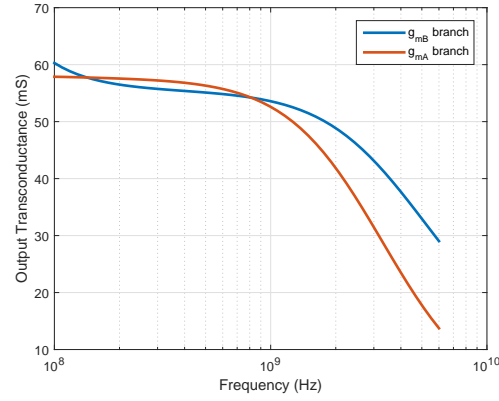
Simulation results shown in Figure 6.1, 6.2, 6.3 and Table 6.3 are at nominal condition with no gain reduction (full gain), 2 aggregated channels, temperature 27°C.



**Figure 6.1:** S11 at nominal condition.



**Figure 6.2:** LNA Noise Figure at nominal condition.



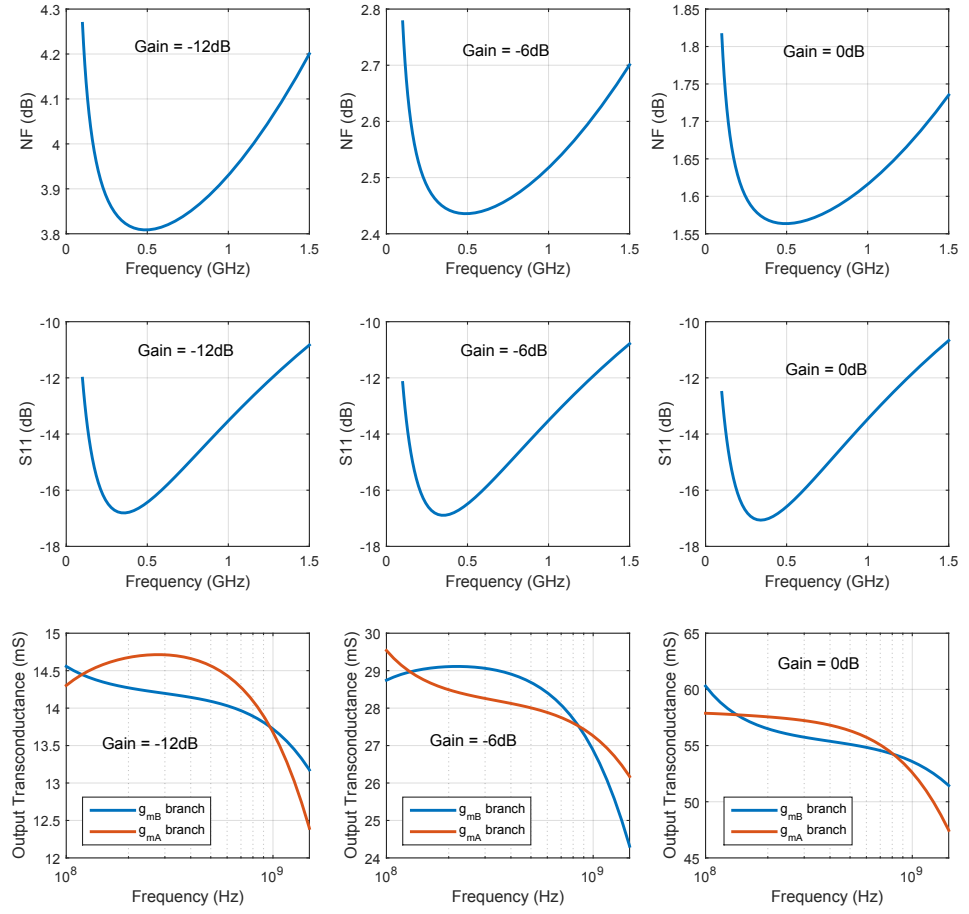
**Figure 6.3:** LNA Output Transconductance at nominal condition.

Parameters	Target	Simulated (worst case)
Current Consumption	<20mA	9.3mA
Frequency Range	600-960 MHz	400-1000MHz
Transconductance to mixer output	17mS	17mS
Noise Figure	<1.5dB	1.62dB @1GHz
CP1	>-15dBm	-16.9dBm
IIP3	>0dBm	-4.3dBm
IIP2	>15dBm	16.2dBm
S11 (input return loss)	<-12dBm	-13.3dB @ 1GHz
Output Impedance	>1k $\Omega$ differential	2k $\Omega$
Gain Control	0, -6 and -12 dB	Included

**Table 6.3:** LNA Target and Simulated Specifications (nominal condition).

### 6.2.2 Gain Switching

The following results are for LNA in gain reduction modes (-6dB and -12dB) at nominal temperature. Here  $g_{mA}$  and  $g_{mB}$  are reduced by 2 and 4 times. Noise figure is worse with lower gain, while S11 is almost unchanged. Table 6.4 shows that IIP3 is almost unchanged with the gains, while IIP2 and CP1 are slightly improved with lower gain. Figure 6.4 shows that NF is significantly reduced by lower gain, while S11 is stable.



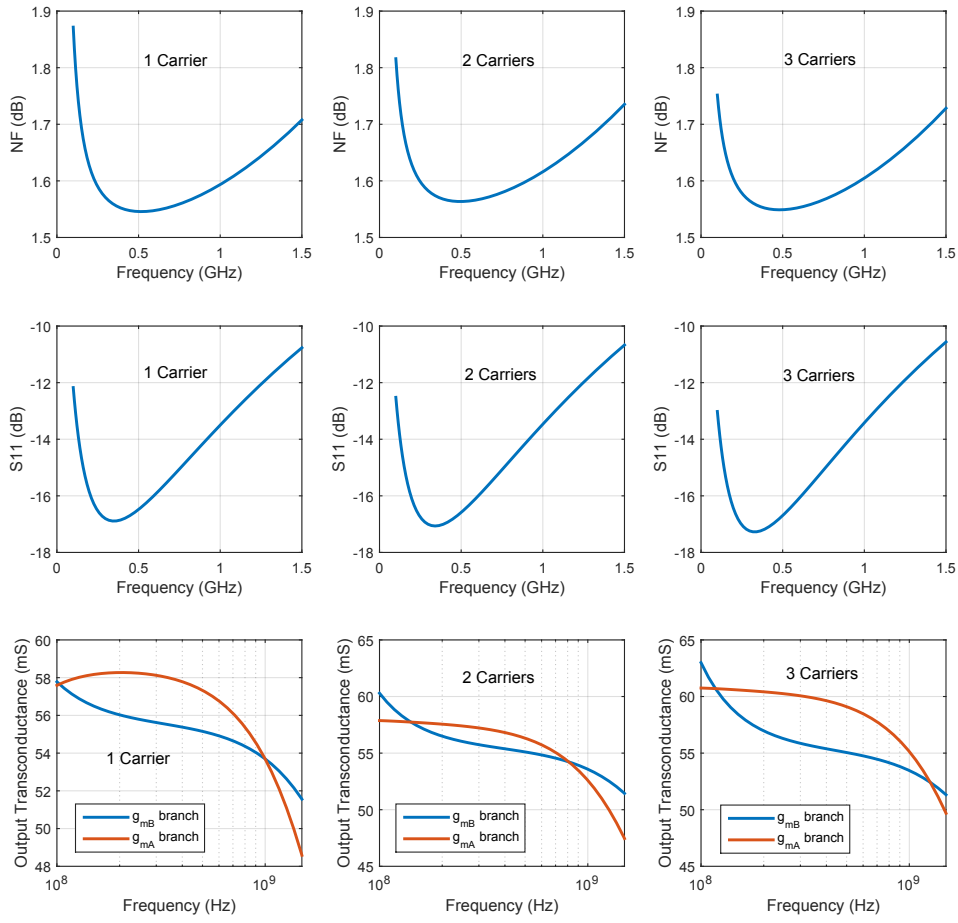
**Figure 6.4:** LNA Performance at different gains.

Parameters	Gain=-12dB	Gain=-6dB	Gain=0dB
CP1	-15.8	-16	-16.9
IIP2	18.5	17	16.2
IIP3	-3.2	-2.7	-4.3

**Table 6.4:** Linearity change at different gains. Unit: dBm.

### 6.2.3 Carrier Aggregation

The following results are for LNA with different number of used carriers, the gain reduction is 0dB, nominal temperature. It was found out from simulations that noise figure and input return loss are relatively independent of the number of carriers (Figure 6.5). The LNA CP1 is also constant with carrier aggregation, as shown in Table 6.5. IIP2 improves with less carriers. IIP3 is worst with maximal carriers.



**Figure 6.5:** LNA Performance with aggregated carriers.

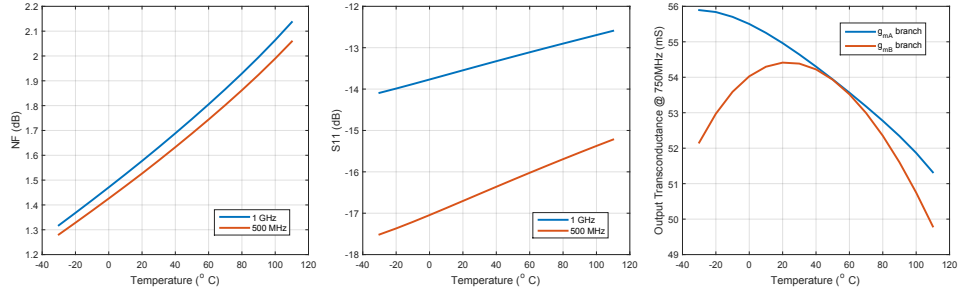
Parameters	1 carrier	2 carriers	3 carriers
CP1	-17.2dBm	-16.9dBm	-17.9dBm
IIP2	24.3dBm	16.2dBm	12dBm
IIP3	-5.1dBm	-4.3dBm	-7.9dBm

**Table 6.5:** Linearity change with number of used carriers.

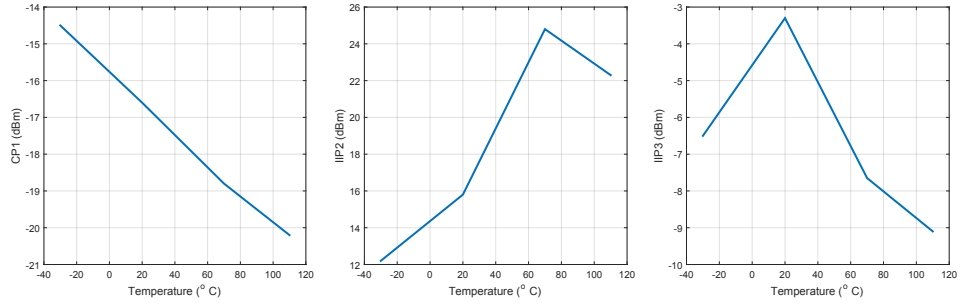
### 6.2.4 Temperature Variation

The circuit performance at different temperatures is very dependent on how biasing circuit is made. In the real chip the bias voltage is provided by a current mirror whose current is kept constant by a temperature-independent current source [17]. In the LNA testbench, an ideal constant current source is combined with a current mirror to provide 500mV bias for the LNA. The following results are for LNA with temperature varied from -30 to 110°C. The other conditions are nominal: 2 used

carriers, no gain reduction. Figure 6.6 shows that NF and S11 exhibit positive temperature coefficient. Also shown is transconductance of the two branches, which are relatively stable with temperature (maximal change  $\approx 10\%$ ). In Figure 6.7, CP1 shows a negative temperature coefficient, while IIP2 and IIP3 show peak values round 20-70°C.



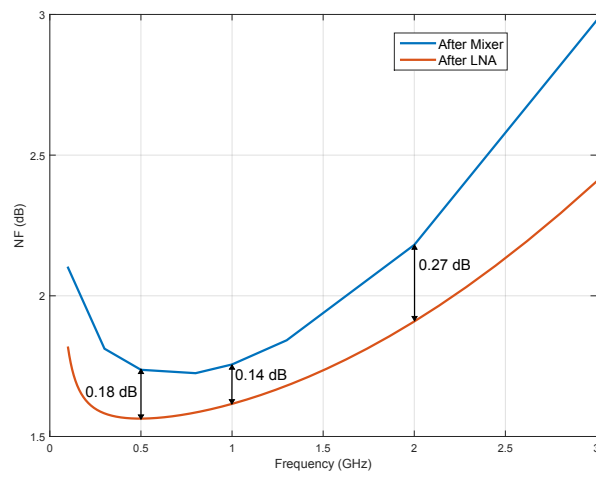
**Figure 6.6:** LNA Performance changes with temperature.



**Figure 6.7:** LNA Linearity changes with temperature.

### 6.3 Final System Simulation

Figure 6.8 shows NF of the front-end at nominal condition. The noise penalty due to noise folding is lowest in 0.5-1.5GHz and increases with lower and higher frequencies.



**Figure 6.8:** Noise figure after LNA and after mixer.





## Conclusion and Future Work

### 7.1 Conclusion

Overall, the thesis is a combination of “cancellation” techniques, which achieve potential results for the inductorless direct-conversion receiver to be used in FDD LTE-A system. Noise figure from the LNA is improved by using an auxiliary amplifying stage to cancel noise contribution of matching stage. The noise folded from higher LO harmonics is significantly reduced by the use of double-balanced mixers to cancel even-order LO harmonics, while odd-order harmonics are rejected by approximating the effective LO signals to sine waves. Nonlinearity is improved by the distortion cancellation of the matching stage, and the use of push-pull (complementary) structures for all LNA stages. Push-pull allows the cancellation of  $g_{m2}$  and  $g_{m3}$  of individual PMOS and NMOS.

The first important result of the thesis is the comparison of harmonic-rejection receivers (HR-Rx) using 4LO 33%, 6LO and 8LO signals. The 6LO receiver showed good trade-off between noise figure and power consumption, which was selected as the circuit for optimization. The 8LO receiver achieves better NF due to the 5LO harmonic rejection and higher- $g_m$  LNA, but consumes more power and needs more mixer and combination amplifier.

The second important result is the adoption of push-pull stages for the LNA. High IIP2 and IIP3 can be achieved at the same time by careful adjusting dimensions and biasing of PMOS and NMOS. Simulation suggests that IIP2 and IIP3 are relatively robust with process and temperature variations.

The third important result is the circuit design for carrier aggregation. Performance is not significantly changed when more carriers are used, which make the solution attractive for LTE-A network.

The limitations of the thesis include low S11, CP1 and IIP3. Input matching is degraded by the large gate capacitance of auxiliary stage to generate high transconductance. The more carriers supported, the more auxiliary stages are required which even worsen the situation. Input matching could be relaxed by adding an inductor at the LNA input. Even though inductorless requirement is violated, a benefit is that the 4 LNAs can share the same inductor so only one inductor is needed for the whole LNA bank. Another source of inductor is from the bonded wires. These options were not analyzed in the thesis.

The low IIP3 shows that  $g_{m3}$  cancellation is quite hard to adjust. This cancel-

lation is probably not a big benefit of push-pull stage and other IIP3 enhancement techniques should be adopted. In the time of this thesis, several ideas were tested, including source degeneration and derivation-superposition [20] but none showed promising result.

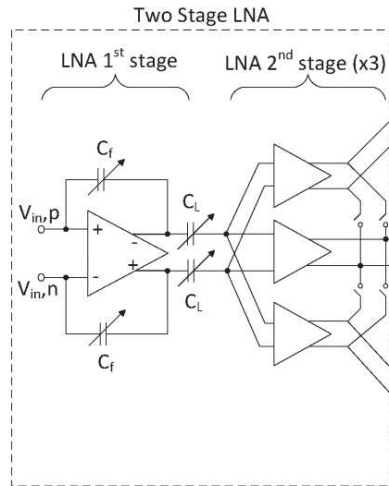
The low CP1 is from high voltage gain of *inv* stage, with aims at low NF. There is still node with voltage amplified in the LNA which limits the CP1. The voltage gain node can probably completely removed by solely using transconductance stages for LNA. Carrier aggregation then may be hard to implement as current now should be shared between stages for separate carriers. Alternatively, the common input voltage node of the LNA can be used for sharing. These options have never been tested or analyzed, but may be good for future analysis.

## 7.2 Future Work

The following ideas can be used for a future improvement:

### 7.2.1 Resistive feedback with a capacitor

In [27], the resistive feedback branch of the LNA can use capacitor instead of resistor. The LNA input impedance is resistive for frequency not too low and not too high, below the transit frequency. This characteristic may be good enough for frequency of interest in this thesis. The capacitor does not generate noise so noise figure would be greatly improved. Figure 7.1 [27] show the circuit.



**Figure 7.1:** Resistive feedback LNA with capacitors [27].

### 7.2.2 Reactance-canceling LNAs

In [2] and in [23], the resistive feedback amplifiers are found to exhibit an inductive input impedance, which can be used to cancel the input capacitance. This characteristic, if used, can improve input matching of the thesis circuit, as input capacitance is quite large. The technique was concerned at the beginning of the thesis and some of its effect were observed (increased input capacitance does not necessarily worsen  $S_{11}$ ) but was never carefully analyzed.

### 7.2.3 Gain reduction by reducing feedback resistor

The option to reduce the LNA gain is done in the thesis by reducing transconductance of  $g_{mA}$  and  $g_{mB}$  stages. The other option is to keep  $g_{mA}$  and reduce voltage gain of  $inv$  stage by reducing its feedback resistor. The advantage is the linearity improved with lower gain. This method was never tried as the former one is easier to implement.



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# A Method for Analyzing IIP2 and IIP3 in Cadence

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This section explains a method developed in the thesis to analyze IIP2 and IIP3 behaviors of push-pull transconductance amplifier, which consists of a PMOS and an NMOS in parallel. Periodic Steady-State (PSS) analysis is used to measure IIP2 and IIP3, but is not convenient for understanding the nonlinearity cancellation characteristics of the circuit. The used approach bases on the dependence of IIP2 and IIP3 on second and third order terms in Taylor expansion of output current upon the input voltage. By plotting these terms versus the input voltage, nonlinearity of the PMOS is shown to cancel that of the NMOS. This method can be used to optimize the circuit, so both second and third order nonlinearity can be canceled.

## A.1 Circuit Description and Theoretical Analysis

The circuit under test is the  $g_{mA}$  stage with schematic and initial dimensions shown by Figure A.1. The dimensions and bias points are selected so transconductance of PMOS and NMOS at dc are equal, as suggested in [10]. The load resistor is chosen to be  $35\Omega$ , which is in the middle of load range (mixer input impedance, from  $25\text{-}50\Omega$ ). The output current is given by (current flowing through the bias resistor of  $20\text{k}\Omega$  is neglected):

$$i_{out} = i_P + i_N \quad (\text{A.1})$$

where  $i_P$  and  $i_N$  are drain currents of PMOS and NMOS.

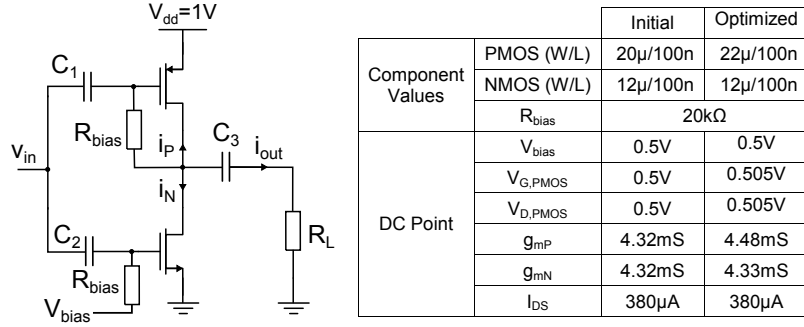
The drain current of each transistor is a nonlinear function of its  $v_{gs}$  and  $v_{ds}$ . In this circuit,  $v_{gs}$  is the only input ( $= v_{in}$ ) and  $v_{ds}$  can be considered as a function of  $v_{gs}$ . Therefore, drain currents can be seen as function of  $v_{gs}$  only. With small  $v_{gs}$ , Taylor expansion can be used to express these functions:

$$i_P = g_{mP}v_{in} + \frac{g_{m2P}}{2!}v_{in}^2 + \frac{g_{m3P}}{3!}v_{in}^3 + \dots \quad (\text{A.2})$$

$$i_N = g_{mN}v_{in} + \frac{g_{m2N}}{2!}v_{in}^2 + \frac{g_{m3N}}{3!}v_{in}^3 + \dots \quad (\text{A.3})$$

$$i_{out} = i_P + i_N = g_mv_{in} + \frac{g_{m2}}{2!}v_{in}^2 + \frac{g_{m3}}{3!}v_{in}^3 + \dots \quad (\text{A.4})$$

where  $g_m$ ,  $g_{m1}$  and  $g_{m2}$  are respectively first, second and third order derivatives of currents versus input voltage.



**Figure A.1:**  $g_{mA}$  stage parameters before and after optimization.  
 $R_L = 35\Omega$

The IIP2 and IIP3 in dBm can be expressed in terms of Taylor terms as followed [14]:

$$IIP2_{x,dBm} = 20 \log_{10} \left| \frac{2g_{m,x}}{g_{m2,x}} \right| + 10dB \quad (\text{A.5})$$

$$IIP3_{x,dBm} = 20 \log_{10} \sqrt{\left| \frac{8g_{m,x}}{g_{m2,x}} \right|} + 10dB \quad (\text{A.6})$$

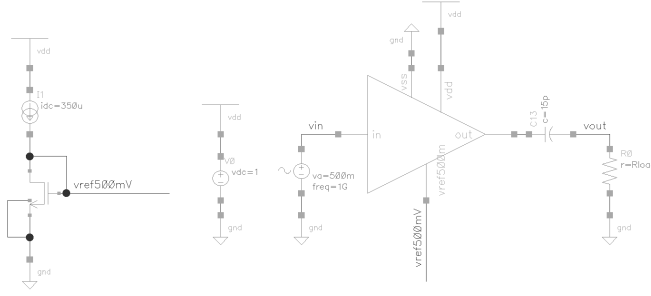
where  $x$  can be  $P$  (for PMOS),  $N$  (for NMOS) or  $tot$  (for the total). The factor  $10dB$  is for conversion from peak voltage to power with reference to  $50\Omega$  [14]. IIP2 and IIP3 therefore can be calculated if Taylor terms are all known.

## A.2 Transient Simulation with Derivatives

The problem with measuring Taylor terms is that they are combinations of nonlinearity of transconductance and output impedance of transistors. They also depend on load value and can only be well defined when the circuit reaches steady-state. Those issues make it impossible to predict these terms from dc simulation. In this thesis, a transient simulation is used for accurate measurement instead. An ac source provides large ac signal at the input. The transient time is long enough for the circuit to enter its steady-state. The currents  $i_P$ ,  $i_N$  and  $i_{out}$  are then extracted for half a sine wave input cycle to cover the whole swing of input voltage. The extracted currents are still functions of time and need to convert to functions

of input voltage. Derivatives of the converted functions are calculated to obtain Taylor series terms.

The circuit testbench is shown in Figure A.2. The input voltage amplitude is 500mVp at frequency 1GHz. A current mirror is used to provide 500mV bias. The waiting time for steady-state is 100ns.



**Figure A.2:**  $g_{mA}$  stage testbench.

The function to change plot axis from time to input voltage is not provided in Cadence, so a function written in OCEAN is used in this Thesis. The function is proposed by Andrew Beckett in Cadence support forum [28] and is re-written here in Listing A.1. The derivative function is already built-in in OCEAN.

**Listing A.1:** OCEAN function to change plot axis.

```

1 (procedure (abChangeXAxis yVar xVar)
2   (let (newWave)
3     (setq newWave (drCreateEmptyWaveform))
4     (drPutWaveformXVec newWave (drGetWaveformYVec xVar))
5     (if (eq (drGetWaveformXVec yVar) (drGetWaveformXVec
6       xVar))
7       /* if the x axes are the same for both, it's
8         simple */
9       (drPutWaveformYVec newWave (drGetWaveformYVec
10         yVar))
11       /* otherwise need to use value() to interpolate
12         */
13       (let (xVec yVec len)
14         (setq xVec (drGetWaveformXVec xVar))
15         (setq len (drVectorLength xVec))
16         (setq yVec (drCreateVec (drGetWaveformYType
17           yVar) len))
18         (for ind 0 (sub1 len)
19           (drAddElem yVec (value yVar (drGetElem
20             xVec ind))))
21         )
22       (drPutWaveformYVec newWave yVec)
23     )
24   )

```

```

18         )
19         newWave
20     )
21 )

```

The use of `abChangeXAxis` function is illustrated as in Listing A.2. Listing A.3 illustrates the use of derivative function in OCEAN to extract  $g_m$  curves.

**Listing A.2:** `abChangeXAxis` function usage illustration.

```

1  /* setting up simulation and saved ouputs */
2  analysis('tran ?stop "100n" ?errpreset "conservative" ?
    step "1p" ?maxstep "1e-12" )
3  desVar( "Rload" 35)
4  save( 'v "/vin" )
5  save( 'i "/R0/MINUS" "/i_inv1_0/M5/D" "/i_inv1_0/M3/D" )
6  temp( 27 )
7  run()
8
9  /* clipping to get outputs in half sine cycle */
10 selectResult( 'tran )
11 newWindow()
12 Vin = clip( v( "/vin" ) 99.35n 99.65n)
13 I_total = clip( i( "/R0/MINUS" ) 99.35n 99.65n)
14 I_P = clip( i( "/i_inv1_0/M5/D" ) 99.35n 99.65n)
15 I_N = clip( i( "/i_inv1_0/M3/D" ) 99.35n 99.65n)
16
17 /* change x axis to input voltage and plot */
18 I_total2 = abChangeXAxis(I_total Vin)
19 I_P2 = abChangeXAxis(I_P Vin)
20 I_N2 = abChangeXAxis(I_N Vin)
21 plot(I_total2 I_P2 I_N2 ?expr list("I_total2" "I_P2" "I_N2"
    ))

```

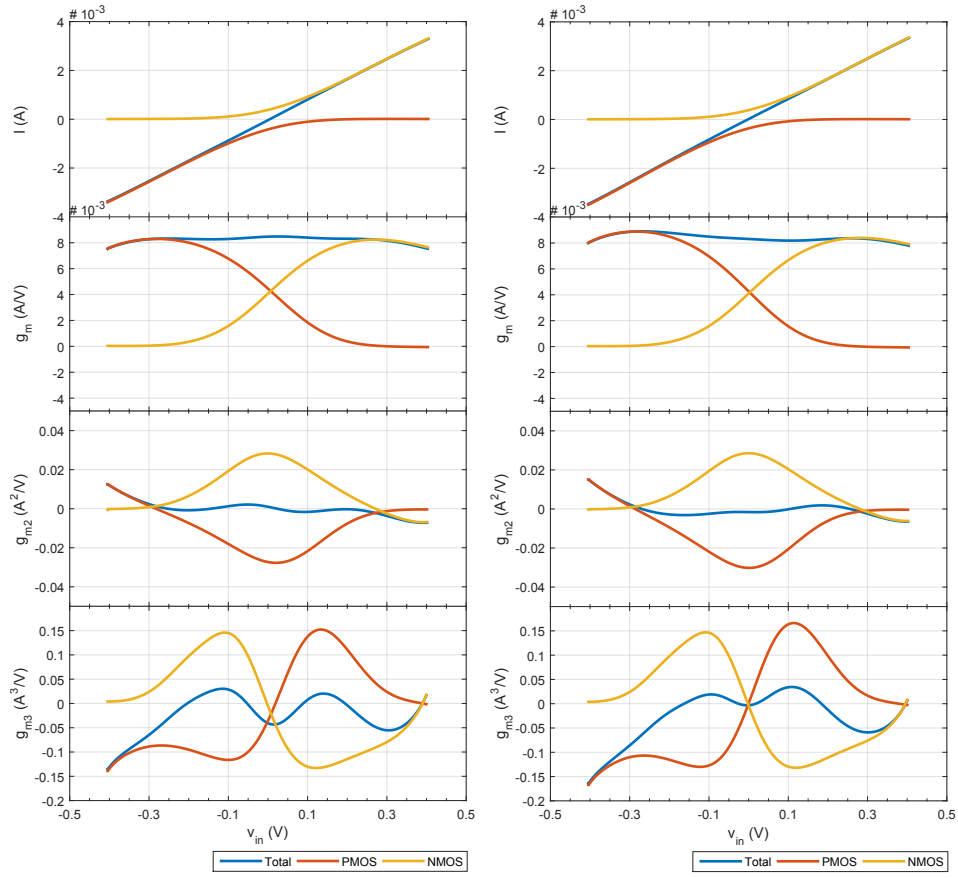
**Listing A.3:** Derivative function illustration.

```

1 gm=deriv(I_total2)
2 gmP=deriv(I_P2)
3 gmN=deriv(I_N2)
4 addSubwindow()
5 plot(gm gmP gmN ?expr list("gm" "gmP" "gmN"))

```

The plots of Taylor terms versus input voltage is shown in left column of Figure A.3. To evaluate the accuracy of the plots obtained, values of Taylor terms at dc (where  $v_{in} = 0$ ) is extracted so IIP2 and IIP3 are calculated and compared with these obtained from PSS simulations. The results are shown in Table A.1. The calculated IIP2 and IIP3 are really close to the actual values obtained from PSS simulation. This fact suggests that the used method is accurate enough for evaluating nonlinearity.



**Figure A.3:**  $g_{mA}$  stage Taylor terms: (left) Before and (right) after optimization.  $R_L = 35\Omega$

Params	PMOS	NMOS	Composite
$g_m$ (mA/V)	4.456	4.072	8.496
$g_{m2}$ (mA/V <sup>2</sup> )	-27.32	28.3	1
$g_{m3}$ (mA/V <sup>3</sup> )	-35.65	-5.02	-40.61
$IIP3_{cal}$ (dBm) <sup>1</sup>	10	18.12	12.3
$IIP3_{PSS}$ (dBm) <sup>2</sup>	10.8	18.1	14.5
$IIP2_{cal}$ (dBm) <sup>1</sup>	0.27	-0.82	34.7
$IIP2_{PSS}$ (dBm) <sup>2</sup>	-0.32	-0.84	29.2

<sup>1</sup> Value calculated from Taylor terms.

<sup>2</sup> Value obtained from PSS simulation.

**Table A.1:** Comparison of calculated and PSS-simulated IIP2 and IIP3.

### A.3 Circuit Optimization

Figure A.3 shows good cancellation for  $g_{m2}$  of PMOS and NMOS but not that good for  $g_{m3}$ . By adjusting the dimension of PMOS,  $g_{m3}$  cancellation is also obtained (see Figure A.1 for PMOS dimension and right column of Figure A.3 for plots of optimized Taylor terms). Table A.2 shows the effectiveness of the adjustment, in which both IIP2 and IIP3 are significantly improved.

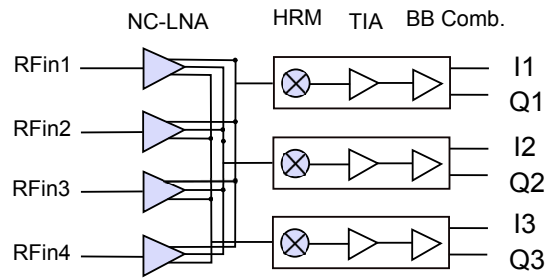
Params	Before Opt.	After Opt.
$IIP2_{tot}$ (dBm)	29.2	37
$IIP3_{tot}$ (dBm)	14.5	20.8

**Table A.2:** Comparison of PSS-simulated IIP2 and IIP3 before and after optimization.

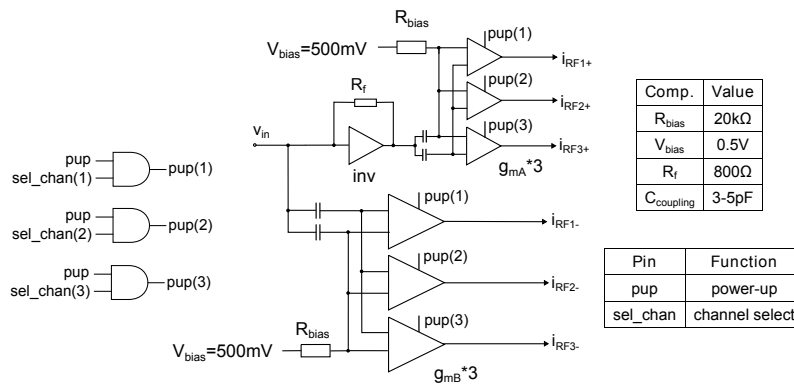
### A.4 Summary

The method presented shows great effectiveness in analyzing and optimizing nonlinear characteristics of the transconductance stage. Other applications are to analyze the change of nonlinearity with load value (already shown in Figure 4.5) and the linearity robustness.

## Final Schematic

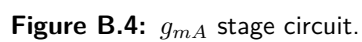
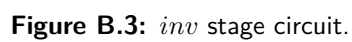


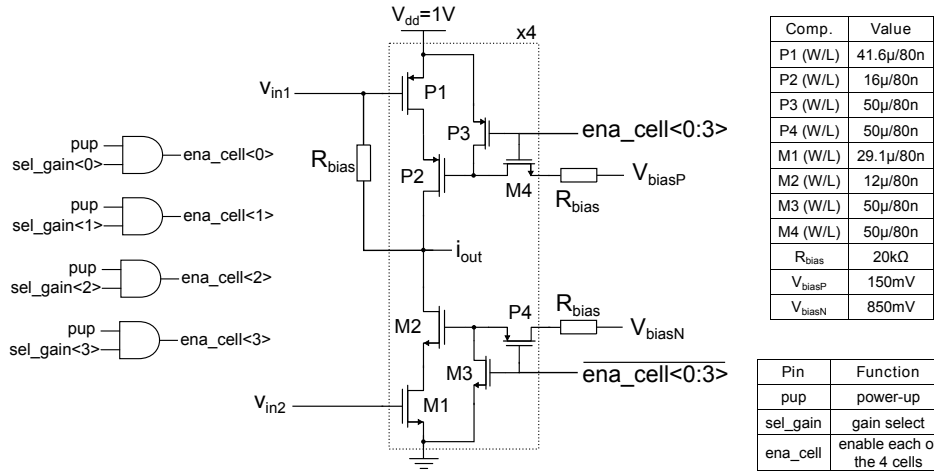
**Figure B.1:** 6LO harmonic rejection receiver (HR-Rx) topology. Colored blocks are focus of this thesis. The rest blocks are ideal.



**Figure B.2:** LNA block circuit.







**Figure B.5:**  $g_{mB}$  stage circuit.

The harmonic-rejection mixer schematic is shown in Figure 5.1. The single mixers are double-balanced passive type as shown in Figure 3.8. The dimension for mixer transistors is  $W/L=216\mu\text{m}/100\text{n}$ .

The TIA and combination amplifiers are ideal components, built from voltage-control-voltage-source (vccs) and ideal resistors of Cadence.



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