Master's Thesis

Modeling And Implementation of All-Digital Phase-Locked Loop Based on Vernier Gated Ring Oscillator Time-to-Digital Converter

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Abstract

In this thesis, a complete design of an All-Digital Phase-Locked Loop (ADPLL) for RF application is presented. A Vernier gated ring oscillator time-to-digital converter (TDC) is utilized in the proposed ADPLL, and a two-dimension architecture is developed for the TDC to improve latency and dynamic range. The proposed TDC is able to achieve a raw resolution of 5 ps while provides a detection range up to 10 ns. Meanwhile, an LC tank based digitally controlled oscillator (DCO) with three tuning banks is employed to realize fast frequency tuning and fine resolution of 4 KHz. The simulation on the presented ADPLL predicts an output frequency ranging from 3 GHz to 6 GHz with a reference input of 50 MHz.

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Chapter 1
Introduction

In recent decades, wireless communication industry has been growing rapidly and the wireless communication devices such as cellular phones, Global Positioning System (GPS) navigation devices, and wireless radio-frequency (RF) devices have became ubiquitous in daily life.

In a radio-frequency system, frequency synthesizer is usually deployed as local oscillator in both transmitter path and receiver path to convert accurate reference frequency. The frequency synthesizer accepts the frequency reference (f_{ref}) input and then generates output frequency according to the frequency command word (FCW). The output frequency of the synthesizer can be described as

$$f_{out} = \text{FCW} \cdot f_{ref} \tag{1.1}$$

The generated output is usually in phase with the input reference. Figure 1.1 displays a frequency synthesizer-based transmitter in a RF system. Since the baseband frequency is generally too low to generate effective radiation, a frequency synthesizer is needed to translate the the baseband signal to a radio frequency, while it is also needed in the receiver to translate the incoming RF signal to baseband for information extraction[1]. High quality of the frequency synthesizer

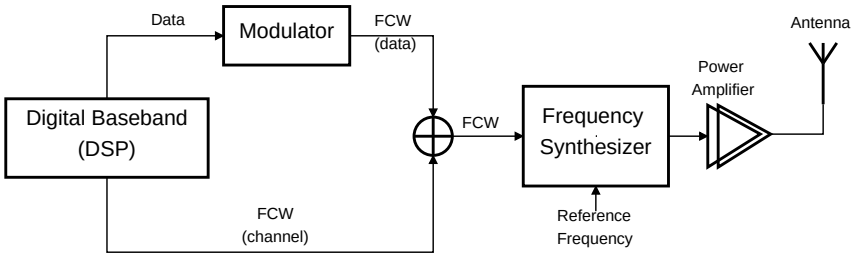

Figure 1.1: Simplified block diagram of a synthesizer-based transmitter.

is demanded to ensure good performance of the transceivers and the entire system. Thus, design and implementation of the high performance RF synthesizers have always been an essential task in modern RF systems. The design of RF synthesizers should meet some very stringent requirements, such as high spectrum purity, low

cost, and low phase noise. In this chapter, major techniques of frequency synthesis are reviewed.

1.1 Frequency Synthesis Techniques

The different approaches for frequency synthesis can generally be classified as:

- Direct-analog
- Direct-digital
- Indirect based on phase-locked loop(PLL)

This section provides a brief introduction of these three techniques and mainly focuses on indirect frequency synthesis based on *phase-locked loop* (PLL).

1.1.1 Direct-Analog Frequency Synthesis

Direct-analog frequency synthesis is a very straightforward frequency synthesis method. The reference frequency is translated directly using analog technique. Typically, a direct-analog frequency synthesizer consists of one or more oscillators, switches, filters, frequency dividers and mixers [2]. One method of using multiple oscillators is shown in Figure 1.2. In this frequency synthesizer, the switches select

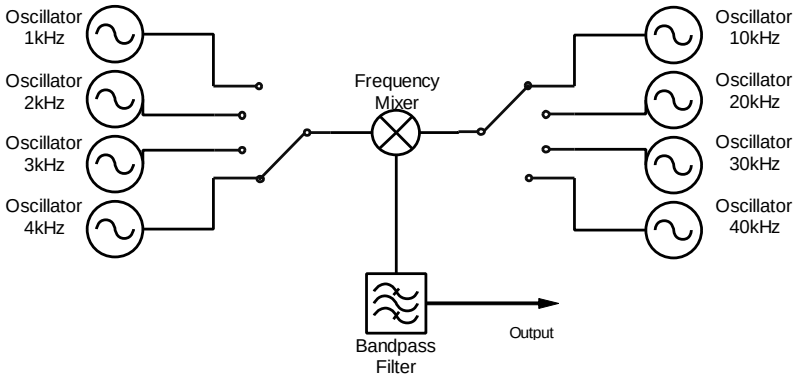

Figure 1.2: A direct-analog frequency synthesizer using multiple oscillators.

one of the oscillators on both side and a frequency mixer combines those two signals. Then, a bandpass filter outputs the higher of the mixer output frequency.

Since the whole process avoids error correction, the quality of the output directly correlates with the quality of the input so that the phase noise is usually excellent. However, that direct-analog frequency synthesis technique requires lots of reference oscillators results in high cost and high power consumption. It becomes impractical to implement in modern RF systems[3].

1.1.2 Direct-Digital Frequency Synthesis

Direct-digital frequency synthesis was firstly introduced in the early 1970s by JOSEPH TIERNE[4]. This method is more flexible than direct-analog and can generate multiple frequencies from a reference frequency source. The basic architecture is shown in Figure 1.3.

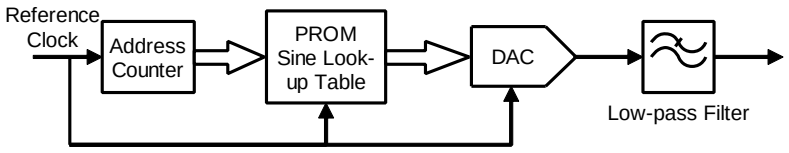

Figure 1.3: A basic model of a direct-digital frequency synthesizer.

In this model, there is an address counter which outputs memory location incrementally in each clock cycle, a *programmable-read-only-memory* (PROM) which stores one or more integral number of cycles of a sinewave, a *digital-to-analog converter* (DAC) and a *low-pass filter* (LPF). As the reference clock is fed into the address counter, the PROM outputs the corresponding digital amplitude of the sinewave at each memory location. Then, this digital signal is converted to analog domain by the DAC[5]. However, the final output frequency is only related to the input reference clock in this basic model. In order to make the frequency synthesizer more flexible , a phase accumulator replaces the address counter as illustrated in Figure 1.4 . The *frequency control word FCW* at the input of phase

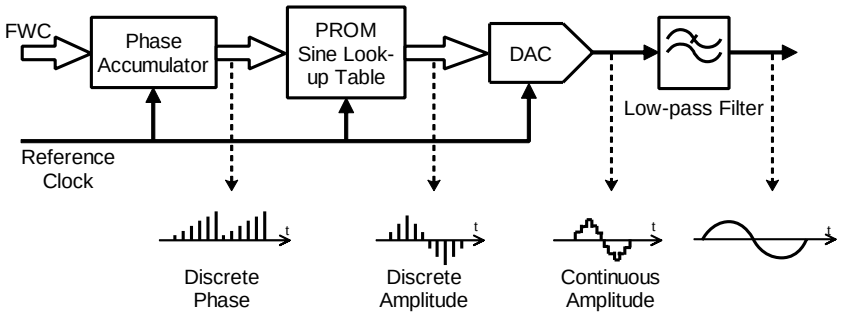

Figure 1.4: A modified model of a direct-digital frequency synthesizer.

accumulator determines the phase increment for each reference clock cycle. Assume that the number of bits of phase accumulator is N and the reference clock frequency is f_{ref}, the out put frequency f_{out} is given by

$$f_{out} = \frac{\mathrm{FCW} \cdot f_{ref}}{2^N} \tag{1.2}$$

The direct-digital architecture of the synthesizer has several advantages including fast settling, fine resolution, and simple implementation. It also allows the users to control the output amplitude, frequency and phase at all times. However, the issues of quantization noise, aliasing, and filtering also emerges as disadvantages. Additionally, the direct-digital frequency synthesis is not feasible at Ghz frequencies since it requires a reference clock frequency at least three times of the output frequency[3], which makes it impractical for RF applications.

1.1.3 Indirect Frequency Synthesis Based on Phase-Locked Loop(PLL)

PLL-based frequency synthesis approach is a widely utilized and most classical choice in all kinds of wireless communication system due to its high performance and flexibility. Basically, this approach employs a PLL which is a negative-feedback loop whose output is in phase with a reference signal to synthesize frequency using a programmable divider in the feedback path, as shown in Figure 1.5. The

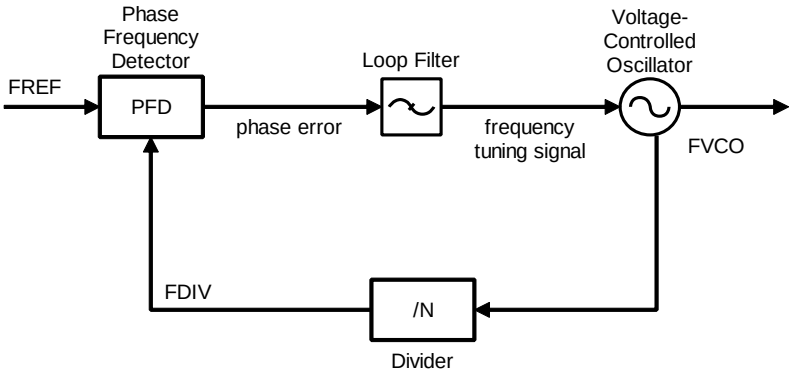

Figure 1.5: Architecture of a phase-locked loop.

phase/frequency detector (PFD) compares the phase of divided output (FDIV) with the phase of the reference input signal (FREF), then outputs the correction commands according to the detected phase deviation to a loop filter. The loop filter suppresses spurs produced in the PFD and generates frequency tuning signal to the *voltage-controlled oscillator* (VCO). At last, the output signal of VCO (FVCO) is fed into the programmable divider in feedback path, which results in the PLL output frequency being a multiple of reference frequency due to the negative-feedback manner. The relationship between input reference frequency (f_{ref}) , output frequency (f_{out}), and division ratio N is described as

$$f_{out} = N \cdot f_{ref} \tag{1.3}$$

The PLLs provide a superior alternative of obtaining a large number of higher frequencies from a single reference frequency. Usually, with a reference frequency in the typical range of 10-50MHz, the output signal may achieve a frequency of multi-GHz, which made PLLs perfectly suitable for modern RF system. Compared to

direct-analog approach, it requires significantly less area and power, meanwhile, generates a large range of frequencies. However, the switching time of PLLs is relatively larger than that of direct-analog and direct-digital techniques, since it is limited by the degradation in transient response resulting from the filter.

1.2 Report Organization

The objective of this report is to present a implementation of an All-Digital Phase-Locked Loop (ADPLL). The report is organized in seven chapters:

- In Chapter 2, some fundamental aspects of PLL is presented in order to give the reader a basic understanding of the PLL. An analog charge pump PLL is introduced in comparison with an ADPLL. This chapter also reveals the theory behind the ADPLL and continues with a general review on different ADPLL architectures.
- In Chapter 3, the fundamental theory of *time-to-digital converter* (TDC) is introduced. Different architectures of TDC is also reviewed with some modeling simulation results. A gated ring-oscillator based vernier TDC used in the ADPLL is introduced emphatically.
- In Chapter 4, the architecture of *digitally controlled oscillator* (DCO) is presented with both system level block diagram and detailed circuits schematic.
- In Chapter 5, the design and implementation of ADPLL is presented. Besides the two key sub-blocks, TDC and DCO, design of the digital loop filter is also introduced. And some descriptions on the entire system is covered in this chapter.
- In Chapter 6, the simulation results of the APDLL is presented.
- In Chapter 7, a conclusion of the entire work is drawn.

Chapter 2

Phase-Locked Loop Basics

2.1 Phase-Locked Loop Design Parameters

The performance of a PLL is characterized by a number of parameters. The requirements of each parameters are various dependent on different application of PLLs. In frequency snythesis application, the following design parameters are considered most important [6]:

- **Frequency tuning range** indicates the the frequency range that the output signal can cover. Most wireless communication systems are narrow-band which only cover 3-10 of the bandwidth. Table 2.1 [7] provides some examples of frequency band designations in wireless communication systems. The frequency tuning range is mostly limited by the oscillator in PLL.

	Frequency Range (MHz)	**Channel Spacing(kHz)**
GSM	925 to 960; 880 to 915	200
GPRS	925 to 960; 880 to 915	200
WCDMA	1920 to 1980	5000
Bluetooth	2402 to 2480	1000

Table 2.1: Frequency range and channel spacing in some wireless communication systems

- **Frequency resolution**, also called step size, defines the smallest frequency increment tuning size. The frequency resolution is mainly dependent on the system channel spacing which is also listed in Table 2.1. In order to synthesize the channel center frequency with sufficient accuracy, the frequency resolution is usually designed smaller than the channel spacing[7].

- **Phase noise or jitter** reflects the signal quality. Phase noise, defined as random phase fluctuation, describes noise in phase domain, while jitter describes the same phenomenon in time domain [6]. The phase noise results in the signal power spreading into nearby frequencies, which causes a skirt around the center frequency in the spectrum as shown in Figure 2.1. Assume

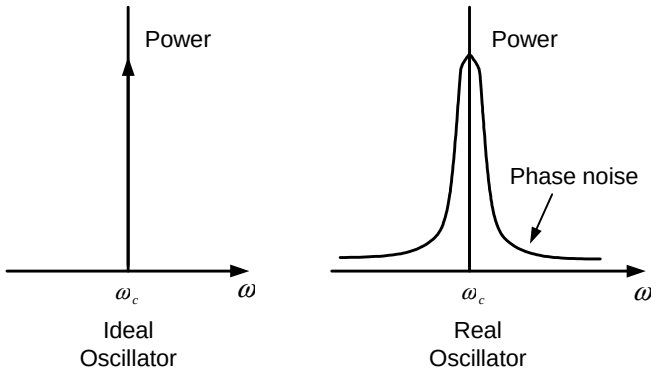

Figure 2.1: Phase noise in frequency domain.

an oscillator operating at frequency ω_c, the output of the oscillator can be described as

$$v(t) = \mathrm{A}\cos(\omega_c t + \Phi(t)) \tag{2.1}$$

where A is amplitude and $\Phi(t)$ is the phase noise. $\Phi(t)$ can be considered as a small random excess phase representing variations in the period [3]. The phase noise can result from various non-idealities such as component mismatches, nonlinearities, and quantization.

- **Spurious signal level** reflects the the level of discrete periodic interference noise in the siganl spectrum[8]. Both the spurious signal and the phase noise attribute to the phase fluctuation, however, the spurious signal refers to the periodic components in the phase fluctuation [7], as shown in Figure 2.2. The spurious tones also degrade the PLL's performance. It could be caused

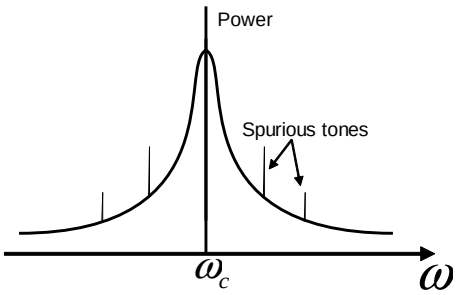

Figure 2.2: Spurious tones in frequency domain.

by the PFD and divider circuits in the PLLs, representing as a periodic timing error in time domain and undesired tones in frequency domain.

- **Loop bandwidth** indicates the dynamic speed of the feedback loop. It is also equal to the loop's natural frequency or the frequency in which the open loop gain is 1. Loop bandwidth is important when optimizing for phase noise, settling time, or filtering.

- **Settling time**, also known as switching time or locking time, is the time needed for the PLLs to switch the VCO from one frequency to another. As illustrated in Figure 2.3, the PLL switches from the initial frequency f_0

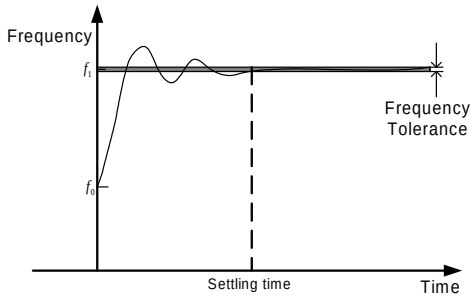

Figure 2.3: Settling time for f_0 switching to f_1.

to the final frequency f_1. Usually there should be a specified tolerance for the final frequency in a wireless communication standard, it is represented as the dark area in Figure 2.3. The settling time is largely dependent on the frequency step size, since the final frequency is approached gradually and asymptotically. It means that the settling time may be various with different initial frequency and final frequency. Therefore, the worst case time is generally considered as the typical settling time of the system. However, a PFD with a charge pump can provide an alternative to tremendously reduce the settling time, which will be introduced in next section. On the other hand, the loop filter used in the PLL to suppress spurs also limits the settling time. There is a design tradeoff between settling time and spur suppression.

2.2 Analog Phase-Locked Loop Architecture

The charge-pump PLLs are the vast majority of the PLLs used for wireless communication applications. According to the ratios of the output frequency to the input frequency, it can be classified into two types, integer-N architecture and fractional-N architecture. A typical charge-pump based PLL is shown in Figure 2.4. The phase frequency detector estimates the phase difference between reference frequency FREF and divided frequency FDIV and outputs the pulse width modulation signal whose width is determined by phase difference measured. This signal, named UP and DOWN in Figure 2.4, controls the charge pump to produce a current pulse $I_P - I_N$ which is a constant amplitude with proportional duty cycle. Then it is converted to VCO control voltage by a loop-filter. The phase detector with charge pump provides a method of measuring the frequency difference directly, which reduces the settling time significantly. With this charge-pump based PFD, the settling time is no more dependent on the initial frequency and target frequency. However, this charge-pump based PFD is vulnerable to glitches which are usually caused by mismatches between the UP and DOWN signal in

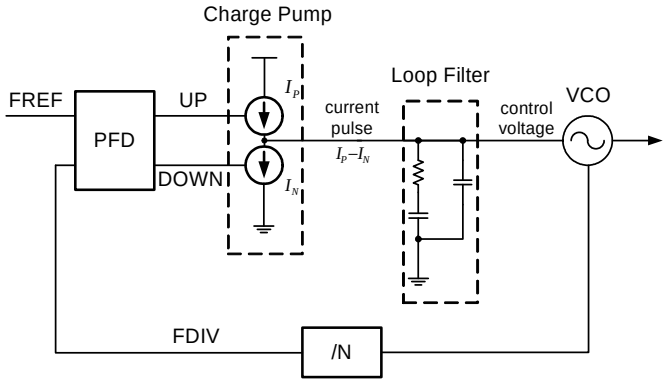

Figure 2.4: Block diagram of a charge-pump PLL.

the PFD and mismatches in the charge pump. Therefore, a loop filter is used to suppress the glitches[3].

In the feedback path, a frequency divider is used to scale the frequency within the loop and to generate the desired frequency at the output. The two different architectures of divider are reviewed in the next subsections.

2.2.1 Integer-N Architecture

For RF applications, the PLL may generate a very high frequency, usually multi-GHz. Thus, it is extremely tough to directly implement a programmable frequency divider working at a multi-GHz frequency. Instead, a pulse swallow frequency divider, shown in Figure 2.5, becomes a more practical solution. The high frequency

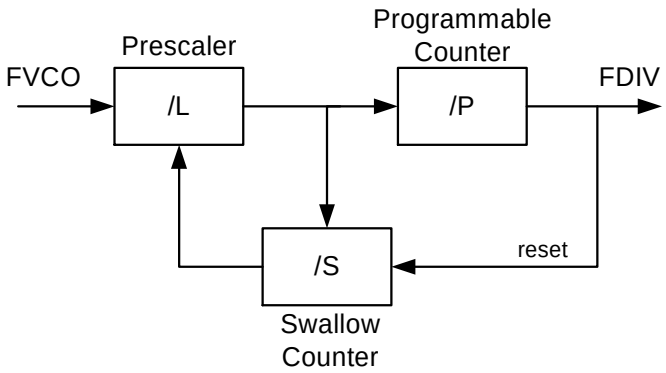

Figure 2.5: Block diagram of a pulse swallow frequency divider.

output of VCO, FVOC, is first prescaled by a factor of L (usually a power-of-2 number). Then, a program counter divides the output of prescaler by P, while a swallow counter divides the output of prescaler by S. The controllable value of S determines the output frequency of FDIV[3]. It is reasonable to assume that the

value of S is smaller than that of P, then the division ratio of the pulse swallow frequency divider is $N = PL + S$.

The integer-N architecture limits the frequency step size, since only integer multiples of reference frequency can be obtained. And due to feedthrough of the reference tone, the PLL bandwidth cannot exceed one tenth of the reference frequency, which further impacts the PLL dynamic behavior.

2.2.2 Fractional-N Architecture

The *integer-N* architecture sometimes can not meet the performance requirements of wireless applications due to the limitation of frequency step size and loop dynamics. Thus, the fractional-N architecture which can achieve finer frequency division ratio is used more widely in frequency synthesis. In the fractional-N architecture, the reference frequency can be set much higher regardless of the channel spacing, while the loop bandwidth can be improved. An example of a fractional-N PLL is shown in Figure 2.6. This fractional-N PLL uses a Sigma-Delta modulated divider

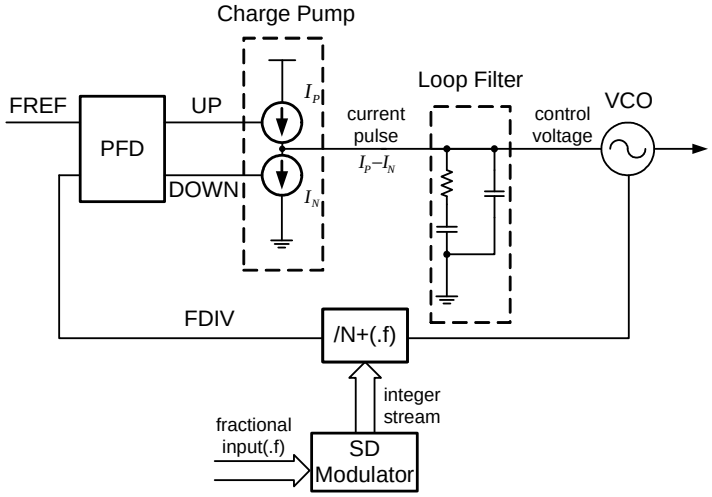

Figure 2.6: Simplified block diagram of a fractional-N PLL.

in the feedback path to generate a time-averaged frequency division ratio which is equivalent to a fractional ratio. The fundamental principle of integer modulation is illustrated in Figure 2.7[3]. As the division ratio alternating between N and $N + 1$, the average division ratio N_{avg} can be described as

$$N_{avg} = N + \frac{T_{N+1}}{T_{N+1} + T_N} = N + (.f) \tag{2.2}$$

where $.f$ is the fractional part of the division ratio, corresponding to the duty cycle of ratio $N+1$. In the fraction-N PLL shown in Figure 2.6, the fractional part $(.f)$ is fed into the Sigma-Delta modulator, then it outputs a small integer stream to the programmable divider. As a result, the VCO steady-state output frequency is

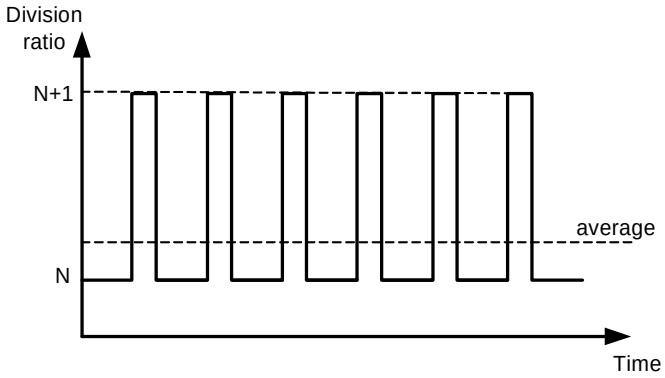

Figure 2.7: Division ratio v.s. time in modulator output.

determined by

$$f_{out} = N \cdot f_{ref} + (.f) \cdot f_{ref} \tag{2.3}$$

2.3 All-Digital Phase-Locked Loop Architecture

Although the charge-pump PLL is a predominant choice for RF synthesis, it is facing difficulties in silicon integration, especially in nowadays nanoscale CMOS. The loop filter in the analog architecture requires some large resistors and capacitors to realize spur suppression, which would consume a very large area on chip. Additionally, the analog intensive architecture lacks flexibility and portability from one process technology to another. Therefore, the demand in all-digital PLL(ADPLL) is obvious.

Unlike conventional PLL, all-digital phase-locked loop consists of only digital or digital-like circuits. Compared with the loop filter that occupies lots of area on the chip in the charge-pump PLL, a digital loop filter does not contain any capacitors and resistors. Its digital implementation significantly reduces the chip area. In the ADPLL, designers are able to access intermediate signals in digital form, which provides a huge advantage. For example, the bandwidth of the ADPLL can be changed easily by setting the parameters of the digital loop filter. Its digital nature also brings other benefits including low power consumption, noise free, and high flexibility.

This section provides a brief overview of ADPLL with two different architectures and comparison between ADPLL and conventional PLL.

2.3.1 Counter-Assisted Architectures

Figure 2.8 shows a *Counter-Assisted ADPLL* architecture. There are four main functional blocks in the ADPLL which are the time-to-digital converter (TDC), phase detector, digital loop filter and digitally-controlled oscillator (DCO). The system is clocked by the reference frequency (FREF). The target frequency is

determined by the input frequency command word (FCW). And the output signal of the ADPLL is noted as variable clock (CKV).

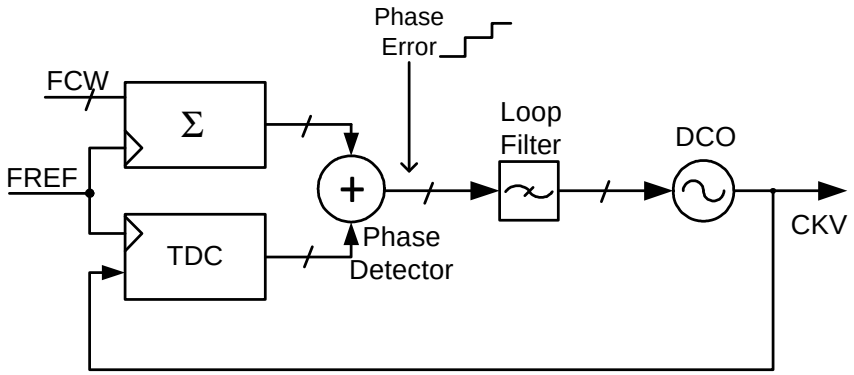

Figure 2.8: A simplified block diagram of counter-assisted ADPLL.

The time-to-digital converter digitizes the phase information of the DCO output by comparing its phase with the reference signal, while the reference phase accumulator stores the FCW value in each clock cycle to form reference phase. In the phase detector, the phase error is obtained by subtracting the TDC-evaluated phase information from the reference phase. Then, in the forward path, this phase error is converted to tuning word in the digital loop filter. According to the digital tuning word, DCO generates signal with frequency proportional to the tuning word. As a result, the output frequency of the DCO is locked to the target frequency due to this feedback mechanism[6].

2.3.2 Divider-Assisted Architectures

The *divider-assisted* architecture has the similar structure as the analog PLL, as compared in Figure 2.9. However, all the sub-blocks are shifted into the digital domain. The TDC and DCO become the interfaces between analog and digital domain. Thus, to be more accurate, the ADPLL is a mixed-signal system.

This divider-assisted architecture contains three essential blocks which are TDC, digital loop filter, and DCO. The TDC acts as a PFD based on charge pump, which measures the phase difference between output and reference directly. Digital loop filter further attenuates the noise generated by TDC and produces tuning word according to the digitized phase error. In the feedback path, a frequency divider is located for frequency division of the DCO output. The function of this divider is almost the same as in an analog PLL, by setting the division ratio, the output frequency of the ADPLL can be changed accordingly. Contrary to PFD and VCO in analog PLL, both the DCO and the TDC introduce the quantization noise to the system, which degrade the purity of output. This quantization noise can be reduced by minimizing the quantization step of both block. Thus, TDC and DCO with fine resolution is essential in ADPLL.

In this thesis, we mainly focuses on this divider-assisted architecture, since the proposed ADPLL is implemented based on this structure.

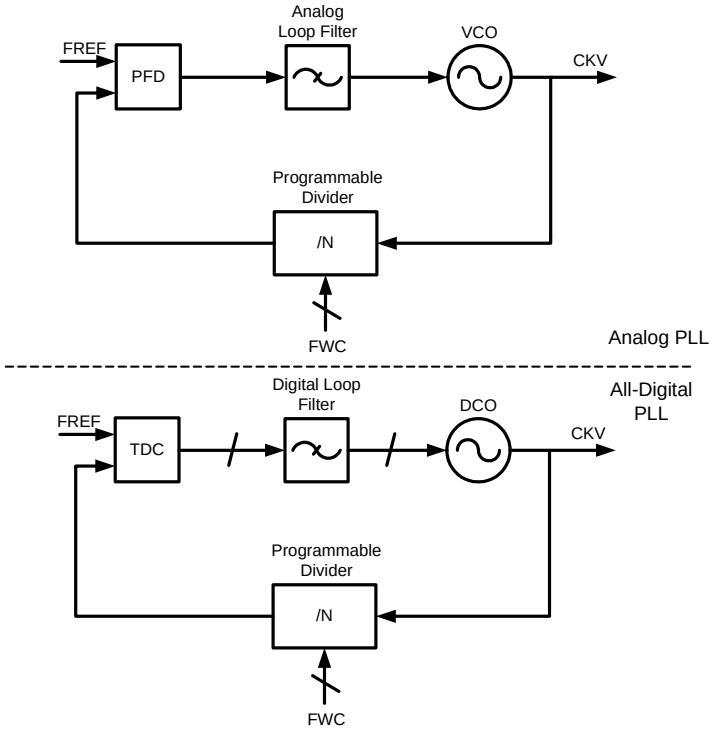

Figure 2.9: Comparios of a divider-assisted ADPLL and an analog PLL.

2.3.3 Comparison of ADPLL and PLL

Although the ADPLL and conventional PLL share similar system structure, there are some fundamental differences between them. One key difference is that the analog PLL does not operate in the phase domain except when the system is locked or close to the locked point. Only under the locked condition, the phase modeling is available as a small-signal approximation. In the charge-pump PLL, PFD based on charge pump generates signals with spurs that require filter, which results in a tradeoff between spur suppression and settling time. On the contrary, the ADPLL can employ a wide-bandwidth loop filter for shorter settling time because of its linear operation. Another key difference is that the traditional PLL converts the phase difference between reference and feedback into an analog quantity, while the ADPLL converts the relationship between reference and feedback to digital words then compares these signals to obtain phase error[3].

Chapter 3

Time-to-Digital Converter

3.1 Introduction to Time-to-Digital Converter

The time-to-digital converters (TDC) that offer precise measurement of the time interval between two events are widely used in different field. For high-energy physics application, it can provide very accurate time-of-flight measurement in term of picoseconds. For measurement instrumentation applications, it can deliver time-related information in digital oscilloscopes and logic analyzers. However, the most famous application of TDC is in frequency synthesis, employed by ADPLL [9].

In a divider-assisted ADPLL, Time-to-digital converter (TDC) is one of the most crucial blocks. Serving as a charge-pump based phase detector, the TDC measures and digitizes the phase difference between reference signal and feedback signal. The TDC is a mixed-signal block and also the interface between time domain and digital domain. Therefore, it is unavoidable that the TDC induces quantization errors when converting time to digital words due to finite resolution. The quantization error could dominate the in-band phase noise at the output of ADPLL while it also limits the loop bandwidth. The limitation on the loop bandwidth in turn reduces the suppression of DCO phase noise, causing poor overall phase noise performance. The key to reduce quantization error is to improve the resolution of the TDC. Thus, design and implementation of high-resolution TDC become the ultimate goal for the designers. With most recent process technology and refined architecture, the resolution can easily reach below 10 ps. Besides high-resolution, low dead time and large dynamic range are also required for high quality TDC. Dead time refers to the minimum time between two measurements. On the other hand, dynamic range, also named detection range, is the maximum time interval that can be measured by TDC[10]. Since the TDC may working at different frequencies, Both low dead-time and large dynamic range secure the functionality and stabilizability of the system.

This chapter provides a review on different TDC architectures and brief explanations on their operation principles. Apart from the fundamentals, design and implementation of the proposed Vernier gated ring oscillator based TDC is also presented.

3.2 TDC Architectures

Generally, according to the circuits implementation, TDCs can be classified into analog TDCs and digital TDCs. In the traditional analog approach, the time interval is first converted into a voltage, then this voltage is translated into digital form by an analog-to-digital converter. However, this approach suffers from non-linearity and unstable. For ADPLL application, the digital approach becomes the most popular choice. Since digital TDCs are designed based on different methods of measurement, they will be introduced accordingly.

3.2.1 Counter-Based TDC

Counter-based TCD is the most straightforward and simplest technique to quantize a time interval. It uses a counter to count the cycles of a reference clock fitting into the respective measurement interval[9]. The time can be roughly estimated by multiplying the reference clock period by the number of clock cycles counted, as illustrated in Figure 3.1. However, the start and the stop signal that define

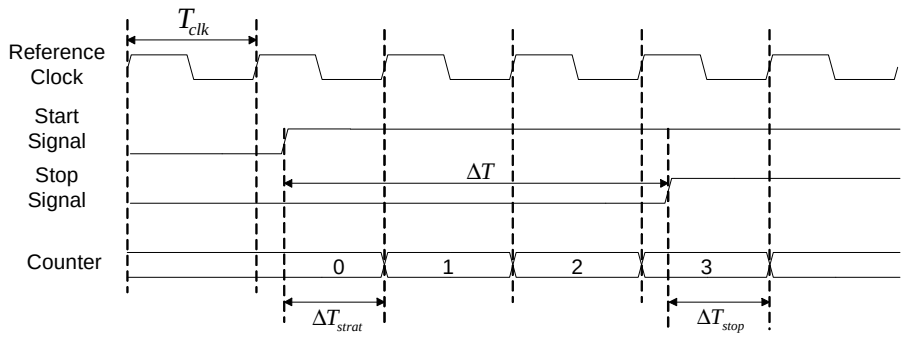

Figure 3.1: Waveform of a counter-based TDC.

the measurement time interval are not synchronous to the reference clock, which induces error to the obtained result. The real time interval measured can be described as

$$\begin{aligned}\Delta T &= N \cdot T_{clk} + (T_{clk} - \Delta T_{stop}) - (T_{clk} - \Delta T_{start}) \\ &= N \cdot T_{clk} + \underbrace{\Delta T_{start} - \Delta T_{stop}}_{\text{quantization error}}\end{aligned} \tag{3.1}$$

where N is the number of clock cycles, T_{clk} is the clock period, ΔT_{stop} and ΔT_{start} are the errors at the beginning and the end of time interval. It is obvious to see that the quantization resolution is dominated by the reference clock period. However, it is not effective to increase the clock frequency for higher TDC resolution. Not only does the higher clock frequency consume more power, but also the counter has a timing restriction. Therefore, some other architecture is developed that can achieve higher resolution without increasing the clock frequency.

3.2.2 Delay-Line-Based TDC

Delay-line-based TDC uses a chain of digital delay elements to quantize the time interval instead of reference clock. This kind of architecture improves the resolution to the delay of the delay elements in the chain. The operation principle of delay-line-based TDC is illustrated in Figure 3.2. The start and stop signals

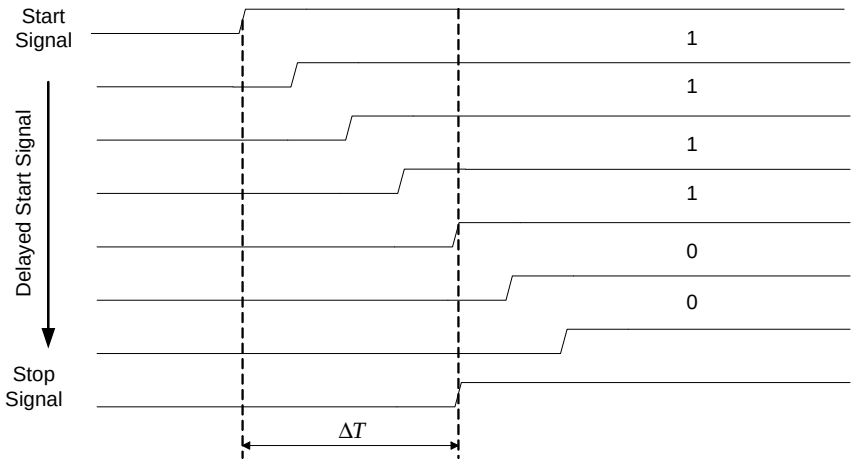

Figure 3.2: Waveform generated by a delay-line-based TDC.

indicate the time interval being measured. As the start signal delayed by a chain of delay elements, the stop signal will be in phase with the N^{th}-stage delayed start signal. In other words, the stop signal and delayed start signal will be sampled simultaneously at some point. Usually, flip-flops are used as sampling block for detection of this point. The delay that causes the two signals in phase reflects the measurement time interval. The core structure of delay-line-based TDC is shown in Figure 3.3. The start signal propagates along a delay chain, and each delayed

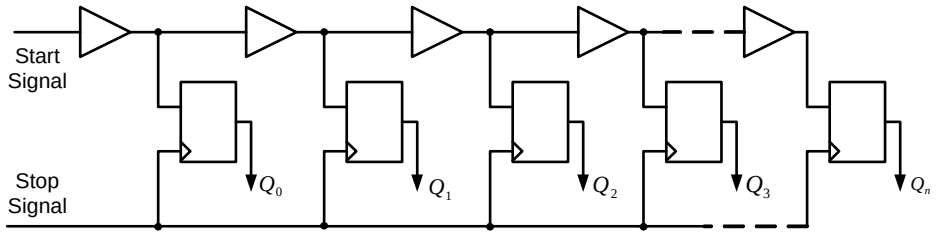

Figure 3.3: Block diagram of a delay-line-based TDC.

start signal is clocked by the stop signal in the sampling flip-flops. When the stop signal samples the delayed start signals at rising edge, the delay stages that have been already passed by the start signal generate "1" at flip-flops' outputs and the delay stages that have not been passed by the start signal yield "0" outputs. The transition point of "1" to "0" indicates that the start signal and the stop signal are

in parallel with each other at this point. Assume that the number of "1" outputs is N, and the delay of each delay element is τ, the measurement time interval ΔT can be described as

$$\Delta T = N \cdot \tau + \epsilon \tag{3.2}$$

where ϵ is the quantization error that arises as a delay element has been either passed by the start signal yet or not[9].

Compared to the resolution of a counter-based TDC, the resolution of delay-line-based TDC does not rely on a high frequency reference clock, but on the delay of each delay element. This architecture improves the resolution to a gate delay, while it consumes not much power. However, the delay is always limited by the CMOS process used by the TDC. This limitation is further overcame by other structures introduced next.

3.2.3 Vernier TDC

Vernier TDC provides a structure to overcome the process limitation. The operation principle of Vernier TDC is very similar to that of delay-line-based TDC, as illustrated in Figure 3.4. Instead of one chain of delay elements, the Vernier TDC

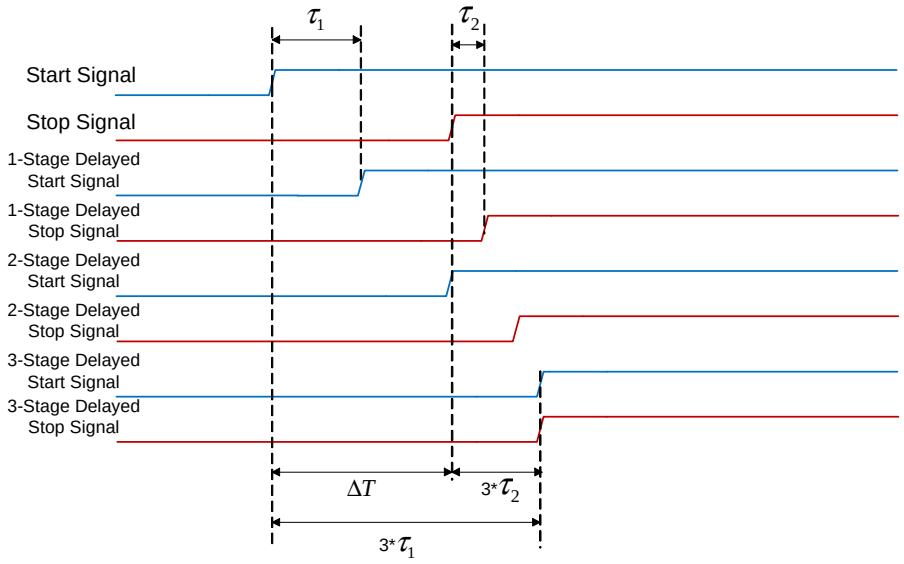

Figure 3.4: Waveform in a Vernier TDC.

uses two to process both start and stop signal. As shown in Figure 3.5, a start signal propagates through one of the delay chain with lager unit delay of τ_1, while the stop signal propagates through the other with smaller unit delay τ_2, clocking the flip–flop at each stage. The resolution is determined by the difference between two propagation delay values. Assume that after N stages of delay the rising edge of stop signal catches up with start signal, the measurement time interval can be

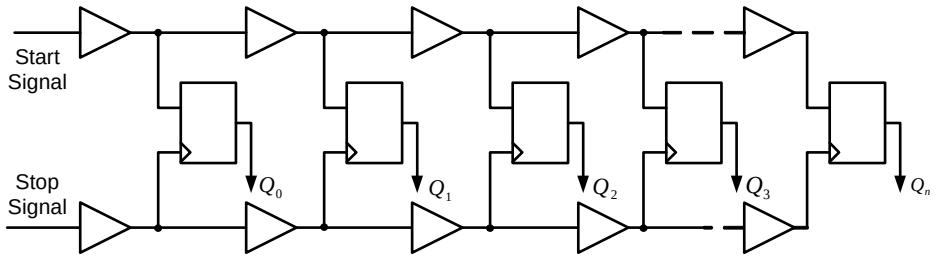

Figure 3.5: Block diagram of Vernier TDC.

given by

$$\Delta T = N \cdot (\tau_1 - \tau_2) + \epsilon \tag{3.3}$$

where ϵ corresponds to the quantization error illustrated in Figure 3.4.

Apart from that Vernier TDC is able to achieve better resolution, it is first-order tolerance of the PVT variation if the delay line are well matched. However, as the resolution getting higher, the dynamic range is limited to $DR = m(\tau_1 - \tau_2)$, where m is the number of delay cells. In order to overcome this limitation, a *Vernier ring oscillator TDC* is put forward. It replaces the delay lines by ring oscillators, as shown in Figure 3.6. Since the ring oscillator is a loop, the start

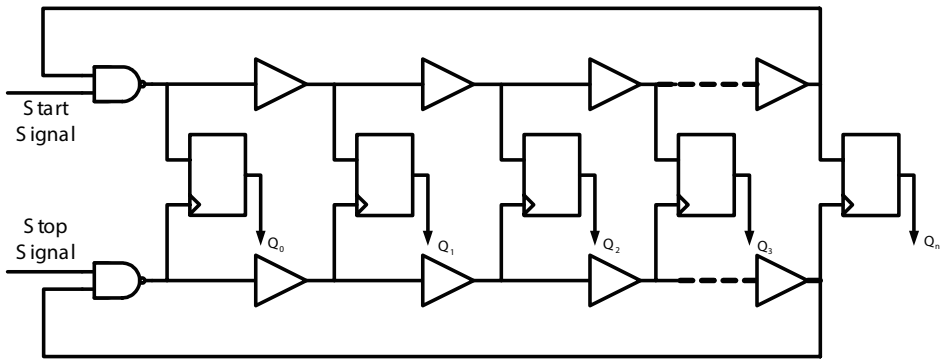

Figure 3.6: Block diagram of Vernier ring oscillator TDC.

and stop signals can propagate endlessly. The dynamic range is no longer limited by the delay stages and can be extended without bound ideally. The operating principle of Vernier ring oscillator TDC is the same as Vernier TDC, thus there will be no more extra explanations.

3.2.4 Gated-Ring-Oscillator TDC

Gated-Ring-Oscillator(GRO) TDC abandons the delay-lines used in the previously introduced TDCs and replaces them with a gated-ring-oscillator. As shown in Figure 3.7, a 3-stage GRO is used to generate the high frequency oscillation phases. A logic block generates the enable signal to control the GRO to oscillate at the

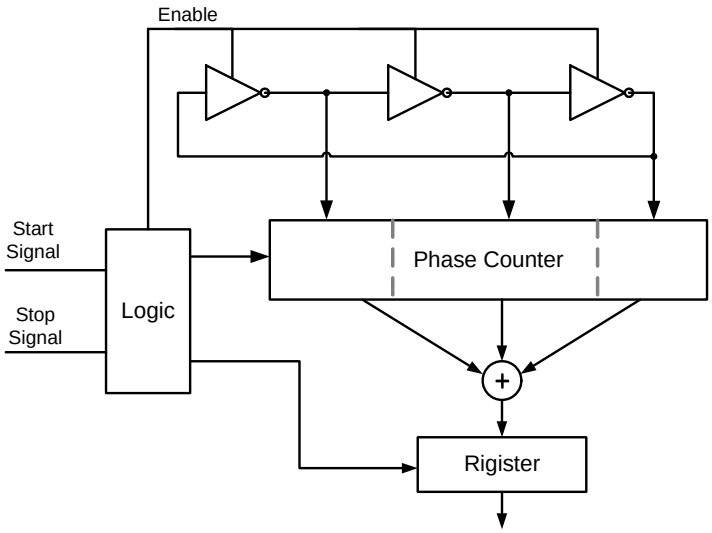

Figure 3.7: Block diagram of a GRO TDC.

arrival of start signal and disables the GRO when stop signal arrives. Then the outputs of GRO are fed into a phase counter. The measurement of time interval is realized by counting the transitions of each GRO output phase during the given time interval [11]. The measurement time interval can be given by

$$\Delta T[k] = N[k] \cdot \tau_{inv} + \epsilon[k] \tag{3.4}$$

where N is the number of counted phase transitions, τ_{inv} is the delay of each inveter in GRO, also equivalent to the raw resolution of GRO TDC, and ϵ is the quantization error. This measurement method provides a very unique property that can be used to improve the in-band noise. Unlike a Vernier ring oscillator TDC, the GRO structure only allows the oscillator to have transitions during a given measurement when the gates are enabled, and strives to freeze the ring oscillator state between measurements, as shown in Figure 3.8. As a result, the residue generated at the end of previous measurement $T_{stop}[k-1]$ is transferred to the next measurement interval, $T_{start}[k]$.

$$T_{start}[k] = T_{stop}[k-1] \tag{3.5}$$

Therefore, according to Figure 3.8, the quantization error can be described as

$$\epsilon[k] = T_{stop}[k] - T_{start}[k] = T_{stop}[k] - T_{stop}[k-1] \tag{3.6}$$

This discrete-time first-order differential operation on time residue of each conversion, T_{stop} , corresponds with a first-order noise shaping in the frequency domain [12]. With this first-order noise shaping effect, the quantization noise is moved to high frequency region, thus a lower in-band noise is achieved [11].

The gated-ring-oscillator TDC can be adapted to a gated-ring-oscillator based Vernier TDC (GVTDC) in the way that the delay-line TDC is modified to a Vernier

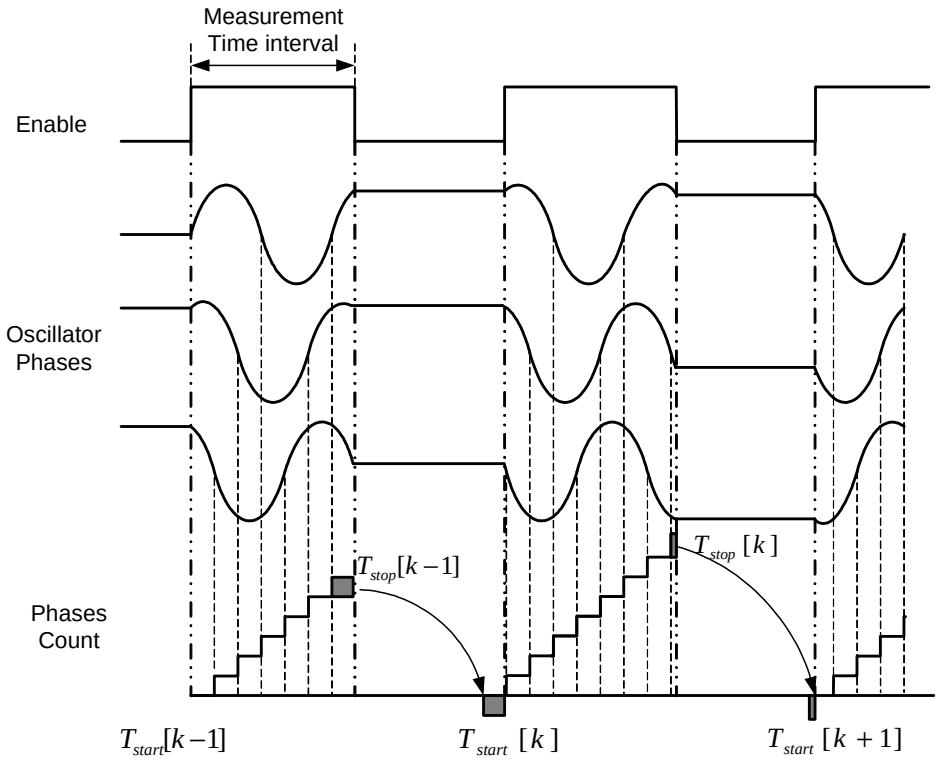

Figure 3.8: Waveform generated by a GRO TDC.

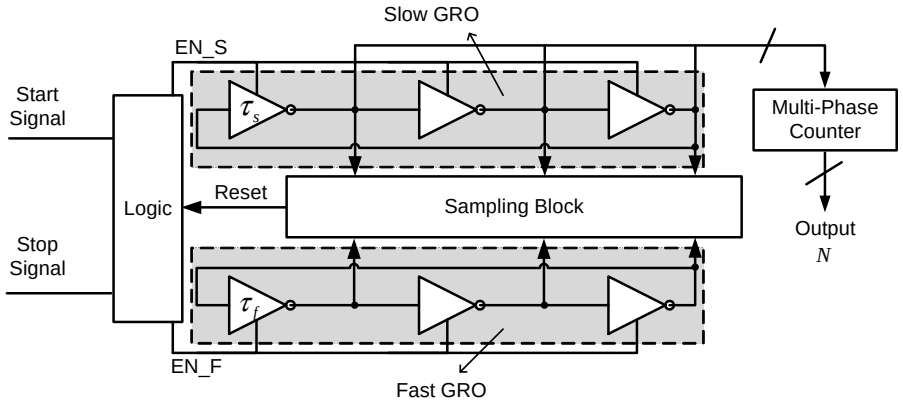

Figure 3.9: Block diagram of a gated Vernier TDC.

TDC, as shown in Figure 3.9. A phase frequency detector accepts the input start signal and stop signal and generates enable signals, EN _S and EN_F, controlling the slow GRO (generates lower output frequency) and fast GRO (generates slightly higher output frequency) respectively. During each measurement, the PFD always

ensures that the EN_S signal leads the EN_F signal. When the sampling block detects that the output of fast GRO catches up with the output of slow GRO like in a Vernier TDC, a reset signal is generated and feedback to the PFD to disable both EN_S and EN_F. Meanwhile, the multi-phase counter counts the number of phases generated by the GRO and stores the result in register. As a result, according to the quantized delay output, the measurement time interval is obtained by

$$\Delta T = N \cdot (\tau_s - \tau_f) + \epsilon \tag{3.7}$$

where τ_s is the unit delay of the slow GRO and τ_f is the unit delay of the fast GRO. Compared to the vernier ring-oscillator, the gated-ring-oscillator Vernier TDC can either achieve the same raw resolution with lower effective quantization noise power or achieve the same effective quantization noise power with lower raw resolution. A lower resolution can provide faster conversion time, decreasing the typical long latency time [13].

3.2.5 High-Order Noise-Shaping TDC

As mentioned in the last section, gated-ring-oscillator Vernier TDC can provide first-order noise-shaping. Since the quantization error is accumulated across successive measurements, the quantization noise is shaped in frequency as in a first order $\Delta\Sigma$ ADC [13]. Similar to the design of $\Delta\Sigma$ ADCs, the noise-shaping concept can also be extended to higher orders. A multi-stage noise-shaping (MASH) architecture is a good choice for high-order noise-shaping TDC, since it can obtain high-order moise-shaping property and offer more freedom to choose a structure for each stage. For instance, a 1-1 MASH GRO TDC, as shown in Figure 3.10, is built by cascading two identical GRO Vernier TDC. The quantization error from

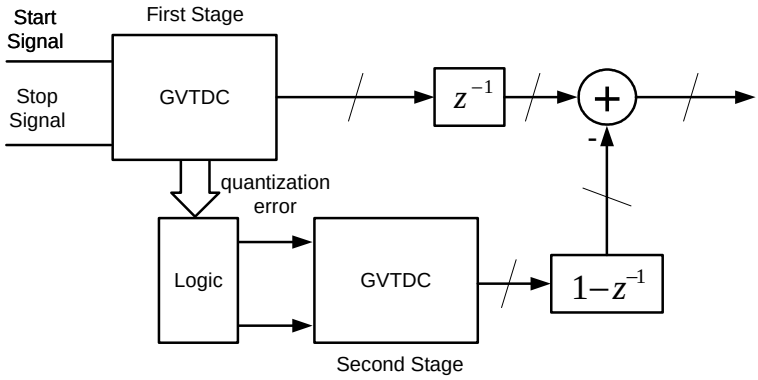

Figure 3.10: Block diagram of a second-order noise-shaping gated Vernier TDC.

the first stage is fed into the second stage. This is done by logic operations on outputs of both GROs. Two TDC blocks are combined together with the help of few additional digital blocks to achieve second-order noise-shaping [14].

Figure 3.11 shows the behavioral simulation results of the 1-1 MASH GRO TDC with second-order noise-shaping. The input signal is a sinusoidal wave which is realized by varying the measurement time interval according to the sinusoidal function. Compared to a signal stage GRO TDC, the in band quantization noise is further suppressed. And an expected second-order 40 dB/decade slope can be observed.

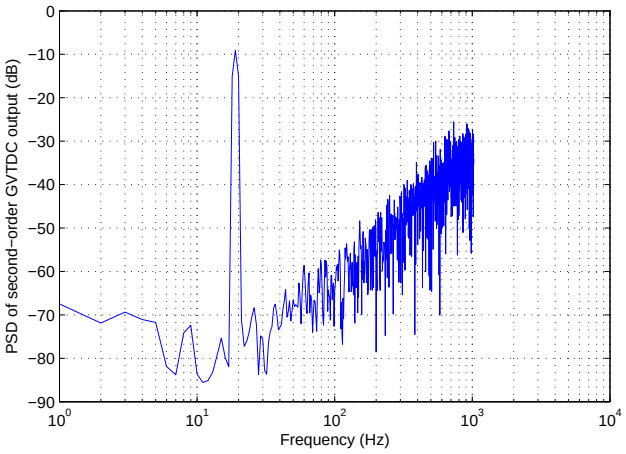

Figure 3.11: The spectrum of second-order noise-shaping TDC output.

3.3 Two-Dimension Gated-Ring-Oscillator Vernier Time-to-Digital Converter

3.3.1 Operation Principle

In this section, the TDC utilized in the proposed ADPLL is introduced. Compared with the GVTDC introduced in the last section, this 2-D GVTDC can not only achieve a higher resolution, but also extent the dynamic range and reduce the latency considerably. In order to understand how the two-dimension GVTDC works, it is good to start with the operation principle of the 2-D Vernier TDC operates.

In a 5-stage linear Vernier, as shown in Figure 3.12, one of the delay line has a delay of 4Δ,and the other has a delay of 5Δ. Assume that the measurement time interval is $n\Delta$ (the stop signal edge lags the start edge by $n\Delta$). Then the stop signal edge will be lined up with the start signal edge after n stages. In this case, the delay quantization is realized by taking the time differences only between taps that locates in the same position of the two delay lines, which results in only five quantization levels for two delay lines with five elements [15]. However, the quantization levels can be increased if all possible differences between the taps are

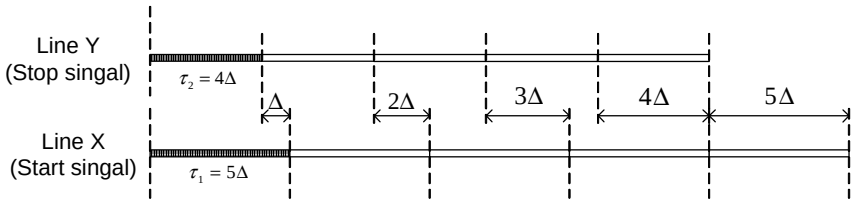

Figure 3.12: 5-stage linear Vernier.

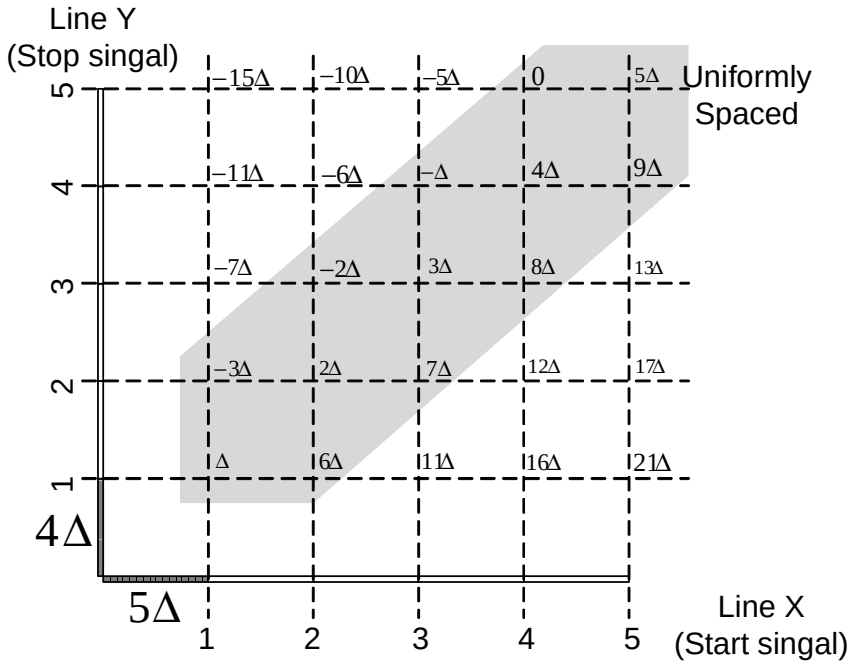

Figure 3.13: 5-stage 2-D Vernier plane.

used, as shown in Figure 3.13, where 25 quantization levels can be obtained from two delay lines with five elements. It should be noticed that only the quantization level from [-3Δ, 9Δ] is uniformly spaced[15].

As mentioned in the beginning of this section, the 2-D Vernier architecture reduces the latency significant for a given number of quantization levels. For the example described in Figure 3.13, it only needs $4\tau_1$ to detect an input of 8Δ. However, $8\tau_1$ is needed for a linear Vernier TDC to detect the same amount of input. In this case, the latency of the shown 2-D Vernier TDC is reduced by a factor of 2. Notice that, some even better latencies can be achieved with the 2-D Vernier architecture.

In a Vernier plane as shown in Figure 3.13, the differential delay generated at the position (x, y), $D(x, y)$, can be described as [15]

$$D(x, y) = x \cdot \tau_1 - y \cdot \tau_2 \tag{3.8}$$

where x and y are the coordinates in Vernier plane, and τ_1 and τ_2 represent the element delay of each delay line. In order to realize time-to-digital converter, the differential delays generated in the Vernier plane is arranged into a vector to obtain an ordered set of time references with a constant quantization step Δ. The conversion operation is performed by a routing function $i = i(x, y) \in \mathbb{N}$ which associates the position i in the vector with the coordinates (x, y). Thus, (3.8) can be rewrite as [15]

$$i(x, y)\Delta = x \cdot \tau_1 - y \cdot \tau_2 \tag{3.9}$$

$$i(x, y) = x\frac{\tau_1}{\Delta} - y\frac{\tau_2}{\Delta} \tag{3.10}$$

It can be conclude from equation (3.10) that the quantization step Δ need to be the *Greast Common Divider* (GCD) of unit delay τ_1 and τ_2 to guarantee the existence of routing function in $\mathbb{N}$[15]. Therefore, we can set that $\tau_1 = k\Delta$ and $\tau_2 = (k-1)\Delta$ where k is an integer to give a particular class of a 2-D Vernier. Under this condition, (3.10) can be modified to[15]

$$i = xk - y(k-1) \tag{3.11}$$

This equation can be inverted, obtaining[15]

$$\begin{cases} x(i) = i - \left\lfloor \dfrac{i-1}{k} \right\rfloor (k-1) \\ y(i) = i - \left\lfloor \dfrac{i-1}{k} \right\rfloor k \end{cases} \tag{3.12}$$

where $\lfloor a \rfloor$ is the inferior integer of a.

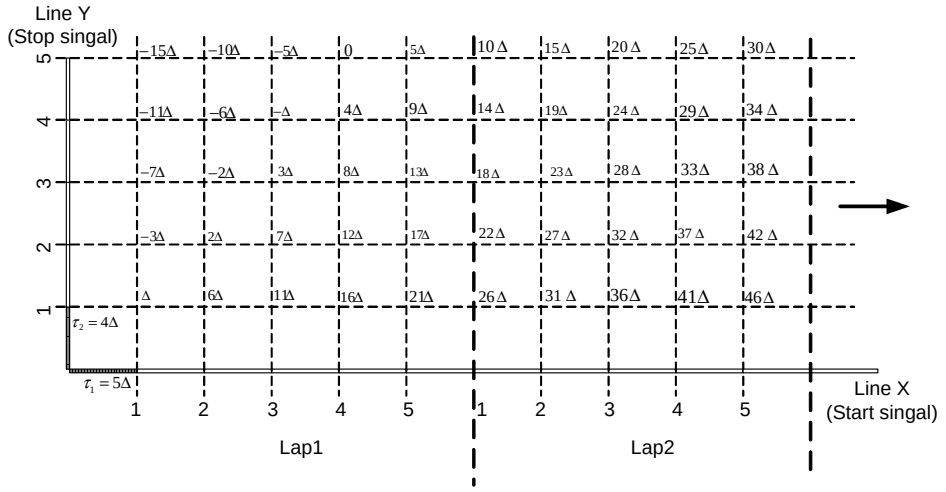

Figure 3.14: An equivalent 2-D Vernier plane of a 2-D GRO Vernier.

However, this equation is obtained under the limitation that y is between 0 and k. To adapt this 2-D Vernier TDC theory to a 2-D GRO Vernier TDC, the

ring operation of the GRO should be taken into consideration. It means that the same coordinate (x, y) in 2-D GRO Vernier may correspond to different delays. For example, in a 2-D GRO Vernier TDC with 2 five-stage GROs, when setting $k = 5$, the equivalent 2-D Vernier plane is illustrated in Figure 3.14. For the same coordinate $(3, 3)$, the corresponding deferential delay counld be 3Δ, 28Δ... Therefore, it can be concluded that the output of 2-D GRO Vernier TDC is determined by both the coordinates (x, y) and the number of laps the GRO have run [16]. Different from the 2-D Vernier TDC that only partial matrix positions (the uniformly spaced positions) in the 2-D plane are used, the 2-D GRO Vernier TDC can fully utilize all positions in the 2-D plane due to its operation property.

3.3.2 Circuit Implementation

A 2-D GRO Vernier TDC can be derived from the classical GRO Vernier architecture where the time measurements are realized with two gated-ring-oscillators and the digital conversion is performed by sampling blocks and thermo-to-binary decoder. Figure 3.15 illustrates the circuits implementation of the 2-D GRO Vernier TDC implemented with 65nm CMOS technology. In the proposed TDC, the ratio between the unit delays of the two GROs, τ_1/τ_2, is set to 31/30. This ratio is chosen based on the target dynamic range and resolution. To define the proper routing function, it is critical that the ratio τ_1/τ_2 is set precisely to 31/30. For this reason, a calibration circuit is utilized to tune the element delay of each GRO before the measurements start, ensuring the accuracy of each measurement.

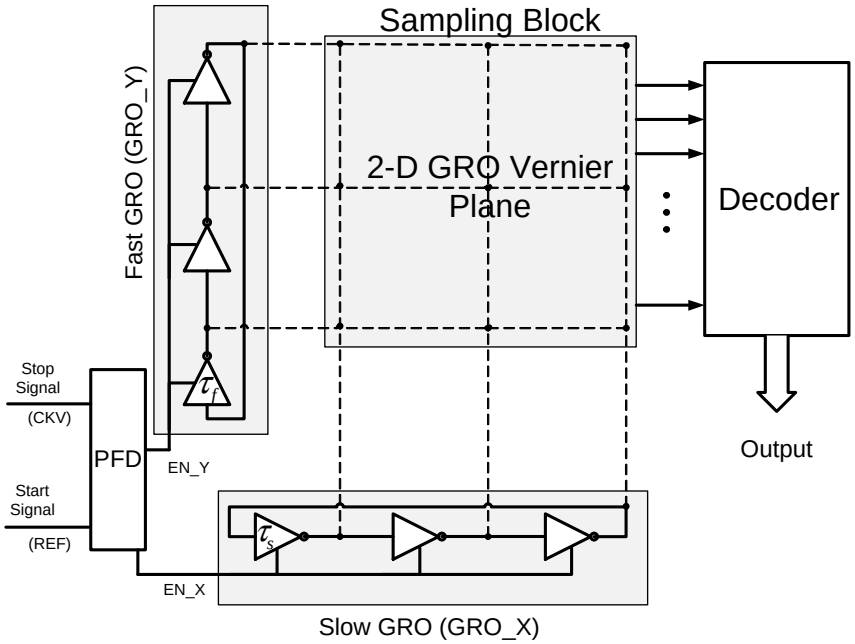

Figure 3.15: Block diagram of the proposed 2-D GRO Vernier TDC.

The proposed 2-D GRO Vernier TDC consists of a phase frequency detector, two 3-stage GROs, sampling blocks and a decoder. The operation function and principle of some sub-blocks have already been introduced in the previous section. However, some of the sub-blocks are modified for the 2-D GRO Vernier architecture. For each point defined by the function (3.10), there is a flip-flop employed as a sampling element to detect at which position of the matrix the phase of fast GRO catches up with the phase of slow GRO. The coordinates information generated by the sampling blocks is then converted and output by a decoder. Since flip-flops are deployed as sampling blocks, only rising edges of the GRO outputs are used, resulting in the raw resolution of TDC becoming twice of the difference between two GROs inverter delay. This sampling technique can avoid the mismatches between rise time and fall time of the inverters. Therefore, combined with the ratio τ_1/τ_2 being 31/30, the inverter delays of slow GRO and fast GRO are forced to be 77.5ps and 75ps respectively to achieve the target raw resolution of 5ps.

Phase Frequency Detector

As illustrated in Figure 3.15, the PFD accepts the input time intervals indicated by start and stop signal. According to the phase of the input signals, the PFD generates the enable signals EN_X and EN_Y that are in phase with the start signal and stop signal to control the slow GRO and fast GRO respectively. When each measurement finishes, a reset signal RBO generated by the decoder is sent to the PFD to disable both GROs. A waveform generated by the PFD is depicted in Figure 3.16. In the entire ADPLL system, TDC is used to detect the phase difference between reference signal and divided DCO output, therefore, the start signal could either lead or lag the stop signal. However, in the GVTDC, signal EN_Y leading signal EN_X will cause wrong outputs. It is necessary for PFD to guarantee that the signal EN_X is generated in phase with the leading one between start and stop signal. In the case of the stop signal being in the lead, a "Sign signal" should be generated by the arbiter in the PFD to indicate that output of the TDC is negative.

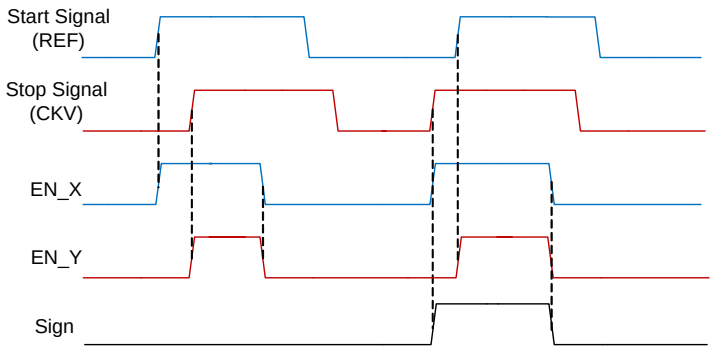

Figure 3.16: Waveforms generated by the PFD of GVTDC.

In the circuit of PFD shown in Figure 3.17, two modified *true-single-phase-clock flip-flops* (TSPC) with always high inputs are used to sample the input phase

and to produce enable signals. The arbiter that consists of D flip-flops and digital logic blocks can generate a select signal to the multiplexers (correspond to the sign signal mentioned in the last paragraph) based on the phase relationship between start signal and stop signal. Then, according to this select signal, the multiplexers output the leading one of the start and stop signals to contribute to the EN_X, and the lagging one to contribute to the EN_Y.

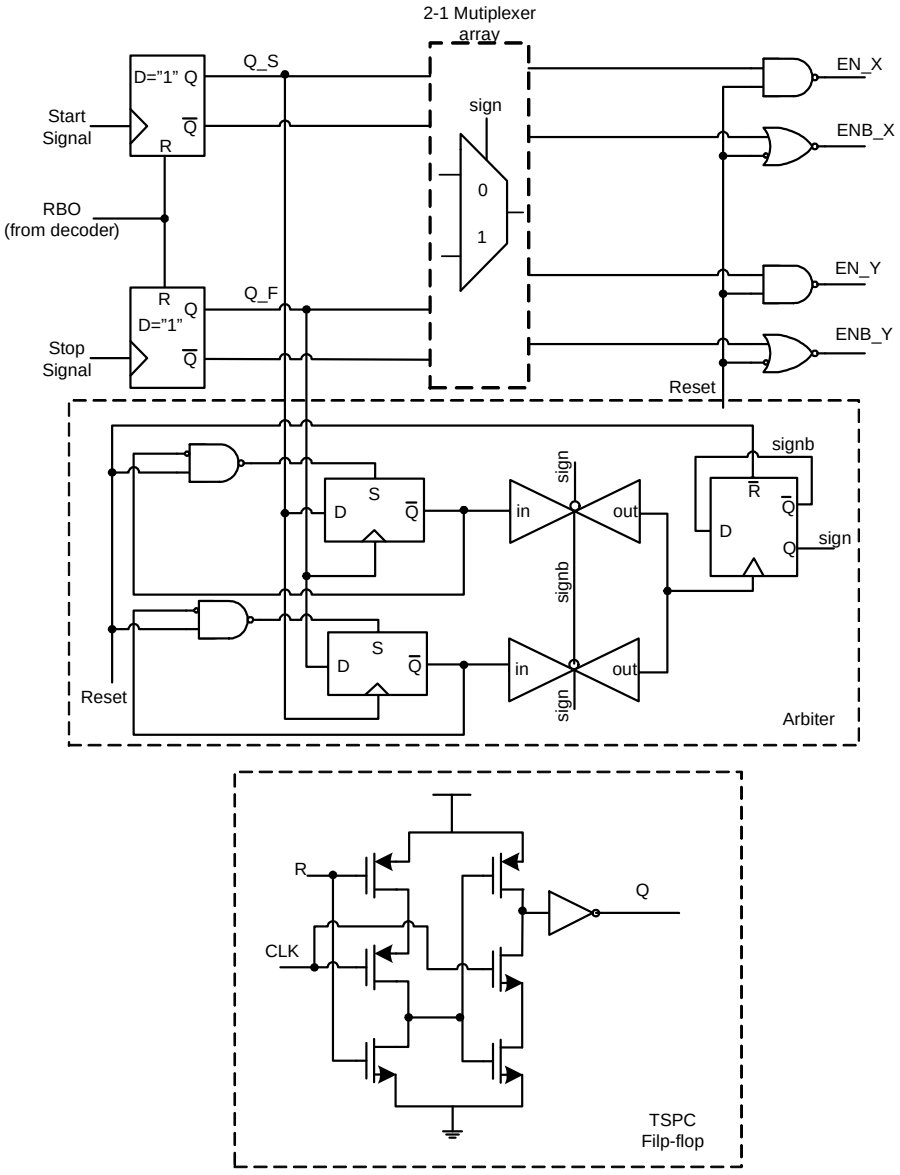

Figure 3.17: Circuit bolck diagram of the PFD and TSPC flip-fliop.

Gated-Ring-Oscillator

Two 3-stage GROs with different oscillation frequency are used in the proposed TDC to form a GRO based Vernier. It consists of 3 identical gated inverters, as shown in Figure 3.18. The slow GRO (GRO_X) which controlled by EN_X has a oscillation period of 465ps (with inverter delay of 77.5ps), while the fast GRO (GRO_Y) which controlled by EN_Y has a oscillation period of 450ps (with inverter delay of 75ps). When the enable signal is logic high, GROs start oscillation like a common ring-oscillator, and when the enable signal is logic low, GROs freeze the state at that time. As mentioned previously in this section, the inverter delay can be tuned by a calibration circuit before the measurements start to ensure the desired delay ratio between two GROs. This is realized by introducing a inverter delay tuning words, V_{ctrl}, which is applied on the NMOS switch controlling the loading capacitors, so that the inverter delay of the ring-oscillator can be tuned. This inverter delay tuning bits is generated by a digital calibration block which is implemented in pure digital flow.

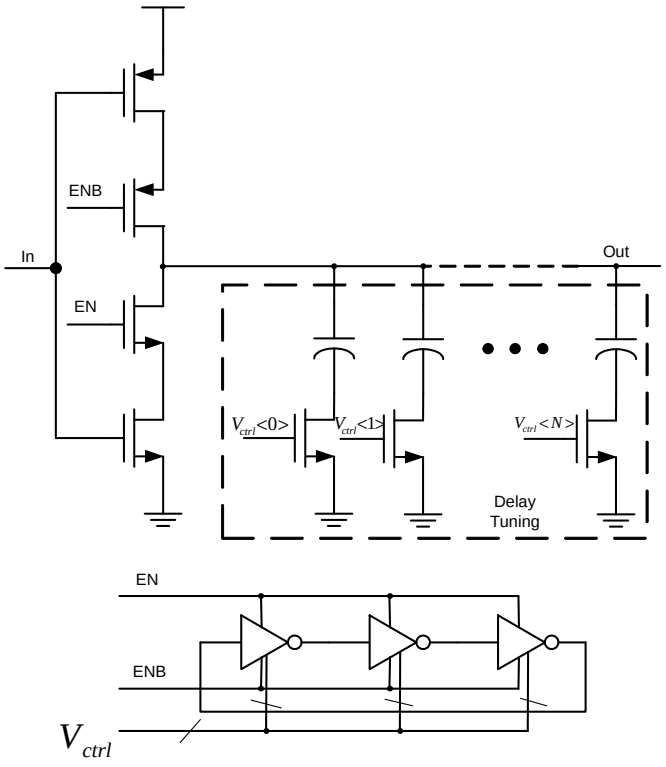

Figure 3.18: Circuit bolck diagram of the GRO cell.

Sampling Blocks And Decoder

The sampling blocks are used to compare the phase of GROs outputs. Since the target resolution of the TDC is 5ps, an even smaller time offset of the sampling blocks is required to avoid extra noise. To realize minimal time offset and narrow metastability region, a modified *sense-amplifier-based flip-flop* which has a sampling window below 1ps is chosen. As shown in Figure 3.19, this architecture compensates the mismatch between D-to-Q and CLK-to-Q delays by reordering the D port and CLK ports in pull-down paths and by adding a dummy capacitor to the D port to balance the input loading [17].

The decoder contains multiphase counter, digital logic and thermo-to-binary converters. The thermo-to-binary converter is used to convert the thermo-codes generated by the sampling blocks into binary codes for calculation. While the multiphase counter is responsible for counting the phases generated by GROs. One single multiphase counter would be enough for counting all phases generated by one of the GROs if combining all phases generated by each stage into one signal [16]. Based on the information provided by the sampling blocks, the decoder obtains the corresponding coordinate of the measurement input, then calculates the TDC output. Unlike 1-D GVTDC whose output can be determined once knowing the number of phases generated by GRO, the output of 2-D GVTDC is dependent on both of the GRO_X and GRO_Y phases. Assume that the number of phases generated by GRO_X is m, and the number of phases by GRO_Y is n, the 2-D GVTDC output can be described as

$$TDC\_out = m \cdot k - n \cdot (k - 1) \tag{3.13}$$

where k is the normalized delay of the GRO_X, in this case, $k = 31$. The calculation of the 2-D GVTDC output is processed by a readout block which is implemented in digital flow.

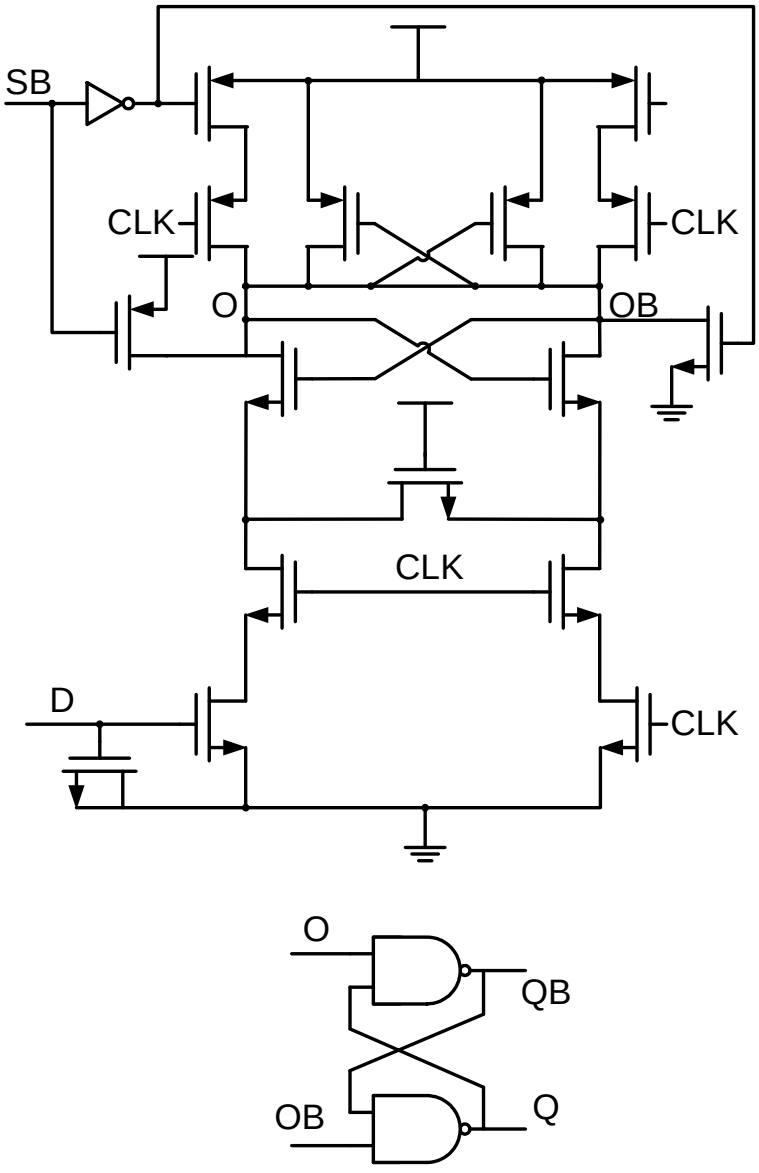

Figure 3.19: Circuit of the sense-amplifier-based flip-flop.

Chapter 4

Digitally Controlled Oscillator

4.1 Introduction to Digitally Controlled Oscillator

The *digitally controlled oscillator* (DCO) that performs the *digital-to-frequency conversion* (DFC) is also an essential component of the ADPLL besides the TDC. It is a cell with only digital inputs and outputs operating in the discrete-time domain, even though the underlying functionality is mainly continuous time and continuous amplitude in nature [3]. The avoidance of analog tuning controls in DCO design allows its loop control circuitry to be implemented in a fully digital manner, which corresponds to the implementation of ADPLL.

The DCO outputs a periodic waveform according to its input *oscillator tuning word* (OTW), which can be described as $f_{out} = \mathbf{f}(OTW)$. Due to the uncertainty and the PVT variation, the mapping of OTW to the output frequency of oscillator is a nonlinear function. The instantaneous value of the frequency also depends on supply power and substrate noise, additionally, truly random phenomena such as thermal and flicker noise [3].

There are several DCO architectures that can be used in the ADPLL. LC tank-based oscillators are the most widely used oscillator in wireless applications due to its low phase noise. Since the quantization noise introduced by the frequency discretization in the DCO can affect the performance in terms of out-of-band phase noise, a relatively high frequency resolution is demanded to keep the additional quantization noise much lower than the intrinsic oscillator phase-noise [18]. Typically, the frequency of the DCO is tuned with varactors which are variable capacitance controlled by OTW. Two or more capacitor banks for coarse and fine tuning are used for digital tuning. The tuning range and frequency resolution are also dependent on the design of varactors [19]. Both of the parasitics and losses of the varactors have a significant effects on the performance of the DCO, especially at high frequency operations.

4.2 Operation Principle of Digitally Controlled LC Tank-Based Oscillator

To realize digital control on an analog LC oscillator, according to [3] introduced by Staszewski at al., a method of weighted switchable capacitance devices as varactors

can be used. As shown in Figure 4.1, an LC tank-based oscillator is constructed with an array of varactors, a fixed inductor and negative resistance circuit. All the varavtors can be switched into a high or low capacitance mode individually by a two-level digital control voltage bus, thus giving very coarse step control for the more significant bits, and less coarse step control for the less significant bits (LSB).

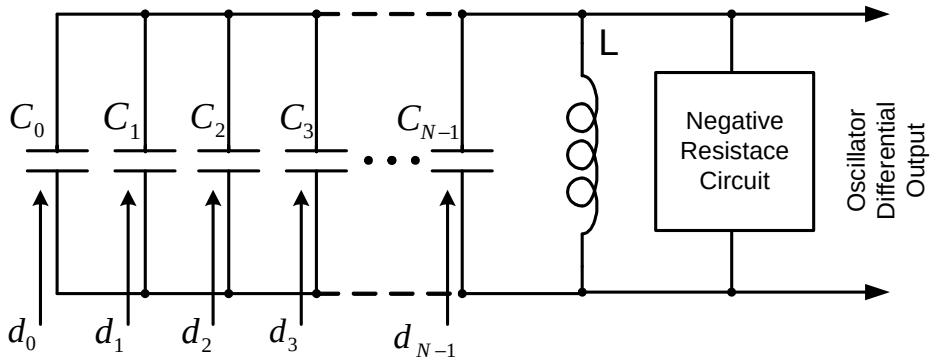

Figure 4.1: System level LC tank-based oscillator.

In the digitally controlled oscillator, each capacitive mode (set by OTW) corresponds to a capacitive value. The total capacitance of the varactor bank in any state of the tuning word combined with the fixed value of inductor determine the output frequency of the DCO according to

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{4.1}$$

The frequency f_{osc} can also be changed by tuning the inductance L. However, in a monolithic implementation it is more practical to keep the inductor fixed while changing the capacitance of a voltage-controlled device such as a varactor [3]. According to Figure 4.1, the total capacitance is the sum of N digitally controlled varactors capacitance. Regardless of what kind of pattern (i.e. binary-weighted pattern) the varactors follow, (4.1) becomes

$$f_{osc} = \frac{1}{2\pi\sqrt{L\sum_{k=0}^{i=N-1} C_k}} \tag{4.2}$$

To introduce digital control bits to (4.2), assume that the individual capacitor of index k is $C_{1,k}$ when it is set to high-capacitive state and that is $C_{0,k}$ when set to low-capacitive state. Thus, the effective switchable capacitance by a signal bit can be derived as the capacitance difference between the two state, $C_{eff,k} = C_{1,k} - C_{0,k}$. As the digital control bit d_k becoming high, the oscillator frequency increases, which must result from lower capacitance. Therefore, the capacitance value should be opposite to the control bit such that the relationship between them can be expressed as

$$C_k = C_{0,k} + \overline{d_k} C_{eff,k} \tag{4.3}$$

Substitutes (4.3) into (4.2), the relationship between the oscillator frequency and the digital control bits can be give by

$$f_{osc} = \frac{1}{2\pi\sqrt{L\sum_{k=0}^{i=N-1}(C_{0,k} + \overline{d_k}C_{eff,k})}} \tag{4.4}$$

4.3 Frequency Planning

As introduced in the previous section, (4.4) describes a DFC (the digital bits d_k directly controls the oscillator output frequency f_{osc}). In the RF band of multi-GHz, it becomes impractical for a straightforward linear DFC, since a large number of control bits (more than 20 bits) are required to achieve a fine frequency resolution of 1kHz. However, according to [20], better than 10-bit resolution would normally require digital error correction techniques. Thus, it is impossible, even with the most advanced component-matching techniques, to achieve the expected precision. To solve this problem, the narrow-band nature of the wireless communication transmission can be exploited. Usually the nominal frequency deviation of the data modulation scheme is around multi-hundred kHz, 9-bit control word should be sufficient for a 1-kHz frequency resolution.

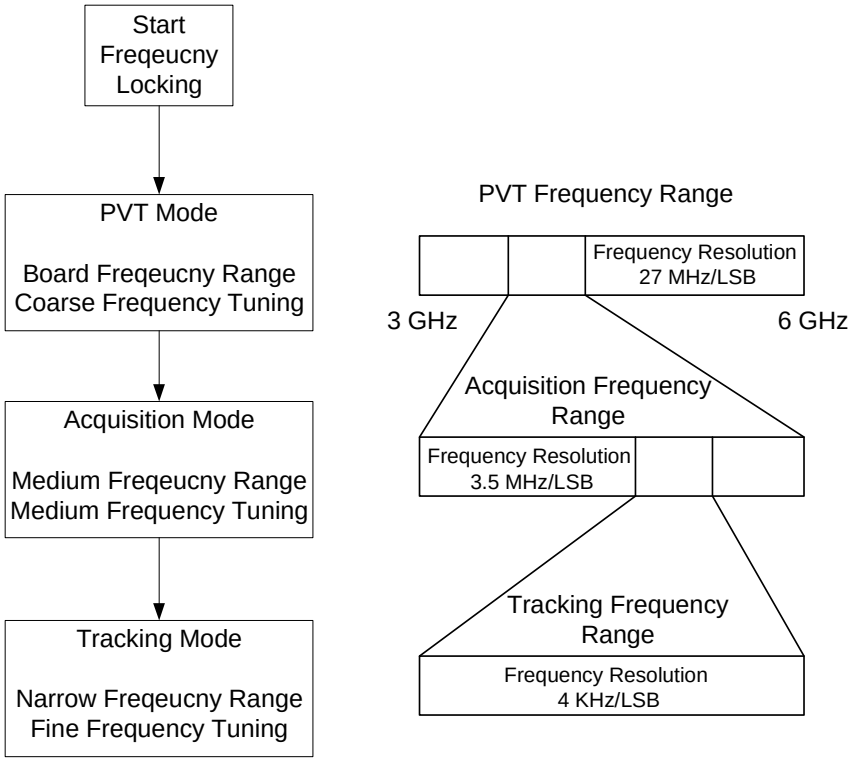

Figure 4.2: DCO operation modes.

However, the overall dynamic range is limited to a very small range. Large dynamic range can be realized by changing the frequency resolution coarser whenever a higher dynamic range is expected [3]. This is accomplished by traversing through different operation modes with low frequency range and high frequency resolution. In the first step, the output frequency of DCO is tuned by *process–voltage–temperature* (PVT) bank with large frequency step and low resolution. In PVT operation mode, the whole frequency range of the DCO (according to frequency planning) is covered and the PVT variations is compensated. After the PVT calibration, the DCO is tuned by acquisition bank with medium-size frequency step and medium resolution. At last, during the tracking mode, the LC tank is be used to track the desired frequency. In Figure 4.2, the operation modes used for the frequency tuning in the proposed DCO is illustrated.

The presented DCO is able to produce an output frequency varying from 3 GHz to 6 GHz with one LSB of 4 KHz. In the proposed DCO, there are three different tuning banks used for each major operation mode. Two 6-bit banks located in the LC tank are responsible for coarse and medium tuning with frequency resolution of 27MHz/LSB and 3.5M/LSB respectively. And a 11-bit fine tuning capacitor band utilizing a different topology provides a frequency resolution of 4kHz/LSB.

4.4 Oscillator Core

Figure 4.3 shows a simplified schematic of the LC tank-based DCO core. The LC oscillator is basically a combination of an LC resonator and an active network. In the LC resonator, three banks of switchable capacitors are used to realized digital frequency tuning. Two different types of capacitor bank are used for coarse tuning and fine tuning, which will be introduced in next section. And the gain block in the DCO is represented as a transconductance of the transistors [7]. In the LC tank, the switches M_1/M_2 short each oscillator output to ground for half of the oscillation period, during which the respective inductor and capacitor are decoupled from each other, as illutrated in Figure 4.4 [21].

According to [21], by increaseing the size of the cross-coupled MOS switches, this topology of DCO can achieve low phase noise, low supply voltage and high efficiency. This DCO can provide a very large oscillation amplitude up to three times that of the supply voltage, meanwhile, improve the power efficiency to 90%, since the product of drain voltage and channel current in the MOS switches is very close to zero across the whole oscillation period, with the result that all power dissipation occurs in the LC tank of the VCO. And the relatively high oscillation amplitude benefits the phase noise and makes it suitable for very low-voltage applications.

4.5 Frequency Tuning Banks

As mentioned earlier, there are three switchable capacitor banks in the LC tank, which are coarse tuning bank, medium tuning bank and fine tuning bank. The coarse and medium tuning provide a wide output frequency range, while the fine tuning ensures the high frequency resolution. In the DCO, the coarse and medium

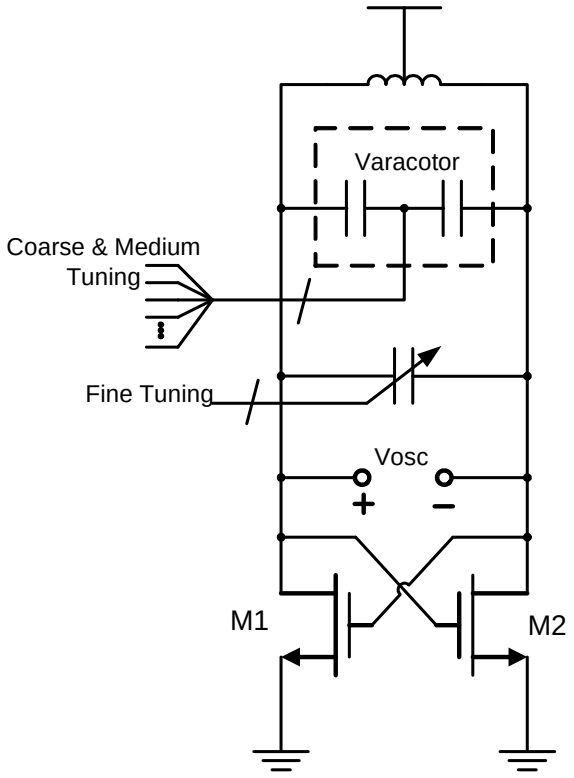

Figure 4.3: Simplified schematic view of the LC tank-based DCO.

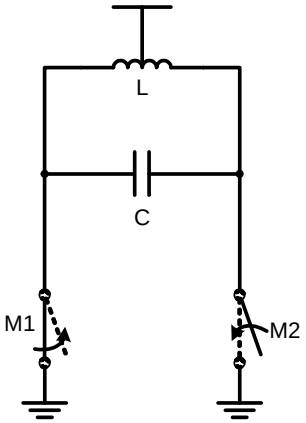

Figure 4.4: DCO operating at the transition point after half of the period.

tuning banks share the same topology but with different capacitance value, on the other hand, the fine tuning bank is implemented with a different circuitry.

4.5.1 Coarse And Medium Tuning Banks

Since the main purposed of the coarse and medium tuning banks is to cover the desired frequency range with coarse steps, varactors with high effective capacitance ($C_{eff,k}$) are suitable for the banks. A simplified varactor is depicted in Figure 4.5. It consists of a NMOS transistor acting as a switch and two capacitors. When the

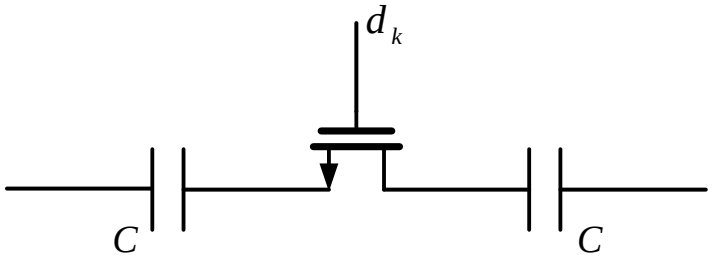

Figure 4.5: Simplified Coarse tuning bank varactor.

control bit applied to the gate of the transistor is high, the total capacitance of the varactor working in ON mode is the series connection of the capacitors. When the control bit is low (OFF mode), the total capacitance becomes the parasitics of the components.

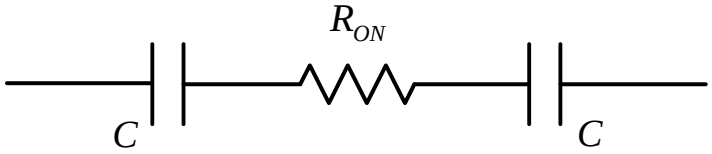

Figure 4.6: The varactor working in ON mode.

However, when the varactor working in the ON mode, there is an on-resistance of the transistor in series with two capacitors, as depicted in 4.6. This resistance could affect the varactor loss. This effect can be examined by the quality factor [22]

$$Q_{on} = \frac{1}{R_{on} C_{on} \omega} \tag{4.5}$$

where C_{on} is the total capacitance of two capacitor in series and ω is the angular frequency. As the DCO working in high frequency, coarse bank varactos loss becomes a considerable part of the total bank loss. To minimize the on-resistance of the NMOS transistor, the width of the transistor can be increased. However, the increasing of the width introduce extra parasitic capacitance to the varactor when it woring in OFF mode, which would decrease the effective capacitance of the varactor, affecting the tuning range of the DCO. The other solution is to increase the gate-source voltage of the transistor, which can be accomplished by adding two pull-down NMOS transistors to the varactor, as shown in Figure 4.7. This

topology pulls down the switch terminal voltage to GND and provides enough overdrive voltage at the same time [22].

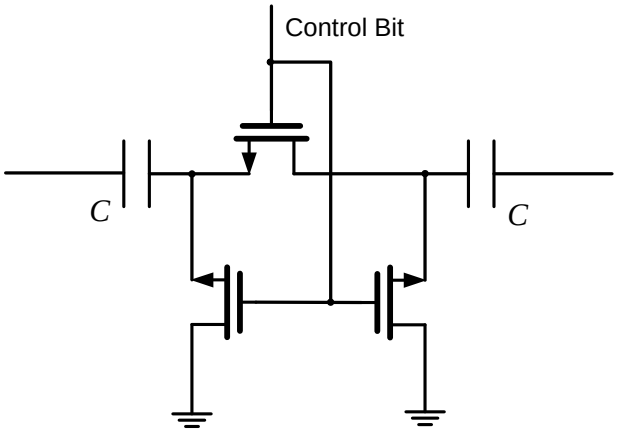

Figure 4.7: Modified varactor with pull-down transistors.

4.5.2 Fine Tuning Bank

The fine tuning bank is realized based on the architecture presented in [18]. There are 11 bits used for fine tuning. The 7 MSBs of them are used to control a matrix of varactors. The rest 4 bits are fed into a digital-to-analog converter (DAC). In the matrix, all elements except one are connected either to the voltage supply or to ground, thus generating a thermometric filling of the matrix (gray and white units). The remaining varactor is connected to the output of the 4-bit DAC that provides an additional 16 voltage levels between Vdd and ground. Since only one varactor is biased at the point of this characteristic with a high voltage-to-frequency gain, the sensitivity of the oscillator to noise and spurious signals is minimized [18].

Chapter 5

All-Digital Phase-Locked Loop

Previously, the two most essential components of the ADPLL, TDC and DCO, are introduced in details. This Chapter first covers the design of the digital loop filter which is used in the ADPLL to convert the TDC outputs into DCO control bits. Then, the design and implementation of the entire ADPLL system is revealed.

5.1 Digital Loop Filter

The digitized realization of the phase-lock loop, which replacing a conventional PFD with a TDC, as well as a VCO with a DCO, allows the utilization of a fully digital loop filter. Different from the conventional loop filter used in charge-pump based PLL, the digital loop filter provide a higher flexibility that the bandwidth can be changed very easily. The digital loop filter consists of a *finite impulse response* (FIR) filter, *infinite impulse response* (IIR) filters as well as an accumulator. The FIR and IIR filters are usually cascaded with the proportional loop gain α, while the accumulator is connected in parallel. IIR filters are generally more beneficial than FIR filters due to its compact structure and stronger filtering capability. However, complex IIR filters are vulnerable to unstableness. In the proposed digital loop filter, this problem is solved by using a cascade of signal-pole IIR filters, which are unconditionally stable [3].

Figure 5.1 shows the digital loop filter implemented for the proposed ADPLL. This loop filter contains five single-pole IIR stages and an accumulator $z^{-1}/(1-z^{-1})$. An external select signal (called *swt_ord* in Figure 5.1) is used to control the output order of the IIR filters, i.e. when the select signal is high the resulting loop-filter order is fifth, and when it is low the order is third. The default order is set to fifth. For a single-pole IIR, the frequency characteristic and the pole location are controlled by the attenuation factor λ, which is realized as a right-bit-shift operator. Its z-domain transfer function is expressed as

$$H_{iir1}(z) = \frac{\lambda z}{z-(1-\lambda)} \tag{5.1}$$

and its s-domain representation is

$$H_{iir1}(s) = \frac{1+s/f_R}{1+s/\lambda f_R} \tag{5.2}$$

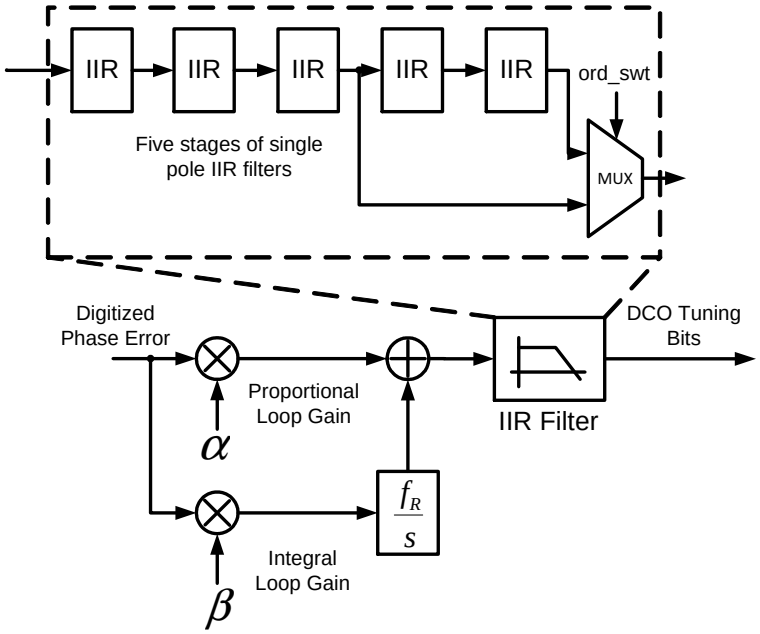

Figure 5.1: Digital loop filter.

According to Figure 5.1, combined with (5.2), the transfer function of the proposed digital loop-filter can be expressed as

$$H_{lf}(s) = (\alpha + \frac{\beta f_R}{s})(\frac{1 + s/f_R}{1 + s/\lambda f_R})^5 \tag{5.3}$$

where α is the proportional loop gain and β is integral loop gain. These two factors are set as $\frac{1}{2}$ to the power of n, where n is an integer. In this loop filter, the α value can be set to 2^{-3}, 2^{-2}, 2^{-1}, 2^0 and 2^1, while the integral loop gain β can be set to 2^{-11}, 2^{-10}, 2^{-9}, 2^{-8} and 2^{-7}. On the other hand, the attenuation factor λ of the single-pole IIR filter is available for 2^{-2} and 2^{-1}. The frequency response for the digital loop filter with different proportional loop gain and integral loop gain values is plotted in Figure 5.2.

In the digital loop filter, it is necessary to choose some proper values for proportional loop gain α and integral loop gain β to fulfill the requirements of stability, transient behavior (lock time, overshoot), and steady state behavior (noise suppression). However, some of these requirements are contradicting. There is a trade-off between lock time and noise suppression, which limits the performance of the ADPLL in one or the other direction. On one hand, a short lock time and a good DCO noise suppression require a large bandwidth. On the other hand, good TDC noise suppression requires a narrow bandwidth. Generally, the bandwidth is defined by the TDC quantization since it is the most critical imperfection in the system. However, to enhance the noise suppression capability of the ADPLL, the additional IIR filtering is used in the proposed digital loop filter for further noise

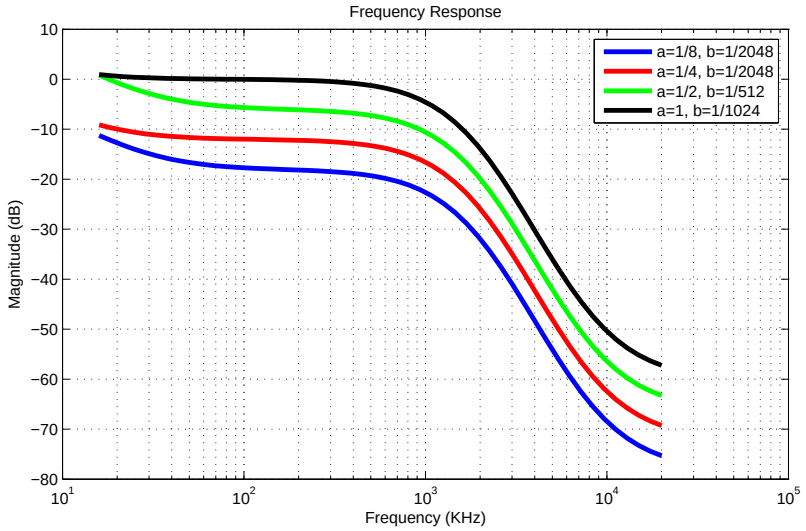

Figure 5.2: Magnitude response v.s. frequency for various α and β values.

attenuation. The additional IIR filtering can provide both better low-pass DCO noise suppression and better high-pass TDC noise suppression [23].

5.2 Implementation of ADPLL

As depicted in Figure 5.3, the implemented ADPLL consists of a TDC converting the phase error into digital form, a DCO with three different tuning banks, a digital loop-filter which converts the digitized phase error into oscillator frequency tuning bits, a tuning bank controller that provides automatic frequency tuning, a Sigma-Delta (SD) modulator generating a time-averaged frequency division ratio, a retiming block and a programmable divider. Since the whole system contains both of analog and pure digital circuits, two different design flows for them are used. Among these components, except the TDC and DCO which are realized in analog design flow, the other components are all implemented in digital flow.

Since the three tuning banks with different resolution in the DCO need to be adjusted one by one during the phase locking process, a *tuning bank controller* is utilized to realize automatically tuning of the DCO. At the beginning of the frequency acquisition, the controller tunes the coarse bank while keeps the other two banks at default values. After a certain period of time, when the coarse tuning word becomes stable or just varying between two values, and keeps for enough time, the controller outputs this coarse tuning word, then switches to medium tuning and repeats this process until phase locking. This tuning bank controller is implemented along with the digital loop filter.

In a ADPLL, it is expected to have the different components of the ADPLL work in a clock-synchronous manner. Thus, the frequency *retiming* is required to

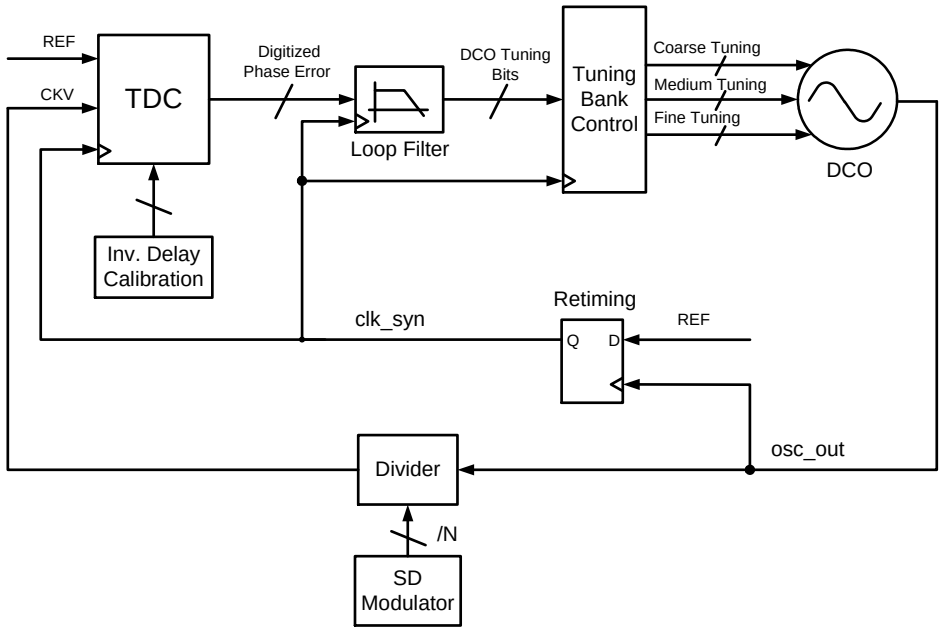

Figure 5.3: Top level schematic of the proposed ADPLL.

generate a synchronous clock for all blocks. This is accomplished by a flip-flop where the reference clock with lower frequency, *REF*, is retimed by a much higher frequency signal, *osc_out*.

Chapter 6
Results

In this project, an ADPLL operating at 1 V supply voltage is implemented in 65 nm CMOS process. The ADPLL consists of both digital blocks and analog circuits. All the digital blocks, i.e. the inverter delay calibration, the TDC readout, the digital loop filter, the tuning bank controller and the SD modulator, are implemented using synthesizable VHDL code. Meanwhile, to test and simulate these digital blocks, a model of the entire ADPLL system is also built in VHDL. By simulating this model, the system-level performance of the ADPLL can be learned. However, it is still necessary to simulate the digital blocks with other analog circuits. In this project, the AMS simulator in Cadence was used to perform mixed-signal simulation and verification.

6.1 TDC Simulation Results

As a most crucial component of the ADPLL, the TDC has been verified and simulate on behavioral level. In the first simulation, a DC input was fed into the TDC. This DC input was realized by adding a constant delay (652 ps) to the *CKV* signal with respect to the reference signal *REF*, so that the output of the TDC corresponds to the constant delay. The reference frequency is 50 MHz in this design. The simulation result of the DC input is plotted in Figure 6.1. It can be noticed that the output value is varying between 130 and 131, due to the first order noise shaping of the gated ring oscillator based TDC.

In the second simulation, a sinusoidal input was applied by varying the delay between *REF* and *CKV* sinusoidally. The Fast Fourier Transform (FFT) result of the output of the TDC is illustrated in Figure 6.2. From the spectrum it can be seen that the first order noise shaping of the TDC leads to a roughly 20 dB/decade slope in the higher frequency.

6.2 ADPLL Simulation Results

In the register-transfer level (RTL) simulation of ADPLL, a reference signal with a frequency of 50 MHz was used , and a division ratio is chosen to be 60 for the divider in the feedback path. Figure 6.3 illustrates the frequency control word during phase locking process. First, the output frequency of the DCO is tuned by

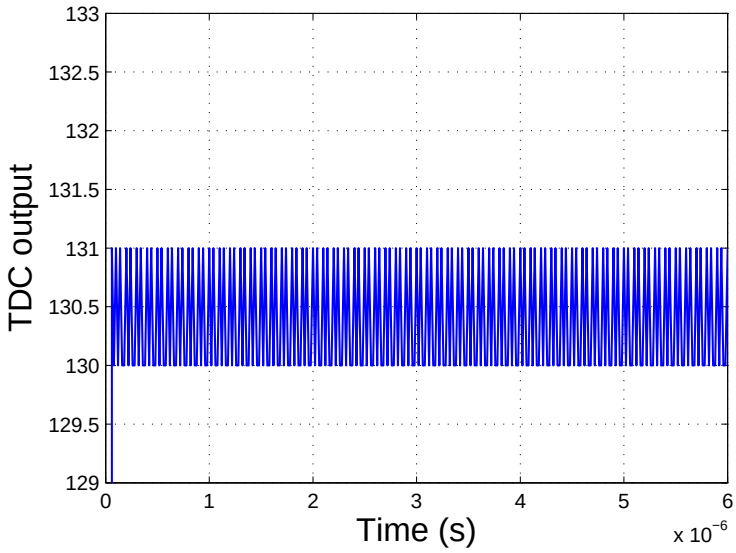

Figure 6.1: Simulated TDC output with DC input of 652 ps.

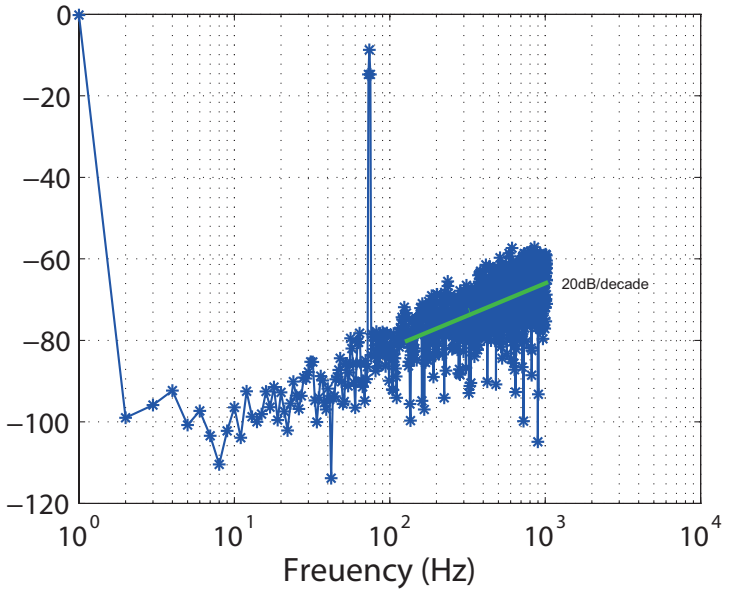

Figure 6.2: FFT result of the TDC output with a sinusoidal input.

the coarse tuning word while the other tuning bits keep the default values. After the coarse tuning word being stable, the medium tuning word start changing to meet the desired frequency. As a results, when the phase is locked, only the last

two bits of the fine tuning word is changing, generating the time averaged value of the frequency control word.

The VCO generated frequency is plotted in Figure 6.4. With an input frequency of 50 MHz and division ratio of 60, an output frequency of 3 GHz is obtained in the simulation. The settling time in this case is about 180 μs.

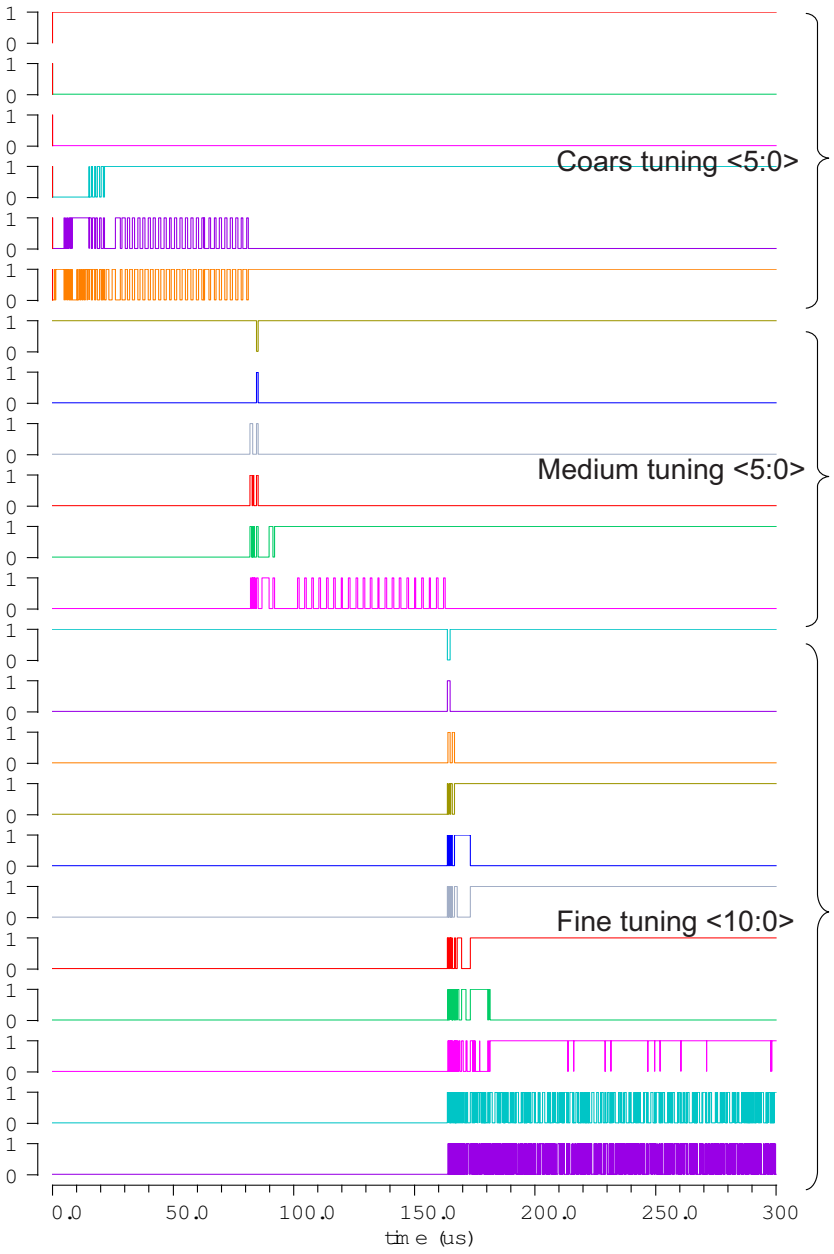

Figure 6.3: The frequency tuning word v.s. time.

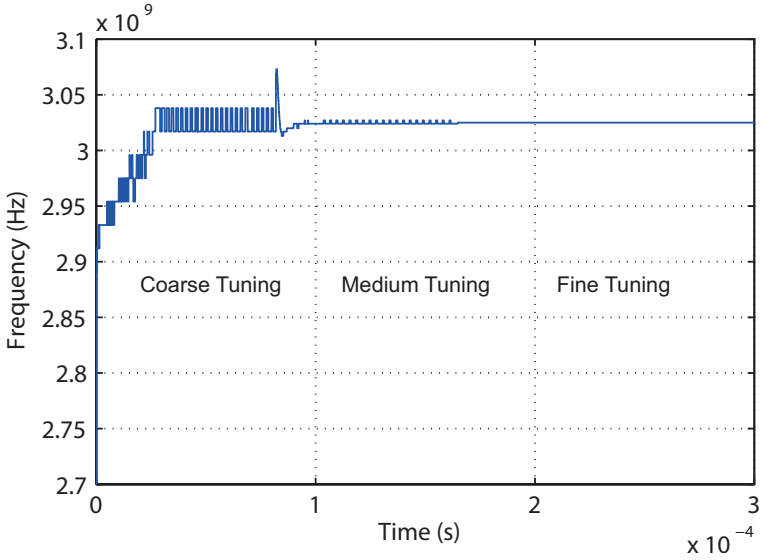

Figure 6.4: The output frequency of the VCO v.s. time.

6.3 Future Work

Since the entire ADPLL system is very large and complex, only few simulation on the entire circuit were completed in limited time. And the result of the entire circuit simulation only provide very few information. It would be worth spending more time on the circuits simulation and collecting more simulation points with different parameters and noise, although the RTL simulation results are satisfactory.

It would also be interesting to explore the possibility of further increasing the bandwidth of the ADPLL for an even faster settling time, meanwhile the suppression on the noise generated by the TDC and DCO should also be taken into consideration.

6.4 Conclusion

In the proposed ADPLL, A 2-D gated ring oscillator based Vernier TDC is employed for providing digitized phase error. The 2-D architecture improves the detection range and latency of the TDC. The raw resolution of the implemented TDC is 5 ps and the detection range is up to 10 ns. On the other hand, An LC tank based DCO is used to generate the target frequency. Three different tuning banks in the DCO realize fast tuning of the output frequency and provide a tuning resolution of 4 KHz. At last, the ADPLL for the RF application has been implemented based on a divider-assisted architecture using 65 nm CMOS. With an input reference frequency of 50 MHz, the ADPLL is able to generate a frequency from 3 GHz to 6 GHz by tuning the division ratio of the divider.

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