Master's Thesis

Design of a SiGe Power Amplifier for the 81–86 GHz E-Band

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Abstract

This thesis presents the design of a two-stage differential cascode Power Amplifier for 81-86 GHz E-Band applications. Two stacked 1-to-1 transformers are used for power combining and single-ended to differential conversion. According to EM simulations, input and output transformers show an insertion loss of -0.63 dB and -0.45 dB respectively. The PA was realized in SiGe technology using Infineon B7HF200 0.18 μm SiGe HBT process with f_T / f_{max} 200/250 GHz. An inter-stage matching network consisting of a LC-match was used in the interface between input and output stage. Although the design has been taped-out, the results presented are based on post-layout simulations as the chip has not arrived on time for publication. The PA delivers 18 dBm saturated output power and exhibits a gain of 15.7 dB at 83.5 GHz when operated from a 3.5 V DC supply, reaching 10.1% peak PAE. The complete design occupies an area of 0.026 mm^2 excluding the pads.

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Chapter 1
Introduction

This chapter presents an overview of the work that was carried out during the making of this thesis. It starts with a short review of the state of the art in RF IC design, specifically targeting power amplifier and power combiner design techniques used in integrated circuits operating at millimeter wave frequencies. It follows with an analysis of the motivation that guided the need to explore new topologies and architectures toward the goal of achieving maximum efficiency. It finishes with a short description of the contents of this report.

1.1 Background

The quick pace set by the advances in integrated circuit design towards new technology nodes, characterized by smaller feature size and low power, has lead to an explosion in the number of mobile devices that have been widely adopted by the masses. An increasing demand for new wireless connectivity technologies has emerged to satisfy the need of mobile communications. As a consequence, new techniques are being developed to build a new set of devices operating at millimeter wave frequencies, see [1] and [2].

New standards for wireless multi-gigabit data rates have started to reach their final definition stage making previously unlicensed frequencies in the E-Band available for research and commercial applications. This is a trend that sets new challenges for RF IC designers as we will describe shortly. Standards like IEEE 802.11ad [3] and IEEE 802.15.3c [4] cover a wide range of applications, these are some of them:

Uncompressed high definition video streaming: Offering film downloads in kiosks, planes or home appliances using short range wireless links [5].

Automotive radar: Integrated in cars for positioning, collision avoidance and autonomous driving systems [6].

Imaging: As the resolution of an image is inversely proportional to the wave length, the use of millimeter wave frequencies is the perfect match for medical, industrial and scientific imaging applications [7].

The need for transmitting more data in a more efficient way has lead to the adoption of more spectral efficient modulation schemes as a way of embedding more data per channel. Examples like Quadrature Amplitude Modulation (QAM) used in LTE, or Orthogonal Frequency-Division Multiplexing (OFDM) to avoid multipath fading in IEEE 802.11a,g,n WLAN standard [8] represent this trend. As some of these modulation schemes use multiple carriers, the signals have a higher Peak-to-Average ratio (PAR) which translates to more strict requirements in terms of linearity. Then, the designer is left with no choice to design a power amplifier but to select either class A or class AB operation since they offer a balance between efficiency and linearity performance.

There are other techniques where non-linear power amplifiers are used to transmit amplitude information in the signals. These techniques are cartesian feedback [9], outphasing [10] and polar modulation [11]. However, their use is not that common in millimeter wave designs compared to linear power amplifiers and they are not considered in this thesis.

In general, the design of radio transceivers targets the goal of being compact and low power and, as a direct consequence, achieving better efficiency. These goals are not easy to fulfil all at once and some compromises have to be done, specially regarding the most power hungry blocks in a radio transceiver, like power amplifiers, for which low power and high efficiency are in clear antagonism.

Often, it is such the optimization required that power amplifiers are implemented in a more mature technology different than silicon like silicon germanium (SiGe), gallium arsenide (GaAs) or indium phosphide (InP) [12]. They offer advantages in the form of higher gain, higher transition frequency or higher breakdown voltages. Obviously, this implies having a separate package when used in conjunction with other CMOS blocks in a transmitter. Sometimes, this requires the presence of external components like inductors, capacitors, filters, etc., which in sum, demands more engineering effort.

1.2 Motivation

There exist several limitations that comes with the design of power amplifiers for millimeter wave applications, all of which represent a bigger challenge as technology nodes keep decreasing the minimum feature size, especially in CMOS technology. As transistors get smaller, and faster, the length of the interconnects is slightly reduced. In part, this is beneficial as the transition frequency f_T gets higher. But not until recently, f_T became sufficiently large in CMOS technology as to be considered for the design of mm-Wave circuits.

This limitation, together with the reduction in supply voltage, makes it difficult to deliver high output power without using transmission lines or inductors as loads, as well as impedance transformation networks. The choice of SiGe bipolar technology, offering a higher f_T and higher breakdown voltages, seems more

appropriate to tackle the problem.

What is more, the Q-factor of passive devices does not scale up in the same manner as transistor size scales down. As dielectrics between layers become thinner, the top metal layer is closer to the substrate, increasing the parasitic capacitance in transformers and inductors. Specially important is to use a low conductivity blocking layer underneath these structures as a way of preventing eddy currents in the substrate induced by changing magnetic fields [8].

The last important point comes from the fact that device models are not characterized for high power and high frequency designs, where small parasitics in the interconnects between transistors could lead to a non working design. Careful layout techniques have to be developed to account for these effects and the design should be driven by post-layout and EM simulations rather that relying on schematic level simulations alone [13].

This work addresses the need of exploring new topologies resulting in compact and efficient PAs with the design of a 2-stage power amplifier using on-chip transformers as power combiners and a interstage LC-matching network.

1.3 Organization

The analysis and design of a power amplifier for the E-Band is discussed in this thesis throughout five chapters, which contents are briefly summarized as follows.

Chapter 2 includes a short review of the state of the art techniques used nowadays for the design of power amplifiers for millimeter wave communication applications. It is intended as an introductory walk through several topologies and architectures focusing in class A and class AB linear PAs. The circuits presented are widely used in CMOS and bipolar technologies, the latter being the choice for this work. Biasing circuits using inductors and resistors and their implications in linearity performance are treated as well. The chapter ends with the analysis and design of the active circuits, input and output stage, together with the inter stage matching network.

Chapter 3 discusses the passive components used in power combining techniques at millimeter wave frequencies. Different monolithic on-chip transformers geometries and interconnects are analyzed and modelled using S-Parameters extracted from EM simulations. The transformers are characterized by their inductance and Q-factor values in the primary and secondary as well as their main performance figure, insertion loss.

Chapter 4 covers the simulation results of the final transformer structures selected for input and output stage and the layout techniques used to reduce the parasitic inductance and capacitance in the interconnects.

Chapter 5 presents the results obtained in post-layout simulations. Linearity, efficiency and power consumption metrics are discussed and compared to those of the state of the art PAs.

Chapter 6 addresses the conclusions of this work, summarizing the achievements and weaknesses of the architecture studied in this thesis. A series of suggestions are given to try to overcome the problems faced during the course of this work. Finally, several recommendations are enumerated for further improvement as well as research opportunities in the modelling of on-chip transformers that can benefit the design of PAs at mm-Wave frequencies in the future.

Chapter 2

Power Amplifiers for mm-Wave Applications

This chapter discusses the analysis and design of the active part of the power amplifier architecture presented in this work. Starting with the main characteristics and performance metrics, followed by a short review of amplifier classes of operation and state of the art architectures for mm-Wave PAs. Cascode devices and differential stages are studied later with emphasis in transistor sizing and reverse isolation to serve as an introduction to the discussion of the architecture developed in this thesis. Finally, a set of biasing circuits using active and passive components is treated with regard to its performance implications.

2.1 Performance constraints

The first trade-off faced in the design of a power amplifier comes with the relationship that exists between output power delivered to the load and voltage swing. The need for high power handling capabilities while achieving some gain do not concur.

For example, consider the common emitter amplifier in Figure 2.1a, in order to drive the load R_L, the supply voltage and v_{o-pp} have to be within the limits of the device voltage breakdown for the transistor $Q1$ to work reliably. On the other hand, using an inductor as a load, Figure 2.1b, we feed DC power to the collector, and assuming that the inductance is large enough, the current through it could be considered to be constant. Then, the voltage at the collector of $Q2$ can swing above VDD, lowering the supply voltage requirements. However, the transistor still has to handle large voltage swings going as high as two times VDD, subjecting the transistor to serious stress conditions for operation.

These stress levels can be relaxed by down-converting the output impedance R_o seen by the transistor to a much lower value allowing small voltage swings while delivering the same amount of power to the load. One way to do impedance transformation is by using on-chip transformers, and at the same time, getting differential to single-ended conversion. This idea is depicted in Figure 2.2 and covered extensively in Chapter 3.

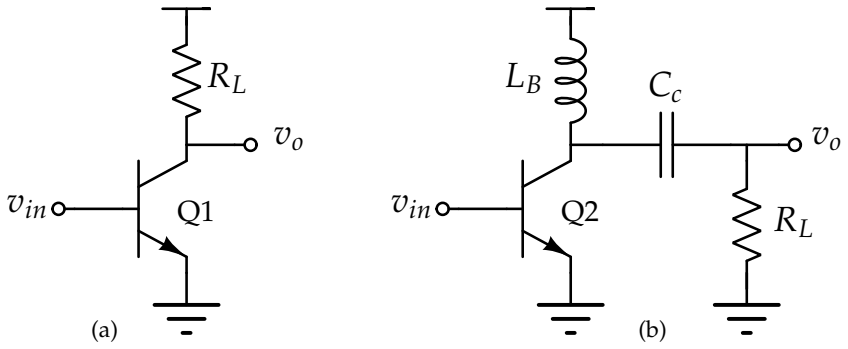

Figure 2.1: Common emitter amplifier using a resistor (a) and a inductor (b) as a load.

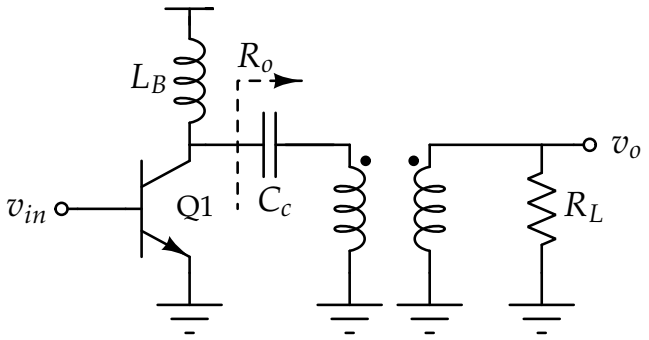

Figure 2.2: Common emitter amplifier with balun used for impedance transformation.

As a result, a reduction in voltage swing has a proportional increase in current delivered to the load. This idea carries other negative implications when using transformers. Since the inductors that constitute the stacked-up transformer structures, Figure 2.3, have a series parasitic resistance R_s, they will dissipate some of the power delivered to the load, causing high losses. While these losses do not present a problem at the input, they can seriously degrade the efficiency at the output, which is of critical importance.

More than parasitic resistance, inductive and capacitive parasitics prove to be of greater importance in millimeter wave circuit design. They can manifest in the form of gain reduction, input-output isolation degradation and feedback from the output to the input, compromising the design. These effects are analyzed below taking the common emitter amplifier of Figure 2.4 as an example.

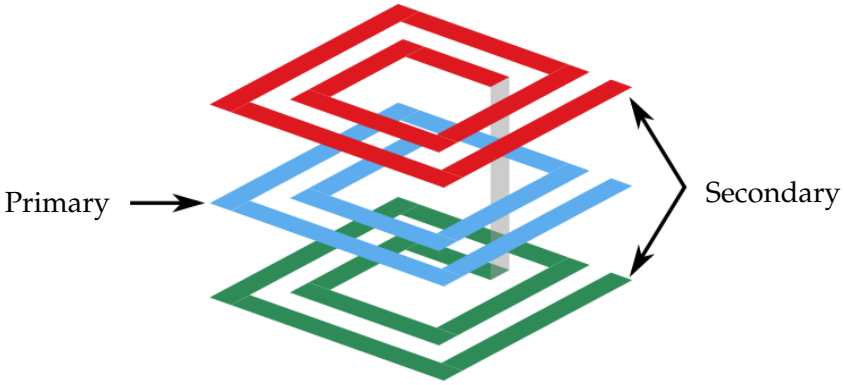

Figure 2.3: 3D structure of a stacked-up 2-to-1 transformer using parallel spirals to realize the primary (blue) and secondary (red and green) windings in different metal layers.

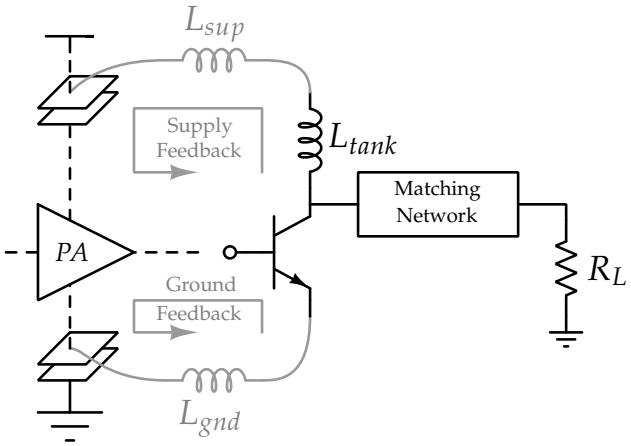

Figure 2.4: Common emitter amplifier with parasitics at the emitter and collector that can degrade the performance of the power amplifier.

Single-ended PAs are quite common mainly for two reasons, the antenna is typically single ended and, single-ended RF circuits are easier to test than their differential equivalent. If we observe the single-ended common emitter PA in Figure 2.4, the parasitic inductance introduced by the bond wire at the collector L_{sup} that connects to the supply voltage can create a feedback path to the preceding stages through the supply rails, apart from de-tuning the resonant tank when $L_{sup} \approx L_{tank}$, or modifying the properties of the matching network at the output if it exists.

In the same manner, the bond wire that connects to ground, inductively degenerates the common emitter amplifier and creates another feedback path through the ground node. As a consequence, the gain is reduced and the input match is affected by increasing the real part of the input impedance proportionally to L_{gnd}.

This problem can be minimized by using a differential amplifier topology which, at the same time, will reduce the "waste" of half of the transmitter voltage gain compared to the single ended approach where only one output of the up-conversion mixer is used, see Figure 2.5a. However, a balun that performs differential to single-ended conversion between the mixer and the PA achieves the same goal, Figure 2.5b. Though the balun introduces its own loss, which will limit the voltage gain improvement to just a few decibels [14]. The best approach is then to use a balun between the PA and the load, using both base-band quadrature signals at the the input of the PA, Figure 2.5c.

2.2 Classes of Operation

There exist more types of operation for power amplifiers than the ones explained here, however, a successful design at millimeter waves frequencies is limited to a subset of these classes of operation in favour of linearity and in detriment of efficiency.

A useful concept to differentiate amplifier classes is the *conduction angle* θ, which is defined as follows:

$$\theta = T_{on} \cdot 360^{\circ} \tag{2.1}$$

where T_{on} is the percentage of the period of the signal during which the transistor remains *"on"*.

The conduction angle is a consequence of the topology chosen and the bias conditions. Class A operation has a conduction angle of 360° which means, the bias levels are chosen so that the transistor operates linearly. In the case of bipolar devices that means avoiding cut-off and saturation regions. Figure 2.6 shows a basic model of a power amplifier.

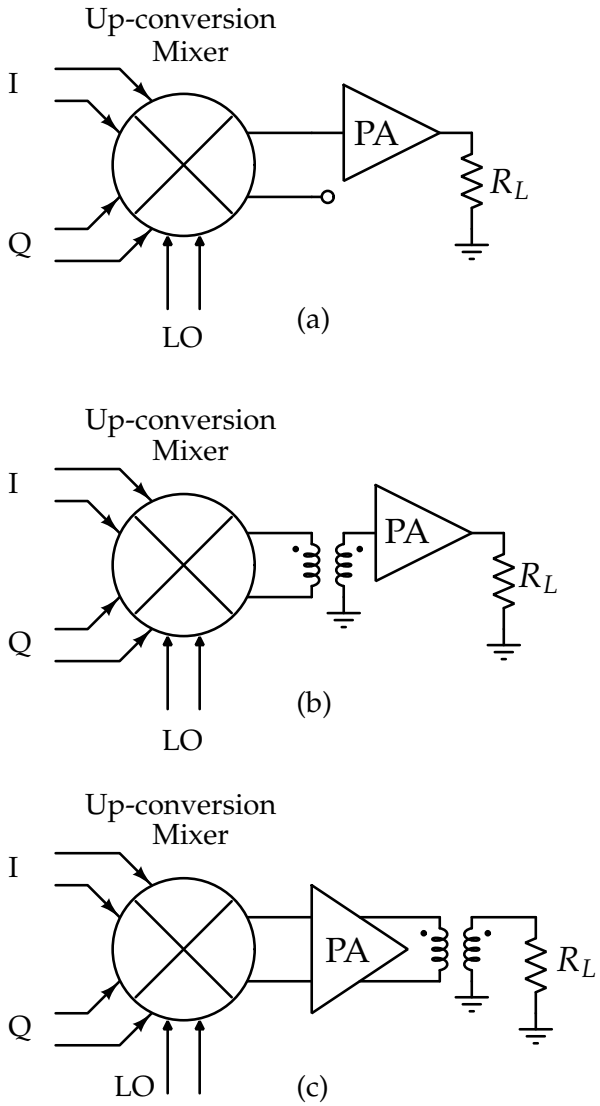

Figure 2.5: Single-ended topology using only one base-band quadrature signal from the up-conversion mixer (a), single-ended using a balun for differential to single-ended conversion between mixer and PA (b), and differential topology using a balun for power combining and differential to single-ended conversion at the output of the PA (c) [14].

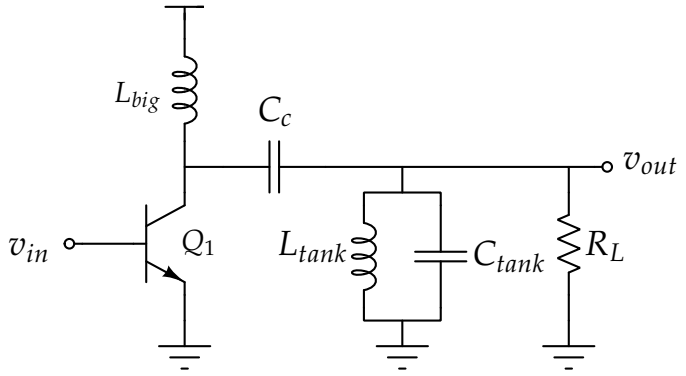

Figure 2.6: Basic model of a power amplifier.

The most important performance parameter in a power amplifier is its efficiency, for which two metrics exists. The *collector efficiency* [15] is defined as

$$\eta = \frac{P_L}{P_{DC}} \tag{2.2}$$

where P_L is the average power delivered to the load and P_{DC} is the average power drawn from the power supply.

Often, power amplifier architectures consist of a driver stage, whose main task is providing gain to drive the output stage into or close to compression, making the output stage to have almost no gain. If a PA has no power gain the calculated collector efficiency can still be high since it only takes into account the RF output power. To account for this effect, there is another metric that considers the power gain as well and it is called Power Added Efficiency (PAE) [15] which is defined as

$$PAE = \frac{P_L - P_{in}}{P_{DC}} \tag{2.3}$$

where P_{in} is the average input power. Note that the power added efficiency will always be less than the collector efficiency.

In case of class A power amplifiers, the drain efficiency has a theoretical maximum of $\eta = 50\%$. This value is far from reality as the interconnects parasitics as well as breakdown voltage of the transistors bring down the efficiency figure to the range of 30-35% at best. A key point to remember is that even if there is no signal power delivered to the load (no signal swing at the collector of $Q1$), the transistor still burns DC power because it is *"on"* all the time.

One way to overcome this limitation is to reduce the conduction angle by using two parallel stages, Figure 2.7, where each of them conducts for only half the signal period ($\theta = 180°$). This behaviour is typical of class B amplifiers.

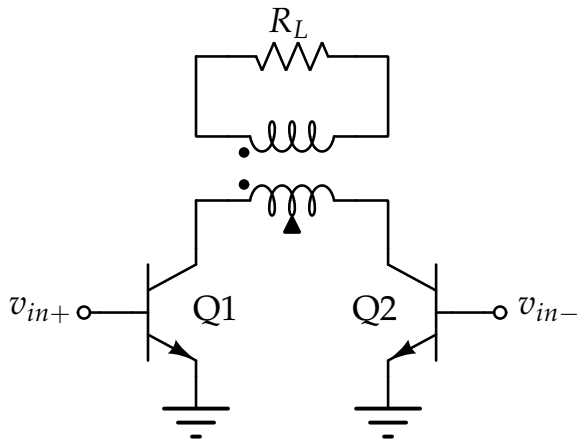

Figure 2.7: Class B power amplifier.

The bias levels here are chosen so that $Q1$ and $Q2$ shut off for half of every cycle. The balun at the output makes the differential to single-ended conversion to drive the load and its primary is used as a center-tapped inductor connected to VDD. As each transistor stays "on" for half a period, they introduce severe non-linearities. Nonetheless, a smaller conduction angle pushes the drain efficiency to $\eta = \pi/4 \approx 78.5\%$ in class B operation [16].

Aside from the fact of being able to get higher efficiency, class B operation is difficult to implement due to the impossibility of making the transistors conduct for exactly 50% of the signal period. There will be a short instant of time where both transistors will remain "on" in the zero crossing of the input signal v_{in}. Finally, just like in class A amplifiers, this topology requires an on-chip transformer that will introduce losses decreasing the efficiency.

This brings us to class AB operation, which offers a compromise between linearity and efficiency. In contrast with class A, where the transistor is "on" for 100% of the time, and class B, transistors conduct 50% of the time, class AB offers a conduction angle $180^\circ < \theta < 360^\circ$, that is, the transistors conduct for more than half the signal period. The linearity performance will be less than that of class A and more linear than class B. This is usually achieved by power back-off which consists of reducing the input voltage swing v_{in-pp} to set the operation region of the PA far from compression.

The power amplifier designed in this thesis operates in class AB regime using a (quasi) differential topology similar to that of Figure 2.7. The bias levels are set accordingly to maximize efficiency. This and other architectures are discussed in the next section.

2.3 Power Amplifier Architectures

The most common architecture of a power amplifier is depicted in Figure 2.8. It consists of a high gain driver stage and a high power output stage with input and output matching networks. The interface between them is a matching network that is often realized using transmission lines and passive components typical on a LC-match.

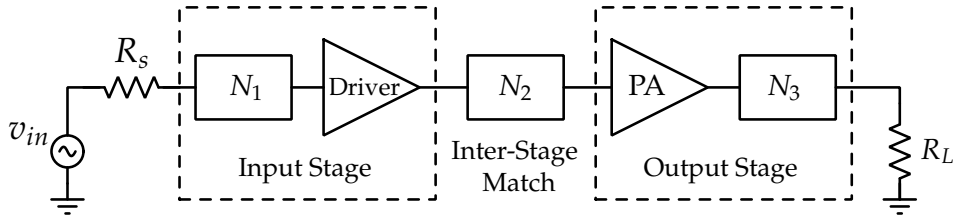

Figure 2.8: Two-stage power amplifier architecture. N_1 and N_3 are input and output matching networks respectively, N_2 is the matching network in the interface between input and output stage.

The use of on-chip transformers as power combiners has become very popular in the design of millimeter wave circuits. The fact that they can provide impedance transformation too, gives the designers the opportunity to use several PAs in parallel using the architecture just described. This has the advantage of presenting a lower load to the PA to drive, which relaxes some of the constraints caused by having a low supply voltage and devices with low breakdown voltage in modern processes.

With slight variations, there are three well differentiated topologies used in state of the art PAs for millimeter wave communication circuits.

2.3.1 Multi-stage PAs

Usually, formed by more than two stages (single-ended or differential), can be arranged with several of them operating in parallel, Figure 2.9. The idea driving this architecture consists of scaling up the size of the transistors in every stage, so the load seen by each PA in the chain increases accordingly. This method relaxes the demand of high voltage swing at the output, splitting the job among several stages. The is a penalty in efficiency as more active devices operating in the linear region are needed.

A different set of techniques are used for power-splitting and power-combining, for example, [17] uses baluns in a 3-stage differential amplifier with cascode devices , [18] uses a Wilkinson power divider/combiner in a 5-stage with two par-

allel PAs, [19] uses transmission line scaling in a stage-scaled PA.

The Wilkinson power divider splits an input signal into two signals with equal phase. Its reciprocal, the power combiner, combines two signals with equal phase into one in the opposite direction. In both cases, quarter-wave length transformers are used to match the split ports to the common port. This power combiner provides high degree of isolation between the output ports and ideally it is 100% efficient [20]. Its use is quite common in mm-Wave circuits as it can be easily realized on-chip using transmission lines.

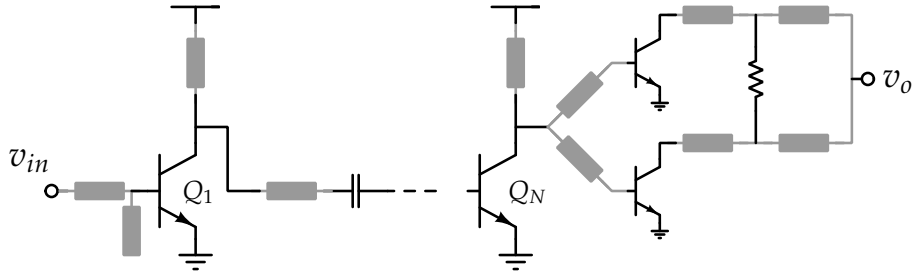

Figure 2.9: N-stage common source power amplifier using transmission lines for impedance matching and a Wilkinson power combiner at the output.

Although, it could be considered a brute-force approach with poor PAE performance compared to other architectures, this topology is quite simple and it could fulfil the requirements for some applications.

2.3.2 Neutralized differential amplifier

This type of PA is built upon a pseudo-differential pair in a common emitter configuration and exploits the idea of neutralization of the collector-base capacitance C_{BC} by using cross-coupling capacitors or varactors between the base and the collector of the input transistors, Figure 2.10. This enables a common emitter amplifier to operate at millimeter wave frequencies yielding high reverse isolation [21]. At the same time, using a single transistor lowers the supply voltage requirements in contrast with a classical cascode topology.

Not only better high reverse isolation but this technique as well, when using on-chip compensation with varactors, is bias and temperature independent within the limits of the junction breakdown voltages [22]. It should be present that overcompensation can lead to potential instability or oscillation so special care should be put into selecting the right value for C_N that guarantees unconditional stability.

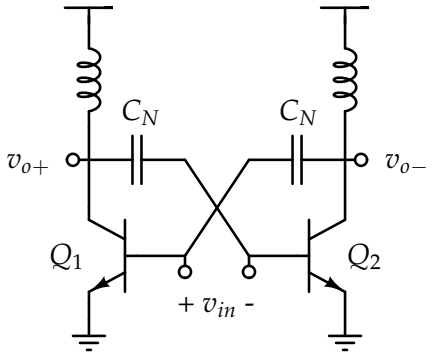

Figure 2.10: Cross coupling neutralization.

Most of the state of the art PAs belong to this category, differing in the power combiners implemented and several layout techniques used to minimize the impact of parasitics, see [23], [24] and [25].

2.3.3 Differential amplifier with cascode devices

An alternative to increase reverse isolation is to use cascode devices instead of cross-coupling capacitors, Figure 2.11. This is a simpler form of mitigating the effect of the Miller capacitance.

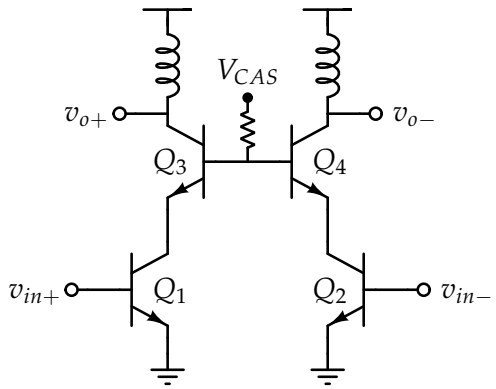

Figure 2.11: Differential amplifier with cascode devices.

Whether this advantage can be exploited or not by the designer usually depends on the available supply voltage in the design process. In this regard, bipolar processes offer higher breakdown voltages as well as higher voltage supply.

Last but not least, using cascode devices offer the possibility of temperature matching the active devices, thing that is not possible using capacitors due to

differences in temperature coefficient between capacitors and transistors. A compact and symmetrical layout helps to prevent temperature variations affecting devices in a different way. A layout where all transistors are placed close to each other minimizes the possibility of uneven temperature variations affecting the performance of the power amplifier core.

2.4 Circuit Design

The power amplifier designed in this work uses a two-stage architecture with 1-to-1 on-chip stacked transformers for differential to single ended conversion, Figure 2.12.

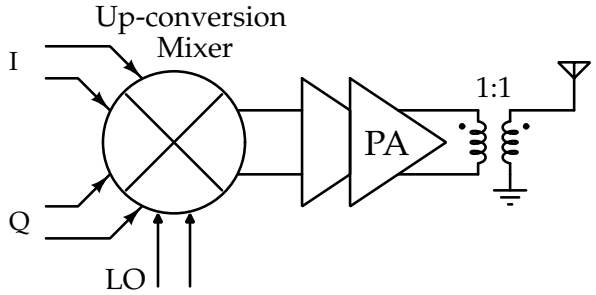

Figure 2.12: Proposed power amplifier architecture.

Rather than cross-coupling neutralization, cascode devices are used in the active part of the power amplifier in both stages, arranged in a differential amplifier topology, that is, a common emitter Q_1-Q_2 followed by a common base Q_3-Q_4. The use of a differential topology with cascode devices proves beneficial to achieve higher gain, to mitigate the Miller effect and to reduce LO pulling. Oscillator pulling happens when part of the output signal of the PA couples to the local oscillator through the substrate or package parasitics. This "injected" signal causes the output phase of the oscillator to be modulated periodically producing a slip in the time domain of the output signal of the PA and an asymmetric spectrum [14]. The complete design is depicted in Figure 2.13.

As it was pointed out at the beginning of this chapter, CMOS technology stands a challenge for circuit designers. Transition frequency f_T and breakdown voltage BV_{CEO} of transistors diverge as new technology nodes appear, thus limiting the signal swing and hence reducing the output power. In contrast, SiGe technology offers an improvement in f_T for which the voltage breakdown constraint is not as serious as in CMOS. This influences the decision of selecting the most appropriate transistors for the job. Two NPN transistors were considered in this design, their most important features are highlighted in Tables 2.1 and 2.2:

Using a cascode topology and a 1-to-1 transformer set the load impedance to 50Ω thus making the need for high supply voltage a necessity to get high output power and high efficiency. The use of a common base stage reduces the stress

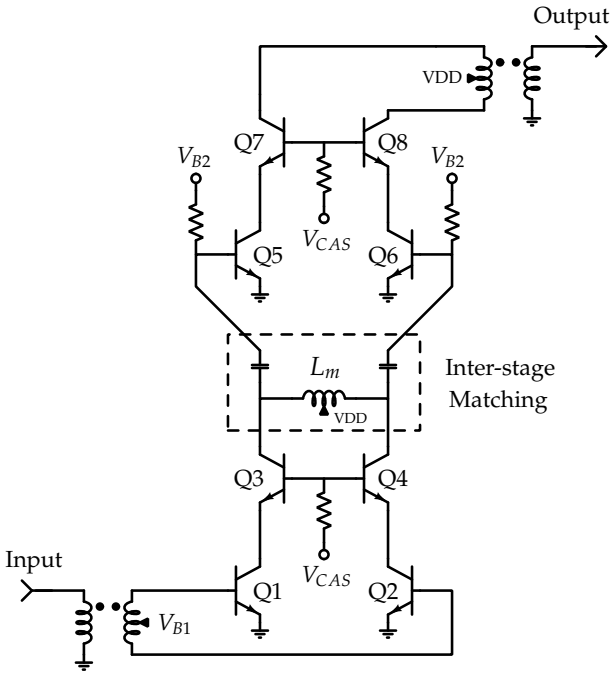

Figure 2.13: Simplified schematic of the proposed PA.

Parameter	Condition	Typical
$A_{E,mask}$		0.35 x 2.80 μm^2
$A_{E,eff}$		0.18 x 2.63 μm^2
BV_{CEO}	I_C = 1 μA	1.7 V
BV_{CES}	I_C = 1 μA; V_{BE} = 0V	6.5 V
Max. $f_T@j_C$	V_{CB} = 1V	170 GHz @ 5 mA/μm^2
Max. f_{max}	V_{CB} = 1V	250 GHz

Table 2.1: High speed NPN transistor characteristics.

Parameter	Condition	Typical
$A_{E,mask}$		0.35 x 2.80 μm^2
$A_{E,eff}$		0.18 x 2.63 μm^2
BV_{CEO}	I_C = 1 μA	1.5 V
BV_{CES}	I_C = 1 μA; V_{BE} = 0V	5.8 V
Max. $f_T@j_C$	V_{CB} = 1V	200 GHz @ 6.5 mA/μm^2
Max. f_{max}	V_{CB} = 1V	250 GHz

Table 2.2: Ultra high speed NPN transistor characteristics.

levels in the input transistors as they can handle larger voltage swings than that of a common emitter with open base. This substantially relaxes the breakdown voltage limitation since in a common base configuration the breakdown voltage resembles that of a P-N diode, see Figure 2.14.

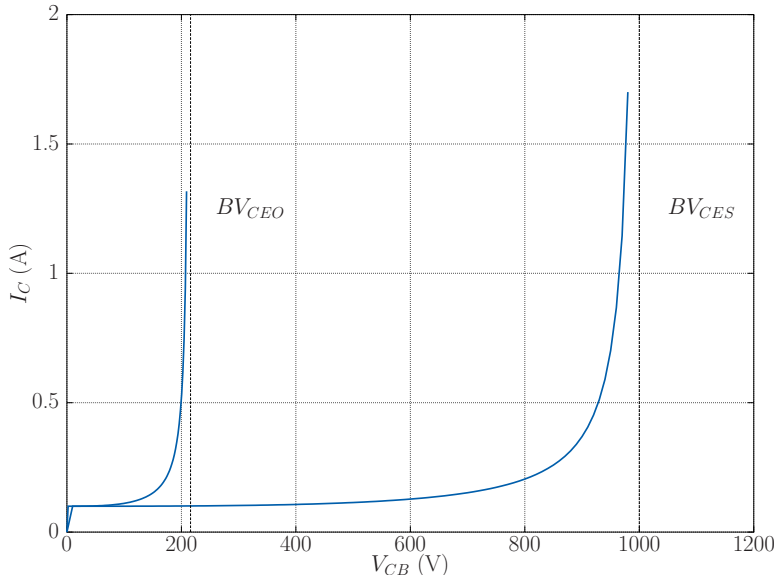

Figure 2.14: Comparison of BJT breakdown in common emitter mode (left curve) versus breakdown in common base mode (right curve) for a BJT with BV_{CES} = 1000V and β = 100 [26].

In a common emitter, base width modulation results in an increase in the collector current with increased collector-emitter voltage. What is more, avalanche breakdown of the base-collector junction is further influenced by transistor action, since the holes generated by impact ionization are pulled back into the base region which results in an additional base current [26]. This current causes a current flow from the base into the collector β times higher as a consequence of the transistor gain. This effect multiplies the generation of electron-holes pairs in the base collector junction. The common emitter breakdown voltage for an open base [27] is given by

$$BV_{CEO} = \frac{BV_{CES}}{\sqrt[n]{\beta + 1}} \tag{2.4}$$

where $2 < n < 6$. It can be seen that the BV_{CES} is significantly smaller than BV_{CEO}.

2.5 Transistor Sizing

The Ultra High Speed NPN transistors were chosen to realize the amplifier as they are the fastest available in the process design kit, achieving a maximum f_T/f_{max} of 200/250 GHz for a collector current density of 6.5 mA/μm^2. Therefore, the transistors are sized accordingly to achieve the maximum f_T for j_C equal to 6.5 mA/μm^2.

The tail currents I_{bias} was set to 36 mA and 18 mA in the input and output stage respectively. In consequence, the transistors were sized using the following procedure.

The emitter width selected for all transistors equals 0.35 μm. To account for the effective size of emitter length and width, 0.17 μm has to be subtracted from both values. Taking the output stage as an example and knowing that I_{bias} is 36 mA, each side will handle a peak current equal to I_{peak} = 18 mA. The peak current is given by

$$I_{peak} = A_{E,eff} \cdot j_C \tag{2.5}$$

where $A_{E,eff}$ is the effective area of the emitter that is calculated as

$$A_{E,eff} = (W_E - 0.17 \cdot 10^{-6}) \cdot (L_E - 0.17 \cdot 10^{-6}) \tag{2.6}$$

Substitution of 2.6 in 2.5 and solving for L_E gives

$$L_E = \frac{I_{peak}}{(W_E - 0.17 \cdot 10^{-6}) \cdot j_C} + 0.17 \cdot 10^{-6} \tag{2.7}$$

All transistor sizes for input and output stage were calculated using equation 2.7 and a multi-contact configuration of one base, two emitters and two collectors (CEBEC) was used. The final sizes are summarized in Table 2.3.

Transistor	$\mathbf{W_E}$ (μm)	$\mathbf{L_E}$ (μm)	# of devices
Q1 - Q4	0.35	1.95	4
Q5 - Q8	0.35	2.60	6

Table 2.3: Transistors size for maximum f_T.

In order to maximize the Power Added Efficiency, a series of simulations were carried out to determine the optimum supply voltage. The results are shown in Figure 2.15, the values for PAE correspond to an input power P_{in} equal to 10 dBm. This value was selected based on previous simulations observing the power level at the input for which PAE reached its peak. It can be seen that PAE increases as VDD increases reaching its maximum at $VDD \approx 3.5V$. Note that the PAE shown in Figure 2.15 was obtained from simulations early in the design stage and it is far from the final results.

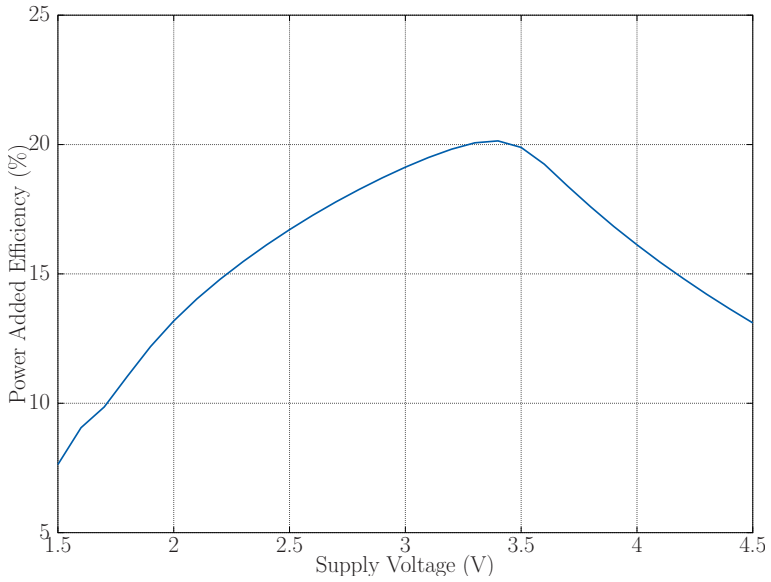

Figure 2.15: Power Added Efficiency versus supply voltage.

It's in the interest of the designer to get as much performance as possible out of the transistors. The maximum voltage swing at the common emitter and common base stage was simulated using a transient analysis to account for stress levels and avoid the devices entering the avalanche breakdown region, see Figures 2.16 and 2.17.

It can be seen that $v_{pp,CE} \approx 1.3V$ which is below BV_{CEO} for VDD equal to 3.5 V. Even though BV_{CEO} is 1.5 V, the base terminal of the input transistor is not open meaning a higher open base breakdown voltage in a real design. Then, a supply voltage of 3.5 V still leaves some room to push the input device even harder at the cost of reducing its life span.

In the case of the common base device, $v_{pp,CB} \approx 5V$ which is below BV_{CES} so same as before, a value of VDD equal to 3.5 V is still conservative in the sense that, although being high, the devices can still be pushed harder. Since there is a bias resistor at the base of 10Ω, the base is not shorted, so the shorted base breakdown value is expected to be higher in this case as well.

2.5.1 Transistor Biasing

The use of on-chip transformers for single-ended to differential conversion and vice versa, offers the possibility of exploiting another feature to the designer's advantage. As the transformer windings are nothing more than an inductor, the symmetry that exist about he x-axis allows a DC connection that creates a virtual ground at the center point, opposite to the ports, also called a center-tapped connection.

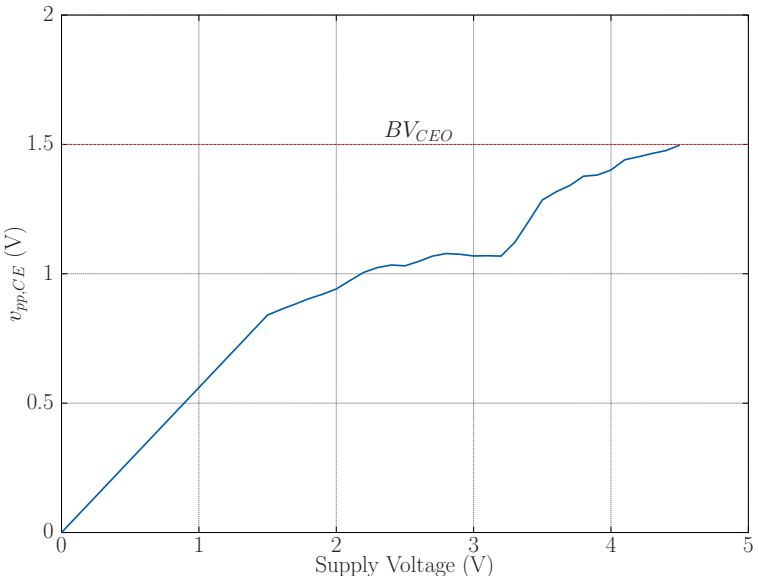

Figure 2.16: Voltage swing $v_{pp,CE}$ versus supply voltage at the collector of the transistor acting as a common emitter amplifier.

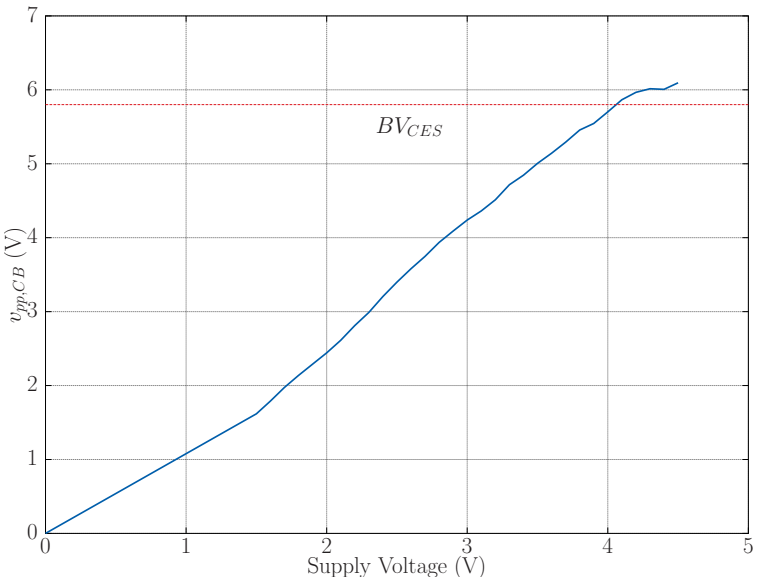

Figure 2.17: Voltage swing $v_{pp,CB}$ versus supply voltage at the collector of the transistor acting as a common base amplifier.

This simplifies the biasing circuitry to just the cascode devices and the input devices of the output stage due to the absence of transformer in the interface that separates input and output stage. Using resistors instead of inductors for biasing the input devices of the output stage can improve the compression point. As the voltage at the base V_B goes up, the collector current I_C goes up; the rate at which I_C increases is smaller using a resistor since I_B decreases as V_B increases.

All bias resistors present in the schematic shown in Figure 2.13 are realized in the TaN layer ($R_{s,tan} = 20\Omega/\square$) with a value of 10 Ω. The bias voltages of the whole design are shown in Table 2.4.

Voltage	Value (V)
V_{B1}	0.868
V_{B2}	0.9
V_{CAS}	1.8
VDD	3.5

Table 2.4: Bias voltages.

2.5.2 Inter-stage matching network

The nature of the two-stage architecture selected for this design comes with an additional problem, that is, how to connect the driver amplifier to the output stage without compromising the gain. The output impedance of a differential amplifier with cascode devices is clearly much higher than the impedance seen looking into the base of a common emitter. For that purpose, an L-match network was designed using a shunt inductor L_p and a series capacitor C_s.

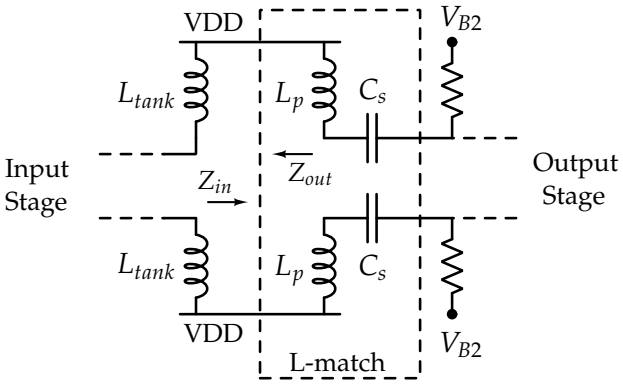

Figure 2.18: Inter-stage matching network.

In the interface of Figure 2.18, Z_{out} corresponds to the impedance looking into the output of the input stage and is equal to 980 Ω. It had to be matched to the input impedance of the output stage Z_{in}, that is equal to 12 Ω. As L_{tank} and L_p are in parallel, L_p will result in a much higher value than L_{tank}, the equivalent inductance will be slightly higher than L_{tank} and can be realized using an small on-chip inductor. The capacitors C_s were realized using MIM capacitors with a capacitance per unit area equal to C_a = 1.4 fF/μm^2.

As L_p is absorbed by L_{tank}, Figure 2.18 there is only one inductor in the interface between stages, L_m in Figure 2.13. A small inductor with a center tap connection was realized in the forth metal layer. It and can be seen at the center of Figure 4.1 in yellow color.

A series of EM simulations were performed to characterize the inductor L_m, including the parasitics introduced by the extra routing needed to connect to the output transistors. This step proved to be extremely difficult as further issues arose regarding reverse isolation associated with the low Q-factor of the matching network, negatively affecting gain, linearity and efficiency performance. These concerns are not surprising as the inter-stage matching network is critical in the whole power amplifier design. Several ways of solving this problem are discussed in Chapter 5.

2.6 Circuit Layout

As mentioned in previous sections, the presence of parasitic capacitance or inductance is of extreme importance in millimeter wave circuit design. Specially relevant is the inductance at the ground node of the input stage and the parasitic inductance and capacitance added by the metal interconnect between stages. There is an extra effort required to reduce the parasitic inductance in the interconnects to the baluns at the input and output of the power amplifier. In this section, only the parasitics associated with the layout of the active devices is treated. The last problem is analyzed and discussed in Chapter 4.

Figure 2.19 illustrates the layout of the input stage driver amplifier with cascode devices while the layout of the output stage is depicted in Figure 2.20. As the width of the transistors was considerable, they were realized using a multi finger structure. It served of great help the availability of a multi-contact transistor configuration, offering two emitters and two collectors contacts per diffusion, plus one base contact per device (CEBEC). The same multi-contact configuration was used for input and output stage. This decision allows a reduction in the parasitic inductance at the ground node as all connections are effectively in parallel. What is more, several substrate contacts were placed along the ground metal trace to assure a good ground connection.

Input and output stage layouts are symmetrical to the x-axis, the placement of input and cascode devices is exchanged to facilitate the connection to the input

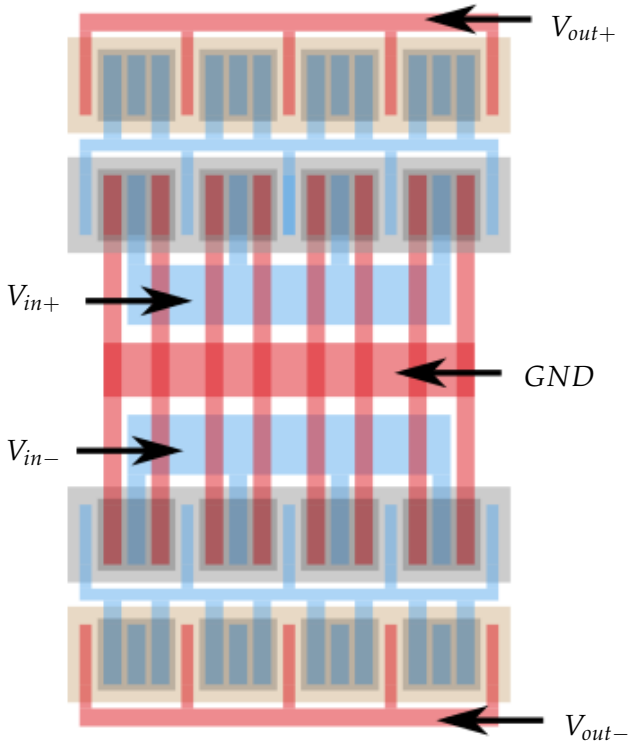

Figure 2.19: Input stage layout.

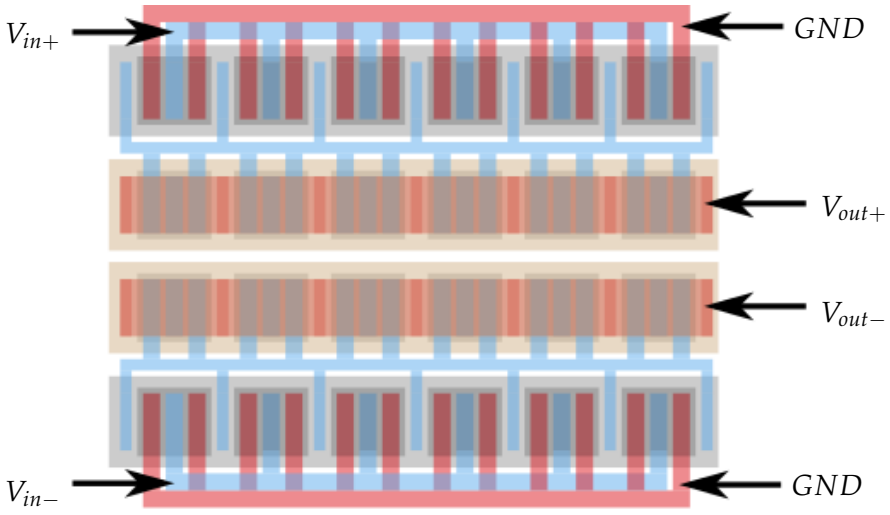

Figure 2.20: Output stage layout.

and output baluns. The metal interconnects at the ground node of the driver amplifier as well as the long metals used to connect to the baluns were simulated in Agilent Momentum to discard any inductance degeneration at the emitter in the former and coupling to the substrate in the latter. The layout of the PA including input and output baluns is shown in Figure 4.1. The complete design including pad frame is depicted in Figure 4.2 and Figure 4.3, including power planes and metal fill. The model used for the pads in simulations is discussed in Appendix A.

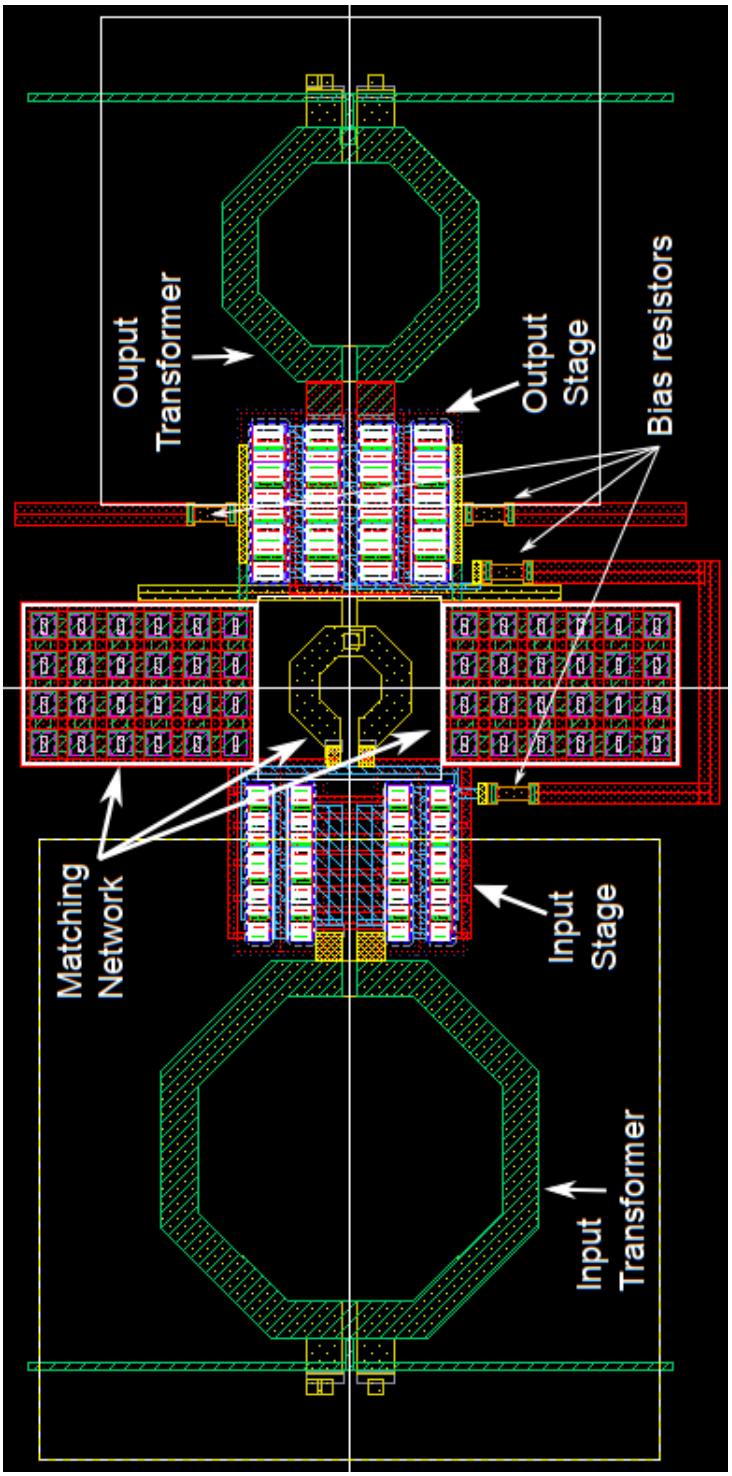

Figure 2.21: Layout of the power amplifier, including input and output transformers.

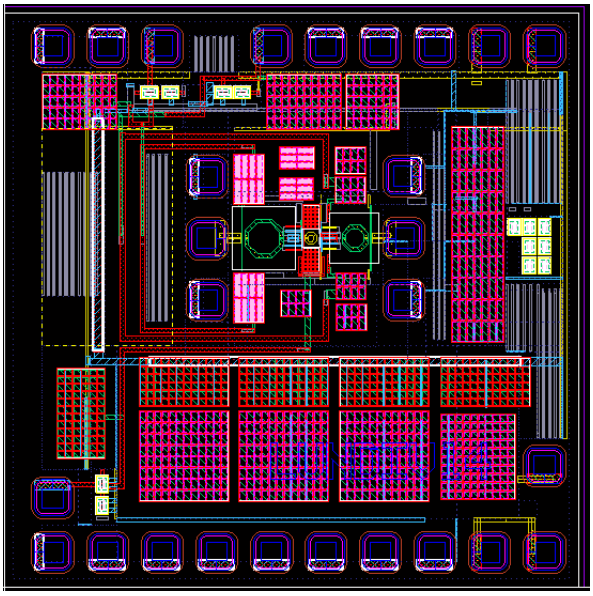

Figure 2.22: Complete layout including pad frame.

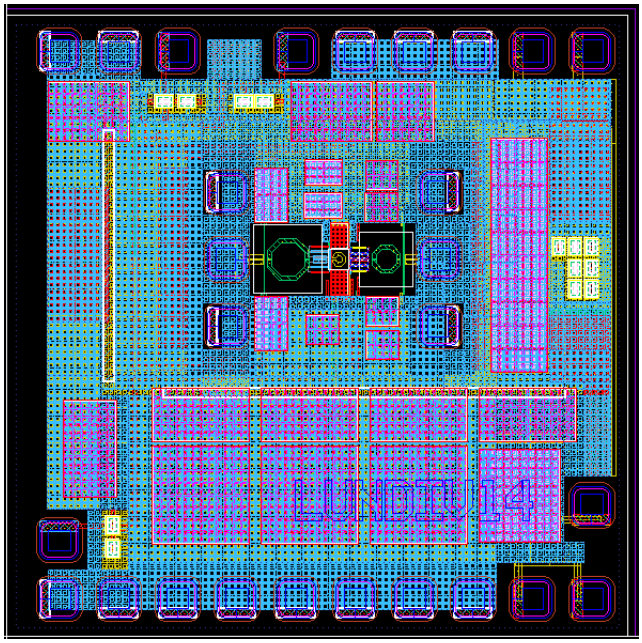

Figure 2.23: Complete layout including pad frame, power planes and metal fill.

Chapter 3

Power Combiner Transformers for mm-Wave Power Amplifiers

This chapter discusses the use of monolithic transformers in millimetre-wave circuits like power amplifiers. These techniques have become very popular lately as on-chip transformers can perform several critical tasks at the same time, that is, impedance matching, single-ended to differential conversion and vice versa and AC-coupling between stages.

The parameters that characterize a good performance in an on-chip transformer are similar to those of inductors and are summed up as follows:

1. Low series resistance (R_s) in the primary and secondary windings.
2. High magnetic coupling (k) between primary and secondary.
3. Low capacitive coupling (C_F) between primary and secondary.
4. Low parasitic capacitances (C_{par}) to the substrate.

The shrinkage in feature size in today's modern integration technologies entail a reduction in supply voltage which affects the output power capabilities of transistors. Assuming a sinusoidal signal and a voltage swing as the output of two times the supply voltage , the output power P_{out} delivered to the load R_L [28] is given by

$$P_{out} = \frac{V_{sup}^2}{2R_L} \tag{3.1}$$

We see that if the supply voltage decreases by half, it imposes a reduction of four times the power that can be delivered to the load. Contrary to that trend, the newest wireless standards come with stringent requirements making these technology constraints appear as new challenges for circuit designers.

Many of the new wireless standards use a non-constant envelope modulation scheme [29], for which it is required a high Peak-to-Average Power Ratio (PAPR). When designing a power amplifier, this sets a requirement for amplitude and phase linearity, which demands a higher conduction angle lowering the overall

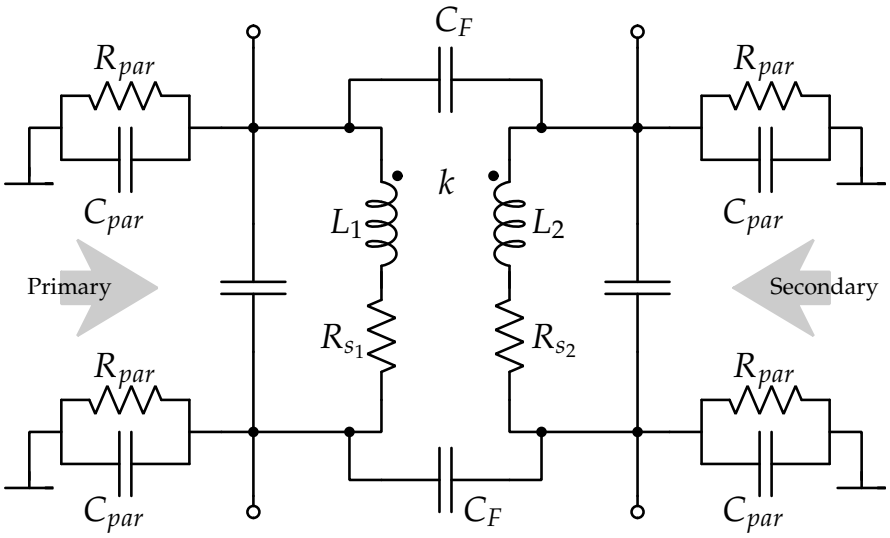

Figure 3.1: Model of a non-ideal transformer.

efficiency [30].

As efficiency is the key metric in the whole design of a RF PA for mobile communications and knowing that the PA will operate at the peak output power, it is desired to have high average power efficiency in order to increase battery lifetime. But taking into account that most radios nowadays include *gain control* circuitry whose main task is to make all signals arrive at the base station with the same power, it is then wise to design a PA that achieves good efficiency for the average output power rather than maximum efficiency for the peak output power [31].

3.1 Layer Stack Up

There exists many techniques used in power combining at mm-Wave frequencies, some of them include the use of monolithic transformers built in different fashions. The use of planar versus stacked (3D) transformers depends mainly on the fabrication process chosen by the designer, that is, the availability of thick metals in the top layers. In the case of this work, the Infineon B7HF200 process [32],[33] provides two thick copper layers in metal layers 3 and 4, see Table 3.1. This fact will condition the selection of the structure as it will be described shortly.

The reason behind the selection of planar versus stacked transformer points us to the discussion of several variables and constraints that will limit the performance of the power combiner, which manifest itself in the form of *power loss*. The skin effect [28] being the most obvious, due to the high frequencies at which the PA is designed to work. The skin effect is the tendency of an AC current to

Metal	Thickness (μm)
Cu 1	0.75
Cu 2	0.75
Cu 3	1.05
Cu 4	2.80

Table 3.1: Metal layers thickness's

flow mainly close to the surface of a conductor and down to a level called the *skin depth* as the frequency increases, thus decreasing the current density towards the center of the conductor and increasing the resistance that the current faces as the effective area for it to flow is significantly reduced.

The current density J decreases exponentially from that at the surface J_s of the conductor inward down to x [34], given by

$$J = J_s \, e^{-x/\delta} \tag{3.2}$$

where δ is the *skin depth* that is given by

$$\delta = \sqrt{\frac{2\rho}{\omega \mu_r \mu_0}} \tag{3.3}$$

where ρ is the resistivity of the conductor, ω is the angular frequency of the current, μ_r is the relative magnetic permeability of the conductor and μ_0 is the permeability of free space. Table 3.2 shows the characteristics of the metal layers available in the process. To get an idea of the range of skin depth we are dealing with at mm-Wave frequencies, a rapid calculation tells us that $\delta \approx 0.85 \ \mu m$ for Aluminium at 10 GHz, while $\delta \approx 0.23 \ \mu m$ for Copper at 84 GHz.

Metal	Conductivity (S/m)	Sheet Resistance ($m\Omega/\square$)
Cu 1	$5.6 \cdot 10^{-7}$	30
Cu 2	$5.6 \cdot 10^{-7}$	26
Cu 3	$5.6 \cdot 10^{-7}$	18
Cu 4	$5.6 \cdot 10^{-7}$	6.5

Table 3.2: Metal layers conductivity ($\sigma = 1/\rho$) and resistance.

This can be clearly seen in Figure 3.2, which is the result of an EM simulation in an on-chip transformer, showing the current density distribution within the area of the primary.

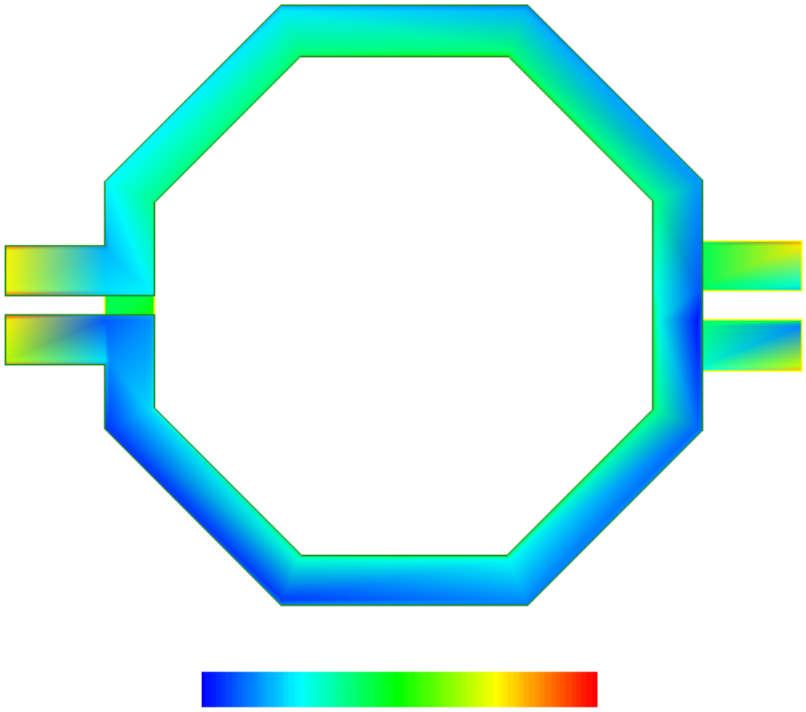

Figure 3.2: Current density J (A/m) in the primary of a transformer with inner radius $r = 25\ \mu m$ and trace width $w = 5\ \mu m$ at 57 GHz. The minimum current density is represented with blue, maximum with red colour. Observe how, as a consequence of the skin effect, the current accumulates on the inner edge of the octagon.

3.2 Transformer Structure

As mentioned before, the design of the transformer targets *minimum power loss*. And in order to minimize the losses, a stacked up design is beneficial as it can achieve higher magnetic coupling between primary and secondary compared to that of a planar design [35]. Although the metal thickness of the copper in layers 3 and 4 is relatively large compared to CMOS processes, the use of a planar structure would yield lower magnetic coupling due to skin effect and the impossibility of changing the thickness of the metals to increase the effective area. Such constraint does not exist in a stacked up structure, as the designer can increase the metal width of the spirals that form the transformer, achieving higher magnetic coupling by means of increasing the area. It should be pointed out that most CMOS designs rely on the top capping layer often made of aluminium [36] to realize one of the transformer spirals, which most of the time is thinner, besides being worse conductor than copper. Then, it is reasonable to assume a better transformer performance by using this process.

The geometry of the transformer was chosen to be an octagonal shape due to mask generation rules. The structure is symmetrical and, since the impedance transformation is from $Z_0 = 50\Omega$ to 50Ω, a 1-to-1 transformation ratio was chosen. There are different approaches for selecting the transformation ratio, all limited by the amount of capacitance left at the output node of the transistors as well as the optimum load Z_{opt} that has to be seeing looking into the output of the PA. This gives the designer the opportunity of placing several amplifiers operating in parallel and performing a power combination by connecting all the secondary together in series. For example, for a 1-to-2 transformation ratio, there will be two transformers with their secondary connected in series, both seeing an optimum load of 12.5Ω each ($Z_0/4$) [37]. This idea could be extended further using up to 4 transformers as reported in [38], performing a 1-to-4 transformation.

Observing Figure 3.3, it can be seen that the secondary of each transformer carries the same current V_{out}/R_L, then, in order to calculate the transformed load impedance R_m seen by each PA it is assumed that all transformers have the same transformation ratio m and the same output impedance, leading to a simplified expression given by

$$R_m = \frac{R_L}{2N \cdot m^2} \tag{3.4}$$

and thus, the total output power delivered to the load is

$$P_L = N^2 \cdot m^2 \cdot \frac{V_{PA}^2}{R_L} \tag{3.5}$$

Now, the impedance transformation ratio can be defined as

$$r = \frac{R_L}{R_m} = 2N \cdot m^2 \tag{3.6}$$

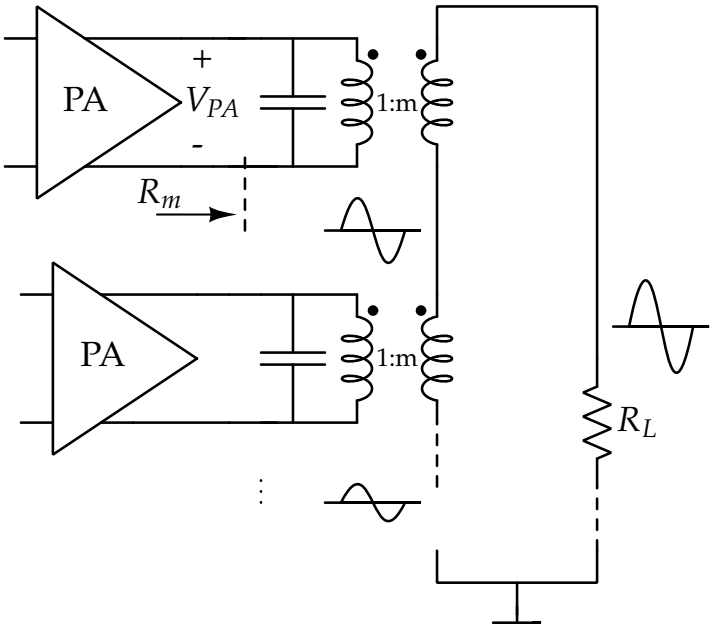

Figure 3.3: PA topology using several transformers for power combining.

As stated in Equation 3.5 the output power can be increased by increasing m or N but note as well that Equation 3.6 shows that the impedance transformation ratio increases quadratically with m and linearly with N. A high r results in a high insertion loss, that together with the energy leakage caused by imperfect magnetic coupling can lead to losses higher than 1.5 dB [39], which will dramatically reduce the performance of the whole design.

3.3 Transformer Design

Starting at the input transformer, the single-ended input winding is realized in the fourth metal layer *Cu4* while the third metal layer *Cu3* is used for the differential output winding which goes to the input of the PA. The balun is optimized to achieve minimum insertion loss for which two factors are of capital importance, magnetic coupling k and port mismatch.

The designer is left with only two degrees of freedom, transformer radius and trace width, as the geometry of the winding has a negligible impact in the design when, for example, it is considered a circular versus octagonal shape. The radius is responsible as well of setting the self-resonance frequency f_{SR} of the input and output windings, that is, it is proportional to the inductance and inversely proportional to the self-resonant frequency. The lower the radius, the lower the

inductance, the higher the f_{SR}.

On the other hand, the trace width sets the *unloaded Q-factor* of each winding and it has a proportional relationship to Q and an inversely proportional relationship to the parasitic resistance. The wider the trace, the less resistance, the higher the Q and f_{SR}.

If chip area were not a constraint, the trace width will be set to the maximum allowed by the process but that will require a large area, quickly turning the design impractical. A set of iterations are required in order to find and optimize both input and output baluns, which is discussed in the next chapter. The input and output baluns are presented in Figures 3.4 and 3.5.

Of course that this ideal balun does not exist as the input and output transformer radius are limited and set by the amount of capacitance in the input and output nodes of the PA plus the parasitics due to interconnects between nodes. This carries a clear implication for the minimum insertion loss that can be achieved since the coil will be sized as to have the right inductance to resonate at $f_0 = 83.5\ GHz$ with the mentioned capacitances. That is the reason why, as a consequence, the input and output transformers differ in size.

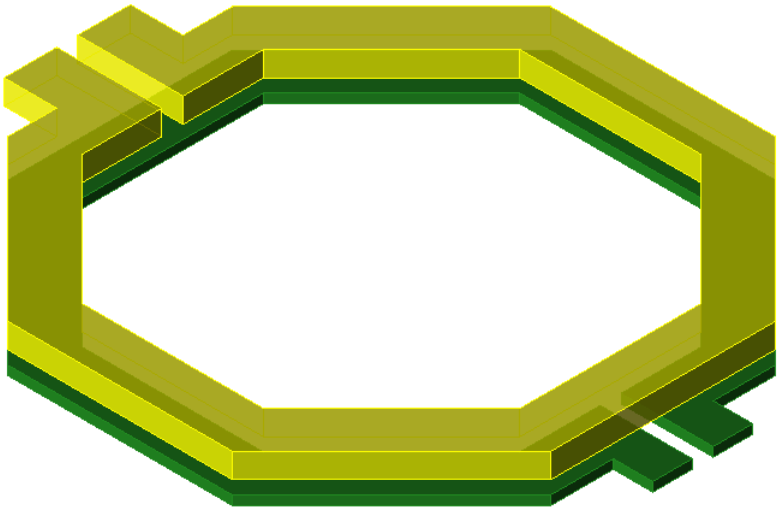

Figure 3.4: Input transformer with inner radius $r = 25\ \mu m$ and trace width $w = 6\ \mu m$.

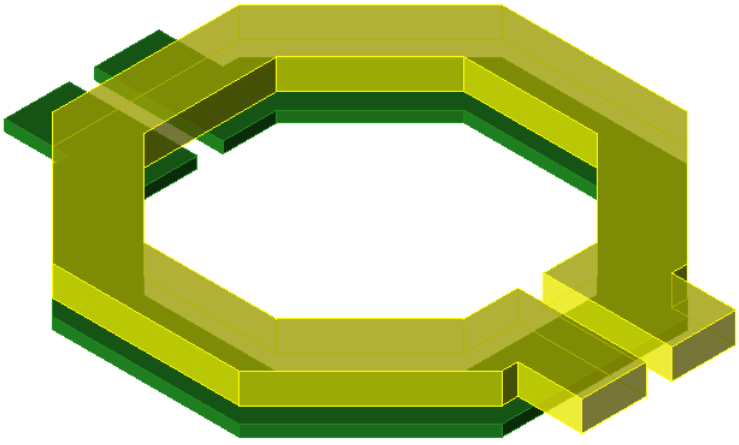

Figure 3.5: Output transformer with inner radius $r = 15\ \mu m$ and trace width $w = 6\ \mu m$.

Chapter 4

Transformer Simulation Results

While the constrains for the design of the transformer were addressed in the previous chapter, this chapter describes the strategy that was followed to meet the performance requirements through a series of iterations targeting the optimization of the insertion loss and transformer size.

4.1 Transformer Geometry

As discussed before, the selected shape was an octagon that performance wise, is on par with a transformer with circular shape and more convenient to comply with mask generation rules. Together with the necessary inductance, that is given by the dimensions of the inner radius, and Q-factor, given by the trace width, it is mandatory to take into account the metal traces used for connecting the secondary of the input transformer to the input transistors of the input stage and in a similar manner, the traces connecting the output transistors of the output stage to the primary of the output transformer.

The goal here is to have as little capacitance as possible at the input and output nodes that allow us to have a reasonable sized transformer with enough inductance to resonate with. Having in mind that the size of the input and output transistors is fairly big, and so that their parasitic capacitance, the risk of being left with not enough inductance represents a challenge itself, since small inductance means small radius and so, the design could turn impractical if this is not taken into account.

Then, the strategy comprised an approach involving transistor sizing of input and output stage, and the length and geometry of the interconnects from the transformer to the transistors and vice versa for input and output stage respectively. The first step is to calculate the amount of capacitance at the input node of the input stage C_{in} and at the output node of the output stage C_{out} using post-layout simulations. Once those values were extracted, Equation 4.1 was used to get an approximation of the amount of inductance needed:

$$f_0 = \frac{1}{2\pi\sqrt{LC_p}} \tag{4.1}$$

where f_0 = 83.5 GHz and C_p can be C_{in} or C_{out} depending of the simulations that were carried out.

Note that, post-layout simulations at mm-Wave frequencies become of extreme importance as a small parasitic inductance to ground in the range of 10 pH in the emitter of the input transistors could degrade the voltage gain of the amplifier, so special care has to be taken during the layout of the differential pair.

It was clear though, that the disposition of the transistors in the layout played an important part in the amount of parasitic capacitance seen by the transformer so two options were considered.

The first option is illustrated in Figure 4.1 consists of placing the transistors in a vertical fashion with the input transistors in the centre (grey) and the output transistors next to them (brown) and connect them to the transformer (green) using a right angle metal trace (blue).

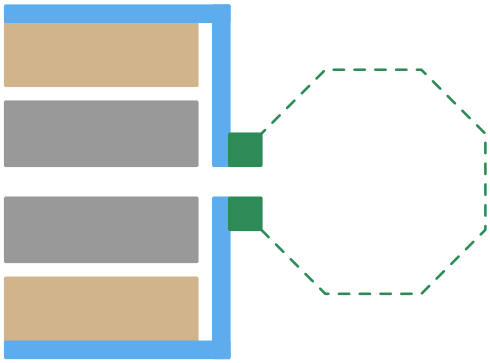

Figure 4.1: Vertical layout with right angle interconnects.

The second option, as shown in Figure 4.2, consists in placing the transistors in a horizontal fashion with the output transistors being closer to the transformer. This helps by reducing the parasitic inductance added by the interconnects as their length decreases but still, the amount of inductance is excessive as we will see now.

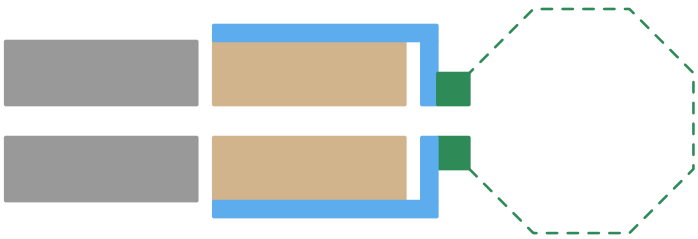

Figure 4.2: Horizontal layout with right angle interconnects.

The effective length of the interconnect metal trace has to be considered before doing EM simulations. As it was described in Chapter 2, the use of wide devices with several collectors render the equivalent interconnect as several inductors in parallel. Then, the simulations account for half the length of the metal trace, that is, the ports were placed starting from the middle point of the output transistors.

A series of simulations were carried out varying the radius while maintaining the same trace width equal to 6 μm. As the results were not conclusive, a third layout disposition was considered, this time using a 45° angle to connect from the output transistors to the transformer. In fact, it was necessary to resize the transistors by decreasing the width by half and at the same time, putting two of them in parallel in order to decrease the vertical size of the metal trace, making the design more compact, see Figure 4.3.

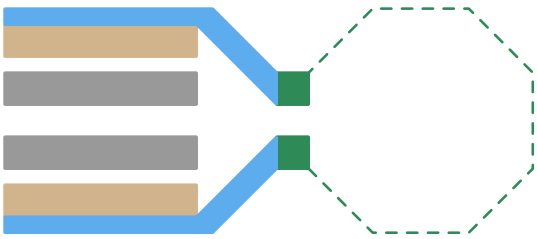

Figure 4.3: Vertical layout with 45° angle interconnects and transistors in parallel.

Observing Figure 4.4, it can be seen that using a 45° angle to connect to the transformer effectively reduced the inductance and thus decreased the Q-factor as it was intended. The downside though, still remains within the large values of inductance in the range of 70 to 80 pH, which is mainly due to the difference in width between the interconnects and the primary of the transformer.

This problem did not appear if the metal traces for the interconnects were not taken into account during simulations, a fact that would render misleading performance results if this model were used. In this case, the output node will not be tuned to resonate at the center frequency f_0. The simulation results of the output transformer structure alone showed approximately half the inductance values of those in Figure 4.4 for the same radius and trace width.

In fact, as we have just mentioned, when not taking into account these parasitics the results could be deceptive as the designer will not notice the implications of this decision. This is illustrated in the following example. An alternative method of dealing with these high inductance values is to reduce or increase the size of the input/output transistors as it will decrease or increase the parasitic capacitance seen by the transformer. A series of simulations were performed with the different geometries studied. Figure 4.5 shows the length of the emitter versus the transformer inner radius.

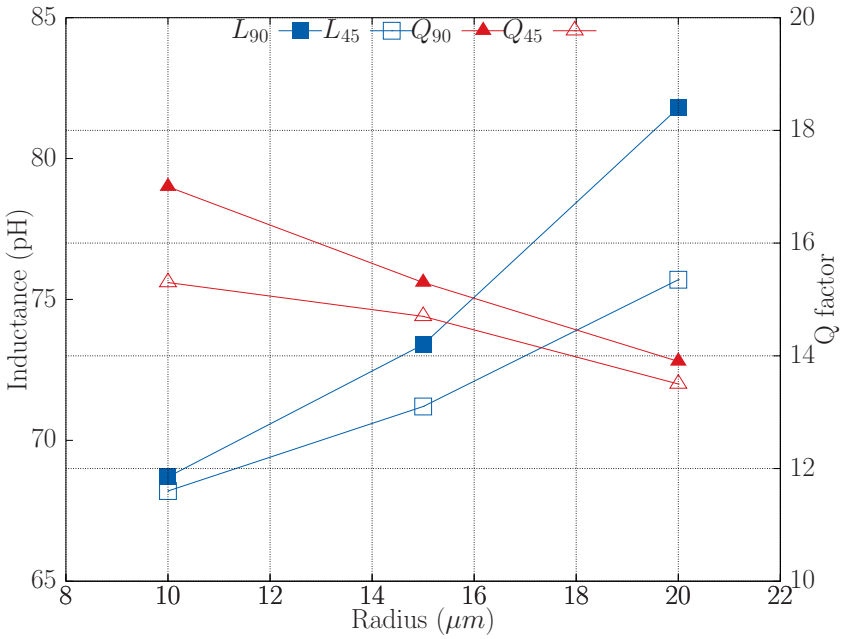

Figure 4.4: Inductance and Q-factor (differential) for different interconnect methods with transformer fixed trace width.

Observe how, despite of the geometry chosen for the interconnects, the results suggest zero to 0.1 μm variation in the emitter length for transformers of radius equal to 15 μm. This small change in emitter length could be incorporated into the design and it will have negligible impact on the overall performance. Taking the output stage as an example, it means a small increase in current handling capabilities of the cascode transistors but as they are limited by the size of the devices in the differential pair (the emitter length has not changed), linearity, efficiency and reverse isolation will not be degraded since a 0.1 μm increase in size does not represent a risk.

4.2 Back-to-Back Simulations

Measuring the insertion loss of a 3-port device is not obvious nor straightforward. Although there are some other ways that involve S-Parameter transformations [35], the approach selected for this work was to use Back-to-Back simulations.

The strategy is to use the extracted S-Parameters from the EM analysis performed by Momentum and add some tuning capacitors to two instances of the same transformer connected back to back as illustrated in Figure 4.6, to resonate with the primary/secondary at f_0 = 83.5 GHz. Adding two 50 Ω terminations guarantees that the input and output ports are perfectly matched. After perform-

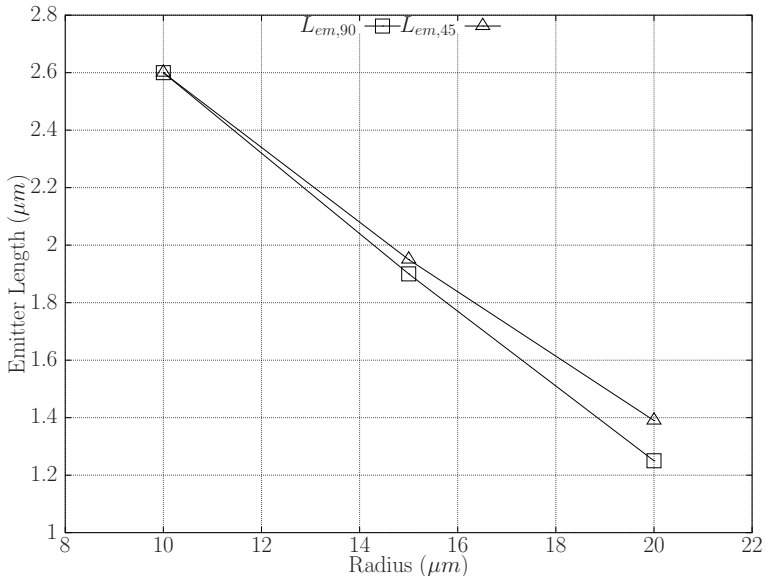

Figure 4.5: Emitter length versus transformer radius for different interconnect methods with transformer fixed trace width.

ing an S-Parameter simulation with this set up, the minimum insertion loss is half of G_{max} in dB.

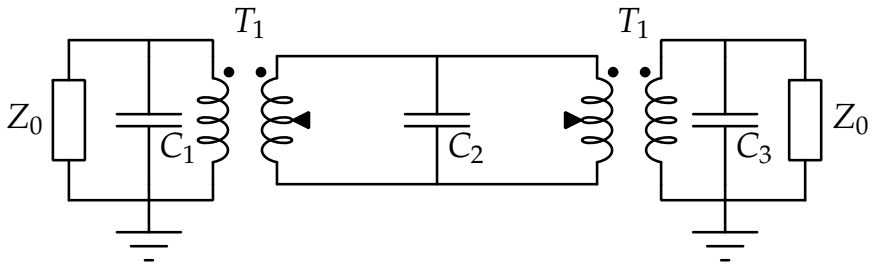

Figure 4.6: Back-to-Back simulation test bench where Z_0 = 50 Ω and C_1, C_3 and C_3 are tuning capacitors (f_0 = 83.5 GHz).

Although the extracted inductance was too high, the insertion loss achieved was on par with that reported in recent publications in state of the art power combiners [40], [41] and [42], being less than 1 dB in some cases. Figure 4.7 shows the insertion loss for the different interconnect geometries that were described in this section.

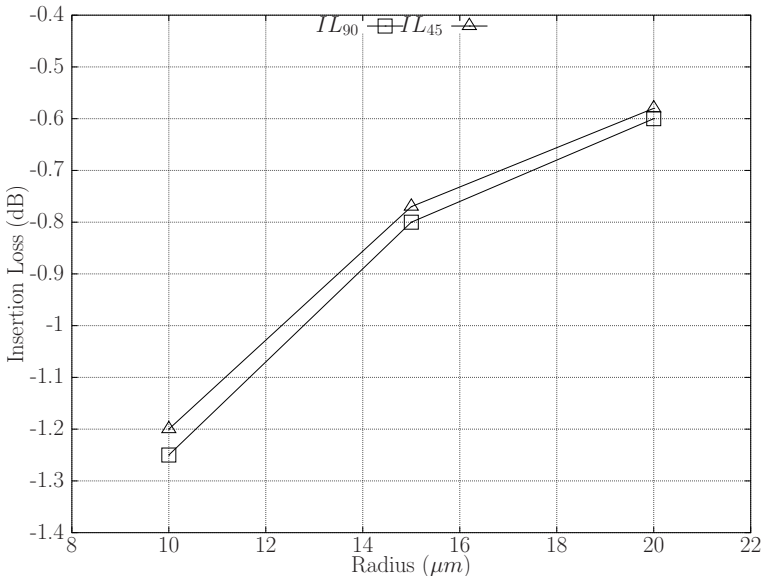

Figure 4.7: Insertion loss for different interconnect methods with transformer fixed trace width (w = 6 μm).

4.3 Layout Technique

A different approach has to be used in the layout to reduce the high inductance while keeping a reasonable sized transformer and the insertion loss at minimum. Keeping a compact layout increases the chances to get a working design after tape-out [43], so a re-arrangement of input and output transistors around the axis of symmetry of the transformer is proposed.

The primary effect of the increase of parasitic inductance is the imbalance in trace width between the interconnects and the input ports in the transformer. It is reasonable then to assume that using a wider metal trace for the interconnects will not have so much impact as far as the length is not extremely large.

The proposed layout for the input and output stage is shown in Figures 4.8 and 4.9 respectively. Note the disposition of the transistors in a vertical fashion together with the exchange in the placement of input and output devices, that is, input devices in the center, output devices in the outer side for the input stage and vice versa. This results in a much more compact layout and a significant reduction in the interconnects between the input and output stage as there is now a direct and shorter path between output devices of the input stage and input devices of output stage.

The main drawback of the proposed layout is that it is prone to an increase in parasitic capacitance to the substrate as a direct consequence of the larger area used by the metal traces for the interconnects and thus, possible negative effects have to be considered.

Once the final layout proved valid, it was incorporated to the design together with the active devices which results are discussed in the next section.

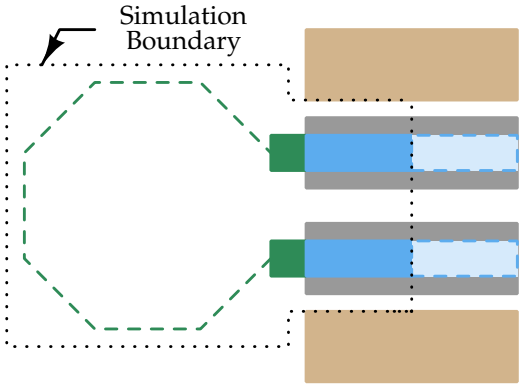

Figure 4.8: Input stage layout with the transistors arranged in a vertical fashion. The secondary of the transformer is in the third metal layer (Cu 3, green) while the base of the input transistors (grey) is in the first metal layer (Cu 1, blue). The extracted S-Parameters only account for half the trace length that covers the base of both input transistors plus the transformer structure (dotted black line).

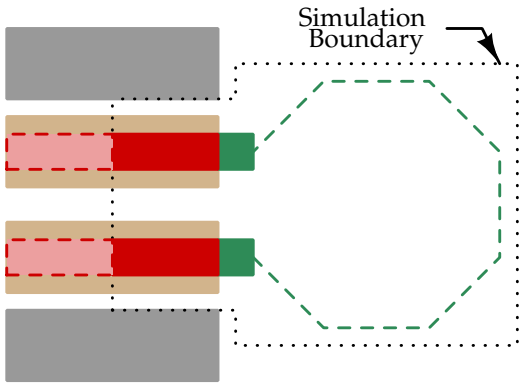

Figure 4.9: Output stage layout with the transistors arranged in a vertical fashion. The primary of the transformer is in the third metal layer (Cu 3, green) while the collector of the output transistors (brown) is in the second metal layer (Cu 2, red). The extracted S-Parameters only account for half the trace length that covers the collector of both output transistors plus the transformer structure (dotted black line).

4.4 Final Design

As mentioned in the previous chapter, the final size of input and output transformer is different, the main reason being the difference in capacitance at the base and at the collector of a bipolar transistor. In the input transistors of the input stage the capacitance at the base will be dominated by the parasitics of the interconnect plus the junction capacitance $C_{j,be}$ and the diffusion capacitance $C_{d,be}$ [27]. On the other hand, at the output devices of the output stage, the capacitance will be much larger due to the base-collector junction capacitance $C_{j,bc}$, also known as the Miller capacitance.

The sizing of the transistors did not offer the possibility of a wide adjustment, mainly because an increase in size carries a penalty in reverse isolation and a reduction in size means less current handling capabilities and thus, a penalty in linearity. The choice was to select the trace width so that to decrease the series resistance and optimize the transformer radius for minimum insertion loss.

For the output stage, see Figures 4.10 and 4.11, the choice was to use a transformer with 25 μm inner radius and 6 μm trace width. In the case of the input stage, see Figures 4.12 and 4.13, the selection was a transformer with 15 μm inner radius and a trace width of 6 μm as well.

Both transformers present an insertion loss of less than 1 dB at f_0. The difference between using thick conductor models (enabling Momentum 3D expansion option) during simulations represents up to a 0.5 dB variation in insertion loss. We must say that these results show a optimistic figure for insertion loss. A series of suggestions are given in chapter 6 that can help to get a more realistic model for the on-chip transformers.

The solution though is to rely on a fabricated model from which S-Parameters can be extracted and used in a *n-port circuit model*. The performance details of the final input and output transformers are shown in the following table.

Stage	L (pH)	Q	Insertion Loss (dB)
Input	51.4	20.8	-0.63
Output	56.1	18.4	-0.45

Table 4.1: Transformers performance details. The secondary (input stage) and primary (output stage) are both in the third metal layer (Cu 3). The inductance and Q-factor on this table accounts for the coil that is connected to the active devices. The model used in the simulations includes an extra port for a center-tap connection. For more details about this model, see appendix A.

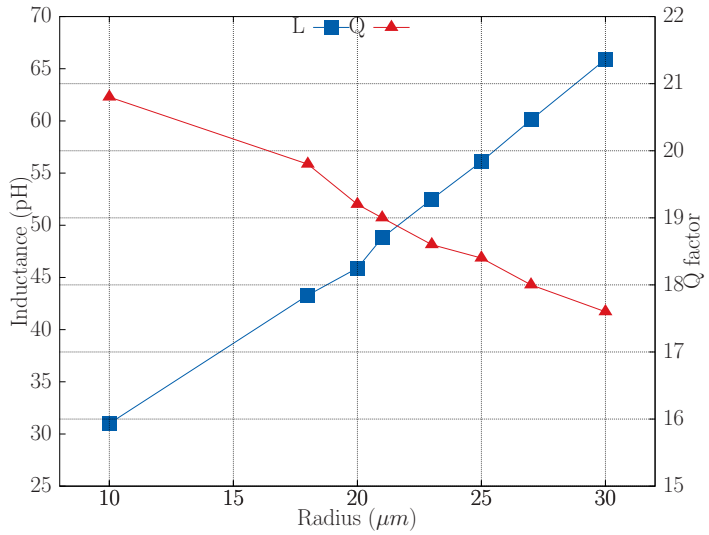

Figure 4.10: Output transformer inductance and Q-factor in primary versus transformer inner radius with fixed trace width (w = 6 μm).

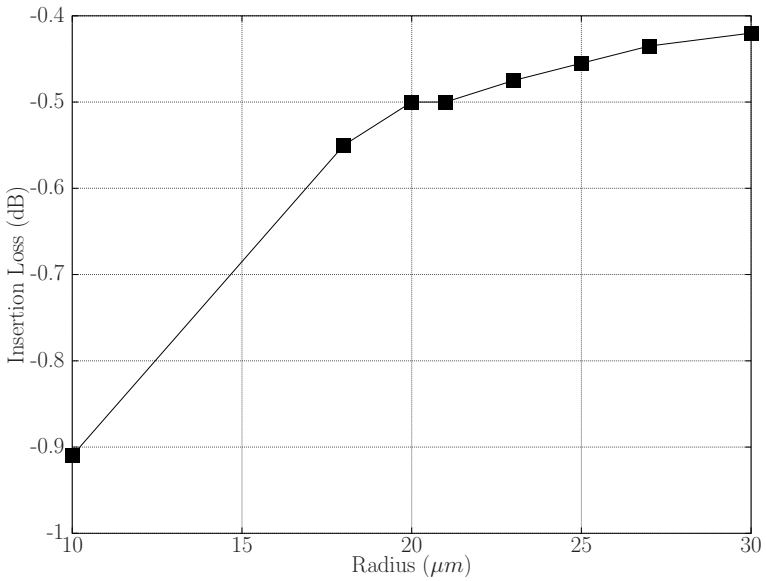

Figure 4.11: Output transformer insertion loss versus transformer inner radius with fixed trace width (w = 6 μm).

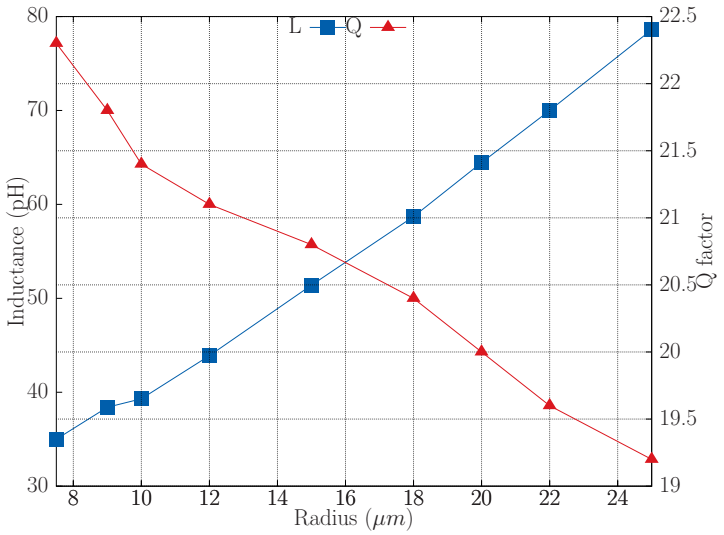

Figure 4.12: Input transformer inductance and Q-factor in secondary versus transformer inner radius with fixed trace width (w = 6 μm).

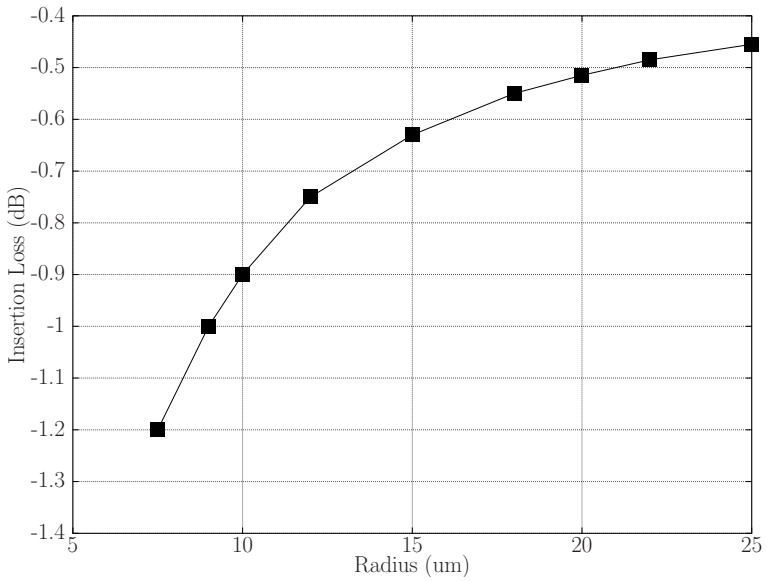

Figure 4.13: Input transformer insertion loss versus transformer inner radius with fixed trace width (w = 6 μm).

Chapter 5

PA Post-Layout Simulation Results

This chapter summarizes the performance results obtained during the course of this project. Linearity and efficiency are analysed based on results from post-layout simulations, followed by a short discussion about stability, reverse isolation and inter-stage matching network.

5.1 Simulated performance

The input and output transformers presented in this work were designed and simulated with the help of 3D Electromagnetic simulation software Momentum® from Agilent Technologies [44]. Furthermore, S-Parameters and SPICE models were extracted and exported into Cadence Virtuoso for schematic level modelling and simulation. The large signal behaviour of the power amplifier was simulated using Cadence SpectreRF® within Cadence Virtuoso Analog Design Environment. The Ultra High Speed NPN transistors used in this design are a SPICE Gummel-Poon model with additional resistors and capacitors to model parasitics, guaranteed to be valid when operated up to the maximum current density of 6.5 mA/μm^2.

The power amplifier is able to achieve a saturated output power P_{sat} of 18 dBm while the 1 dB compression point referred to the output is equal to 14.1 dBm as it can be seen in Figure 5.1.

The efficiency performance was simulated using a Periodic Steady State analysis using the harmonic balance method. The Power Added Efficiency reaches a maximum of 10.1%, while at the compression point is slightly reduced to 7.5%. Monte Carlo simulations were performed to see how process variations affect the peak PAE. The results in Figure 5.3 show a mean peak PAE of 9.8% and a standard deviation of 1.5% for 100 runs.

Figure 5.4 shows that the design is unconditionally stable as the stability factor k is greater than one for all frequencies.

The power gain S_{21}, the quality of input and output match, S_{11} and S_{22}, as well as reverse isolation S_{12} were simulated using a S-Parameter analysis. Figure 5.5 shows that the power amplifier achieves a power gain of 15.7 dB at 83.5 GHz, being higher than 15.2 dB in the whole band. The reverse isolation is better than -69 dB as can be seen in Figure 5.8.

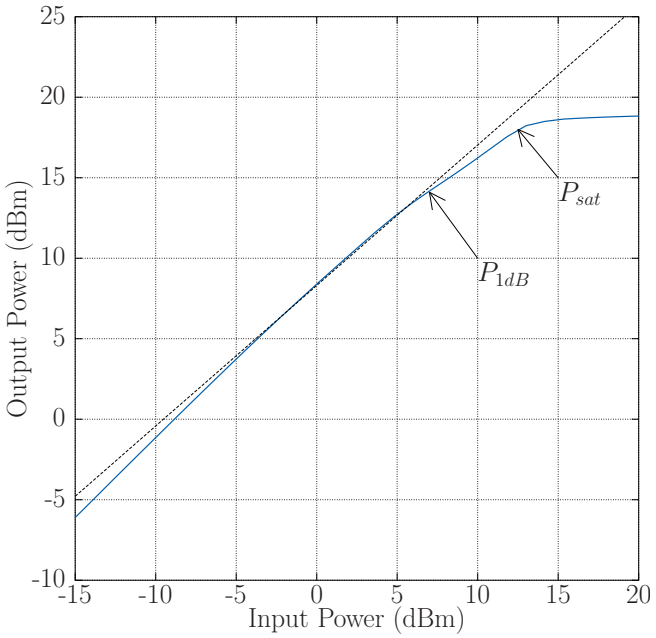

Figure 5.1: Output power versus input power.

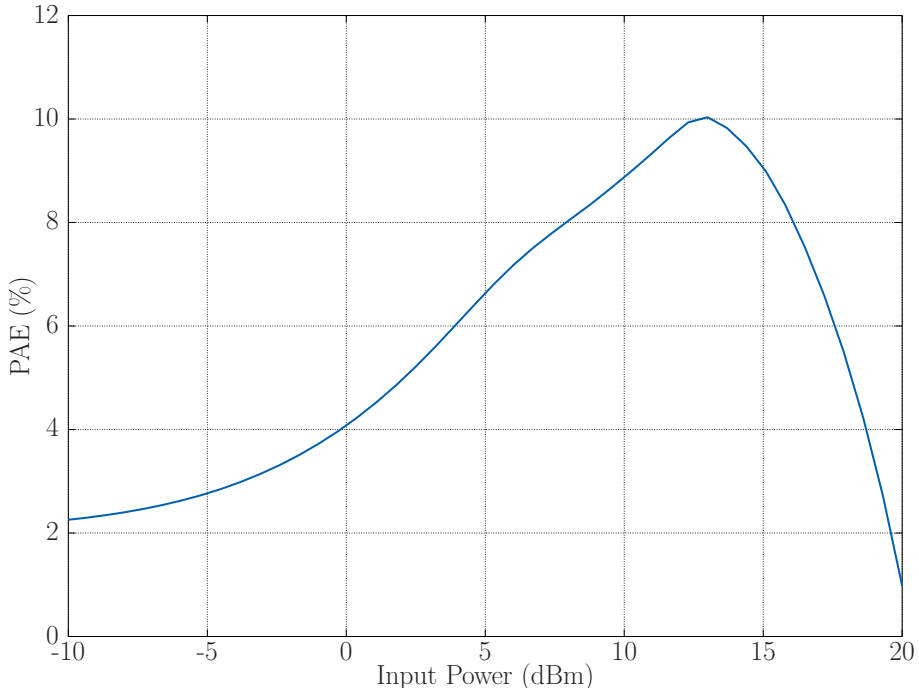

Figure 5.2: Power Added Efficiency versus input power.

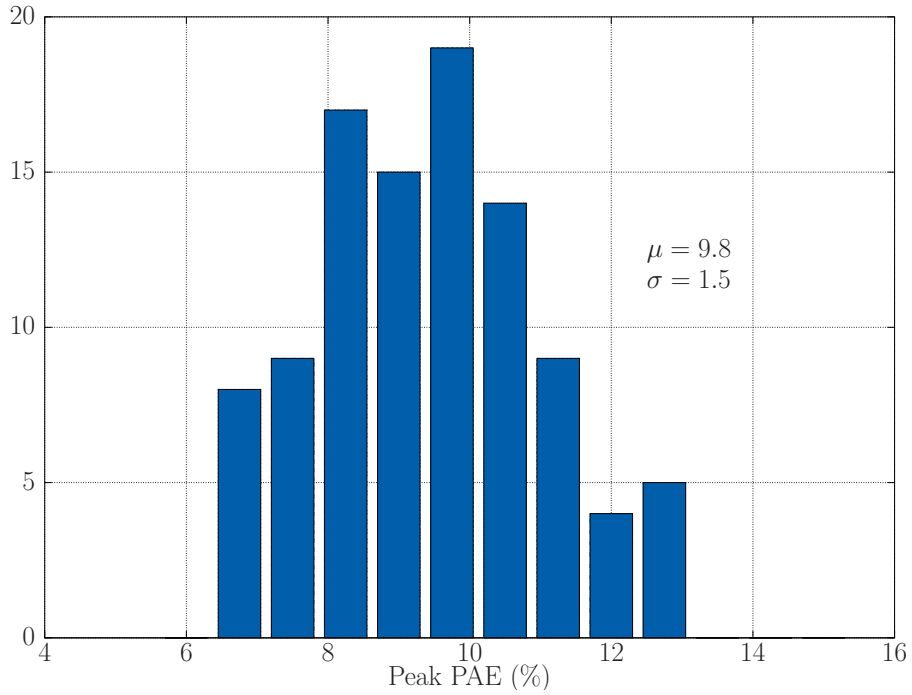

Figure 5.3: Monte Carlo simulations for peak PAE (100 runs).

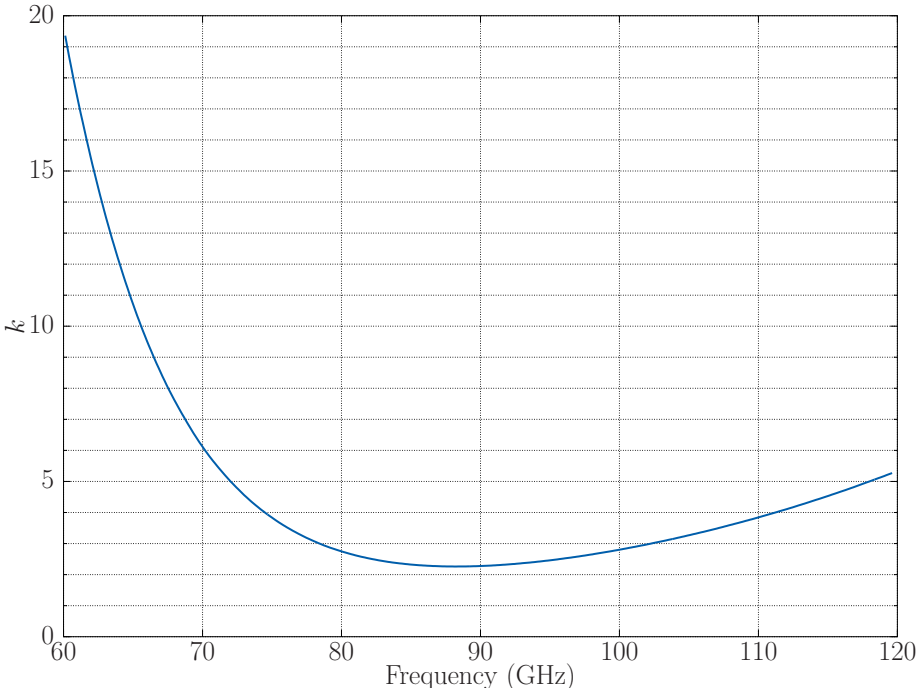

Figure 5.4: Stability factor k versus frequency.

The input match shows a bandwidth of 42.4 GHz from 60.2 GHz to 102.6 GHz for an input return loss better than -10 dB, Figure 5.6. On the other hand, the bandwidth of the output match is 20.1 GHz from 70.3 GHz 90.4 GHz for an output return loss better than -5 dB in the whole band, Figure 5.7.

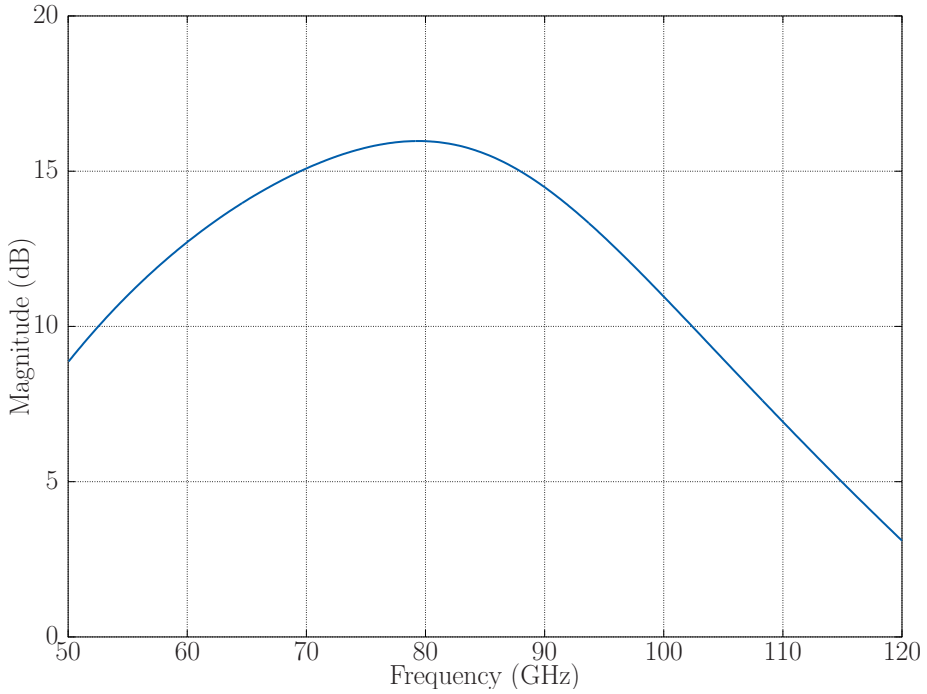

Figure 5.5: Gain (S_{21})

Despite achieving a good performance, the results show that the quality of the output match could be further improved. The presence of a inter-stage matching network which, far from being ideal, introduces losses at expense of gain, made the optimization of this design a real challenge. A low Q-factor for the impedance transformation network not only has an impact in the form of losses due to parasitic series resistance, inductance and capacitive coupling, but as well, due to its intrinsic wide band behaviour.

For that matter, the use of cascode devices boosts the output resistance of the input stage by approximately $\beta_0/2$ [27], thus increasing the impedance transformation ratio by the same amount and as a result, a smaller capacitor is required in the LC-match. This was proved to have some drastic effects on the performance of the power amplifier as the reverse isolation was seriously reduced.

Two different approaches were put into test, which involved active and passive element optimization. The reduction in reverse isolation can be mitigated by decreasing the size of the cascode devices. That will effectively reduce their

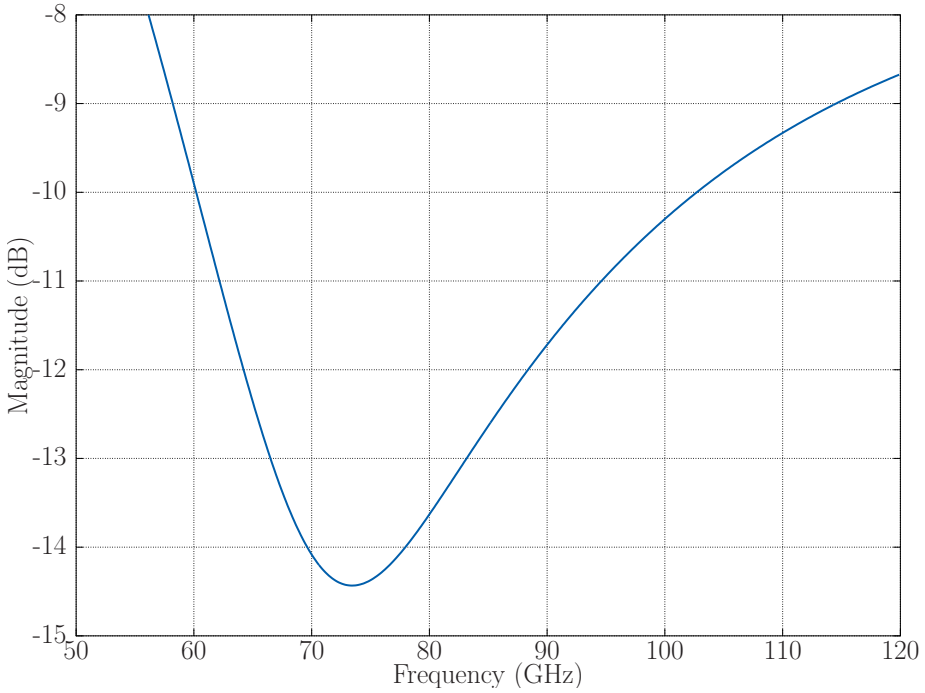

Figure 5.6: Input return loss (S_{11}).

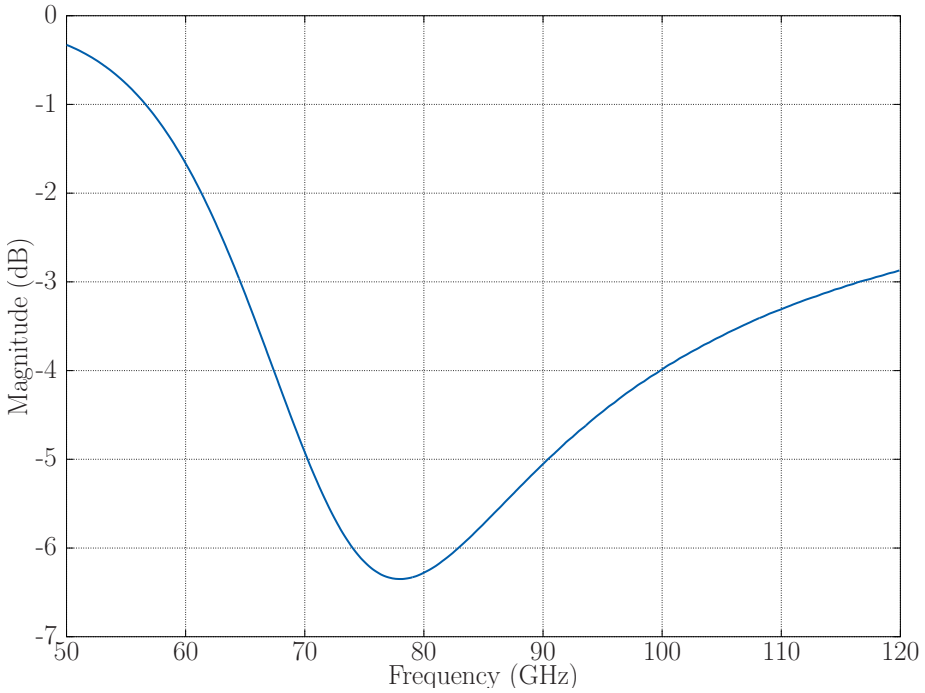

Figure 5.7: Output return loss (S_{22}).

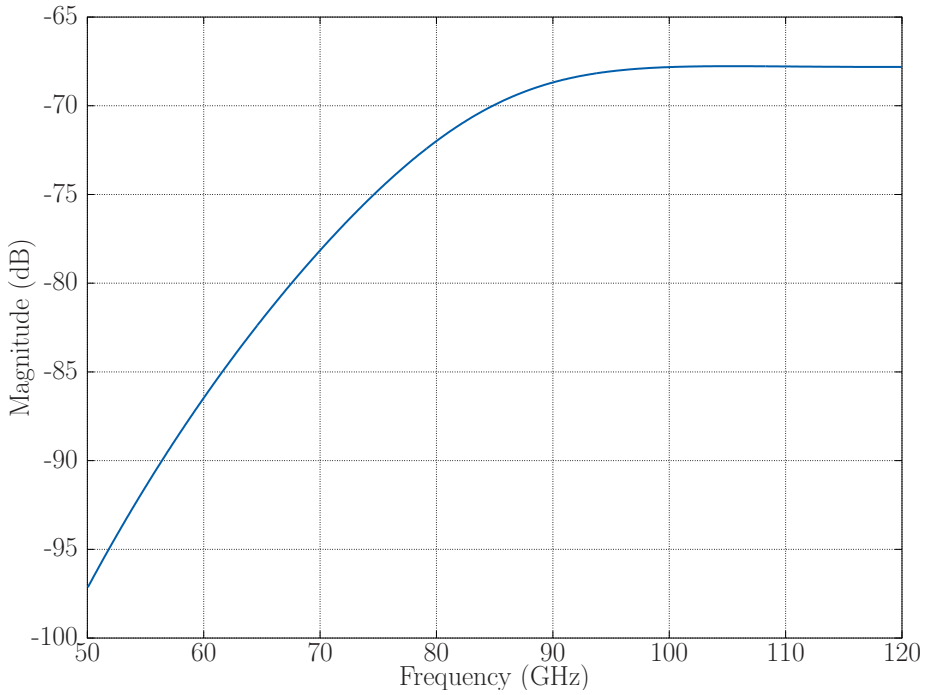

Figure 5.8: Reverse isolation (S_{12}).

Miller capacitance and improve the output-input signal leakage. In order to avoid high levels of stress in the cascode transistors, reductions in size going from 10% to 50% were simulated in both input and output stage, which meant that the transistors size will be down to half the size for DC-operation. This is standard procedure in high frequency design but did not serve as a solution to fix the problem. All performance metrics were seriously degraded, including the quality of the input and output match. What is more, the size of the transformer at the output has to be re-adjusted to accommodate the much smaller parasitic capacitance present at the the collector of the output devices. This lead to a reduction in inner diameter of the output transformer that turned out to be impractical.

The second option involved the optimization of the inter-stage matching network. The strategy to improve the Q-factor of the impedance transformation network was to increase the size of the capacitor. As discussed in Chapter 2, the inductor in the interface is in parallel with a much smaller inductor at the resonant tank of the input stage, thus having a negligible impact. This resulted in a more narrow band behaviour and a better performance at the end. The capacitor value has been selected to fit in a compact layout while maintaining unconditional stability. If die area is not a constraint, the capacitor could be even bigger rendering a stability factor one order of magnitude above of that in Figure 5.4.

The performance achieved by the power amplifier designed for this work is compared with state of the art PAs in Table 5.1.

Ref.	Tech. (nm)	Freq. (GHz)	VDD (V)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE_{max} (%)	Area mm^2	Topology	Power Combiner
[45]	130	77	2.5	22.5	15	-	7.5	-	2-stage cas. CE	Transformer
[24]	130	84	2.5	27	18	16	9	0.68	3-stage diff. CE	4-way
[18]	120	71	2	21	20.1	17.6	11	2.1	5-stage CE	Wilkinson
[17]	180	85	3.3	32	16.6	14.6	11.8	0.51	3-stage cas. CE	Transformer
[38]	180	78	3.2	16.8	14	12.5	-	0.85	2-stage cas. CE	8-way
[46]	180	83.6	2.8	13.4	4.5	-	-	0.27	2-stage cas. CE	Transformer
[47]	120	77	1.8	17	17.5	14.5	12.8	0.60	4-stage CE	T-Line
[37]	180	84	1	12	15.9	13	13.9	-	2-stage CE	Transformer
[48]	130	77	2.5	19	14.5	12	15.7	0.11	1 cas + 2 CE	T-Line
This work	180	83.5	3.5	15.7	18	14.1	10.1	0.03*	2-stage cas. CE	Transformer

Table 5.1: SiGe mm-Wave Power Amplifiers Performance Comparison. *The size does not include the pads, only the power amplifier core plus the transformers are accounted for.

Chapter 6
Conclusions

This chapter finalizes the discussion of the work carried out during this thesis. A brief overview of the contributions follows accompanied by a series of recommendations for improvement and research opportunities.

6.1 Contributions

A two-stage power amplifier architecture with on-chip baluns is proposed, consisting in a classical differential pair with cascode devices topology for the active part. The selected topology helps to reduce LO pulling, to achieve higher gain and to mitigate the Miller effect. A direct connection to the up-conversion mixer reduces the losses associated with the extra transformer necessary to perform single-ended to differential conversion at the input of the power amplifier and decreases the waste of power as both quadrature baseband signals are fed to the PA. The inter-stage matching network was realized using a simple L-match with minimum number of components producing a compact layout that minimizes losses.

The use of cascode devices relaxes the limitations in voltage swing imposed by the voltage breakdown of active devices. A larger compression point can be achieved by using resistors instead of inductors for biasing the common emitter devices of the output stage. Modelling the top metal layers as thick conductors and taking into account vertical current flow reduce the insertion loss in on-chip transformers.

A strategic vertical placement of the transistors exchanging positions in the input and output stage guarantees a low parasitic inductance at the ground node of the common emitter amplifier. Shorter interconnects between input and output stage make the design less prone to gain loss at the impedance transformation network. Finally, a symmetric layout about the x-axis facilitates the access to the input and output baluns while minimizing unwanted parasitics.

6.2 Future Work

Although the performance reported is on par with the latest publications, the design can be further improved in several ways:

- The quality of input and output match suffers due to the high impedance transformation ratio product of using a cascode configuration. A different approach than using a simple L-match can be considered.
- The proposed vertical layout facilitates the connection between stages so a direct connection or the use of transmission lines could be explored.
- Although the operating conditions of the transistors could not be considered ideal, the working regime is close to the device breakdown. There is still some margin to push the transistors harder for the sake of achieving better performance.
- The absence of reliable device models for high frequency and high power does not give the designer enough insight into the operating conditions of active devices. For that reason, the creation of accurate models based on parameter extraction from fabricated transistors could effectively help in the design of mm-Wave circuits.
- The same idea could be applied to accurately calculate insertion loss in on-chip transformers. The results for insertion loss presented in this work can be considered too optimistic depending on the models chosen for the metal conductors in EM simulations. A model measured from a fabricated transformer will give the designer more control over the required power and efficiency figures.
- The advances in new and faster integration technologies, the low transistor count on a PA and the use of proven topologies could benefit the research of new ways for power combining towards a much efficient way of delivering power to the load.

Appendix A

Models and Equations

This Appendix describes the analytical models and equations that were used during the design and simulations of the input and output transformers and interstage matching inductors.

Transformer Model

In case of the modelling of the transformer, the differential inductance L_{diff} and differential Q-factor Q_{diff} were calculated for the primary or secondary coil which was center-tapped for biasing of the corresponding stage [49]. The model had at least 3 ports, where the third port was assumed to be connected to the center-tap and was open-circuited. If the simulated geometry happened to have additional ports, they were assumed to be connected to a patterned ground shield and were short-circuited.

The simulations results presented in Chapter 4 include all parasitic elements between the inductor and ground in the computed values for differential inductance and Q-factor. The circuit model used for parameter extraction is shown in the figure below.

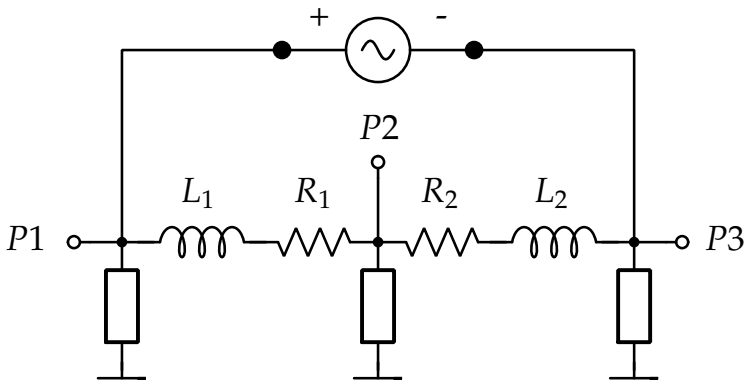

Figure A.1: Three ports circuit model for parameter extraction.

After converting from S-Parameters to Y-Parameters [50] and defining Y as

$$Y = \left(\frac{Y_{13}Y_{13} + 2\,Y_{13}Y_{23} + Y_{23}Y_{23} - Y_{11}Y_{33} - 2\,Y_{12}Y_{33} - Y_{22}Y_{33}}{Y_{33}Y_{12}Y_{12} - 2\,Y_{12}Y_{13}Y_{23} + Y_{22}Y_{13}Y_{13} + Y_{11}Y_{23}Y_{23} - Y_{11}Y_{22}Y_{33}} \right) \tag{A.1}$$

The differential inductance L_{diff} (pH) of the center-tapped primary or secondary is calculated as follows

$$L_{diff} = 10^{12} \cdot \frac{\mathrm{Im}(Y)}{2\pi f_0} \tag{A.2}$$

and consequently, the differential Q-factor Q_{diff} for a center-tapped inductor is defined as

$$Q_{diff} = \left| \frac{\mathrm{Im}(Y)}{\mathrm{Re}(Y)} \right| \tag{A.3}$$

Inductor Model

The inductor of the inter-stage matching network was modelled as a two port network following a π-model as depicted in the figure below:

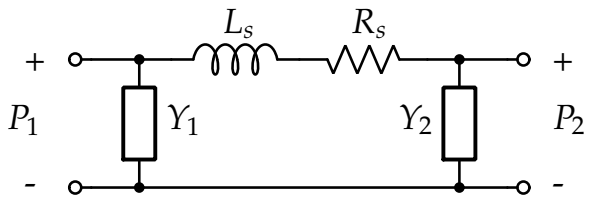

Figure A.2: Two ports circuit model for parameter extraction.

The series inductance L_s corresponds to the results of the calculations where the parasitics to ground Y_1 and Y_2 were not included. The series inductance L_s (pH) is given by

$$L_s = -10^{12} \cdot \frac{\mathrm{Im}\left(\frac{1}{Y_{21}}\right)}{2\pi f_0} \tag{A.4}$$

and the Q-factor for a two port is

$$Q = \left| \frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \right| \tag{A.5}$$

Pad Model

In order to reduce losses to the substrate, a ground shield was realized in the first metal layer, Cu1. The pads were modelled in Momentum and a extracted SPICE model was used for simulations. A simplified schematic of the connection between the output pad and the antenna is shown in Figure A.3. The value of C_c is approximately 50 fF and L_{par} varies from 10 to 20 pH depending on the length of the connection between the output transformer and the pad.

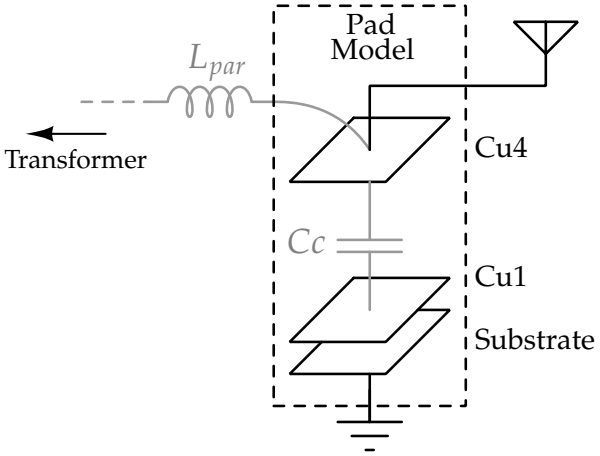

Figure A.3: Simplified SPICE model for the output pad.

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