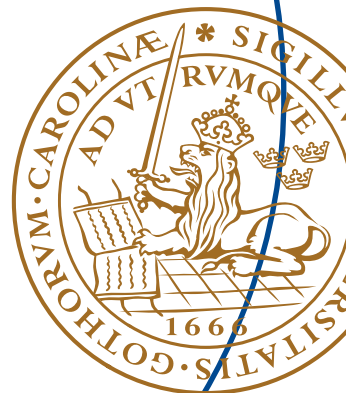


Master's Thesis

A 0.9-V 37- μ W 98-dB DR Inverter-Based $\Delta\Sigma$ Modulator for Hearing Aids

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Abstract

A complete design of a low-voltage, low-power, high dynamic range, switched-capacitor (SC) $\Delta\Sigma$ modulator for hearing aids is presented. A review of state-of-the-art analog to digital converters (ADCs) and a thorough analysis of circuit non-idealities leads to the selection of a third order, single-bit, single-loop modulator. Several different operational transconductance amplifiers (OTAs) are compared, based on multiple performance parameters, resulting in the design of a class-C inverter based OTA. A switched bias scheme allows the OTA to be switched off during half the clock period, lowering power dissipation and $1/f$ noise. Circuit simulations predict 98.7 dB dynamic range (DR) and 78 dB signal to noise and distortion ratio (SNDR) in 10 kHz signal bandwidth for over sampling ratio (OSR) of 256, while consuming total power of $36.6 \mu\text{W}$ at 900 mV.

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Introduction

The audio analog-to-digital converter (ADC) plays a key role in modern hearing aids. It converts the analog audio signal from the microphone to a digital signal which can then be further processed by a digital signal processor (DSP). Since the advent of digital hearing aids in the mid 1990s, the audio ADC has typically limited the input dynamic range (DR) of the system. A preamplifier generally precedes the ADC in order for the ADC to detect the lowest input signals, but during very loud sounds, the ADC will clip, introducing a large amount of distortion. Automatic gain control (AGC) is a commonly used approach to increase the input DR, where it amplifies the signal depending on the signal strength. However, AGC can introduce some unwanted sound artifacts in specific sound environments, such as when listening to music with high DR.

The goal of this project is to design an audio ADC capable of converting the full dynamic range of the microphone and thereby eliminate peak clipping or the need for preamplifiers with AGC. The project shall cover the following points:

- A survey of current state of the art low power audio ADCs
- An architecture study on sigma-delta ($\Delta\Sigma$) ADCs, SAR ADCs and SD-SAR hybrid topologies.
- Transistor level design of a low power audio ADC in a 65nm process fulfilling the specifications listed in section 1.2.

1.1 Hearing Impairment and Hearing Aids

Hearing impairment is one of the leading causes of disability, affecting more than 1.3 billion people or 18.6% of the population worldwide [11], with over 250 million people with significant hearing loss. It is the most frequent sensory deficit in humans, often causing inability to understand speech and associated difficulties with communication and language acquisition. It frequently causes educational and economic disadvantage, and social isolation, especially with childhood onset [12].

There are many different causes of hearing impairment, both external and pathological, but it is most frequently due to aging of the auditory system itself, known as age-related hearing impairment (ARHI) or presbycusis. Typically ARHI is symmetrical, sensorineural and more severe at higher frequencies although ARHI can take many different forms [13]. Approximately 23% of people, aged between 65 and 75, suffer from partial or full loss of hearing. About 40% of people older than 75 years are hearing impaired or deaf [14]. A sensorineural hearing impairment has been shown to be a combination of attenuation and distortion of the sound, resulting in difficulty discriminating speech from noise [15]. Consequently, amplification alone cannot compensate for the problem and the required sounds have to be selectively amplified relative to the background noise.

1.1.1 A Brief History of Hearing Aids

For many centuries a cupped hand behind the ear was the only aid people had to fight hearing loss. In 1800, Frederick Rein of London, began to make ear trumpets, hearing fans and conversation tubes, which “amplified” the sound by collecting and concentrating sound waves [16].

With the invention of the first portable carbon transmitter the first dedicated electrical hearing aid was born, the *akouphone*. Following the invention of the vacuum tube in 1904, sound could be amplified with much greater loudness and clarity, however, the tubes had problems of their own, they were fragile, took time to warm up and got very hot and their high power consumption meant very frequent battery changes. The first commercial vacuum tube hearing aid, manufactured by Western Electric, weighed 220 pounds and cost \$5000. The vacuum tube hearing aids shrunk considerably in size over the next decades and in the 1930s wearable models started to appear [1].



Fig. 1.1: Advertisement from Maico showing the miniaturization of early hearing aids [1].

After World War II there were further advances in circuit miniaturization. In

1947, the first Printed Circuit Board was used in a hearing aid and in 1953 the first all-transistor hearing aids were introduced, the *Micro Transmatic* and the *Maico Transist-ear*. In the following years the transistor hearing aids continued to shrink in size and in 1958 Jack Kilby made the first Integrated Circuit which later found it's first commercial application in hearing aids. In the next 20 years the number of transistors on the ICs grew, however it was not until in the late 1970s that digital ICs were used in hearing aids, as until then they had not been powerful enough to process audio signals in real time [1]. In 1982 the first completely digital hearing aid was developed by the City University of New York. It comprised a minicomputer and a digital array processor and was quite large or as someone put it, "It may be a good hearing aid, but you'll need a friend with a wheelbarrow to carry the instrument" [17]. Digitally assisted hearing aids became commercially available in the 1990s allowing features such as adaptive sound cancellation (Davanox Genius, 1990), speech detection (Siemens PRISMA) and automatic gain control (Oticon Multifocus, 1991) [18]. However, it was not until 1995 that the first true DSP hearing aids were launched, the Oticon DigiFocus and the Widex Senso, paving the way for the future of hearing aids.

Today, invisibility largely remains the design standard for hearing aids, keeping hearing aid design at the forefront of electronics miniaturization. However, still only approximately one in five wears a hearing aid that could benefit from one, a fact attributable to personal preference, device performance, social stigma, and cost [19].

1.2 ADCs for Hearing Aids and Specification Rationale

The human ear is a remarkable device. A healthy individual is capable of detecting sounds from approximately 0 to 138 dB SPL, an astonishing 138 dB dynamic range. This ranges from rustling leaves (10 dB) to a normal conversation (60 dB) to a jet taking off 100 m away (138dB). However, in a hearing aid, the lower end of this scale is typically determined by the noise floor of the microphone, with microphones commonly used in hearing aids having noise floor around 27dB [20, 21, 22] and good quality studio condenser microphones as low as 10 dB [23]. On the top end, short term exposure to sounds above 120 dB can cause hearing damage and people are actually seldom exposed to sounds much above 117 dB [24].

Hearing aids were initially optimized for speech, which is natural considering it is the most important aspect of hearing loss to compensate for. Speech signals only range from 50 dB for soft speech to 90 dB for shouted speech, thus the dynamic range needed to accurately convert those signals is limited to 30-40 dB [25]. However, louder signals, such as a busy highway in the background or a jackhammer in the street, will quickly exceed the speech levels, overloading the converters and not only distorting the jackhammer signal but more importantly the foreground speech. Larger dynamic range is also important at for example sporting events and live concerts, where the sounds can be highly dynamic in nature. The conclusion is that a converter should be able to accurately convert signals from 20 dB to 118 dB, resulting in a 98 dB dynamic range.

Ultimately, the DR is also determined by the microphone, where the typical sensitivity results in 88 dB DR for 900 mV supply [20, 21, 22]. 6 dB are added, to make sure the noise is dominated by the ADC and further 4 dB, to account for variability in sensitivity, confirming the 98 dB DR stated before.

The properties of human hearing allow us to detect very faint sounds, but only in a very quiet environment. We can hear a needle drop in a completely noiseless room but not in a rock concert. This implies that the noise level can increase with increasing signal amplitudes thus a peak SNR of 70dB is justified.

The ANSI Specification for Hearing Aids Characteristics standard recommends the total harmonic distortion (THD) of hearing aids to be at a level of 5-10% [26], which translates to -20 to -26 dB. However, -20 dB distortion is in many cases audible and possibly objectionable, while -40dB is most likely undetectable for hearing aid purposes [27]. These values are for the sound output of the device and as such they are governed by the electroacoustic properties of the receiver making it the largest source of distortion. The distortion requirements for the input converter, on the other hand, should be significantly more strict to allow manipulation of the signal by the DSP. A value of -54dB is considered to be safe and realistic value.

The receiver is also the biggest limitation of the frequency range, typically limiting the range to 100 to 6000 Hz [27]. Allowing for some margin, a bandwidth of 10kHz is chosen for the converter.

The supply voltage is limited by the small zinc air batteries typically used in hearing aids. The voltage varies with discharge from 1.3 V to 1.1 V. To allow room for filtering and regulation, the supply range is set to 900 - 950 mV, with 800 mV minimum in case the supply is used as an ADC reference voltage. The input referred PSRR is also determined by the microphone, which typically ranges from 10 dB to 40 dB [20, 21, 22].

Table 1.1 summarizes all the specifications for the hearing aid ADC.

Table 1.1: Proposed specifications for the ADC.

Parameter	Min	Typ	Max	Unit
Supply voltage	900		950	mV
Operating temperature	0		50	°C
Supply current			50	uA
Dynamic range	98			dB
Peak signal to noise ratio	70			dB
Signal bandwidth		10		kHz
THD			-54	dB
Input signal range	0		vdd	V
PSRR	40			dB
Area			0.1	mm ²

1.3 Report Outline

Following this introduction, Chapter 2 will review different ADC architectures, look at state-of-the-art ADCs and conclude with a selection of the most suitable architecture for the application. Chapter 3 introduces the $\Delta\Sigma$ ADC, covering theory and practical aspects of implementing such a converter. Chapter 4 covers noise analysis relevant for $\Delta\Sigma$ ADCs and Chapter 5 presents the design of the converter. Finally, the results of transistor-level simulations are presented in Chapter 6.

Analog-to-Digital Converter Architectures

A vast array of different analog-to-digital (A/D) converter architectures exist, some excel at very high conversion rates, with high power consumption and medium accuracy, while others are more suitable for high accuracy at low conversion rates. Understanding and selecting which architecture to use for a given application can be a difficult and daunting task. However, with the aid of some basic understanding of the different architectures, along with a good overview of the state-of-the-art converters, we will select a suitable architecture to achieve the performance specifications stated in Chapter 1.

2.1 Introduction to Different Types of A/D Converters

A/D converters can be classified into two main groups:

Nyquist-rate converters can be loosely defined as converters having output values that have one-to-one correspondence with a single input value. In theory, they can sample at the Nyquist rate, however due to practical limits of the anti-aliasing filters they usually sample at 3 to 20 times the input signal's bandwidth [28].

Oversampling converters operate much faster than the Nyquist rate, typically from 20 to 512 times faster, and improve the signal-to-noise ratio (SNR) by removing the quantization noise outside the signal bandwidth with a simple digital filter¹. *Noise shaping* can then be used to further reduce the quantization noise level in the signal band. Fig. 2.1 illustrates the different noise spectrum of Nyquist-rate (a) and oversampling converters (b), along with noise shaping (c).

¹This applies to A/D converters, but D/A converters would filter out the quantization noise with an analog filter.

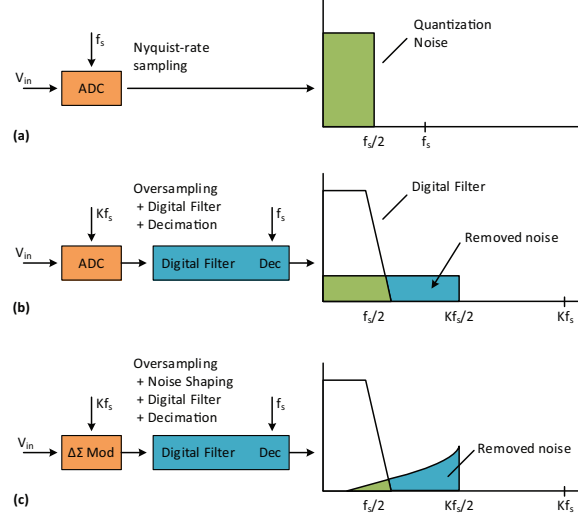


Fig. 2.1: Comparison of Nyquist-rate (a), oversampling (b) and oversampling with noise shaping (c).

Nyquist-rate converters include many different converter architectures, of which the flash, pipeline, successive-approximation-register (SAR) and folding architectures are the most popular[2, 29].

The *full-flash* converter (Fig. 2.2(a)) is perhaps the simplest converter architecture, where the input signal is fed to 2^{n-1} comparators, each of which has its own reference level (i.e. from a thermometric voltage divider) which is then compared to the input signal. The name comes from the fact that all the comparators operate in parallel and produce the results quickly, like a flash, in only one period. The thermometric code from the comparators can then be decoded to produce an n -bit digital output. The accuracy of the flash converter is limited by the resistive divider that needs very low unity resistance for high-resolution and high-speed and thus requires a very low output impedance reference buffer. Additionally, the circuit complexity increase exponentially with the number of bits which results in exponential increase in power consumption[30].

The *successive approximation* converter (Fig. 2.2(b)) performs an iterative search over multiple clock cycles where previous bits are used to determine the next bit. In each clock cycle the input signal is compared to a reference voltage generated from a DAC controlled by the successive approximation register (SAR) and the result of the comparison is used to further adjust the DAC reference voltage for the next conversion. SAR converters are generally very power efficient but slow, due to the multiple clock cycles required for a single conversion and the RC time constant of the capacitor array and switch resistance. The accuracy is limited to the on-chip matching of elements which is typically on the order of 0.1% and thus, without some sort of calibration, the SAR converters are limited to 10 bits [30, 10].

In a *pipeline* converter (Fig. 2.2(c)) the conversion is performed using a cascade of stages, where each stage performs a part of an iterative search. The iterative

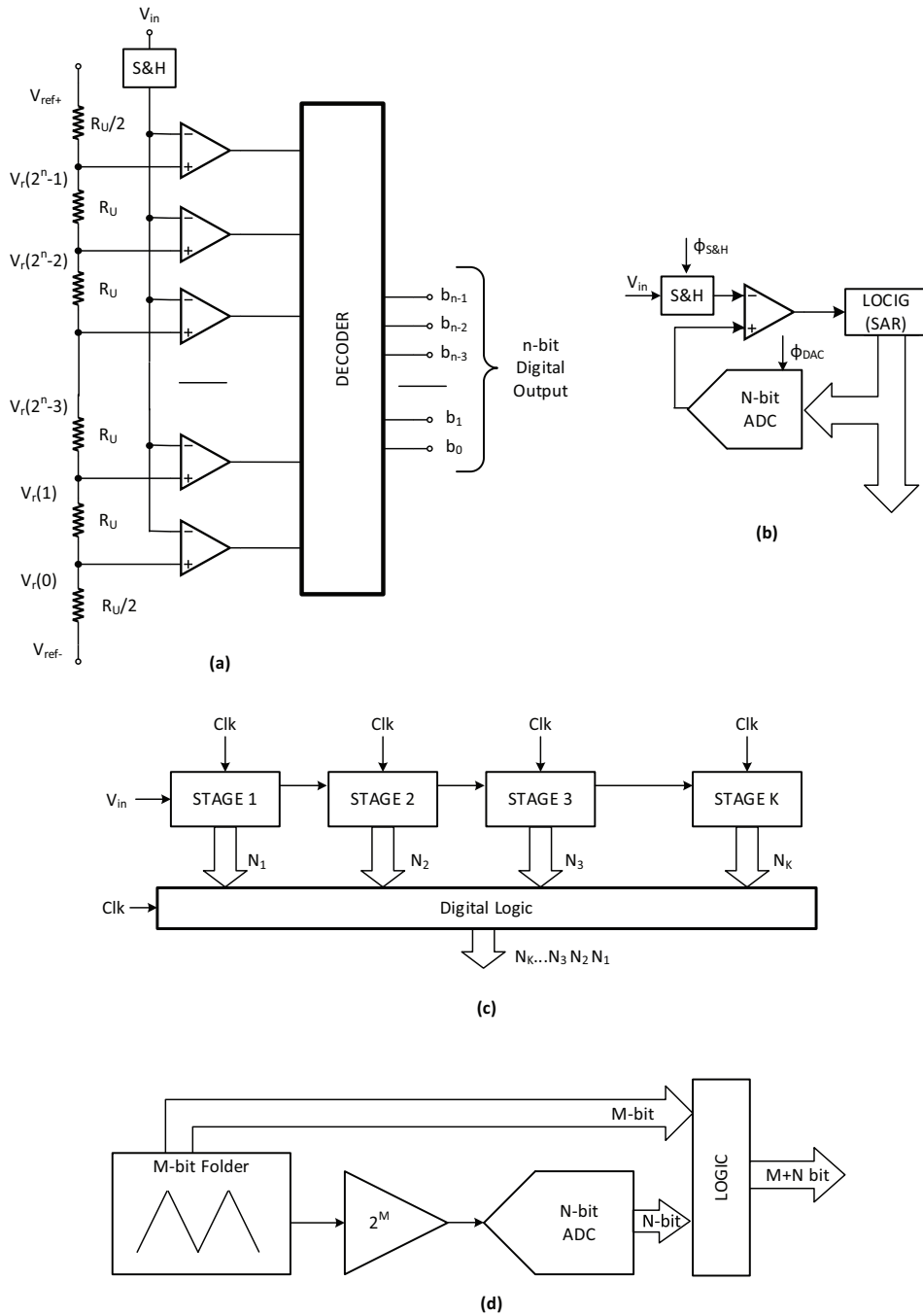


Fig. 2.2: A block diagram of a simple n-bit Full-Flash A/D converter (a), SAR converter (b), pipeline converter (c) and folding converter (d).

search is similar to the SAR except that the stages are unwound in space not in time. A result is generated in each clock cycle but the converter needs several clock cycles to process one conversion thus there is a latency time that increases with the number of bits. Each stage can be a single-bit or a multi-bit stage, depending on design tradeoffs. The accuracy requirements and the design difficulties are greatest for the S&H and first stages and they limit the overall performance of the converter [30, 10].

In a *folding* converter (Fig. 2.2(d)), the input signal is split into a number of sectors by means of a non-linear transformation called folding, which results in a linear response within each sector with alternate positive and negative equal slopes. The purpose of the folding is to reduce the number of comparators needed to quantize the signal, i.e. an M-bit folder only needs to use $2^{n-M} - 1$ comparators to complete an n-bit conversion. The folder also needs to know the segment number of the input to determine the most significant bits [30].

From this very basic overview of some of the most popular converter architectures we can see that not all architectures are equal in terms of speed and accuracy. Table 2.1 summarizes the typical performance categories that these converters are used in. More information on these different architectures can be found in some of the excellent textbooks on the subject [10, 30, 31].

Table 2.1: A/D converter architectures can be roughly categorized after performance, although the boundaries are unclear [10].

Low-to-Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-to- Medium Accuracy
Integrating	SAR	Flash
Oversampling	Algorithmic	Two-step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

2.2 State-of-the-art ADCs and Suitable Architectures

To further understand the potential of each converter architecture, it is beneficial to review recent publications and compare performance characteristics. Reading through the thousands of papers published on ADCs in the last 10 years would be a large undertaking, but fortunately there exist a number of different A/D converter review papers. Walden's widely cited paper from 1999 [32] is getting quite old and was published just before a large leap in performance of ADCs so is therefore perhaps of least use. Bin Le et al. [29] reviewed nearly 1000 commercial ADCs in 2005 and in 2011 Jose de la Rosa [33] published a paper specifically reviewing $\Delta\Sigma$ Modulators but also comparing them to Nyquist-rate converters. Perhaps the best source of information is the excellent paper by Boris Murmann, published in 2008 [34], and its accompanying and continuously updated on-line spreadsheet

[2], where he has collected data from designs presented at the IEEE International Solid-State Circuits Conference (ISSCC) and the VLSI Circuit Symposium from the last 17 years.

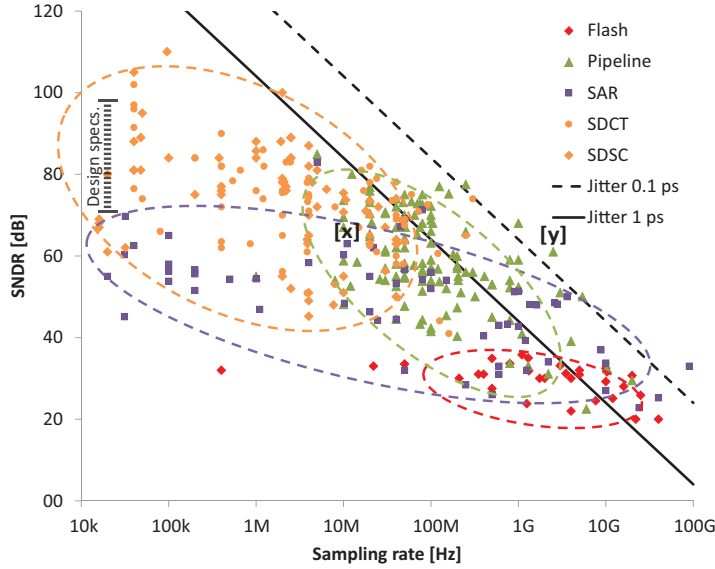


Fig. 2.3: SNDR versus conversion bandwidth of the most popular ADC architectures based on data from Murmann [2].

There are many ways to compare ADC architectures, but it is good to start out by looking at accuracy (here signal-to-noise-and-distortion-ratio (SNDR) is used for accuracy) versus conversion bandwidth. Fig. 2.3 shows four of the most popular ADC architectures, based on the data from Murmann [2]. The data matches quite well to that previously reported by Bin Le [29] and de la Rosa [33], although the SAR group is even more spread out in frequency, covering the entire range from 10k up to almost 100G. This is perhaps not surprising as there has been a significant increase in the interest in SAR ADCs over the last ten years (Fig. 2.4), which has pushed out the operation boundary of the SAR. Furthermore, performance has been increasing at a remarkable rate, with aperture uncertainty decreasing from $1ps_{rms}$ jitter², which was state-of-the art in 2007, to below $0.1ps_{rms}$. From Fig. 2.3 alone, it is clear that the $\Delta\Sigma$ ADC dominates the high-accuracy region and it seems that for SNDR above 85dB it is the only choice.

²The jitter limit is based on an ideal sampler with sinusoidal input and the sampling jitter specified [34]

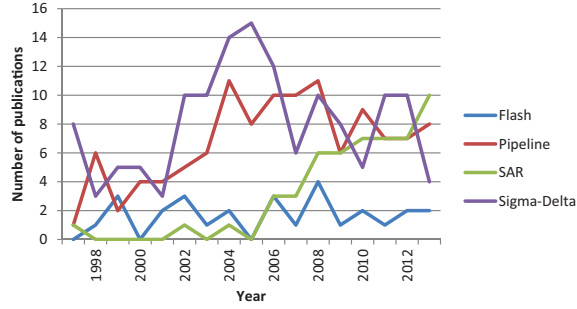


Fig. 2.4: Trends in published papers from 1997 to 2013 [2].

Power consumption is another very important parameter, and one that has been increasingly under optimization. Fig. 2.5 plots the accuracy versus the energy per Nyquist sample, for the same data set as before. The plot purposely avoids normalizing the energy per number of quantization steps, as done in the commonly used figure-of-merits (FOM), as it can be misleading when comparing a large range of architectures [35]. Instead, included in the plot are lines based on two figure-of-merits: Walden's FOM (FOMW) is a commonly used FOM, which normalizes by the number of quantization steps which assumes that doubling the precision would double the power [32]

$$FOMW = \frac{P}{2f_{bw}2^{ENOB}} \quad (2.1)$$

where

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02} \quad (2.2)$$

Schreier's FOM assumes that thermal noise sets the power requirements for ADCs and as such the power will quadruple for 6dB increase in precision. Schreier originally defined the FOM based on dynamic range (DR) [36], but it has become more common to include distortion [2], which leads to

$$FOMS = SNDR + 10 * \log\left(\frac{f_{bw}}{P}\right) \quad (2.3)$$

It is quite clear from Fig. 2.5 that FOMS is a much better metric for medium to high-resolution designs ($SNDR > 50dB$) which implies that they are in fact limited by thermal noise. However, the low-resolution designs do not follow this trend, as they are likely to have other limitations such as speed. This applies especially to the group of flash converters, where they are rather pushing the jitter boundary in Fig. 2.3. A remarkable increase in power efficiency can also be seen in Fig. 2.5, where $FOMS = 160dB$ was state of the art in 2008 but now multiple designs exceed $FOMS = 170dB$.

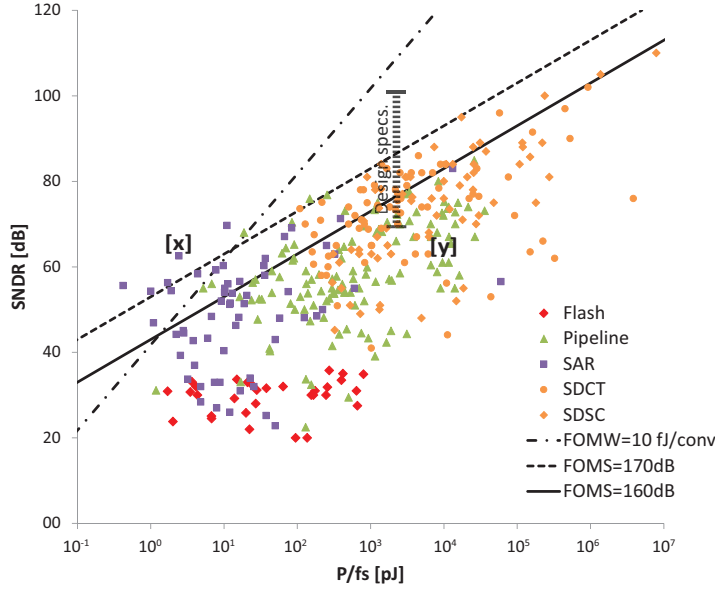


Fig. 2.5: SNDR versus power efficiency of the most popular ADC architectures [2].

It is also interesting to note that there are very few, if any, designs that measure well on both Fig. 2.3 and 2.5. Design [x], marked in Fig. 2.3 and 2.5, achieves one of the best power efficiencies but has only mediocre bandwidth performance where as the opposite is true of design [y], which shows excellent bandwidth performance but quite poor power efficiency. These examples confirm that designing close to the speed limits of a given technology will affect power consumption. There does not seem to exist a single-number figure of merit that captures this tradeoff for all resolutions and architectures [34].

A well known challenge is to design ADCs (and other analog circuits for that matter) with modern technologies and reduced voltage headroom since lower supply voltage mean lower absolute noise in order to maintain the same SNR. This limitation is much more significant in high-resolution designs where power efficiency is limited by thermal noise compared to low resolution designs, where it is at least partially limited by underlying technology. Murmann [34] found that for designs with $\text{SNDR} > 75\text{dB}$ the P/f_s halved only every 5.4 years while for designs with $\text{SNDR} < 75\text{dB}$ P/f_s halved every 1.6 years. Since it is much more difficult to attain high SNDR at low supply voltages, most recent designs in sub-90nm technologies are low to medium-resolution designs as Fig. 2.6 shows.

High-resolution designs still get some benefit from the shrinking technologies, however they have to be applied indirectly. By utilizing the increasing transit frequency (f_T) of the active devices, high transconductance-to-current ratios (g_m/I_D) can be obtained by biasing the devices in moderate or weak inversion. This can be further exploited by using high oversampling ratios, as g_m/I_D no longer improves beyond a certain minimum bias, and thus it is counter productive

to target transistors f_T below a certain value, implying that there is a minimum sampling rate for the best power efficiency in SC circuits [34]. Additionally, digitally assistive logic, used for calibration and/or error correction, becomes cheaper with shrinking technologies and with high-accuracy converters the energy of each conversion equals switching millions of logic gates, therefore allowing considerable digital logic to be added without significant power penalty. Finally, minimalistic designs have also proved to minimize power consumption. This is especially true for SC circuits that traditionally rely on class-A op-amps, where the charge transfer is very inefficient due to the fixed bias current [34].

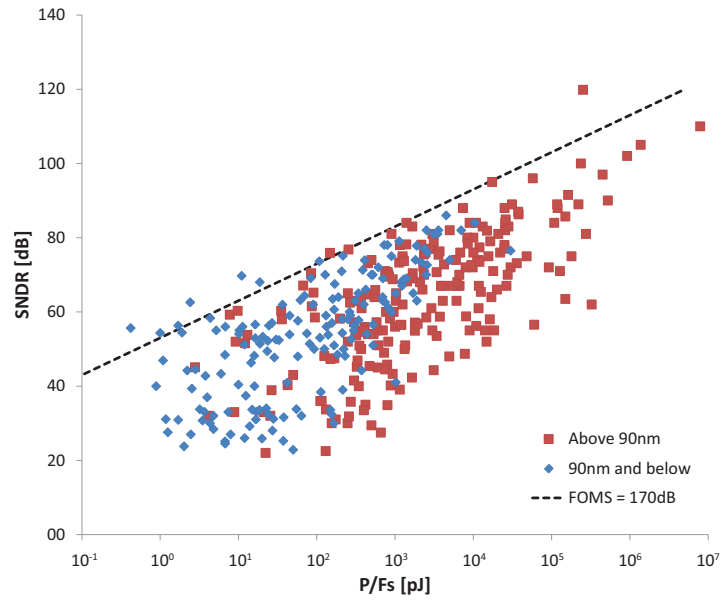


Fig. 2.6: Accuracy versus power efficiency of ADCs designed in 90nm CMOS and below [2].

From the previous discussion it is clear that the most obvious way to meet the accuracy and bandwidth requirements is to use a $\Delta\Sigma$ modulator. To meet the power requirements, a combination of minimalistic design eliminating class-A amplifiers, a relatively high oversampling ratio and perhaps some additional assistive digital logic should be considered. The FOMS for published high-resolution $\Delta\Sigma$ modulators are plotted versus bandwidth in Fig. 2.7. Switched capacitor modulators show the best performance while their continuous time counterparts seem more suitable for wide-band converters. The highest ranking design uses an 18-level quantizer through the use of an analog switch matrix, a digital deserializer and a single comparator [37]. Several designs, [38, 39, 40], use inverter based integrators with very good results while [41] achieves very good performance with amplifiers with inverter output stage, double sampling and 1.5 bit quantizer. A multi-bit SAR quantizer is used with standard telescopic cascode op-amps in [42] while [43] uses single stage class-AB amplifiers. An interesting tradeoff be-

tween dynamic range and SNDR is used by [44] and [45] using non-linear DAC or quantizer respectively, which we will investigate further in the subsequent chapter.

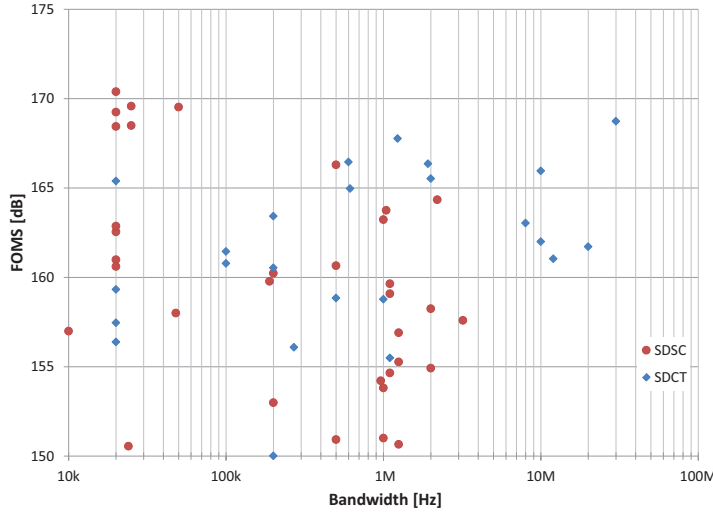


Fig. 2.7: Schreier's FOM for published $\Delta\Sigma$ modulators versus bandwidth [2].

2.3 Non-linear ADCs and DR/SNR Tradeoff

The large dynamic range (DR), but relatively low SNR requirements of this particular application, opens up interesting possibilities not commonly used for traditional data converters. Compression techniques, such as the widely used logarithmic μ -law compression, have been used for a long time in telecommunication [46] as well as being proposed to be very suitable for low-power hearing aid applications [47].

Francesconi and Maloberti proposed a low power logarithmic A/D converter [48] where the DR and SNR could be set independently. The number of bits in the exponent controlled the dynamic range ($DR \approx 20 \log 2^{2^n}$) while the number of bits in the mantissa determined the number of discrete levels in each octave, thereby setting the signal to noise ratio ($SNR \approx 20 \log 2^{m-1}$). Using this architecture it is possible to get very high DR with moderate SNR, see Fig 2.8.

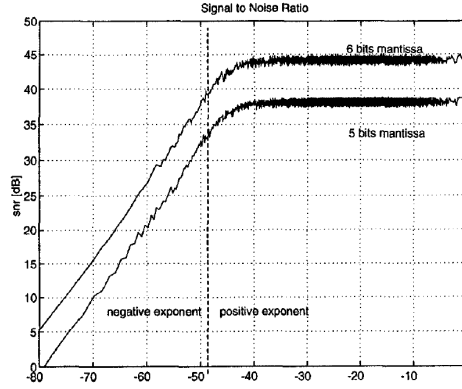


Fig. 2.8: Simulated SNR of a logarithmic converter with 3 bit exponent and 5 and 6 bit mantissa (taken from [3]).

Zhang and Temes [3] suggest a $\Delta\Sigma$ modulator with a multi-bit exponential quantizer and a corresponding logarithmic DAC. They show that this non-uniformly quantized modulator can achieve much higher dynamic range for the same SNR compared to uniformly quantized modulators. The same concept has been used in [45], in which a 3rd order modulator with 3-bit non-uniform quantizer achieves 76-dB peak SNR and 110-dB dynamic range. An interesting logarithmic pipelined converter is described by Lee et al. [49], which achieves 80 dB DR and only 36 dB SNDR.

These examples show that there is potential to trade SNR for increased dynamic range, however the noise in the input stage will always set a fundamental limit to the minimum signal that can be detected. For the remainder of this thesis we will focus on traditional converter design and leave the non-linear quantization as a possible future enhancement.

2.4 Validation of the Proposed Specifications

As a confirmation that the proposed design specifications, presented in Table 1.1, are neither too conservative nor impossible, it is good to analyze how they compare to the state-of-the-art previously covered. The approximate range of the specifications has been plotted in Fig. 2.3 and 2.5, marked as “Design spec”. Fig. 2.5 shows that the specifications are close to the state-of-the-art, but within achievable limits, especially if the low distortion requirements can be utilized to reduce power dissipation. As expected with the high DR requirements, the design does not target very high speeds (Fig. 2.3), further confirming that the specifications proposed are reasonable.

Delta-Sigma ADCs

In 1954 C.C. Cutler, of Bell Telephone Labs in the U.S., filed an important patent on a new type of *pulse code modulation* (PCM) transmission system [50]. The invention was an extension to a modulation system called *differential* PCM, invented four years earlier [51], and covered essentially the same concept as the *delta modulation* scheme, invented at the ITT Laboratories in France in 1946 [52]. The aim of these inventions was not to design Nyquist ADCs, but rather to achieve higher efficiencies in data transmissions. However, Cutler's design encompassed all the concepts of a delta-sigma ($\Delta\Sigma$) converter, apart from the *digital filtering* and *decimation*, which was not possible (or at least feasible) to implement in the vacuum tube technology of that time. As transistors started to replace the vacuum tubes, the design could be expanded, and in 1962, Inose, Yasuda and Murakami published the first paper on a single-bit, first and second order $\Delta\Sigma$ modulator [53], coining the term delta-sigma to describe the architecture. The first actual ADC using the $\Delta\Sigma$ modulator was not published until 1969 by D. J. Goodman at Bell Labs [54], which included a digital filter and a decimator following the modulator. The $\Delta\Sigma$ modulator architecture stands as one of the most successful architectures for high resolution converters and since its early days it has seen continuous improvements on both architectural and circuit level. It has proven to be excellent choice for modern VLSI technology, especially fine-linewidth CMOS, with its fast and inexpensive digital logic [55, 56].

Following this brief history lesson we will introduce the basic operating principles of $\Delta\Sigma$ modulators, review some simple models that can be use to get a qualitative understanding of the system and finally introduce the design methodology and select a suitable modulator architecture.

3.1 Fundamental Principles

The function of $\Delta\Sigma$ modulators depend on two signal processing techniques, *over-sampling* and noise filtering and feedback, commonly referred to as *noise shaping* [33]. A $\Delta\Sigma$ modulator based ADC comprises the same fundamental operations as any other ADC, namely anti-aliasing filter (AAF), sampling and quantizing with the addition of output decimation, see Fig. 3.1. First the AAF ensures that the signal is sufficiently band-limited to avoid aliasing, next the sampling action dis-

cretizes the analog signal in the time domain and finally the quantizer discretizes the signal in amplitude, which in turn can be represented by a digital word [4].

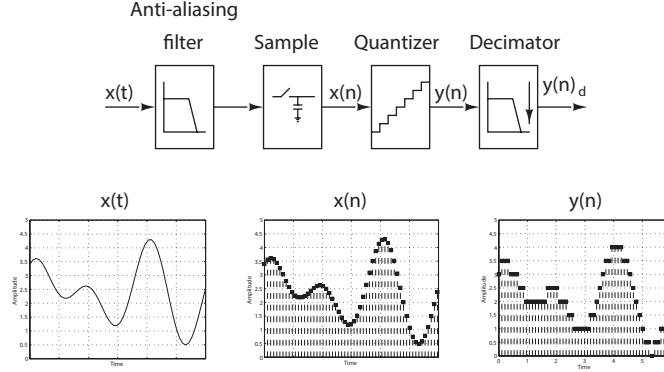


Fig. 3.1: The fundamental process of converting an analog signal to a digital representation. The decimator only applies for an oversampled converter (based on figures from [4]).

For busy (i.e. quickly and randomly changing) input signals, the error e caused by the quantization can be approximated with white noise of mean squared (MS) value of

$$\overline{e^2} = \frac{\Delta^2}{12} \quad (3.1)$$

where Δ is the quantization step. As this is white noise with a flat spectrum spread over the entire band, the single sided noise power spectral density (PSD) of this quantization noise is

$$S_e(f) = \frac{\Delta^2}{6f_s} \quad (3.2)$$

3.1.1 Oversampling

The minimum rate at which a signal with bandwidth f_{bw} can be sampled without information loss is known as the Nyquist rate and is defined as $f_{nyq} = 2f_{bw}$. If a signal is sampled at a frequency $f_s > f_{nyq}$ then it is known as oversampling and the oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{2f_{bw}} \quad (3.3)$$

A digital filter can then be used to remove the out of band noise and the remaining quantization noise power becomes

$$\overline{q_n^2} = \int_{-f_{bw}}^{f_{bw}} S_e(f) df = \frac{\Delta^2}{12} \left(\frac{1}{OSR} \right) \quad (3.4)$$

Compared to (3.1), the noise is reduced by a factor of $1/OSR$ when using oversampling, increasing the accuracy by half a bit per doubling of the sampling frequency. Furthermore, the oversampling reduces the requirements of the AAF as it does not have to be nearly as sharp. However, this decrease in quantization noise comes at the cost of increased sampling rate (or decreased signal bandwidth) and thus we have effectively traded speed for accuracy. This ability, to trade speed for accuracy, is especially important when realizing high resolution converters at low supply voltages. Compared to a traditional Nyquist approach to data conversion, where resolutions above 13 bits require trimming to achieve sufficient component matching, the oversampling converters offer greatly relaxed analog requirements and often much higher efficiencies can be achieved [57].

The oversampling has an even more important implication, as it allows both filtering of signal and noise, since the signal occupies only a small portion of the total frequency range. This opens up the possibility to suppress the quantization noise energy in the signal band and thus greatly increase the in-band SNR. This suppression of in-band noise is commonly called noise shaping [36].

3.1.2 Noise shaping

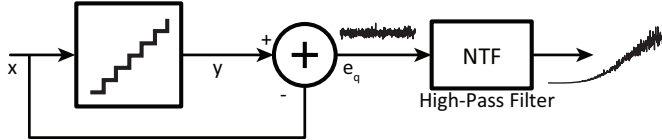


Fig. 3.2: Illustration of quantization noise shaping.

Filtering the quantization noise is a powerful tool to further increase the accuracy of the digital-to-analog conversion. Conceptually, noise shaping can be viewed as high-pass filtering the total in-band noise while leaving the signal unaltered (Fig. 3.2). The transfer function of this filter is usually called the noise transfer function (NTF) and commonly implemented using a maximally flat high-pass filter function, whose transfer function in the z -domain is

$$NTF(z) = (1 + z^{-1})^L \quad (3.5)$$

where L is the order of the filter [33].

The NTF in the frequency domain, after z is replaced by $e^{j2\pi f/f_s}$ is simply

$$NTF(f) = (1 + e^{-j2\pi f/f_s})^L = 2\sin(\pi f/f_s) \quad (3.6)$$

Observing that $f_s = 2 \cdot OSR \cdot f_{bw}$, and assuming $OSR \gg 1$ and as previously stated that the quantization noise can be modeled as having flat PSD, the in-band filtered MS noise power is approximately given by

$$\overline{q_n^2} = \int_{-f_{bw}}^{f_{bw}} \frac{\Delta^2}{12f_s} |NTF(f)|^2 df = \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \quad (3.7)$$

In contrast to only oversampling, as in (3.4), when additionally employing noise shaping, the in-band quantization noise further decreases by around $6L$ dB/octave with OSR [33].

Shaping the noise in this way might be quite intuitive but the questions becomes how to distinguish the signal from the noise to be filtered and this is exactly what $\Delta\Sigma$ modulators cleverly do.

3.2 Delta-Sigma Modulators and the Linear Model

An ADC, which employs both oversampling and noise shaping by using a filter embedded in a feedback loop (called a loop filter) as illustrated in Fig. 3.3(a). The feedback loop contains (typically a low resolution) internal quantizer and DAC, and the loop filter is in this case an integrator. Due to the quantizing effect of the internal ADC the system is non-linear and due to the memory in the integrator it is also dynamic, hence its complete mathematical analysis are complex. However, a simple linear model (Fig. 3.3(b)) can be used to gain qualitative understanding of its operation [36].

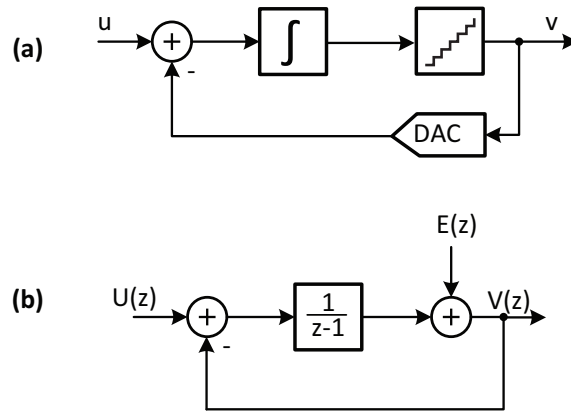


Fig. 3.3: A conceptual block diagram of a first order $\Delta\Sigma$ modulator(a) and its linear z-domain model (b).

As the gain of the integrator is large inside the signal band and small outside, we can intuitively see that due to the action of the feedback, the input signal, u ,

and the analog version of the output, v , will nearly coincide (and thus subtract) within the signal band. Therefore most of the difference between the signals will be placed at higher frequencies resulting in shaped quantization noise. Analysis of the linear model shows that the (digital) output signal at time n is

$$v(n) = u(n-1) + e(n) - e(n-1) \quad (3.8)$$

which shows that the output v contains a delayed replica of the input signal and a differentiated quantization error e . This differentiation suppresses the error at frequencies which are small compared to the sampling rate f_s which leads to the noise shaping and confirming the previous observation.

The model of Fig. 3.3(b) can be generalized by expressing the output of the modulator as

$$V(z) = STF(z)U(z) + NTF(z)E(z) \quad (3.9)$$

where STF is the signal transfer function and NTF is the noise transfer function which can be calculated as

$$STF = \frac{H(z)}{1 + H(z)} \quad (3.10)$$

$$NTF = \frac{1}{1 + H(z)} \quad (3.11)$$

where $H(z)$ is the transfer function of the loop filter, which for the integrator is given by

$$H(z) = \frac{1}{z-1} \quad (3.12)$$

Again, we can see the effective noise shaping by looking at the STF and NTF when the loop filter is designed to have a large gain within the signal band, that is when $|H(f)| \rightarrow \infty$ within the signal band, then $|STF(f)| \rightarrow 1$ and $|NTF(f)| \rightarrow 0$. In practice the error can never be canceled completely due to the finite gain of the filter [33, 4].

The signal-to-noise ratio (SNR) and dynamic range (DR) for a sine wave input signal of amplitude A_u are given by

$$SNR = \frac{A_u^2}{2q_n^2} \quad DR = \frac{(U_{FS}/2)^2}{2q_n^2} \quad (3.13)$$

where U_{FS} is the full-scale input signal. Inserting the expression for the quantization noise power in (3.7) we get

$$DR|_{dB} = 10 \log \left[\frac{3(2^B - 1)^2 (2L + 1) OSR^{2L+1}}{2\pi^{2L}} \right] \quad (3.14)$$

where B is the number of bits in the quantizer and L is the order of the loop filter [33]. From this we can see that by combining oversampling (OSR) and noise shaping (L), high dynamic range can be achieved with low number of bits in the internal quantizer (B). It is very important to note, however, that this does not include reductions in DR caused by stability issues in higher order loop filters, which for single bit 5th order modulators can be on the order of 60 dB [36]. It is beneficial to summarize the possible (nonexclusive) ways, and the associated drawbacks, to increase DR:

Increasing L , the order of the modulator. Using a first order modulator only ($L=1$) implies using very high OSR to achieve moderately high effective resolution as DR increases with OSR only at 1.5 dB/octave. Moreover, first-order modulators suffer from idle-tones due to the quantization noise being correlated to the input signal. Using a 2nd order filter reduces the correlation of the noise enough so that the tones disappear and furthermore, the DR increases with OSR at 2.5 dB/octave. Further increasing the order increases the DR according to (3.14) but as mentioned before, for $L>2$ stability problems start to limit performance. A number of alternate topologies exist to address this problem such as using an IIR NTF, such as the cascade of resonators with distributed feed forward (CRFF) structure [36, 58]. Another widely used topology for higher order modulators is the multi-stage noise shaping (MASH), where two or more modulators are cascaded and their outputs processed together using some form of digital cancellation logic. The problem with the MASH topology is that circuit non-idealities such as mismatch and finite integrator gain causes incomplete error cancellation, referred to as noise leakage [36, 33].

Increasing OSR is an obvious way to increase DR. However, the sampling frequency will always set a limit to the OSR and for wide-band signals this can make large OSR impractical due to the prohibitively high clock rates and associated increase in power consumption [33]. Nevertheless, as technologies have scaled, the device speeds have been increasing making very high clock rates practical as a number of $\Delta\Sigma$ modulators show, which are being designed for signals bandwidths high in the MHz range and sampling frequencies up to 10 GHz [59, 60, 61]. There are also examples of very high OSR , of up to 2000, combined with a GHz range clock [62].

Increasing B , the number of bits in the internal quantizer, increases the DR proportionally. However, this requires a multi-bit feedback DAC which is not inherently linear, resulting in non-linear errors being injected directly at the input of the modulator, degrading performance. There exists a large number of ways to relax the linearity requirements on the multi-bit DACs, of which the dynamic element matching (DEM) is perhaps the most common [55, 63].

3.3 High-level modelling

Relying on the linear model is only useful to gain a qualitative understanding. In order to move on in the design process of $\Delta\Sigma$ modulators it is necessary to utilize a more accurate model.

3.3.1 DS Toolbox for MATLAB

Schreier's open source Delta-Sigma Toolbox for MATLAB [64] is very powerful high-level modelling tool to aid in the design of $\Delta\Sigma$ modulators. The toolbox facilitates the synthesis of noise transfer functions for any combination of OSR and order, with the possibility of adding stability requirements and zero optimization. It allows the simulation of the synthesized NTF using an arbitrary input signal. Furthermore, the SNR can quickly be determined for various amplitude sine waves and finally scaling coefficients can be extracted for common single-loop modulator topologies¹. Additionally, the toolbox can simulate a variety of element selection logic (ESL) for multi bit DACs.

3.4 Effects of Circuit Non-idealities

Finally, the effects of circuit imperfections on the modulator performance will be analyzed. For this we will focus on switched capacitor (SC) circuits.

3.4.1 Integrators

The loop filter is arguably the most critical part of a $\Delta\Sigma$ modulator. As previously discussed, this loop filter is typically implemented using SC integrators, whose ideal transfer function is given by (3.12). However, when implemented using real transistors the circuit deviates from this ideal in several ways, most notably with finite gain and bandwidth and non-linearity.

Finite gain

The ideal integrator, characterized by (3.12) has infinite gain at DC but this is not possible with a real circuit. An integrator is typically implemented with an operational amplifier (op-amp) which has a finite DC gain A , and then the transfer function becomes

$$H_f(z) = \frac{1}{z - p} \quad (3.15)$$

where the pole $p = 1 - 1/A$ is slightly less than 1 and the integrator is said to be *lossy* or *leaky*. We intuitively see that this limited gain at low frequencies causes

¹The toolbox currently supports the following single loop topologies: CIFB, CIFF, CRFB, CRFB, CRFBD and CRFFD. However, multi-loop systems can also be simulated with a little manual work, although not explicitly supported.

reduced attenuation of the quantization noise in the baseband and ergo the loss of overall modulator SNR. For a typical second order modulator, the increase in in-band quantization noise is given by [5]

$$\frac{\Delta \overline{q_n^2}}{\overline{q_n^2}} = \frac{5}{\pi^4} \left(\frac{OSR}{A} \right)^4 + \frac{10}{3\pi^2} \left(\frac{OSR}{A} \right)^2 \quad (3.16)$$

This is shown in Fig. 3.4 along with simulation results and confirm that the penalty is minor when the integrator gain is of the same magnitude as the OSR.

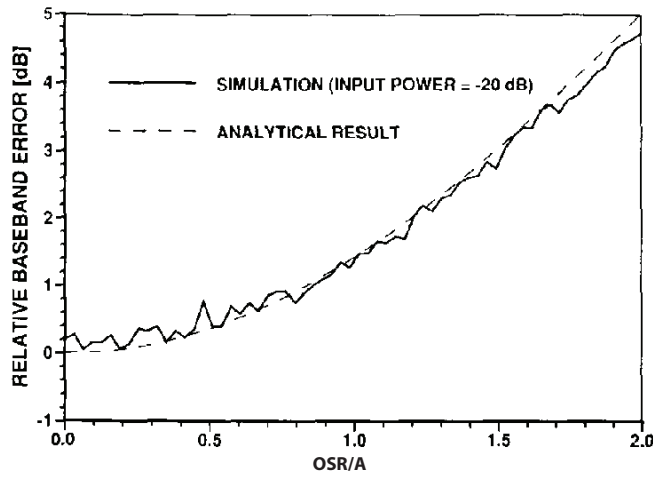


Fig. 3.4: Effect of finite integrator gain on in-band noise [5].

Limited bandwidth

The bandwidth of the integrator controls how fast the signal settles from an impulse on the input. Traditionally, the settling time of SC circuits is chosen so that the signal fully settles to within the application accuracy limits. However, it has been shown that significantly lower bandwidths do not reduce the performance of $\Delta\Sigma$ modulators. For integrators based on amplifiers with a single dominant pole, the settling time constant can be almost equal to the sampling period [5]. However, most designs use somewhat higher bandwidth, commonly five times the sampling frequencies, to account for deviation from ideal exponential settling and other second order effects [38, 39, 40].

Limited slew rate

If the integrator amplifier is slew rate limited, the settling will significantly deviate from the exponential settling outlined earlier. Boser [5] shows that the slew rate needs to be above $1.1\Delta/T$ to avoid a sharp increase in firstly harmonic distortion but also quantization noise.

Non-linearity

Most real circuits are non-linear to some extent. Apart from large signal non-linearities such as slewing and clipping, differential non-linearities, such as due to capacitor voltage dependency or amplifiers with input dependent gain, also need to be considered. These non-idealities generally lead to harmonic distortion. This only applies to the first integrator in higher order modulators as the errors of subsequent integrators are suppressed by the feedback loop [5].

3.4.2 Quantizer and DAC

Any non-linearity, offset or noise of the quantizer is not of large concern as the error is combined with the quantization error and therefore suppressed by the noise shaping. If using a single bit quantizer, hysteresis of up to 10% of the modulator input range will have a minimal effect on performance [65]. However, non-linearity in the DAC is directly applied to the input and thus affects the output error without any shaping. The simplest way to ensure full linearity is to use a single bit quantization and DAC. This makes the input/output characteristics only consist of two points and thus it can be said that it is inherently linear. Using multi-bit quantizers has many advantages such as reduced quantization error (6dB per added bit), better loop stability allowing larger input signals and/or more aggressive NTFs, and relaxed requirements for the amplifiers due to smaller signal changes. There exist a number of methods to solve the problem with a non-linear multi-bit DAC such as dual quantization (MASH), mismatch-shaping and digital error correction [36].

3.4.3 Switches

The switches are typically composed of CMOS transistors, operating as analog switches. The non-linear impedance causes harmonic distortion and the switching causes charge injection and clock feedthrough which can be minimized with correct switching delays [66].

Noise Analysis of Delta-Sigma Modulators

For high performance A/D converters, noise is a critical factor in limiting the performance of the circuits, as it sets a fundamental limit on the minimum signal level that can be processed without significant deterioration in quality. The quantization noise, which is inherently generated when the input signal is quantized, can be controlled with different arrangements of the ADC, such as the over sampling ratio, order of the modulator and number of quantization steps in the quantizer, all of which was discussed in more detail in Chapter 3. However, the *intrinsic* noise generated within the transistors themselves usually poses a much more challenging problem and thus it is important to have a good understanding of the sources of noise and how it affects the performance of a $\Delta\Sigma$ ADC. Additionally, there is also *extrinsic* (interference) noise that typically originates from on-chip digital circuitry, which couples into the sensitive analog stages via the substrate, ground or supply lines [35].

In this chapter, we will begin with a short high-level discussion of noise in analog circuits along with some definitions, followed by a brief overview of the sources of noise in modern MOS transistors. Then we will look at noise in simple switched-capacitor (SC) circuits such as the track and hold and gradually move on to more complex circuits before analyzing a complete $\Delta\Sigma$ modulator.

4.1 Introduction to Analog Noise

Noise is used in engineering to describe a large variety of phenomena that degrade a signal in some way. From an analog (small-signal) perspective it is a time-varying, independent alternating current (ac) source, which can be represented as either a current $i_n(t)$ or a voltage $v_n(t)$, with an average value of zero. The mean-square (MS) value (in units of I_{rms}^2 or V_{rms}^2) or root-mean-square (RMS) value (in units of I_{rms} or V_{rms}) are therefore commonly used to quantify analog noise.

For noise that varies with frequency it is beneficial to look at the noise power spectral density (PSD), which is defined as the ratio of the MS value of spectral components in a narrow bandwidth Δf to the bandwidth or as [67]

$$S_I(f) = \lim_{\Delta f \rightarrow 0} \frac{\overline{i_n^2(t)}}{\Delta f} \quad (4.1)$$

The inverse relationship can also be used to derive the mean-square (MS) noise current from the noise PSD. This is intuitively the sum of the power spectral densities at all frequencies or

$$\overline{i_n^2} = \int_{f_1}^{f_2} S_I(f) df \quad (4.2)$$

A variety of nomenclature is used for discussing analog noise in the literature and for clarification it is listed in Table 4.1.

Table 4.1: Analog noise nomenclature

Name	Symbol (I)	Units	Symbol (V)	Units
Noise signal	$i_n(t)$	A	$v_n(t)$	V
MS noise signal	$\overline{i_n^2(t)}$	A_{rms}^2	$\overline{v_n^2(t)}$	V_{rms}^2
RMS noise signal	$\sqrt{\overline{i_n^2(t)}}$	A_{rms}	$\sqrt{\overline{v_n^2(t)}}$	V_{rms}
Noise PSD	$S_I(f)$	A^2/Hz	$S_V(f)$	V^2/Hz
Root noise PSD	$\sqrt{S_I(f)}$	$A/\sqrt{Hz}$	$\sqrt{S_V(f)}$	$V/\sqrt{Hz}$

4.2 Noise in MOS Transistors

Electrical signals in integrated circuits are corrupted by noise due to small current and voltage fluctuations that are generated within the devices themselves. These fluctuations are fundamentally due to the electrical charge not being continuous, but rather carried in discrete quantities equal to the electron charge [66]. The two most important intrinsic noise sources in modern CMOS are thermal noise and flicker noise.

4.2.1 Thermal noise

Thermal noise is created by the random thermal motion of the electrons in a conductor and is directly proportional to absolute temperature but unaffected by presence or absence of direct current. The power spectral density (PSD) of the voltage noise in a resistor of resistance R is given by

$$S_{v,th}(f) = 4kTR \quad (4.3)$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant and T is the absolute temperature. It is clear that (4.3) is independent of frequency and thus the PSD of thermal noise is flat [66].

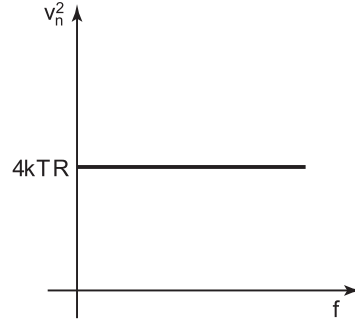


Fig. 4.1: Thermal noise in resistors and transistors has a flat PSD.

Thermal noise in CMOS transistors is due to the resistivity of the channel and for a transistor operating in the triode region (as it does for a conducting switch) the noise is the same as for a resistor where the noise source is in series with the device and R is replaced by R_{on} for the MOSFET. When the MOS transistor operates in the active region, the thermal noise can be modeled with a current source in parallel with the channel where the PSD of the noise current is approximately [35]

$$S_{i,th}(f) = 4kTg_m\gamma \quad (4.4)$$

where g_m is the transconductance of the transistor and γ is the thermal noise coefficient ¹.

In strong inversion the noise is due to *drift thermal noise* but in weak inversion it is due to *diffusion current noise* which is reduced to thermal noise when the charge carriers are in thermal equilibrium with the semiconductor and therefore we can use the same model to describe the thermal noise in strong and weak inversion [68]. For a MOS transistor operating in strong inversion the thermal noise coefficient is approximately 2/3 and in weak inversion it is approximately 1/2 [68, 38], although it can be significantly larger for short channel devices.

It can be convenient to refer the thermal noise back to the gate as a series voltage noise source connected to the gate of the transistor. This can be done by dividing (4.4) by g_m^2 . Thus the thermal voltage noise of a MOS transistor referred back to the gate is

¹A more precise way of expressing the channel thermal noise in MOS transistors is to use the channel conductance g_{do} instead of the transconductance g_m . It should be further noted that this simple noise model is only valid for long channel lengths ($L > 1.6\mu$ m) and for devices with negligible body effect [68]

$$S_{v,th}(f) = \frac{4kT\gamma}{g_m} \quad (4.5)$$

4.2.2 Flicker noise (1/f)

Flicker noise is present in all active devices and some passive elements such as carbon resistors. It is caused by several different mechanisms but most importantly by traps associated with impurities and defects in the crystal structure. The charge carriers are then randomly trapped and released by these traps and the time constant associated with the process gives rise to the low frequency concentrated PSD of the noise, hence it is often called 1/f noise.

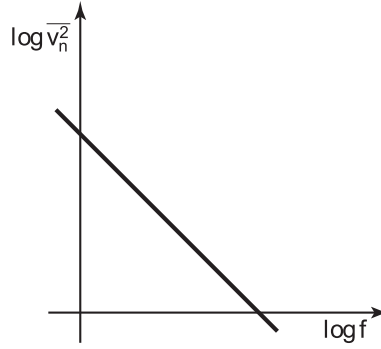


Fig. 4.2: Flicker noise in transistors has a PSD that is inversely proportional to frequency.

Flicker noise is characteristically different from thermal noise and its average power cannot be predicted easily and it varies significantly between CMOS processes. The flicker voltage noise is roughly given by

$$S_{v,f}(f) = \frac{K}{WL} \cdot \frac{1}{f} \quad (4.6)$$

where W and L are the width and length of the channel, f is the frequency and K is a process dependent constant. It should be noted that this is only an approximation and the actual flicker equation is more complex [69].

It becomes immediately obvious that the flicker noise can only be minimized by increasing the overall device size (increasing W and/or L) or using devices with low K . Additionally, clever circuit design techniques such as chopper stabilization can be used to modulate the 1/f noise to frequencies outside the signal band or correlated double sampling can be used to suppress the noise [7]. More in depth discussion on 1/f noise suppression in $\Delta\Sigma$ modulators can be found in Chapter 5.

To determine over what part of the frequency band 1/f noise becomes dominant it is best to plot both noise PSDs on the same axis (Fig. 4.3). The point at

which the $1/f$ noise becomes dominant is known as the *noise corner* and is given by [69]

$$f_C = \frac{K}{WL} \frac{g_m}{4kT\gamma} \quad (4.7)$$

From (4.7), we see that the device dimensions and transconductance largely determine the corner frequency. For submicron transistors, typical values are 500 kHz to 1 MHz [69] but in practice they can extend far outside this range.

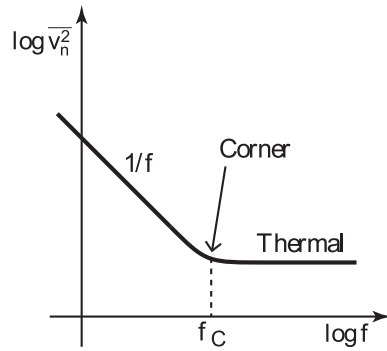


Fig. 4.3: The noise in CMOS circuits is a combination of thermal and flicker noise.

For the remainder of this chapter we will focus on the thermal noise, as it remains the main constraint on how accurately we can process signals in SC circuits.

4.3 Elementary Track and Hold

In the effort to analyze thermal noise in switched capacitor circuits it seems obvious to start looking at the simplest switched capacitor circuit, the elementary track and hold, see Fig. 4.4(a). It consists of a single MOS transistor acting as a switch and a capacitor which tracks the input voltage when the switch is on and holds the end value when the switch is turned off. For this analysis we will represent the transistor with a resistor R (for the on-resistance of the MOSFET) and an ideal switch with infinite off resistance. The only thermal noise source in this circuit is the one associated with the on resistance of the switch and thus we add a voltage noise source in series with the resistance to ground [30], see Fig. 4.4(b). From this we can see that the noise source will disturb the output during the on-time of the switch but during the off-time the output is held constant at the last value before the switch opened, see Fig. 4.4(c). It is clear that the output waveform is a somewhat complex continuous time signal but it can conceptually be split into two orthogonal components, v_t in track phase and v_h in hold phase [70].

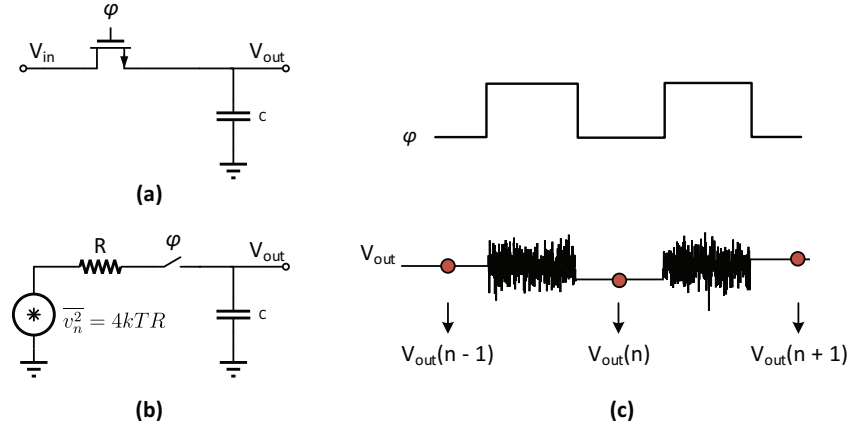


Fig. 4.4: A MOSFET track and hold circuit (a), the equivalent model with a voltage noise source and a noiseless resistor and an ideal switch (b) and the output of the circuit (c).

During the track phase, the output noise consists of a bandlimited white noise, generated by the resistor and filtered by the RC time constant of the capacitor loading the switch. If we first assume that the switch is always closed (now this is a simple continuous time circuit), the output voltage simply becomes low-pass shaped white noise. For the general case of white noise, shaped by the first order transfer function

$$H(s) = \frac{G_0}{1 + s\tau} \quad (4.8)$$

the PSD of the output noise is given by

$$S_{no}(f) = S_{ni} \cdot |H(s)|^2 = 4kTR_{on} \cdot \left| \frac{G_0}{(1 + s\tau)} \right|^2 \quad (4.9)$$

and the mean-square (MS) noise power is then simply the integral over all frequencies, from DC to infinity

$$\overline{v_{no}^2} = \int_0^\infty S_{no}(f) |H(j2\pi f)|^2 df = 4kTR_{on} \cdot \left(\frac{G_0^2}{4\tau} \right) \quad (4.10)$$

For the simple RC filter with $\tau = R_{on}C$ and $G_0 = 1$, the PSD of the output noise in track mode becomes

$$S_{RC}(f) = \frac{4kTR_{on}}{1 + (2\pi f R_{on}C)^2} \quad (4.11)$$

and the mean-square (MS) noise power is then simply

$$\overline{v_{RC}^2} = 4kTR_{on} \cdot \left(\frac{1}{4R_{on}C} \right) = \frac{kT}{C} \quad (4.12)$$

The results of (4.12) is the somewhat famous kT/C and to explain why the total RMS noise is independent of R_{on} , we observe that the noise density over the bandwidth of the RC filter is proportional to R_{on} , but that bandwidth is inversely proportional to R_{on} , simply making the total MS noise independent of R_{on} .

When the switch is cyclically operated with a frequency f_s and with a duty cycle m (the switch is closed for m/f_s and open for $(1-m)/f_s$) the results will be a cyclostationary noise process with time-average PSD and MS noise power are simply scaled by the duty cycle m [6],

$$S_t(f) = \frac{4mkTR_{on}}{1 + (2\pi f R_{on}C)^2} \quad (4.13)$$

$$\overline{v_t^2} = \frac{mkT}{C} \quad (4.14)$$

Moving on to the hold mode, we can see that it is conceptually made out of two steps. Firstly, sampling the input signal at the very end of the track phase; secondly, holding that value for the duration of the hold phase. We will call these two signals v_s and v_h respectively. When the input signal is sampled, it results in aliasing of the switch noise (the sampling frequency f_s is much lower than the bandwidth of the signal, determined by the $R_{on}C$ time constant), with the noise density of (4.11) being replicated at intervals of f_s and summed up to give the noise PSD for the sampled signal [6]

$$\hat{S}_s(f) = \sum_{k=-\infty}^{\infty} \hat{S}_{RC}(f - kf_s) \quad (4.15)$$

It should be noted that a double sided representation of S_s and S_{RC} is used here (denoted by $\hat{S}_s$ and $\hat{S}_{RC}$ respectively) to correctly take aliasing into account. As v_s is a sequence of real numbers with rate f_s , S_s will be periodic with period $1/f_s$ and conjugate symmetric around 0. This means for a single sided transform, everything outside the frequency range of interest, 0 to f_s , is either a repeat, or a repeat of a mirror image. The total noise power density in S_s can be approximated with a rectangular noise density that has the same total power and noise density at low frequencies. The bandwidth of this rectangular noise power density can be called the effective bandwidth, f_{EBW} and from (4.11) and (4.12) we get [6]

$$f_{EBW} = \frac{kT}{C} \frac{1}{4kTR_{on}} = \frac{1}{4R_{on}C} \quad (4.16)$$

Using this approximation the effective noise bandwidth can be split into N rectangles², each of width f_c and height $2kTR_{on}$ ³, see Fig. 4.5, where

$$N = 2 \frac{f_{EBW}}{f_s} = \frac{1}{2R_{on}Cf_s} \quad (4.17)$$

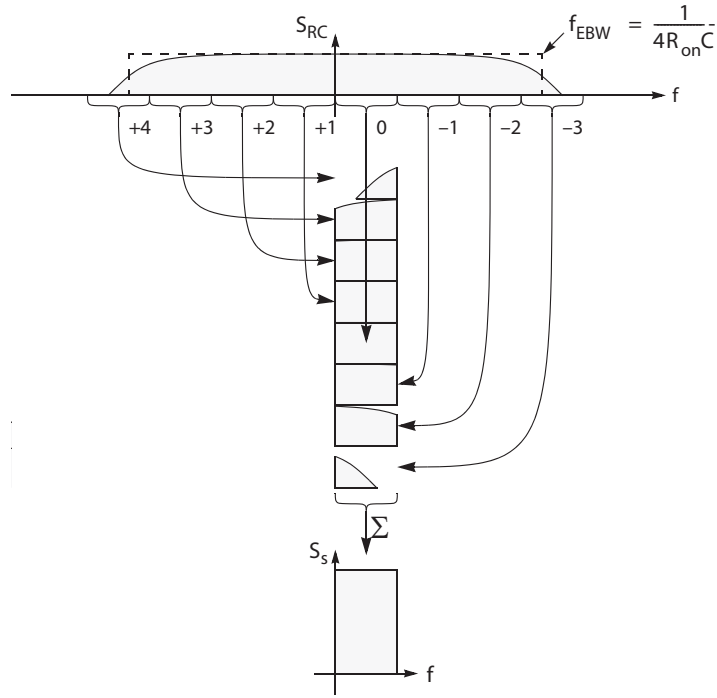


Fig. 4.5: An illustration of the folding of noise due to aliasing in the sampled signal (figure from [6]).

Another way to look at N is how many $R_{on}C$ time constants fit into the Track phase (given that the duty cycle is $1/2$)

$$N = \frac{T_s/2}{\tau} = \frac{1}{2R_{on}Cf_s} \quad (4.18)$$

where $\tau = R_{on}C$ and $T_s = 1/f_s$. From this we can also intuitively see that if N is very large, then we effectively have a white process, where in the time domain there is no correlation from noise sample to noise sample. Alternatively if N is small, then the noise samples would be highly correlated, leading to a shaped PSD [70].

²This approximation holds when $N > 3$ [70]

³Here $2kTR_{on}$ is the double sided representation of (4.11), $4kTR_{on}$

The N rectangles can be combined⁴ by summing their noise powers, resulting in

$$\hat{S}_s(f) \cong \sum_{k=-N/2}^{N/2-1} 2kTR_{on} = (2kTR_{on})N = 2kTR_{on} \frac{1}{2R_{on}Cf_s} = \frac{kT}{Cf_s} \quad (4.19)$$

Using the single sided representation the noise power density of the sampled noise can be written as

$$S_s(f) = 2 \frac{kT}{Cf_s} \quad (4.20)$$

To get the total noise power in the sampled signal v_s , we can integrate over the range of 0 to $f_s/2$ as defined by (4.2)

$$\overline{v_s^2} = \frac{kT}{C} \quad (4.21)$$

This again shows that the total noise power of kT/C is uniformly spread across the range of discrete time frequencies from 0 to $f_s/2$ and that it is independent of the switch resistance.

Now, looking at the hold signal, v_h , and its noise power density we need to account for the effect of the zero-order hold on $S_s(f)$ [6]. This results in

$$S_h(f) = [(1-m)\text{sinc}(f(1-m)T_s)]^2 2 \frac{kT}{Cf_s} \quad (4.22)$$

We can then combine (4.22) with (4.13) to find the total noise power density of both the track and hold phases,

$$S_{th}(f) = S_t(f) + S_h(f) = \frac{4mkTR_{on}}{1 + (2\pi fR_{on}C)^2} + [(1-m)\text{sinc}(f(1-m)T_s)]^2 2 \frac{kT}{Cf_s} \quad (4.23)$$

Finally, the total MS noise of both track and hold phases can be found by integrating from $f = 0$ to ∞

$$\overline{v_{th}^2} = \frac{mkT}{C} + \frac{(1-m)^2}{2(1-m)T_c} 2 \frac{kT}{Cf_c} = m \frac{kT}{C} + (1-m) \frac{kT}{C} = \frac{kT}{C} \quad (4.24)$$

⁴As the noise in S_{RC} is a stationary process and uncorrelated over frequency as shown in [71].

4.3.1 Correspondence with SPICE

It is interesting to complement the previous theory with a simple spice simulation, where we can compare the theory to an ACnoise simulation and a Transient Noise simulation of the sampled signal⁵. For this example lets assume $R_{on} = 1k\Omega$, $C = 1nF$ and $f_s = 10k$ samples/s. From (4.9) we expect the PSD of the continuous time ACnoise analysis to have a value of $4kTR_{on} = 1.66 \times 10^{-17} V^2/Hz$ from DC up to approximately 160 kHz where it rolls off with -6dB/dec. The total noise power is according to (4.12) $kT/C = 4.14 \times 10^{-12} V^2$.

For the sampled waveform, we know from (4.20) that the PSD should have a value of $S_s(f) = 2 \frac{kT}{Cf_s} = 8.28 \times 10^{-16} V^2/Hz$, equally distributed up to $f_s/2$. Finally, from (4.21) we know that the total noise power in the sampled waveform, which is the integral of the PSD from 0 to $f_s/2$, should equal the continuous time total noise power or $kT/C = 4.14 \times 10^{-12} V^2$.

From Fig. 4.6 we can see that the AC noise analysis (blue) matches perfectly the theory. The sampled noise (red) has a higher PSD as expected and the value matches reasonably well. Integrating both curves results in approximately the same total noise power of kT/C as expected.

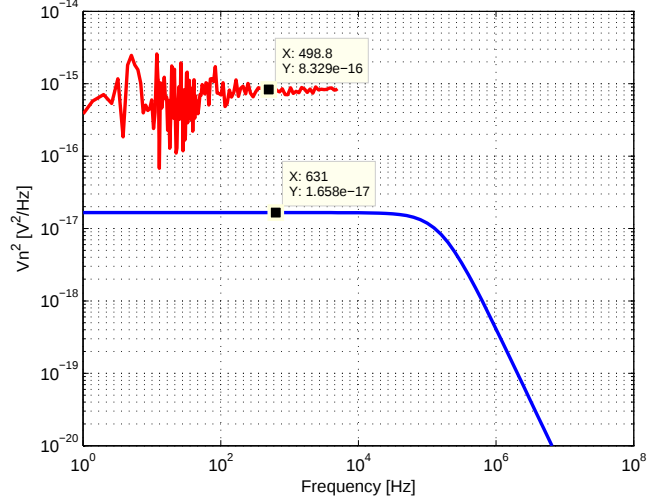


Fig. 4.6: ACnoise analysis (blue) and Transient Noise analysis (red) for a simple sampled circuit.

⁵It is also possible to use periodic steady state (PSS) and periodic noise (pnoise) simulations for this S&H circuit but unfortunately it does not work for a complete delta-sigma modulator (DSM) as the circuit is non-periodic. However, PSS and pnoise can be used with a block-level multi step approach for DSM [72].

4.4 Noise in a SC Integrator

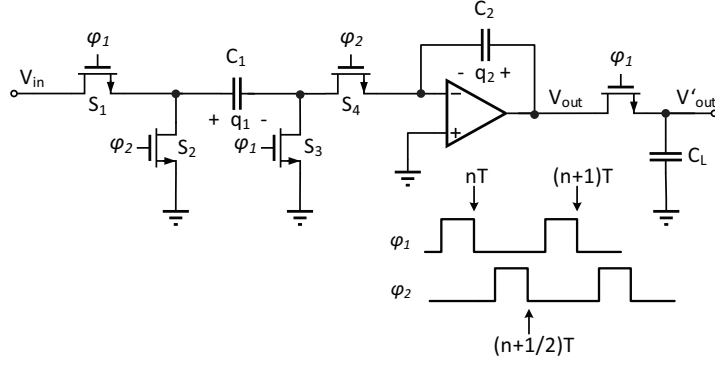


Fig. 4.7: A stray-insensitive SC integrator with its two non-overlapping clock phases.

Next we can expand the previous theory to a more complex sampled system, the stray-insensitive SC integrator shown in Fig. 4.7. As indicated by the non-overlapping clock phases, the input voltage is sampled on phase ϕ_1 , where the charge on the sampling capacitor C_1 is $q_1(n) = C_1 v_{in}(n)$ at time nT at the end of the phase. In phase ϕ_2 the circuit performs integration by discharging C_1 into the virtual ground node of the op-amp and causing the charge on the integration capacitor C_2 to become [35]

$$q_2(n + 1/2) = q_2(n + 1) = q_2(n) + C_1 v_{in}(n) \quad (4.25)$$

Therefore the output voltage v_{out} is

$$v_{out}(n + 1) = v_{out}(n) + (C_1/C_2)v_{in}(n) \quad (4.26)$$

We can clearly see from (4.26) that the integrator is summing up the input voltage with a gain of C_1/C_2 , which is the required integration function.

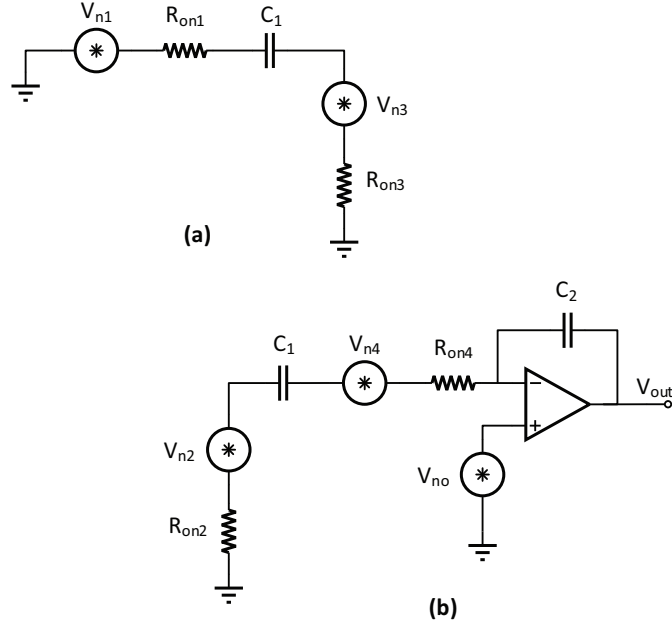


Fig. 4.8: A tray-insensitive SC integrator with its two non-overlapping clock phases.

Now we can consider the noise generated by the circuit, and we can intuitively see that it will be composed partly of noise from the switches S_1 to S_4 and partly of noise from the op-amp. During phase ϕ_1 the circuit is in sampling mode and the noise voltage $v_{C_1}(n)$ across the sampling capacitor C_1 is only due to noise generated by the switches S_1 and S_3 and more specifically only due to thermal noise as the current in these switches only consists of short pulses occurring at the clock rate f_s and thus $1/f$ noise has negligible effect⁶. As covered earlier, MOS transistors used as switches can simply be replaced by a resistor with the equivalent on resistance R_{on} . Fig. 4.8(a) shows the equivalent noise circuit for the sampling phase (ϕ_1) and since the noise sources in the switches are uncorrelated they can simply be combined resulting in the same circuit as in the previous example for the track and hold in Fig. 4.4(b). From the previous discussion we know that the voltage noise across C_1 has a low-pass filtered spectrum with a time constant $\tau_0 = (2R_{on})C_1$ and from (4.12) we know that the MS value of the noise on C_1 is

$$\overline{v_{C_1, sam}^2} = \frac{8kTR_{on}}{4\tau_0} = \frac{kT}{C_1} \quad (4.27)$$

In the integrating phase (ϕ_2) both the switches and the op-amp contribute noise as the equivalent noise circuit in Fig. 4.8(b) shows. For the analysis, we

⁶As $1/f$ noise is a random process with a very long memory and thus with long self-correlation times, by switching the current off can be seen as a means to reduce these long term memory processes that are responsible for the $1/f$ noise such as the trapping and release of charge carriers occurring at long intervals [9]

assume that the loop gain of the stage satisfies the condition $\beta G_m R_L \gg 1$, where $\beta = C_2/(C_1 + C_2)$ and thus we can assume $1/R_L = 0$ and the calculations become somewhat simpler. The noise voltage across C_1 can be found by using the Laplace transform[35]

$$V_{C_1}(s) = \frac{V_n(s) - V_{no}(s)}{1 + s\tau} \quad (4.28)$$

where

$$\tau = (2R_{on} + 1/G_m)C_1 \quad (4.29)$$

and V_n is the sum of the individual noise sources in Fig. 4.8.

Focusing only on thermal noise⁷, we see that this is again a low-pass filtered white noise with a time constant that is determined by the G_m of the amplifier and the on-resistance of the switches. The thermal noise PSD of a general OTA can be found based on the results of the noise of a MOS transistor (4.5) which is

$$S_{n,MOS} = \frac{4kT\gamma}{g_m} \quad (4.30)$$

where γ is the device thermal noise coefficient (typically 2/3 for strong inversion and 1/2 for weak inversion). The noise of the OTA can be described based on the noise of a differential input pair with additional noise contributed due to the topology using a OTA noise factor, N_{OTA} ⁸

$$S_{n,OTA} = \frac{2 \cdot 4kT\gamma}{G_m} \cdot N_{OTA} \quad (4.31)$$

From (4.10) we can find the MS noise power for both the switches and the amplifier over C_1

$$\overline{v_{C_1,sw}^2} = \frac{S_{n,sw}}{4\tau} = \frac{4kT \cdot 2R_{on}}{4\tau} \quad (4.32)$$

and

$$\overline{v_{C_1,OTA}^2} = \frac{S_{n,OTA}}{4\tau} = \frac{2 \cdot 4kT\gamma \cdot 1/G_m \cdot N_{OTA}}{4\tau} \quad (4.33)$$

⁷Using only thermal noise simplifies the analysis and 1/f noise can also be suppressed by clever circuit design (see section 5.4.2).

⁸A single stage op-amp is most commonly used in SC integrator noise analysis [36], [35] and [72], and where the noise is dominated by the input pair $N_{OTA} = 1$. Refer to section 5.4.1 for analysis on different OTAs.

Again, we can sum up these noise powers as they are un-correlated and thus the total MS noise in the integrating phase becomes⁹

$$\overline{v_{C_1,int}^2} = \frac{kT}{C_1} \frac{2R_{on} + 2\gamma \cdot 1/G_m \cdot N_{OTA}}{2R_{on} + 1/G_m} \quad (4.34)$$

For an OTA with transistors in weak inversion, $\gamma = 1/2$, and where the input transistor pair dominates the noise, $N_{OTA} = 1$ the expression simplifies to

$$\overline{v_{C_1,int}^2} = \frac{kT}{C_1} \frac{2R_{on} + 1/G_m}{2R_{on} + 1/G_m} = \frac{kT}{C_1} \quad (4.35)$$

To gain some insight into the expression in (4.34), we can also look at the case when $R_{on} \ll 1/G_m$, for which the OTA noise dominates. The total noise then becomes

$$\overline{v_{C_1,int,OTA}^2} = \frac{kT}{C_1} 2\gamma \cdot N_{OTA} \quad (4.36)$$

which shows the importance of selecting an OTA with a low noise factor, N_{OTA} , which will be covered in detail in section 5.4.1.

Finally, the total noise on C_1 is simply

$$\overline{v_{C_1}^2} = \overline{v_{C_1,sam}^2} + \overline{v_{C_1,int}^2} = 2 \frac{kt}{C_1} \quad (4.37)$$

The noise charge stored on C_1 is transferred to C_2 during $\phi_2 = 1$ as C_1 and C_2 become series connected as ϕ_2 rises and thus the MS noise voltage of C_2 is increased by

$$\overline{\Delta v_{C_2}^2} = 2 \frac{ktC_1}{C_2} \quad (4.38)$$

during each ϕ_2 clock phase[35].

It is then possible to represent the total noise in an integrator stage by an equivalent voltage noise source at the input of an otherwise noiseless integrator and this voltage noise source has the same MS value as that of v_{C_1} given in (4.37). We now see that the capacitor size fully determines the noise level of the integrator circuit.

⁹Several non-idealities of MOSFET switches are not considered in these expressions, most importantly the finite transition time of the switches from R_{on} to R_{off} and the charge injection when the switches are turned off. It is possible that expression (4.34) might somewhat underestimate the noise[35].

One interesting aspect to consider, especially for the input stage of SC $\Delta\Sigma$ modulator, is the use of single or multiple capacitors at the input. This is relevant as it is possible to both implement the input branch and the DAC feedback branch using a single capacitor or two separate capacitors. Using two capacitors introduces up to twice as much noise as a single capacitor because the noise charge adds up[35].

4.5 Thermal Noise Analysis of a $\Delta\Sigma$ Modulator

A $\Delta\Sigma$ Modulator has several noise sources, thermal noise, quantization noise and other extrinsic noise such as noise coupled through the substrate power supplies. The first step in a design is to determine the required noise level to achieve the specified performance and then split this noise budget between the different noise sources in an economical fashion. The total permissible noise power is

$$\overline{v_{n,tot}^2} < \frac{1}{2} A_{max}^2 \cdot 10^{\frac{SNR}{10}} \quad (4.39)$$

where A_{max} is the maximum signal input amplitude and SNR is the required signal-to-noise ratio.

Assigning 75% of the noise budget to the thermal noise, 10% to quantization and 15% to other sources is considered safe for most applications[36]. The total permissible input-referred thermal noise is then

$$\overline{v_{n,th}^2} = 0.75 \cdot \overline{v_{n,tot}^2} \quad (4.40)$$

For large OSR the first integrator dominates the thermal noise contributions, for $OSR = 16$ the second integrator contributes only about 1% of the total thermal noise. The output noise power for the first integrator is to a good approximation (for large OSR) [35]

$$\overline{N_{i1}^2} \approx \frac{\overline{v_{n,i1}^2}}{OSR} \quad (4.41)$$

where $\overline{v_{n,i1}^2}$ is the MS value of the input referred noise voltage of the first integrator, given by (4.37). The minimum value of the first sampling capacitor can then be found by equating $\overline{N_{i1}^2}$ to the permissible thermal noise, $\overline{v_{n,th}^2}$, and solving for C_1

$$C_{s1} = \frac{2kT}{\overline{v_{n,th}^2}} \frac{1}{OSR} \quad (4.42)$$

The subsequent sampling capacitors can be chosen much smaller than C_{s1} .

Converter Design

This chapter will cover the design of a $\Delta\Sigma$ modulator that fulfills the specifications presented in section 1.2. The design methodology will be introduced first, then the system design and topology selection will be covered followed by the circuit design of the various functional blocks.

5.1 Design Methodology

It is essential to use a proper design methodology and tools to efficiently design a high performance $\Delta\Sigma$ ADC in modern CMOS processes. The well-known *top-down/bottom-up* hierarchical methodology is most commonly used in publications [36, 33, 73, 74, 75]. The design process starts from the modulator specifications, most significantly bandwidth and effective resolution. Next the design space is explored for modulator architecture and NTF. The simple linear model design equations (3.13) and (3.14) can be used to get an idea of approximate values for the main parameters (OSR, L and B). From there more accurate non-linear models should be used, such as using the DS Toolbox in MATLAB. Once the modulator architecture has been selected it is possible to proceed with a top-down design, where the architecture is translated to a high-level circuit (with ideal switches, capacitors, amplifiers and quantizers), using the extracted scaling coefficients for the NTF. The correct timing and operation of the loop filter is confirmed with a quick open-loop simulation before running a full closed-loop transient simulation from which a DFT will reveal if the circuit implements the correct transfer function. From there specifications for each circuit block can be mapped out with high-level simulations and the blocks are then finally translated to transistor-level designs. Within each design stage multiple iterations can be run to optimize the different blocks while using bottom-up verification to speed up simulation times. Fig. 5.1 shows a diagram illustrating this methodology.

5.2 Noise Budget

Before exploring possible modulator topologies, the allowed signal-to-quantization noise (SQNR) needs to be established. From the previous discussion on noise (section 4.5), it was recommended that around 10% of the total noise budget

should be allocated to quantization noise. Assuming to begin with that $\text{SNR}=\text{DR}$, we assign 108 dB to the SNQR. Next we allocate 75% of the total noise to thermal noise or 99.2 dB. From the input amplitude specifications, the total allocated thermal noise power can be found

$$\overline{v_{n,th}^2} = \frac{1}{2} A_{in,fs}^2 * 10^{-\text{SNR}_{th}/10} = 9.51 \times 10^{-12} \text{V}^2 \quad (5.1)$$

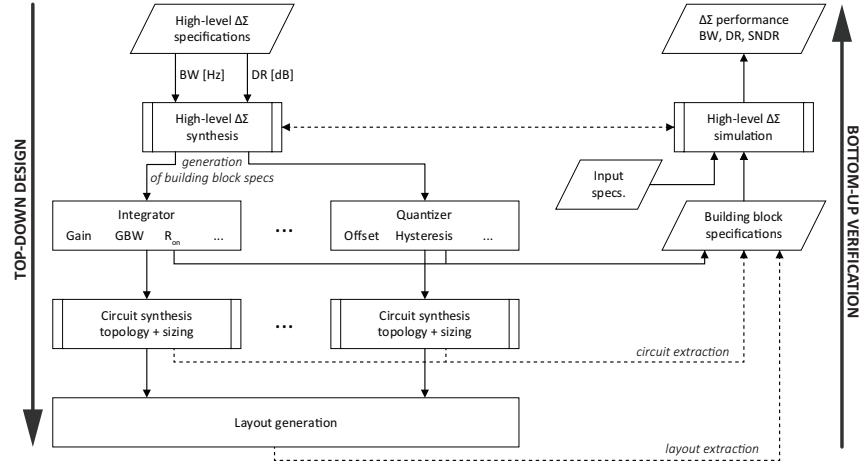


Fig. 5.1: Top-down design, bottom-up verification methodology for $\Delta\Sigma$ modulators.

Due to the low noise requirements of the converter, we see from (4.42) that a relatively large OSR is needed in order to keep the sampling capacitor size reasonable. Selecting $\text{OSR} = 256^1$ requires $C_s > 3.4 \text{pF}$ which is completely acceptable. For some additional margin we select $C_s = 4 \text{pF}$. From the signal bandwidth requirements, the required sampling frequency becomes 5.12 MHz, a very reasonable frequency in modern CMOS [36]. In thermal noise limited converters, the power dissipation is, to a first order approximation, independent of OSR. The GBW is approximately given by

$$\text{GBW} = \frac{G_m}{2\pi C_L} \quad (5.2)$$

where C_L is the loading capacitance. At first glance it would seem that for higher OSR, higher GBW is required and thus proportionally higher G_m , resulting in increased power dissipation. However, increasing OSR will decrease the sampling capacitance proportionally (and correspondingly the loading capacitance), making GBW unchanged. This is because for higher OSR, the thermal noise is spread over

¹An oversampling rate which is a power of two if preferable as it makes the construction of the decimation filter much easier [36].

a larger bandwidth and proportionally less noise resides in the signal bandwidth, allowing smaller sampling capacitance to be used [65]. However, there are also other effects that need to be considered. The transistors can be pushed further into weak inversion for slower clock speeds, increasing the g_m/I_d ratio and reducing power dissipation. This has diminishing returns beyond a certain point, as the parasitics become excessively large and the f_T of the transistors sharply drops and thus it is not beneficial to operate below a certain clock rate [34]. Furthermore, all the switch parasitics need to be charged in every clock cycle, requiring more power for higher clock speeds. On an architectural level, however, a significantly lower OSR requires the use of higher order filters and increases the strain on both the anti-aliasing filter and decimation filter, both requiring sharper roll-offs. Finally, the OSR impacts the gain required in the first integrator to suppress harmonic distortion, where the gain needs approximately to be equal to the OSR [65] as previously discussed.

The exact optimization of the OSR is left for future analysis but here it will be assumed that it is limited enough by the maximum sampling capacitor size and that it should be a power of two, thus the selection of OSR=256.

5.3 System Design

By adding 10 - 20 dB to the SQNR to account for degradation due to circuit non-idealities, we can get a rough estimation from the linear-model (3.13) on suitable order (L), oversampling ratio (OSR) and number of bits in the quantizer (B). As previously discussed, it is more accurate to use the non-linear model and Fig. 5.2, 5.3 and 5.4 show the achievable SQNR for modulators of order 1 to 8 with OSR from 4 to 1024 and single bit, 2-bit and 3-bit quantizers, based on high-level simulations in MATLAB.

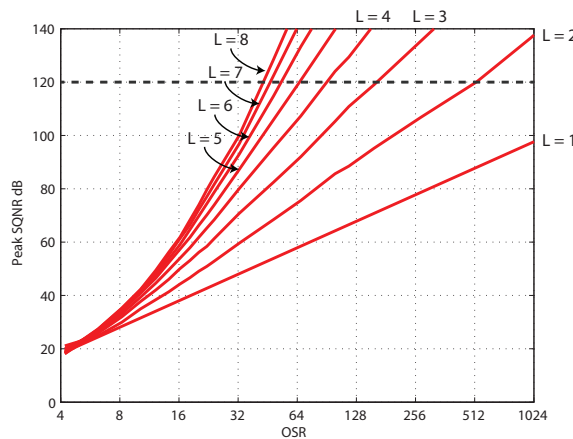


Fig. 5.2: Simulated SQNR limit for 1-bit modulators of order L.

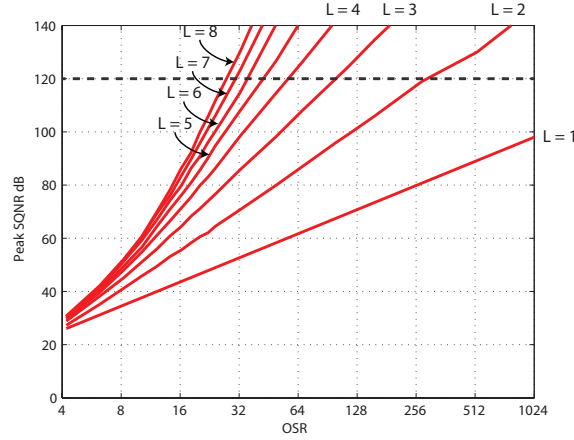


Fig. 5.3: Simulated SQNR limit for 2-bit modulators of order L .

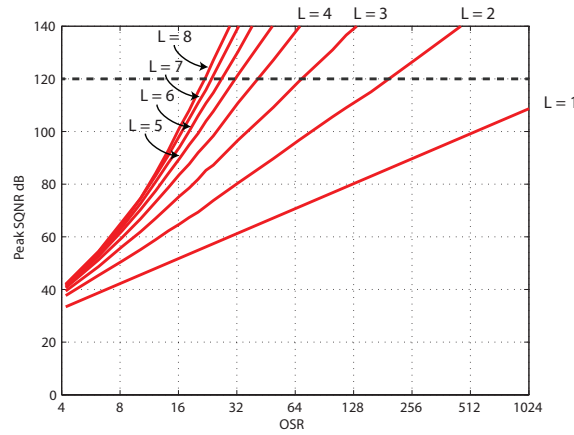


Fig. 5.4: Simulated SQNR limit for 3-bit modulators of order L .

If we aim for 120 dB we can see that there are multiple choices. Multi-bit quantization provides significantly improved SQNR over the single-bit. This is firstly due to the smaller quantization steps but also due to smaller signal swings in the loop filter which improves stability of the filter allowing higher out of band gain and higher input levels. Single bit quantizers are, however, inherently linear (as discussed in Section 3.4.2) resulting in simpler modulator design as they do not need any additional means to improve the linearity of the DAC. Multi-bit quantization, especially combined with intentional non-linearity in the quantizer and DAC (see section 2.3) are very interesting, but in order to limit the scope of the project a single-bit modulator topology is chosen.

Additional to the single-loop topologies reviewed so far, are so called MASH or cascade structures, which reduce the stability problems in higher order modulators [36]. However, these topologies are more sensitive to circuit non-idealities,

especially integrator finite DC gain and switch resistance, making them less attractive for low-voltage, low-power designs [43]. By selecting a single-loop, single-bit topology, it is clear from Fig. 5.2 that a 3rd order modulator is most suitable, delivering more than 120dB SQNR with minimum complexity.

Traditional feedback topologies, such as the second order modulator in Fig. 5.5(a), have a $STF = z^{-L}$ and thus the output v contains a delayed version of the input u . This in turn causes the error e to contain a high-pass filtered version of the input signal which the integrators restore to its full amplitude [76]. The delay can be eliminated by canceling the transfer function from u to the intermediate nodes, x_1 and x_2 , by feeding the input signal along with the signal from x_1 directly to the input of the quantizer, thus making the $STF = 1$. An example of such a topology, originally proposed by Steensgaard [77, 78], is depicted in Fig. 5.5(b). Now the input signal u is no longer present in loop filter, only the quantization noise e is processed by the integrators. This can significantly reduce the amplifier output swings and relaxing the non-linearity requirements, such as slew rate and DC gain, accordingly. This becomes exceedingly important in low-voltage, low-power designs. Furthermore, there is only one DAC required in the feedback loop, a significant advantage, especially for higher order, multi-bit designs [76]. Finally, the feed-forward structure results in smaller integrating capacitors, especially important in higher order, low-OSR designs [36].

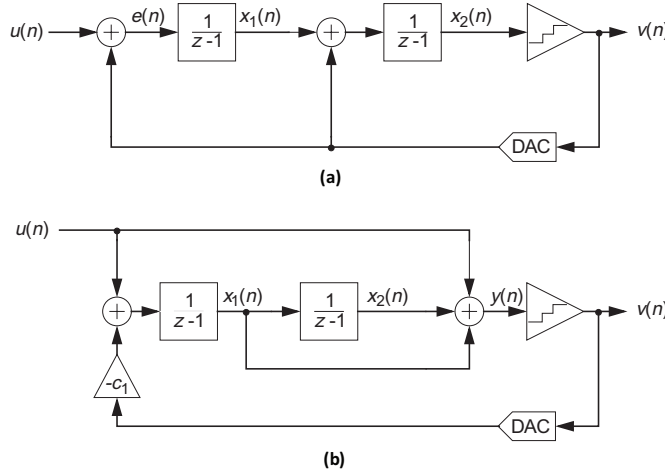


Fig. 5.5: Second order $\Delta\Sigma$ modulator with feedback structure (a) and feed-forward structure (b).

The previous topologies only realize NTFs with zeros at DC. By including a local feedback path within the loop filter, local resonators are formed and the zeroes can be shifted up in frequency along the unit circle, which can then be used to optimize the SQNR of the modulator[36]. Based on the previous discussion, a third order feed-forward topology, with local feedback, commonly called *cascade of integrators with feed-forward* (CIFF) is chosen. Fig. 5.6 shows the block diagram for the chosen topology.

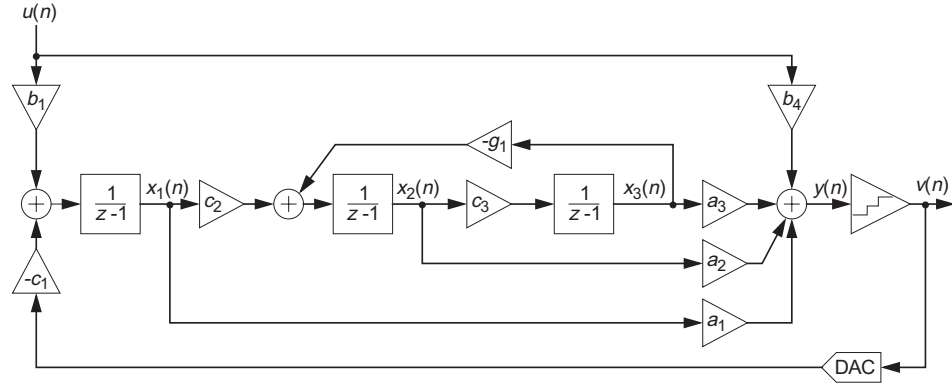


Fig. 5.6: Chosen topology, a third order cascade of integrators with feed forward (CIFF) and a local feedback loop.

The NTF is synthesized using Schreier's Delta-Sigma Toolbox [64]. Using the aforementioned zero-optimization, limiting the out of band gain ($\|H_\infty\|$) to 1.5 and selecting the CIFF topology, simulations show that the maximum stable input amplitude is -1.3 dBFS with maximum SQNR of 136 dB. The toolbox can then be further used to scale and extract the coefficients which yields the parameters shown in column two of Table 5.1. As the coefficients will be implemented using capacitor ratios they need to be approximated by rational numbers. The adjusted coefficients and the corresponding capacitor ratios can also be seen in Table 5.1. The resulting NTF is

$$NTF(z) = \frac{(z-1)(z^2-2z+1)}{(z+0.1387)(z^2-1.555z+0.6307)} \quad (5.3)$$

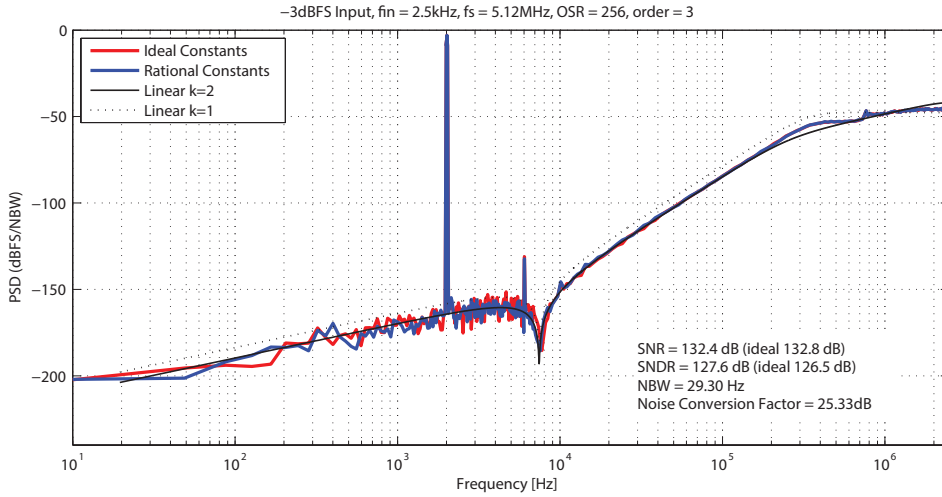
The adjustment of the coefficient has changed the NTF to some extent but the impact on the SNR is marginal. Fig. 5.7 plots the simulated spectrum for ideal and rational coefficients, demonstrating the small change of the NTF. The linear model is also plotted in Fig. 5.7, for two gain values, the default $k = 1$ and $k = 2$ which fits well to the non-linear results². This gain value is used to scale the input feed-forward coefficient, $b_4 = 1/k$, to make sure that the feed-forward works correctly with the binary quantizer to cancel out the signal component [36].

²This was done by finding the value of k that fit best to the simulated NTF

Table 5.1: Coefficients and capacitor ratios for the selected modulator.

Coefficient	Value	Rational approx.	Capacitor Ratio
a_1	2.1168	$19/9 = 2.1111$	C_{ff2}/C_T
a_2	2.7129	$19/7 = 2.7143$	C_{ff3}/C_T
a_3	2.3879	$12/5 = 2.4$	C_{ff4}/C_T
b_1	0.3778	$3/8 = 0.375$	C_{S1}/C_{I1}
b_2	0	N/A	N/A
b_2	0	N/A	N/A
b_4	$1/k$	$1/2$	C_{ff1}/C_T
c_1	0.3778	$3/8 = 0.375$	C_{S1}/C_{I1}
c_2	0.2810	$2/7 = 0.2857$	C_{S2}/C_{I2}
c_3	0.1732	$1/6 = 1.6667$	C_{S3}/C_{I3}
g_1	$5.2169 \cdot 10^{-4}$	$1/2000 = 5.0 \cdot 10^{-4}$	C_{fb}/C_{I2}

$$C_T = \sum_{i=ff1}^{ff4} C_i$$


Fig. 5.7: Simulated spectrum with ideal and rational scaling coefficients.

From the noise requirements we know the value of the first sampling capacitor, $C_{S1} = 4pF$. Based on the scaling coefficient b_1 (Table 5.1), we see that the first integrating capacitor becomes $C_{I1} = 10.67pF$, a very reasonable value.

5.3.1 Behavioral schematic, timing and voltage scaling

Now that we have a modulator topology that implements the desired NTF and a scaled block diagram, we can move forward towards practical implementation. To ensure that the modulator follows the correct timing and implements the desired difference equations we construct a simplified behavioral schematic, shown in Fig. 5.8, and a corresponding timing diagram in Fig. 5.9. The difference equations are extracted by inspection from the modulator block diagram in Fig. 5.6.

Desired difference equations:

$$x_1(n+1) = x_1(n) + b_1 u(n) - c_1 v(n), \quad (5.4a)$$

$$x_2(n+1) = x_2(n) + c_2 x_1(n) - g_1 x_3(n), \quad (5.4b)$$

$$x_3(n+1) = x_3(n) + c_3 x_2(n), \quad (5.4c)$$

$$y(n) = b_4 u(n) + a_3 x_3(n) + a_2 x_2(n) + a_1 x_1(n), \quad (5.4d)$$

$$v(n) = Q(y(n)), \quad (5.4e)$$

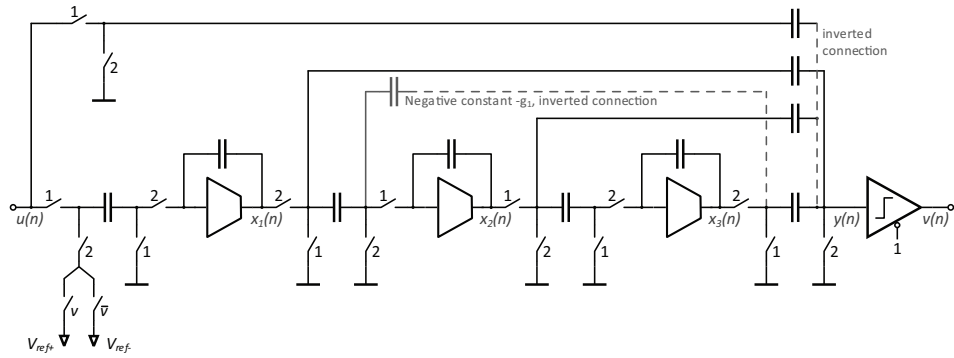


Fig. 5.8: High-level schematic for the proposed modulator.

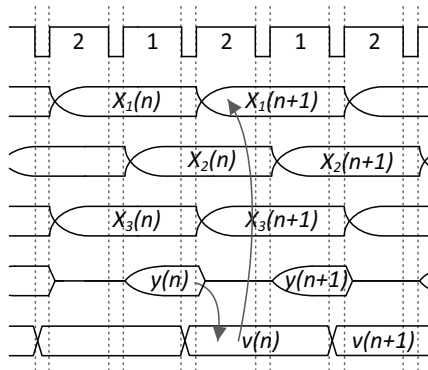


Fig. 5.9: Switch timing diagram for the proposed modulator that implements the desired difference equations.

Sampling and integration phases alternate through the loop, the first and third integrators sample on phase 1 and integrate on phase 2, while the second integrator samples on 2 and integrates on 1. The feed-forward capacitors are also charged alternatively and thus the need to connect the first and the third to the negative path to implement the correct summation. The comparator holds the output until the next falling edge of phase 1, allowing the output to be fed back and used for generating $x_1(n+1)$. The feedback capacitor is very small and can be implemented with a capacitive T circuit [36], not shown here for simplicity. There are other timings that implement the same equations, of which one is commonly used where all the integrators sample and integrate synchronously. However, the benefit of using the proposed switch timing is that the integrators are only active in one of the phases and thus can possibly be turned off during idle phase.

The input branch and feedback branch can share the same capacitor because b_1 and c_1 are the same. However, this can introduce some signal dependent loading on the reference voltage [36]. The scaling coefficients may need to be adjusted for real circuit voltage levels as the delta-sigma toolbox assumes that the input of the modulator ranges from -1 to 1 and that the integrators also occupy the same range. These values are given in normalized (unit-less) form but in the actual circuit they need to take form of physical voltage levels. Since the full scale input is the same as the full differential voltage range in the integrators (from -800mV to 800mV), the values from the toolbox can be used directly.

With the behavioral schematic, timing and scaling coefficients verified, we can move on to constructing a full schematic and verifying the operation of the modulator.

5.3.2 High-level modelling using VerilogA

The schematic presented thus far has been only single ended, however fully differential circuits are preferred, do to their ability to reject extrinsic noise and suppress even order harmonics, increased voltage swings and lower intrinsic noise [79]. Schreier et. al [35] have shown that for an equivalent dynamic range, a differential circuit uses as little as 35% of the power consumed by its single ended counterpart.

Following the design methodology outlined earlier in this chapter, a fully differential circuit is constructed using ideal behavioral models for the circuit components. Fig. 5.10 shows the full schematic for the third order modulator. An open-loop simulation, with a unit impulse input, confirms that the loop-filter is implemented correctly, showing the correct impulse response of

$$l_1(n) = \left\{ 0, 0, \frac{1}{28}, \frac{3}{28}, \frac{6}{28}, \frac{10}{28}, \frac{15}{28}, \frac{21}{28}, \frac{28}{28}, \dots \right\} \quad (5.5)$$

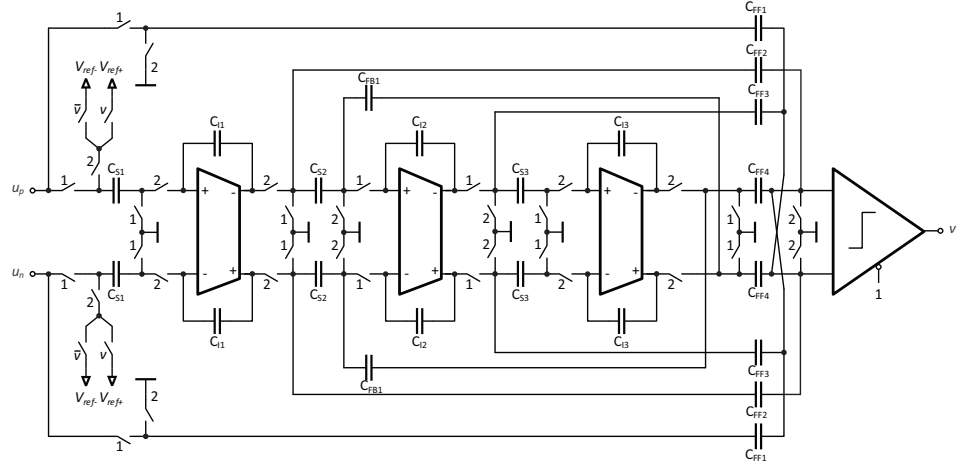


Fig. 5.10: Fully differential schematic used for high-level simulations. The OTA model contains the CM feedback.

Using high-level models, such as VerilogA, in the early design stage is very important as it greatly reduces simulation time which is essential when running multiple simulations to extract the performance requirements for the transistor-level blocks. Transient simulations of $\Delta\Sigma$ modulators require simulations for thousands of clock cycles due to the high oversampling ratio to get a good estimation of the spectrum.

The first integrator is the most critical component of the system and using VerilogA, the operational transconductance amplifier (OTA) was modeled as a voltage controlled current source with variably limited gain bandwidth (GBW) and DC gain. Fig. 5.11 shows how performance changes with these parameters. The SNR and SNDR follow closely for all DC gain values tested but drop sharply for values below 40 dB. GBW below 25 MHz causes a proportionally faster decrease in SNDR than SNR but performance remains adequate down to almost 15 MHz, three times the sampling frequency.

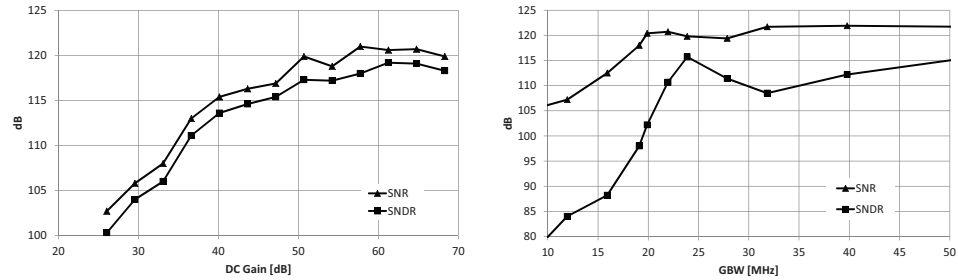


Fig. 5.11: High-level simulation results indicating DC gain and GBW requirements for the first integrator.

With these results we can move on to circuit design.

5.4 Circuit Design

The fast scaling of modern CMOS, mainly driven by digital circuits, down to tens of nanometers has serious implications for analog circuit design. The small feature size requires lower supply voltage to avoid oxide breakdown. Simultaneously, battery powered designs are becoming more important, often using supply voltages below 1 V and relying on very low power consumption to operate. Lower supply voltage means lower signal swings which requires lower noise to retain the same dynamic range (DR). The supply voltage also scales faster than the threshold voltage, leaving less headroom for stacking transistors and reducing output swing further limiting DR. Finally, the intrinsic gain of transistors in nanometer CMOS has also greatly diminished, and along with the small voltage headroom makes traditional gain boosting techniques such as cascoding difficult.

In this section the circuit-level design will be covered. Most effort will be spent on the OTA but the switch and quantizer design will also be covered.

5.4.1 Integrator OTA

An operational transconductance amplifier (OTA) is a voltage input, current output amplifier, where the relationship between the input voltage and the output current is given by a proportionality constant, termed the transconductance g_m of the amplifier. The output current is typically used to charge and discharge a capacitive load. Figure 5.12 shows OTAs in three different configurations, single ended, differential input to single ended output and a fully differential input/output and their equivalent circuit models.

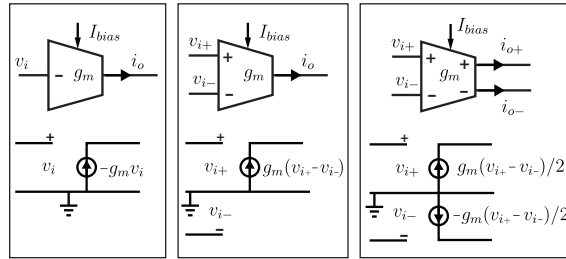


Fig. 5.12: Three types of OTA and their circuit models: single ended (a); differential input, single output (b); and fully differential.

The OTA can be considered the most important building block in $\Delta\Sigma$ modulators as it determines a very large fraction of the total power consumption. The requirements consist mainly of the gain bandwidth (GBW), DC gain, output swing and slew rate.

The GBW controls how fast the output of the integrator settles and is approximately determined by the transconductance, G_m , and load capacitance, C_L ,

$$GBW = \frac{G_m}{2\pi C_L} \quad (5.6)$$

where the load capacitance depends on the sampling and integration capacitance but also on any additional loading on the input and output

$$C_L = \frac{(C_{S1} + C_{in})C_{I1}}{(C_{S1} + C_{in}) + C_{I1}} + C_{out} \quad (5.7)$$

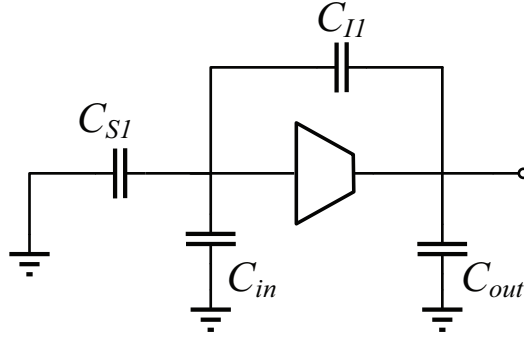


Fig. 5.13: Parasitics of an OTA.

The DC gain determines the accuracy of the charge transfer and is especially important in multi-loop or MASH modulators. It is determined by the output impedance and transconductance of the OTA

$$\text{DC gain} = G_m \cdot R_o \quad (5.8)$$

The current consumption of the OTA is largely determined by how efficiently it delivers its transconductance and as such it is useful to use that as bases for comparison between different OTA topologies. Meanwhile, it is important to remember the other three main requirements, DC Gain, output swing and slew rate. A number of OTA topologies have been used in SC integrators. The classic topologies include the Single Stage OTA, Telescopic Cascode, Folded Cascode, the Miller two-stage OTA and the Current Mirror OTA. More recent topologies are the Bulk-Driven OTA [80] and Inverter based OTA [38], which all try to address the low-voltage, low-power environment.

Single-Stage OTA

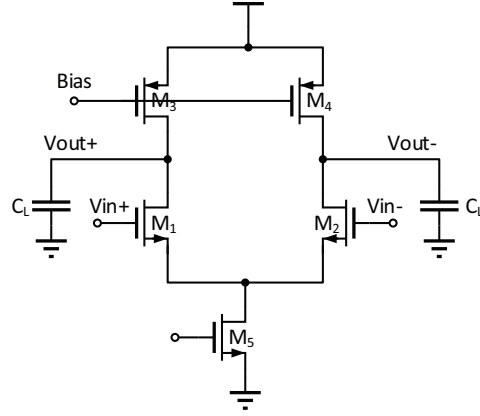


Fig. 5.14: A single-stage OTA.

The single stage OTA is perhaps the simplest and best known topology. It consists of an input differential pair with a single current source and two active load transistors. Assuming that the input transistors operate in weak inversion we have

$$g_m = \frac{I_D}{nV_T} \quad (5.9)$$

where $V_T = kT/q$ is the thermal voltage and n is the slope factor. We can now use this as a basis of comparison between the OTAs. If we assume the same current in each branch of the single stage, and we know for the differential pair that $G_m = g_{m1}$, we have

$$I_{Single} = GBW \cdot 2\pi \cdot nV_T \cdot 2C_L \quad (5.10)$$

Assuming MOS noise given in (4.4), the input referred thermal noise power is [69]

$$S_{v,Single}(f) = 2\gamma \frac{4kT}{g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} \right) = 2\gamma \frac{4kT}{G_m} \underbrace{\left(1 + \frac{g_{m3}}{G_m} \right)}_{N_{OTA}} \quad (5.11)$$

The main drawback of the single stage topology is the low output impedance which results in low DC gain and limited output swing.

Two-Stage Miller OTA

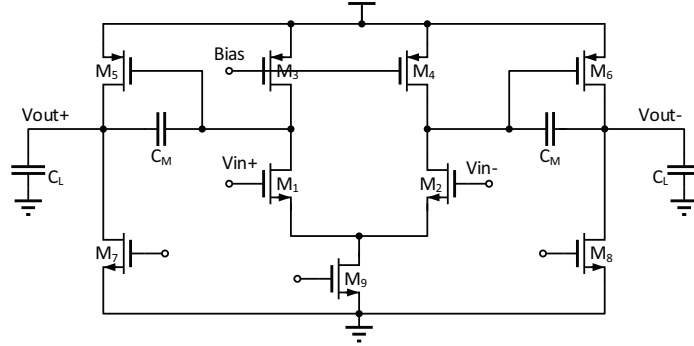


Fig. 5.15: A two-stage Miller OTA.

To improve the DC gain and output swing, we can cascade two amplifiers, the first with high gain followed by a high output swing stage, realizing for example the classic Miller two-stage OTA. However, cascading two amplifiers causes an additional pole to form, causing closed-loop stability issues unless properly compensated with an internal compensation capacitor, called the Miller capacitor [4]. There are two current branches, one in the input stage and the other in the output stage. The current in the input branch is

$$I_{D1} = GBW \cdot 2\pi \cdot nV_T \cdot C_M \quad (5.12)$$

where C_M is the Miller compensation capacitor. To ensure stability, the non-dominant pole should be placed at 3 times the GBW which results in the current in the output branch [4]

$$I_{D3} = GBW \cdot 2\pi \cdot nV_T \cdot 3(C_M + C_L) \quad (5.13)$$

The total current then becomes

$$I_{Miller} = GBW \cdot 2\pi \cdot nV_T \cdot (8C_M + 6C_L) \quad (5.14)$$

The current consumption is much higher than for the single stage OTA, a penalty for using two compensated amplifier stages. The intrinsic noise is given by [69]

$$S_{v,Miller}(f) = 2\gamma \frac{4kT}{g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} + \frac{(g_{m5} + g_{m7})(g_{ds1} + g_{ds3})^2}{g_{m1}(g_{m5})^2} \right) \quad (5.15)$$

Here it is important to realize that the GBW is set by g_{m1} and C_M , not the load capacitor. To ensure stability, $C_M < C_L$ and thus g_{m1} needs to be smaller for the same GBW. However, the exact ratio depends on transistor parameters and operating condition, and is thus not easily determined for a general case. It is clear that N_{OTA} for the two-stage topology is significantly larger than one.

Telescopic OTA

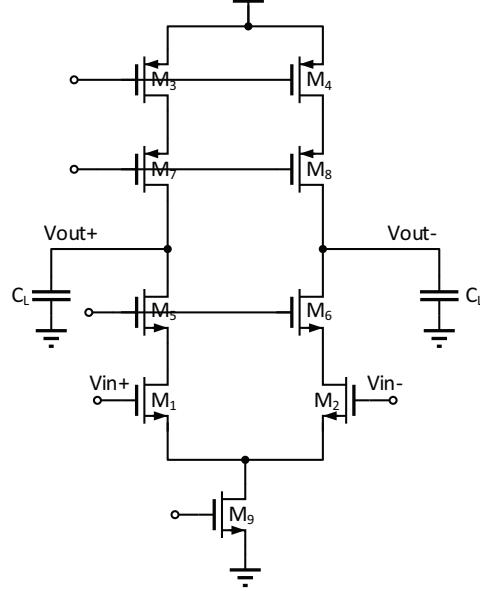


Fig. 5.16: A single-stage telescopic OTA.

The telescopic OTA can be used to increase the DC Gain of the single stage, while consuming the same current. However, it requires cascoding transistors to increase gain and thus greatly reducing the output swing. It has additional problems with shorting the input and output. For completeness, the current for the telescopic OTA is

$$I_{Telescopic} = GBW \cdot 2\pi \cdot nV_T \cdot 2C_L \quad (5.16)$$

The noise in the telescopic OTA is almost exactly the same as for the single stage OTA, as the cascodes contribution to noise is negligible [81]

$$2\gamma \frac{4kT}{g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} \right) = 2\gamma \frac{4kT}{G_m} \underbrace{\left(1 + \frac{g_{m3}}{G_m} \right)}_{N_{OTA}} \quad (5.17)$$

Folded Cascode OTA

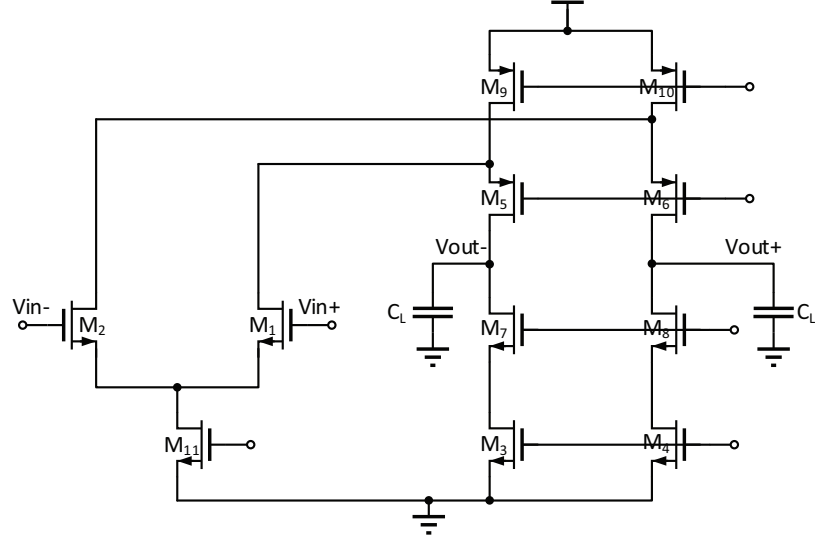


Fig. 5.17: A single-stage folded cascode OTA.

The folded cascode topology addresses the issues with limited output swing and shorting of input and output by providing separate current branches for the input and output. The current dissipation is approximately twice the current of the telescopic [69]

$$I_{Folded} = GBW \cdot 2\pi \cdot nV_T \cdot 4C_L \quad (5.18)$$

The folded cascode has higher noise due to the additional current sources in the output branch. As for the telescopic, the cascode devices do not contribute any significant noise and thus the total noise becomes

$$S_{v,Folded}(f) = 2\gamma \frac{4kT}{g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}} \right) \quad (5.19)$$

$$= 2\gamma \frac{4kT}{G_m} \underbrace{\left(1 + \frac{g_{m3}}{G_m} + \frac{g_{m9}}{G_m} \right)}_{N_{OTA}} \quad (5.20)$$

Inverter OTA

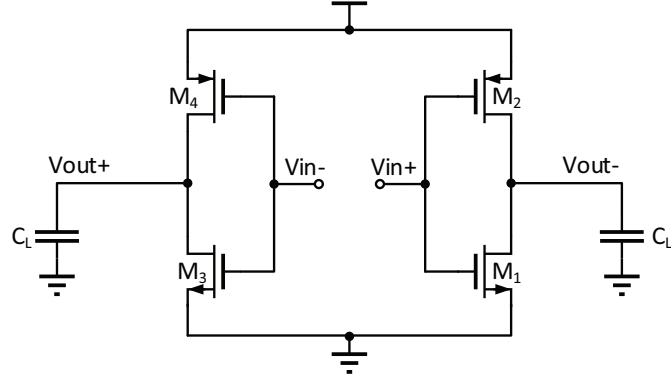


Fig. 5.19: An inverter OTA.

One interesting topology is the inverter based OTA, recently proposed for use in $\Delta\Sigma$ modulators [38]. The topology has very high transconductance efficiency as both the NMOS and PMOS devices contribute to the overall transconductance $G_m = g_{m1} + g_{m2}$. If we assume that both have the same transconductance, the current in the inverter OTA is

$$I_{Inverter} = GBW \cdot 2\pi \cdot nV_T \cdot C_L \quad (5.26)$$

The inverter based OTA not only exhibits the lowest current consumption of the compared topologies, but it has rail-to-rail output swings and can operate as class-C output stage, resulting in very high slew-rate. The total noise in the inverter OTA is

$$S_{v,Inverter}(f) = 2\gamma \frac{4kT}{g_{m1} + g_{m2}} = \gamma \frac{4kT}{g_{m1}} = 2\gamma \frac{4kT}{G_m} \underbrace{\left(1\right)}_{N_{OTA}} \quad (5.27)$$

From 5.27 it is clear that the inverter based OTA does have the lowest intrinsic noise, however, it has also higher bandwidth causing more noise folding in SC applications. In terms of overall transconductance, G_m , the OTA noise factor becomes exactly 1, the best of the topologies reviewed. However, the inverter based OTA suffers from the same low DC gain as the single stage and current mirror OTAs and further more, there is no built in biasing, making it difficult to use in many applications.

Table 5.2 summarizes the performance characteristics of these different topologies. It is clear that for a single-loop $\Delta\Sigma$, where high gain is not required, the inverter based OTA has the best overall performance and therefore it will be selected.

Table 5.2: Comparison of different OTA topologies.

	Single-stage	Two-stage Miller	Telescopic	Folded	Current Mirror	Bulk Driven	Inverter
Low supply voltage	0	0	-	-	0	++	++
Power efficiency	0	-	0	-	0	-	++
Noise	0	0	0	-	0	0	++
DC gain	0	++	++	+	0	-	0
Slew rate	-	+	-	-	+	-	++
Output signal swing	-	++	-	+	++	+	++
Speed	++	+	+	-	+	-	0
CMRR/PSSR	+	+	+	+	+	+	-

++: very good, +:good, 0:average, -:poor

Inverter as an amplifier in SC circuits

Switched capacitor circuits, using a traditional OTA, typically use two non-overlapping clocks. During phase 1, the charge is sampled onto a sampling capacitor C_S and during phase two the charge is transferred on to a feedback capacitor, C_I while the OTA keeps its negative input as virtual ground. However, when using a logic inverter as an OTA, there is no inherent virtual ground due to the single terminal topology. When the feedback is formed, the input node is pulled to the offset voltage of the inverter. This offset can be removed by employing a traditional auto-zeroing technique. During sampling phase, the inverter can be switched to a unity-gain configuration, where the offset is stored onto an additional offset cancellation capacitor C_C . Then during charge transfer the offset is canceled, forming signal ground. This additional sampling action adds more thermal noise to the circuit, while reducing $1/f$ noise as will be investigated in more detail in section 5.4.2. However, in audio applications, a DC offset is not of large concern, given that it is small enough to not affect the circuit operation. Fig. 5.20 shows a SC integrator using conventional OTA and an inverter OTA during sampling and integrating phase.

A pseudo-differential inverter based SC integrator is shown in Fig. 5.21. The circuit uses a low-power SC common-mode feedback (CMFB) circuit which does not limit the swing of the integrator [38]. At phase 1, the CMFB capacitors C_M are shorted to ground and at phase 2 they realize a common-mode voltage detector, where the difference between the detected common-mode voltage and signal ground is injected back to the integrator, forming a CMFB loop with gain defined by C_M/C_I .

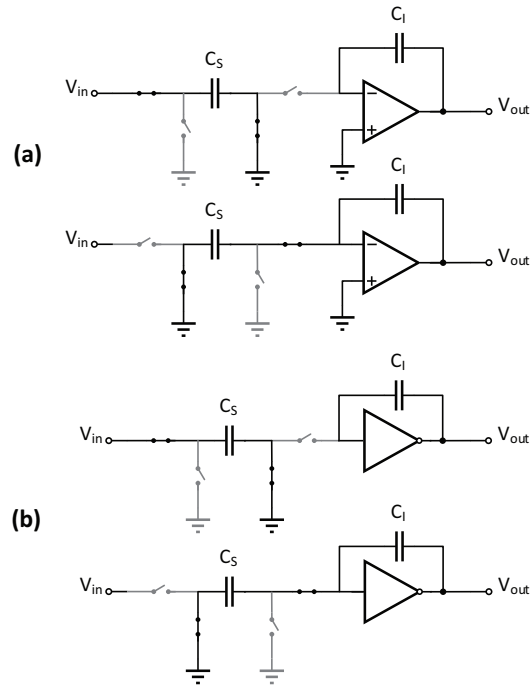


Fig. 5.20: SC integrator using conventional OTA (a) and using inverters(b).

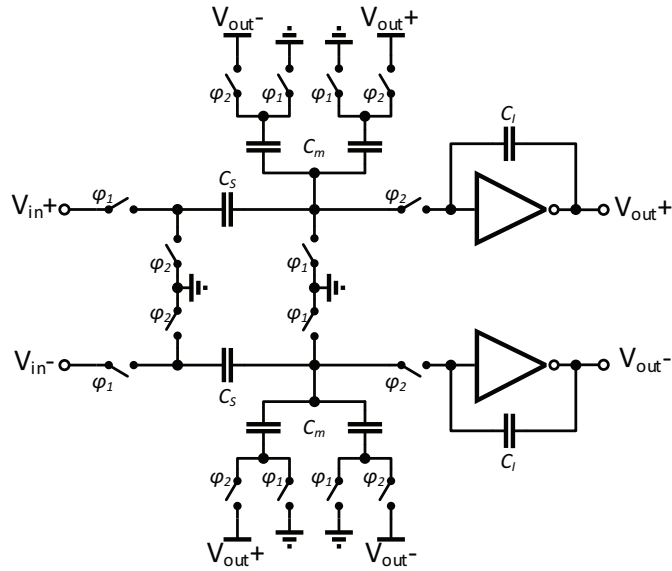


Fig. 5.21: Pseudo differential integrator with low power SC CMFB loop.

An inverter can be operated as a class-C push-pull amplifier when the supply voltage equals the sum of the nominal threshold voltages, $V_{th,N}$ and $V_{th,P}$ causing both transistors to be biased in weak to moderate inversion. This is especially attractive for low-voltage SC circuits as it provides high slew-rate, rail-to-rail output swing, low noise and high power efficiency, as previously discussed. During charge transfer, when used in a SC integrator, a step change in the input voltage causes one of the transistors to be biased fully in strong inversion, while the other is turned off completely. This creates a large current charging the capacitive load with minimum static current dissipation, resulting in high slew-rate. As the voltage settles towards mid-rail due to the negative feedback, then both transistors will move into weak inversion, providing high DC gain [38].

Achieving the required DC gain (approx. 37dB from High-level simulations in Fig. 5.11) requires long transistors to maximize the output impedance. However, longer transistors result in larger parasitics and at some point the DC gain becomes limited by the input parasitics, $C_{in,par}$, but more importantly, the speed of the amplifier will be affected. During integration phase, the equivalent gain of the amplifier becomes approximately [10]

$$A_{eq} = A \frac{C_S}{C_S + C_{in,par}} \quad (5.28)$$

A similar, albeit more complicated analysis, can be done using both the phase and gain error as done in [38, 40] but the results remain similar.

The input parasitics also behave as an additional load on the output (together with the output parasitics, $C_{out,par}$) thus reducing the GBW. The equivalent load capacitance becomes

$$C_{L,eq} = \frac{(C_S + C_{in,par})C_I}{C_S + C_{in,par} + C_I} + C_L + C_{out,par} \quad (5.29)$$

and from that we can find the equivalent GBW.

This shows that there are conflicting requirements for the DC gain and GBW. As we increase the length to increase gain, the GBW drops. The same holds true for the width, increasing the width maximizes the g_m/I_D as it pushes the transistor further into weak inversion but at some point we get a diminishing return and further more, the DC gain starts to be reduced. Additionally, due to the limited supply voltage, the selection of aspect ratio for the transistors is somewhat limited. Fig. 5.22 shows how the required supply voltage and parasitics change with different device size. The simulation was performed using a standard threshold devices, biased with 9 μ A.

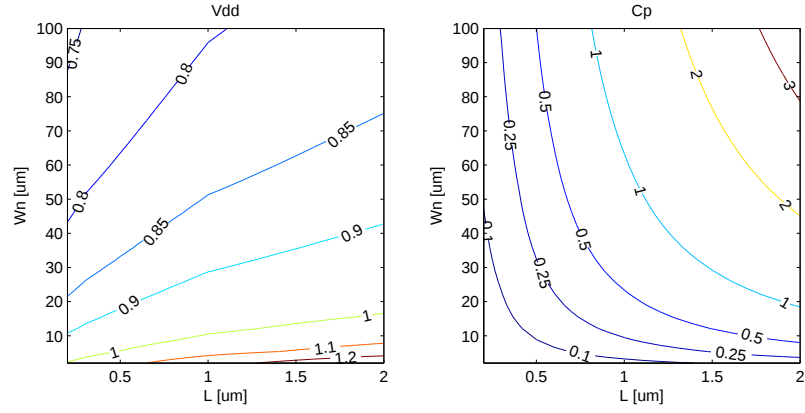


Fig. 5.22: Variation in supply requirements (V_{dd}) and parasitic capacitance (C_p) with variations on device width and length for a fixed bias current of $9\mu\text{A}$.

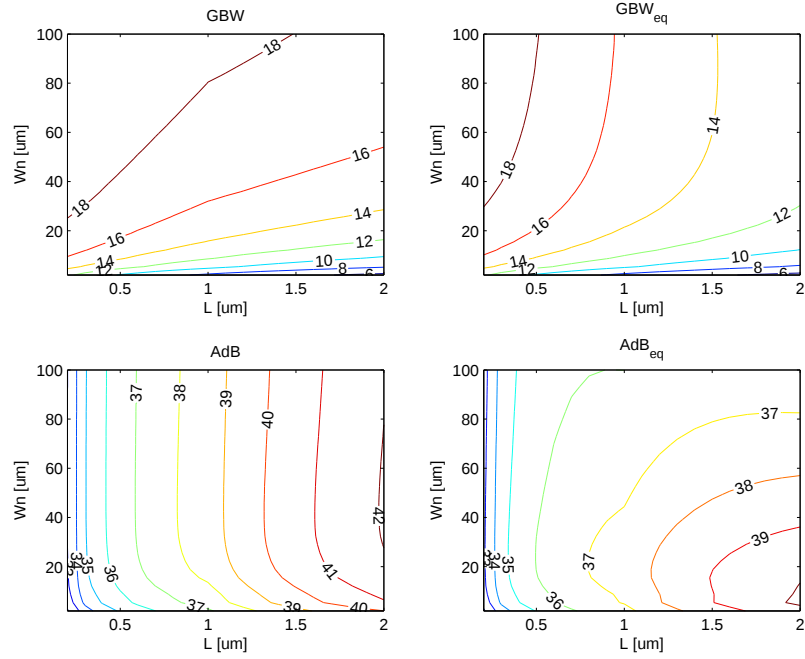


Fig. 5.23: Variation in GBW and DC gain, both with (right) and without (left) the effects of parasitic capacitors.

Fig. 5.23 shows how the parasitics affect the GBW and DC gain as previously discussed and how both these performance parameters change with transistor size.

An optimum can be found, given some minimum requirements, by plotting a combined value of the two. Here we need to be careful as more DC gain does not compensate for lower GBW, thus we cannot simply take the product of the two. However, if we define the minimum required equivalent DC gain (here as 37 dB) and the minimum equivalent GBW (here as 14.5 MHz), then we can establish the device dimensions that satisfy this requirement. Further more, by overlaying the voltage curves, we can establish the sizing which fulfills the low supply voltage. As can be seen from Fig. 5.24, $W/L = 52/1.2\mu m$ fulfills these requirements, while needing only 850mV supply.

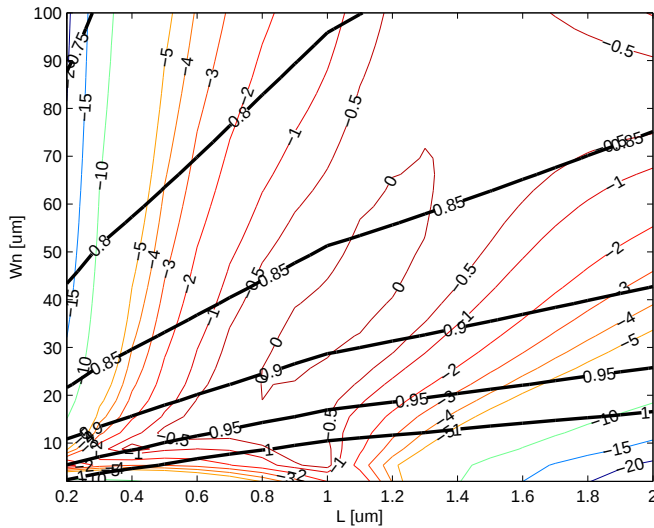


Fig. 5.24: Transistor sizes that fulfill (positive values) the minimum DC gain and GBW requirements and the corresponding supply voltages for a fixed bias current of $9\mu A$.

Increasing the bias current increases the GBW but has little effect on DC gain. At the same time it pushes the area that fulfills the minimum requirements down to the right on the graph, where it quickly becomes outside the available supply voltage. On the other hand decreasing the current reduces GBW and DC gain, below the required level.

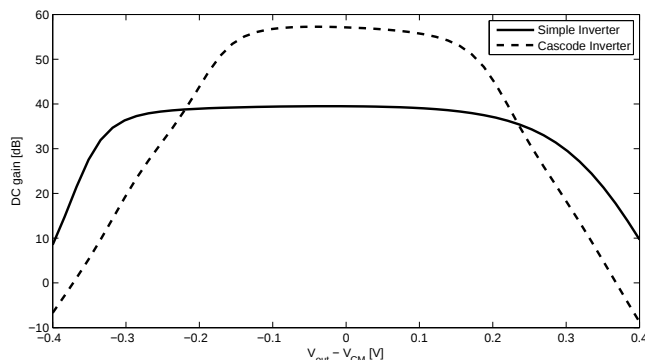


Fig. 5.25: DC gain versus output voltage for a simple inverter and a cascoded inverter to increase DC gain.

Cascodeing can be applied to inverters to increase the DC gain, but as with other topologies it reduces the output swing and the DC gain linearity. However, with careful sizing, these effects can be minimized. Fig. 5.25 shows the gain of two inverters, simple and cascoded, plotted against output voltage. However, the main problem with using the cascode inverter in a SC integrator is the drastic effect on slew rate. Using very wide cascode devices to increase the slew rate has limitations due to the increased effect of the internal node with its second pole. It can be concluded that the simple inverter is much more suitable for this application. It is, however, interesting to note that future smaller technologies, with further reduction in intrinsic gain, might render the simple inverter unfeasible, unless the gain requirements are further reduced.

Finally, it is important to realize that the performance of the inverter base OTA is highly dependent on supply voltage, temperature and process variations. One option is to employ replica biasing, where a separate unity OTA, outside the SD modulator, controls the biasing of the OTAs. This would, to large extent, cancel the variations with voltage, temperature and process. Designing the inverter OTA with 850mV supply, makes it feasible for such a regulation scheme to operate on a supply of 900mV. Further analysis and/or implementation of this concept is not pursued in this project.

5.4.2 Flicker noise reduction

For flicker ($1/f$) noise, the primary controlling factor is the total area $W \cdot L$, as stated before. When the signals of interest lie below the corner frequency, as is typically the case for audio signals, it would be of great benefit to be able to reduce the $1/f$ noise. This is possible with specific circuit techniques, namely auto-zeroing, correlated double sampling, chopper stabilization and switched biasing, which will be discussed next.

Auto-Zero (AZ)

The AZ technique works in two phases: during the sampling phase Φ_1 the noise is sampled on capacitor C while the inputs are shorted together and during the signal processing phase Φ_2 the noise sample is subtracted from the signal with noise. The $1/f$ noise is strongly reduced as the sampled noise and the low-frequency continuous $1/f$ noise are highly correlated during a sampling period. Fig. 5.26 shows the principle of operation [7].

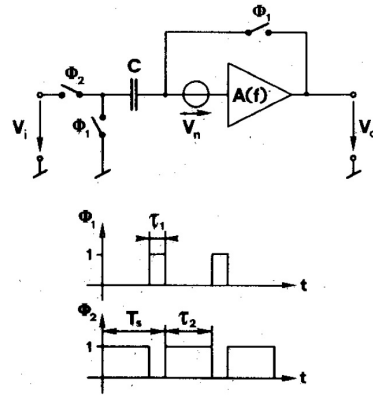


Fig. 5.26: Principle of the auto-zero technique [7].

The problem with the AZ technique is that while it effectively cancels low-frequency and DC noise components it is a sampling system and as such the wide-band thermal noise will be aliased down to the base-band, resulting in an increased in-band noise.

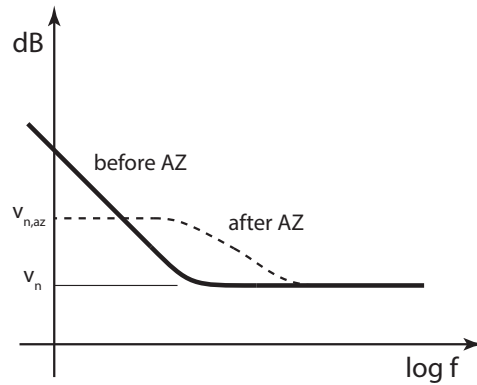


Fig. 5.27: Residual noise of AZ system.

Fig. 5.27 shows what the residual noise level looks like for a auto-zeroed system. The residual noise can be approximated as

$$V_{n,az} \approx \sqrt{\frac{2\pi f_c/2}{f_s}} \cdot V_n \quad (5.30)$$

for a first order LPF with $BW = \pi f_c/2$, and where f_c is the $1/f$ noise corner frequency, f_s is the sampling frequency and V_n is the thermal noise level [8]. Two possible switch arrangements realize the AZ for a SC integrator, one with a half delay integrator (Fig. 5.28(a)) and the other with a full delay integrator (Fig. 5.28(b)). As (5.30) shows, the wideband thermal noise level is increased due to the folding of the thermal noise by the sampling action.

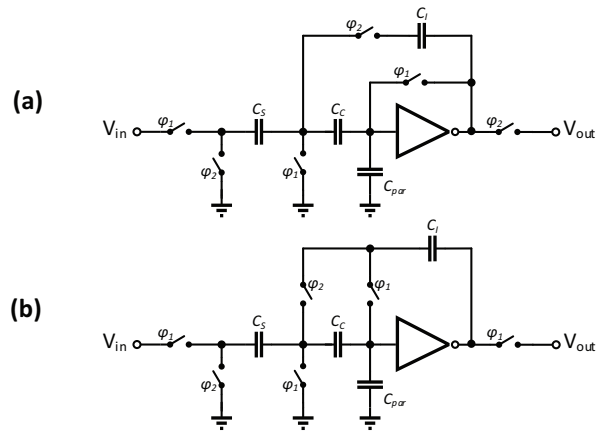


Fig. 5.28: Two possible implementation of AZ for a SC integrator, utilizing a half-delay integrator (a) and a full-delay integrator (b).

Correlated Double Sampling (CDS)

Correlated Double Sampling is a specific case of AZ where the circuit low-frequency noise is sampled twice in each period. It is best described as an AZ operation followed by a Sample-and-Hold (SH) operation. The effects of noise reduction are very similar to that of the AZ [7]. Fig. 5.29 show how CDS can be implemented in a SC integrator.

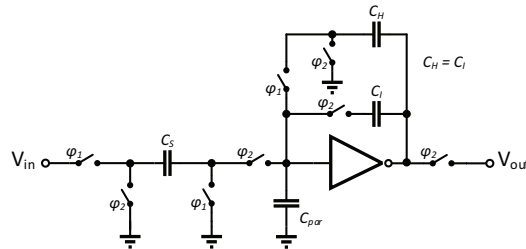


Fig. 5.29: Implementation of a CDS for a SC integrator.

Chopper Stabilized amplifier (CHS)

Chopper Stabilization is distinctively different from the previously discussed auto-zero technique as in it does not use sampling to remove low-frequency noise. Instead it uses modulation to transpose the signal to a higher frequency where there is no $1/f$ noise component and then demodulates it back to the base-band after amplification [7].

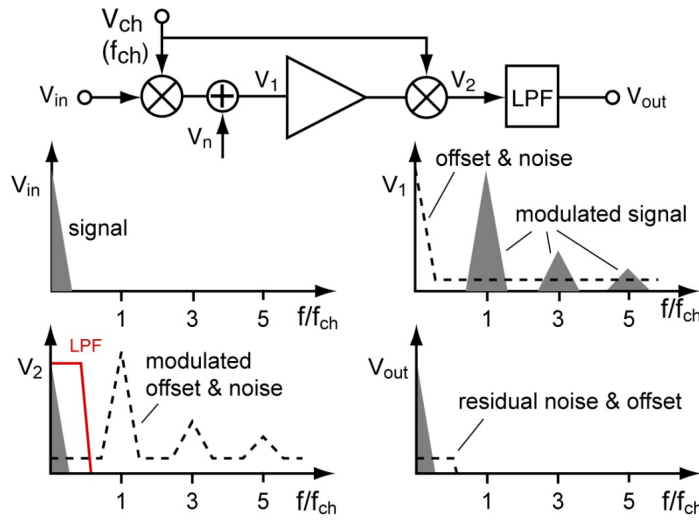


Fig. 5.30: Principle of the chopping technique [8].

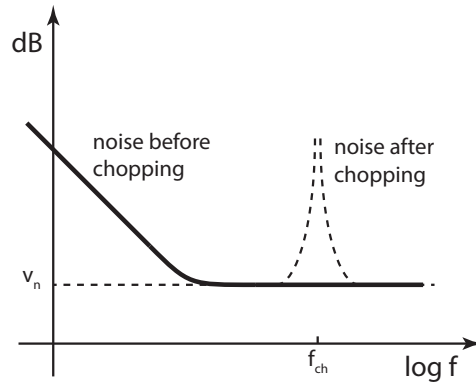


Fig. 5.31: Residual noise of the chopper stabilized system.

The system is comprised of input choppers, switches that modulate the signal, the amplifier with its internally generated noise, an output chopper which demodulates the signal and finally a low-pass filter. Figure 5.30 shows the system with its signal waveforms appearing along the signal chain. The $1/f$ noise can be completely removed using this technique, given that the chopping frequency, f_{ch} ,

is larger than the $1/f$ corner frequency [7]. The wide-band thermal noise is not reduced but it is not folded into the base-band as in the AZ. Fig. 5.31 shows the residual noise after chopping. It is important to note that the chopping frequency has to be outside the signal band.

It is clear that the CHS is much more effective at removing the low-frequency noise but at the expense of bandwidth. It should be noted that although the CHS effectively removes low-frequency noise, there will always be some residual offset due to charge injection and clock feedthrough of the chopper modulator [85], [86], [7]. In a SC integrator, two main approaches are used in adding a CHS. First, and perhaps the most obvious, is to simply flip the amplifier by adding crossed switches in series with its inputs and outputs as shown in Fig. 5.32. The other method is to flip the integrating capacitances instead of the amplifier. These two methods produce exactly the same results to first order approximation, the main difference lies in the settling behavior as described in [87].

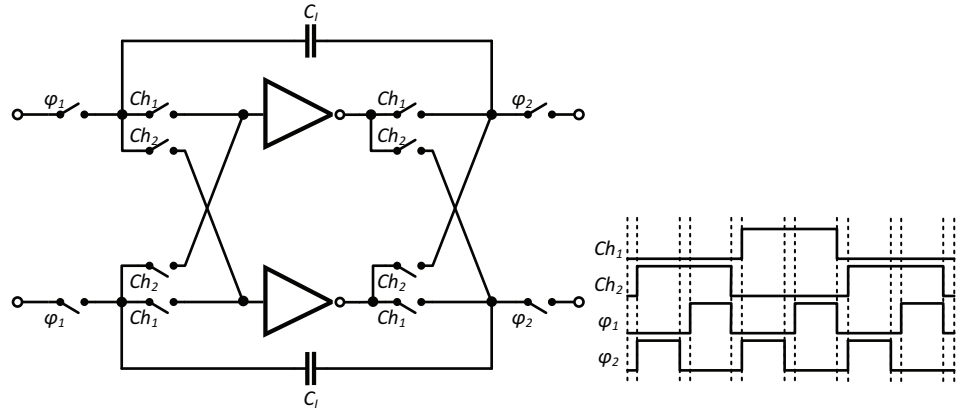


Fig. 5.32: Implementation of a CHS for use within a SC integrator.

Adding a chopper modulator to a $\Delta\Sigma$ modulator seems to be a simple task and without penalty, however, as [87] shows, there are some downsides that need to be considered. Even small parasitic capacitance at the amplifier input may lead to a significant performance degradation due to quantization noise demodulation into the baseband. Even parasitics as small as 32 aF for integrating capacitors of the order of 20pF start to degrade performance. There are additionally risks of coupling into the voltage references if the chopper is operated at $f_s/2$, which is the operation frequency for most designs found in the literature.

Switched Bias

Cycling a MOS transistor between strong inversion and accumulation reduces its $1/f$ noise, as first reported in 1991 by Bloom et. al [88]. Conceptually, this can be explained by looking at the properties of $1/f$ noise and realizing that it is a random process with a long memory and thus long self-correlation times, and by switching

the transistor off, this long term memory is interrupted and thus it cannot exhibit the same low-frequency behavior. This feature was first exploited in circuit design by Klumpernik et. al [9] in 2000, where the *switched biasing technique* is defined and applied to ring oscillators. In addition to reducing $1/f$ noise, by switching the devices off, power consumption can in theory be almost halved.

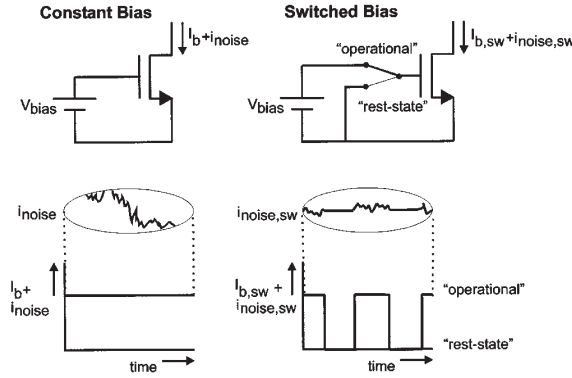


Fig. 5.33: The concept of switched biasing [9].

Periodically switching off transistors is of course not feasible for all circuits but the half-delay SC integrator does offer this freedom, as it only needs to be operational during the integration phase. Fig. 5.34 shows a possible implementation of an inverter that can be switched off. During turn-off, M_3 and M_4 cut off the supply voltage, while M_5 and M_6 short the drain and source ensuring that the sources are kept at the output level. A further reduction of the noise can be achieved by also applying switched forward substrate bias during the off state [89]. A very recent paper describes a $\Delta\Sigma$ modulator that uses switched-biasing to reduce $1/f$ noise in the feedback DAC [90], however, no $\Delta\Sigma$ modulator publications were found describing switched-biasing for the integrator OTAs.

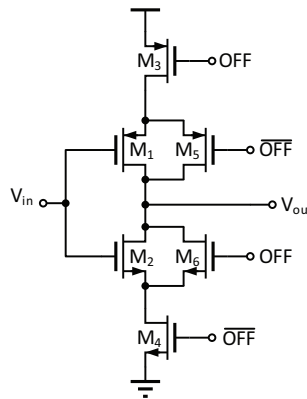


Fig. 5.34: An inverter that can be switched off, thus reducing power consumption and $1/f$ noise.

5.4.3 Switches

CMOS transistors are inherently good switches as they are high impedance during off-state and relatively low impedance during on-state. However, PMOS devices are only properly turned on when the input voltage is more than one threshold below the gate voltage and the same problem applies to NMOS devices. A simple solution to this problem is to use a pair of PMOS and NMOS switches, known as a transmission gate. This enables the switch to be fully turned on over the entire supply range. Another problem appears for low-voltage supplies. If the supply drops to around the sum of the threshold voltages, then there is a region around mid-supply where neither device is fully turned on. Many ways have been proposed to mitigate this problem, such as clock bootstrapping [91] and clock over-driving. Here we will assume that over-driven clocks are available, at $-V_{dd}$ and $2V_{dd}$ and to avoid oxide breakdown, thick oxide I/O devices are used. The downside of using over driven clocks with twice the voltage is that current dissipation at supply voltage level is at least doubled. Problems with using CMOS transmission gates is signal dependent charge injection and clock-feedthrough, however, spice simulations show that the distortion levels are far below what is required for our application and the offset can be minimized by delaying the sampling and feedback switches.

Switch sizing

From the noise analysis of SC integrators in section 4.4, we see that the time constant of the integrator is based on the switch resistance, R_{on} , and transconductance, G_m , of the OTA. It follows that the noise contribution from the switches and the amplifier are based on the ratio of R_{on} and the equivalent resistance of the amplifier, $1/G_m$. The time-constant $\tau = (2R_{on} + 1/G_m)C_1$ determines the Gain Bandwidth (GBW) of the integrator and thus R_{on} needs to be small enough and G_m large enough to achieve the required GBW. Fig. 5.35 shows how the power consumption of the integrator is composed of the switch drive current and the bias current for the inverter. For large switch resistance the amplifier dominates the power consumption as G_m needs to become very large but for very small R_{on} the switches need to become very large and thus the power required to drive the large input capacitance will dominate the power consumption.

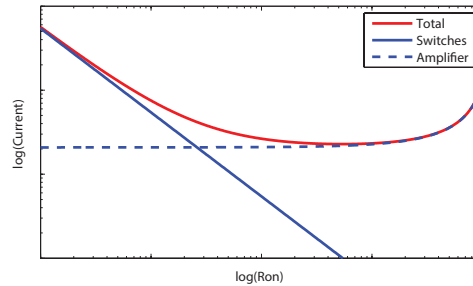


Fig. 5.35: Power consumption depending with different R_{on} given a fixed GBW requirement.

From this it is clear that there exists a optimum balance between the size of R_{on} and the inverter size. Fig. 5.35 shows how the switch size was determined for minimum power consumption and given the GBW requirements and inverter size previously set, the switch resistance was selected as 52Ω . The relative size of the NMOS and the PMOS in the transmission gate were then scaled to achieve near linear impedance over the full range of input voltages, resulting in $(W/L)_n = 0.26/16\mu m$ and $(W/L)_p = 0.26/48\mu m$. The switches for the second and third integrators are scaled down versions.

5.4.4 Quantizer

The quantizer for a single bit modulator consists simply of a comparator. The main requirements are low power and low-voltage operation where as the offset and noise requirements are quite relaxed for a third order $\Delta\Sigma$ modulator due to the suppression of the quantizer non-idealities. A simple low voltage, dynamic comparator is used, with a dynamic clocked pre-amplifier and a dynamic latch to minimize power consumption, shown in Fig. 5.36 [92]. The input differential pair are biased in weak inversion and the tail in triode to achieve maximum gain of around 11 V/V. The sizes are increased from minimum length to achieve below 20 mV offset under 3σ mismatch. A low-power SR-Nand latch follows the comparator to hold the output value.

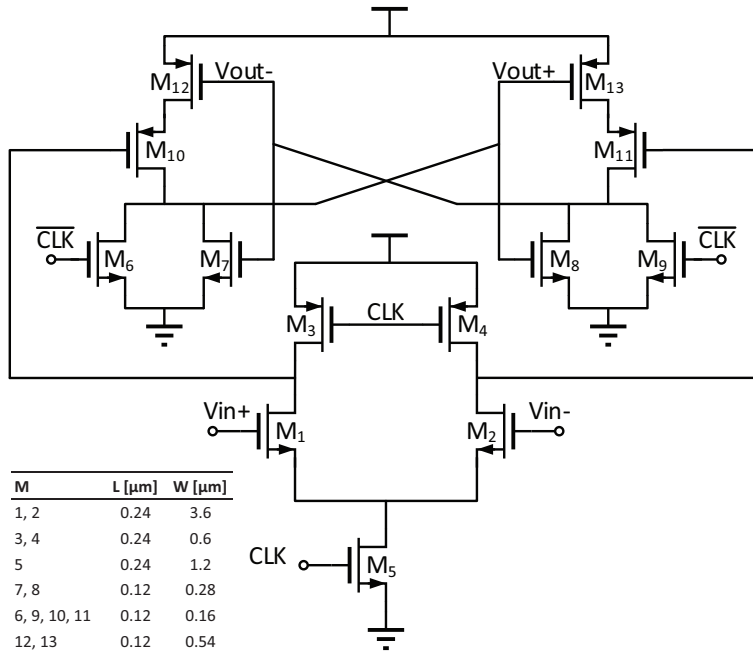


Fig. 5.36: A power efficient, low voltage, dynamic comparator used for the quantizer.

Fig. 5.37 shows the schematic for the complete modulator.

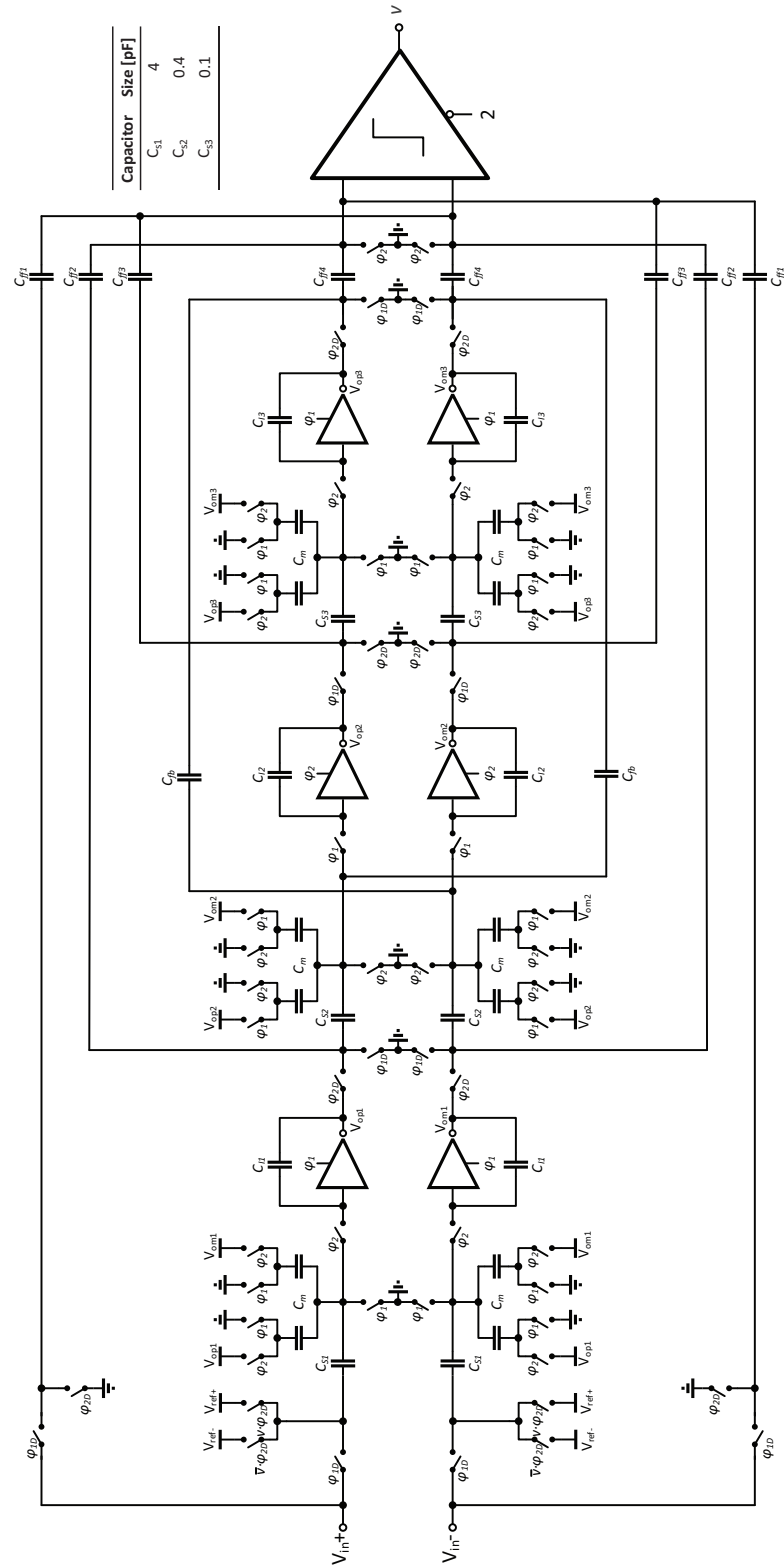


Fig. 5.37: Schematic of the complete modulator.

Results

During the course of this project many different converter topologies have been reviewed and state-of-the-art performance metrics compared, focusing on low-voltage, low-power and high-resolution converters. This extensive review has resulted in the selection of a switched capacitor delta-sigma ($\Delta\Sigma$) modulator for this particular application. Following this choice, a comprehensive analysis of $\Delta\Sigma$ modulators has been carried out, first from a theoretical perspective, then on a practical implementation level with high-level modelling, and lastly down to circuit level non-idealities affecting performance. This study has been essential to gain good understanding of the trade-offs involved in designing a high-performance $\Delta\Sigma$ ADC.

A thorough noise analysis for switched capacitor circuits has been introduced, allowing the design to be optimized for thermal noise performance. This is especially important for high-resolution converters where the thermal noise floor has a large impact on the power dissipation of the modulator. The analysis is a significant part of the modulator design process, especially considering the long run times for transient noise simulations in highly oversampled SC circuits.

The system level design, utilizes available high-level simulation tools for optimization, resulting in efficient transfer of an optimized topology to schematic level with minimum errors. A significant effort has been put into selecting and designing a low-noise, low-power, low-voltage compatible OTA. A total of six different OTA topologies have been analyzed and compared, based on multiple performance metrics, most importantly power dissipation and noise. An inverter based OTA is a good choice for the application with its excellent low-power, low-noise performance. The systematic transistor level design succeeds in sizing the transistors to achieve the required performance with minimum bias current. Finally, four different flicker noise reduction techniques for the OTAs have been reviewed, resulting in a novel switching scheme for the inverter which not only reduces flicker noise but also saves power. The circuit level design concludes with the design of a low-power dynamic comparator.

6.1 Simulated Performance

The modulator is simulated using the Spectre simulator in the Cadence Virtuoso Analog Design Environment with the TSMC 65nm CMOS technology. The high OSR, combined with the fact that at least 64 FFT bins should be resolved in the baseband¹, leads to very long transient simulation times. In addition, the high DR requirement of 98dB means that the simulator has to be set to “conservative” and the relative tolerances (RelTol) have to be further reduced 1e-5 to avoid arithmetic errors that corrupt the results.

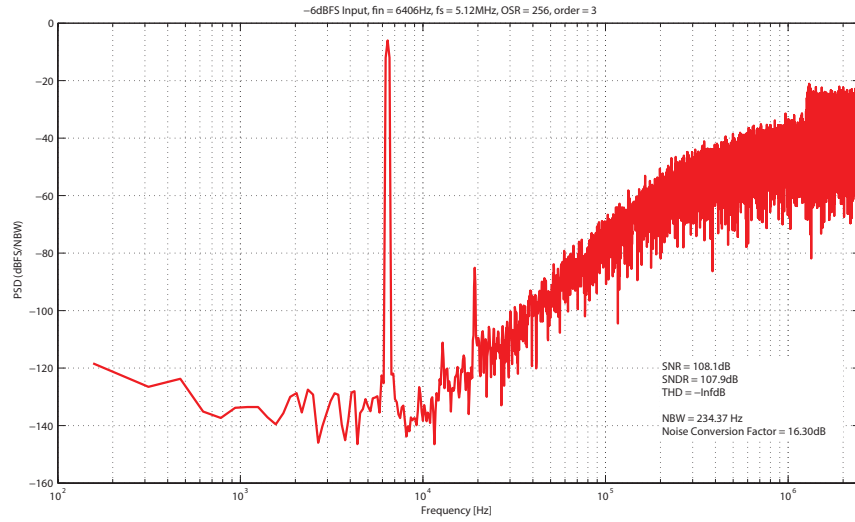


Fig. 6.1: A simulated spectrum for a -6 dBFS input signal.

Fig. 6.1 shows the simulated performance of the modulator for a -6 dBFS input signal at 6.4 kHz, without transistor level noise. The signal bandwidth is 10 kHz. The spectrum shows SNR of around 108dB, which is in line with the required quantization noise level. When simulating with a lower frequency input signal and taking into account distortion, the SNDR becomes 78dB, significantly lower than the SNR, but well above the required 54dB. This shows that we have successfully traded increased distortion for lower power consumption due to the low transconductance selected in the first integrator OTA. Fig. 6.2 shows how SNR and SNDR change with input amplitude. The DR is approximately 110dB, which with the addition of the thermal noise level calculated from (4.42) results in 99.5dB dynamic range. This calculation does not account for any extrinsic noise, but according to the noise budget we allocated 15% to extrinsic noise which results in **98.7 dB total DR**.

¹This is considered to be a minimum number of bins in the baseband for useful results, however 256 bins is often recommended.

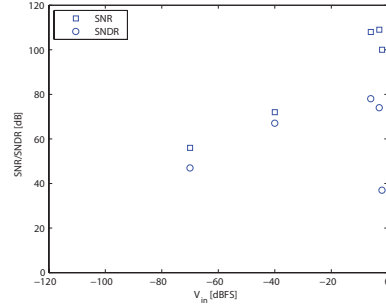


Fig. 6.2: Simulated performance versus input signal amplitude.

The simulations indicate that the average total supply current is approximately 43 μ A, 27 μ A for the first integrator, 10 μ A for the clock signals driving the switches and only 90 nA for the quantizer. This is below the requirements of 50 μ A. To compare with other similar ADCs, the FOMS based on SNDR (2.3) is

$$FOMS_{SNDR} = SNDR + 10 * \log\left(\frac{f_{bw}}{P}\right) = 162.4 \text{ dB} \quad (6.1)$$

This in itself is not remarkable, but if we consider that the application mainly requires high DR, while distortion was deliberately sacrificed, we can use Schreier's original figure of merit, based on dynamic range to get a fairer comparison

$$FOMS_{DR} = DR + 10 * \log\left(\frac{f_{bw}}{P}\right) = 183.1 \text{ dB} \quad (6.2)$$

Table 6.1 compares the proposed ADC to state-of-the-art published converters. Most of the converters try to maximize SNDR, however, the designs by Lee and Kumar specifically optimize DR. From the data it is clear that the proposed design achieves the best performance in terms of dynamic range.

Table 6.1: Performance comparison of published ADCs.

Names and year	Supply [V]	Tech [nm]	DR [dB]	SNDR [dB]	Bandwidth [kHz]	Power [μ W]	FOMS _{SNDR} [dB]	FOMS _{DR} [dB]
Akçakaya, 2013 *	N/A	180	76.8	76.8	25	16.9	168.5	168.5
Yao, 2004	1	90	88	81	20	130	162.9	169.9
Chae, 2008	0.7	180	85	81	20	36	168.4	172.4
Yang, 2012	0.5	120	85	81.7	20	35.2	169.2	172.5
Pena Perez, 2011	1.5	180	88	84	50	140	169.5	173.5
Park, 2008	0.7	180	100	95	25	870	169.6	174.6
Lee, 2009	1.6	180	80.2	35.6	11000	2540	132.0	176.6
Luo, 2013	0.8	70	98	91	20	230	170.4	177.4
Kumar, 2012 *	N/A	180	107.3	76.1	24	860	150.6	181.8
This work *	0.9	65	98.7	78	10	36.6	162.4	183.1

* Results based on simulations

6.2 Future Work and Research Opportunities

Due to the long simulation times, only a few simulations were completed and all without device noise. It would be worth spending more time to get more simulation points for different amplitude levels and possibly including device noise, although the results from benchmark simulations (especially the I/O transistors) were questionable. Significant effort is left to transfer the circuit to layout before any possible tape-out and actual circuit testing.

Looking into multi-bit design would be an interesting path to explore in more detail, especially trying to exploit intentional non-linearity to control SNR and DR independently as quickly discussed in section 2.3.

A further investigation into how OSR affects power consumption in thermal limited converters would also be very interesting. This seems to be a controversial subject as there were several conflicting statements found in the literature. Finally, a further review of the proposed switching scheme for the inverter OTA, especially its effect on flicker noise, could be interesting.

References

- [1] M. Mills, “Hearing aids and the history of electronics miniaturization,” *Annals of the History of Computing, IEEE*, vol. 33, no. 2, pp. 24–45, 2011.
- [2] B. Murmann, “Adc performance survey 1997-2014.” [Online]. Available: <http://www.stanford.edu/~murmann/adcsurvey.html>.
- [3] Z. Zhang and G. Temes, “Multibit oversampled σ - δ a/d convertor with nonuniform quantisation,” *Electronics Letters*, vol. 27, no. 6, pp. 528–529, 1991.
- [4] L. Yao, M. Steyaert, and W. M. Sansen, *Low-power low-voltage sigma-delta modulators in nanometer CMOS*, vol. 868. Springer, 2006.
- [5] B. E. Boser and B. A. Wooley, “The design of sigma-delta modulation analog-to-digital converters,” *Solid-State Circuits, IEEE Journal of*, vol. 23, no. 6, pp. 1298–1308, 1988.
- [6] K. Kundert, “Simulating switched-capacitor filters with spectrerf,” *The Designers Guide Community*, 2006.
- [7] C. C. Enz and G. C. Temes, “Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization,” *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.
- [8] K. A. A. Makinwa, “Smart sensor systems ’02.” Lectures, 2002.
- [9] E. A. Klumperink, S. L. Gierkink, A. P. van der Wel, and B. Nauta, “Reducing mosfet 1/f noise and power consumption by switched biasing,” *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 7, pp. 994–1001, 2000.
- [10] D. A. Johns and K. Martin, *Analog integrated circuit design*. Wiley. com, 2008.
- [11] T. Vos, A. D. Flaxman, M. Naghavi, R. Lozano, C. Michaud, M. Ezzati, K. Shibuya, J. A. Salomon, S. Abdalla, V. Aboyans, *et al.*, “Years lived with disability (ylds) for 1160 sequelae of 289 diseases and injuries 1990–2010: a systematic analysis for the global burden of disease study 2010,” *The Lancet*, vol. 380, no. 9859, pp. 2163–2196, 2013.

- [12] C. Mathers, A. Smith, and M. Concha, "Global burden of hearing loss in the year 2000," *Global burden of Disease*, vol. 18, 2000.
- [13] E. Van Eyken, G. Van Camp, and L. Van Laer, "The complexity of age-related hearing impairment: contributing environmental and genetic factors," *Audiology and Neurotology*, vol. 12, no. 6, pp. 345–358, 2007.
- [14] N. I. for Occupational Safety and Health, "Criteria for a recommended standard: occupational noise exposure: revised criteria 1998," *US Department of Health and Human Services Publication Number*, pp. 98–126, 1998.
- [15] R. Plomp, "Acoustical aspects of cocktail parties," *Acta Acustica united with Acustica*, vol. 38, no. 3, pp. 186–191, 1977.
- [16] H. Alexander, "Hearing aids: Smaller and smarter @ONLINE," November 1998.
- [17] H. Levitt, "Digital hearing aids : Wheelbarrows to ear inserts," *The ASHA Leader*, December 2007.
- [18] M. A. Hersh and M. A. Johnson, *Assistive technology for the hearing-impaired, deaf and deafblind*. Springer, 2003.
- [19] NIDCD, "The basics: Hearing aids @ONLINE," 2010.
- [20] K. Electronics, "Em-23356-c36." <http://www.knowles.com/eng/content/download/4560/62717/version/3/file/EM-23346-C36.pdf>, 2013.
- [21] Sonion, "65gc31." <http://www.sonion.com/Products/Transducers/Microphones/6500%20mni%20Microphone.aspx>, 2012.
- [22] InvenSense, "Inmp801." <http://www.invensense.com/mems/microphone/documents/INMP801.pdf>, 2014. originally from Analog Devices.
- [23] Sennheiser, "Mkh 800 p48." <http://en-us.sennheiser.com/studio-condenser-microphone-digital-recording-systems-mkh-800-p48>, 2014.
- [24] M. Chasin and F. A. Russo, "Hearing aids and music," *Trends in Amplification*, vol. 8, no. 2, pp. 35–47, 2004.
- [25] M. Chasin, "Hearing aids for musicians," *Hearing Review*, vol. 13, no. 3, p. 24, 2006.
- [26] ANSI, "Ansi s3. 22-2003, specification of hearing aid characteristics," 2003.
- [27] J. Agnew, "The causes and effects of distortion and internal noise in hearing aids," *Trends in Amplification*, vol. 3, no. 3, pp. 82–118, 1998.
- [28] T. Carusone, D. Johnson, and K. Martin, *Analog Integrated Circuit Design*. Analog Integrated Circuit Design, John Wiley & Sons, Limited, 2012.

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- [29] B. Le, T. W. Rondeau, J. H. Reed, and C. W. Bostian, "Analog-to-digital converters," *Signal Processing Magazine, IEEE*, vol. 22, no. 6, pp. 69–77, 2005.
- [30] F. Maloberti, F. Maloberti, and F. Maloberti, *Data converters*, vol. 1. Springer, 2007.
- [31] R. J. Baker, *CMOS: mixed-signal circuit design*. John Wiley & Sons, 2008.
- [32] R. H. Walden *et al.*, "Analog-to-digital converter survey and analysis," *IEEE Journal on selected areas in communications*, vol. 17, no. 4, pp. 539–550, 1999.
- [33] J. M. de la Rosa, "Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, no. 1, pp. 1–21, 2011.
- [34] B. Murmann, "A/d converter trends: Power dissipation, scaling and digitally assisted architectures," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pp. 105–112, IEEE, 2008.
- [35] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 11, pp. 2358–2368, 2005.
- [36] R. Schreier and G. Temes, "Understanding delta-sigma data converters," *IEEE PressPiscataway, NJ*, pp. 127–136, 2005.
- [37] H. Park, K. Nam, D. K. Su, K. Vleugels, and B. A. Wooley, "A 0.7-v 870-w digital-audio cmos sigma-delta modulator," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 4, pp. 1078–1088, 2009.
- [38] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 2, pp. 458–472, 2009.
- [39] F. Michel and M. S. Steyaert, "A 250 mv 7.5 μ w 61 db sndr sc $\delta\sigma$ modulator using near-threshold-voltage-biased inverter amplifiers in 130 nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 3, pp. 709–721, 2012.
- [40] H. Luo, Y. Han, R. C. Cheung, X. Liu, and T. Cao, "A 0.8-v 230-w 98-db dr inverter-based modulator for audio applications," 2013.
- [41] Z. Yang, L. Yao, and Y. Lian, "A 0.5-v 35-w 85-db dr double-sampled modulator for audio applications," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 3, pp. 722–735, 2012.
- [42] F. M. Akcakaya and G. Dundar, "Low power sigma delta converter with sar adc for audio frequencies," in *Faible Tension Faible Consommation (FTFC), 2013 IEEE*, pp. 1–4, IEEE, 2013.

- [43] L. Yao, M. S. Steyaert, and W. Sansen, "A 1-v 140- μ w 88-db audio sigma-delta modulator in 90-nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 11, pp. 1809–1818, 2004.
- [44] J. R. Custodio, J. Goes, N. Paulino, J. P. Oliveira, and E. Bruun, "A 1.2-v 165-w 0.29-mm multibit sigma-delta adc for hearing aids using nonlinear dacs and with over 91 db dynamic-range," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 7, no. 3, pp. 376–385, 2013.
- [45] S. Kumar and S. Chatterjee, "A 110-db dynamic range, 76-db peak snr companding continuous-time? s modulator for audio applications," in *Proceedings of the 2012 25th International Conference on VLSI Design*, pp. 51–56, IEEE Computer Society, 2012.
- [46] D. R. Smith, *Digital transmission systems*. Springer, 2004.
- [47] J. Mahattanakul, "Logarithmic data converter suitable for hearing aid applications," *Electronics Letters*, vol. 41, no. 7, pp. 394–396, 2005.
- [48] F. Francesconi and F. Maloberti, "A low power logarithmic a/d converter," in *Circuits and Systems, 1996. ISCAS'96., Connecting the World., 1996 IEEE International Symposium on*, vol. 1, pp. 473–476, IEEE, 1996.
- [49] J. Lee, J. Kang, S. Park, J.-s. Seo, J. Anders, J. Guilherme, and M. P. Flynn, "A 2.5 mw 80 db dr 36 db snr 22 ms/s logarithmic pipeline adc," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 10, pp. 2755–2765, 2009.
- [50] C. Cutler, "Transmission systems employing quantization," March 1960. US Patent 2,927,962.
- [51] C. Cutler, "Differential quantization of communication signals," July 1952. US Patent 2,605,361.
- [52] B. Derjavitch and M. Edmond, "Communication system utilizing constant amplitude pulses of opposite polarities," Feb. 24 1953. US Patent 2,629,857.
- [53] H. Inose, Y. Yasuda, and J. Murakami, "A telemetering system by code modulation- δ - σ modulation," *Space Electronics and Telemetry, IRE Transactions on*, no. 3, pp. 204–209, 1962.
- [54] D. J. Goodman, "The application of delta modulation to analog-to-pcm encoding," *Bell System Technical Journal*, vol. 48, no. 2, pp. 321–343, 1969.
- [55] Y. Geerts, M. Steyaert, and W. M. Sansen, *Design of multi-bit delta-sigma A/D converters*. Springer, 2002.
- [56] J. C. Candy and G. C. Temes, *Oversampling delta-sigma data converters: theory, design, and simulation*. IEEE press New York, 1992.
- [57] C. Toumazou, G. S. Moschytz, and B. Gilbert, *Trade-offs in analog circuit design: the designer's companion*. Springer, 2004.

- [58] W. L. Lee and C. G. Sodini, "A topology for higher order interpolative coders," ISCAS PROC, 1987.
- [59] V. Srinivasan, V. Wang, P. Satarzadeh, B. Haroun, and M. Corsi, "A 20mw 61db sndr (60mhz bw) 1b 3 rd-order continuous-time delta-sigma modulator clocked at 6ghz in 45nm cmos," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pp. 158–160, IEEE, 2012.
- [60] H. Shibata, R. Schreier, W. Yang, A. Shaikh, D. Paterson, T. C. Caldwell, D. Alldred, and P. W. Lai, "A dc-to-1 ghz tunable rf adc achieving dr 74 db and bw 150 mhz at 450 mhz using 550 mw," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 12, pp. 2888–2897, 2012.
- [61] E. Martens, A. Bourdoux, A. Couvreur, P. Van Wesemael, G. Van der Plas, J. Craninckx, and J. Ryckaert, "A 48-db dr 80-mhz bw 8.88-gs/s bandpass $\delta\sigma$ adc for rf digitization with integrated pll and polyphase decimation filter in 40nm cmos," in *VLSI Circuits (VLSIC), 2011 Symposium on*, pp. 40–41, IEEE, 2011.
- [62] L. Luh, J. F. Jensen, C.-M. Lin, C.-T. Tsen, D. Le, A. E. Cosand, S. Thomas, and C. Fields, "A 4ghz 4th-order passive lc bandpass delta-sigma modulator with if at 1.4 ghz," in *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, pp. 168–169, IEEE, 2006.
- [63] S. R. Norsworthy, R. Schreier, G. C. Temes, *et al.*, *Delta-sigma data converters: theory, design, and simulation*, vol. 97. IEEE press New York, 1996.
- [64] R. Schreier, "Delta sigma toolbox." 14 Jan 2000 (Updated Dec 2011) [Online]. Available: <http://www.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox>.
- [65] B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," *Solid-State Circuits, IEEE Journal of*, vol. 26, no. 4, pp. 618–627, 1991.
- [66] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. Analysis and Design of Analog Integrated Circuits, Wiley, 2009.
- [67] W. K. Chen, *The electrical engineering handbook*. Academic press, 2004.
- [68] S. Tedja, J. Van der Spiegel, and H. Williams, "Analytical and experimental studies of thermal noise in mosfet's," *Electron Devices, IEEE Transactions on*, vol. 41, pp. 2069–2075, Nov 1994.
- [69] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill higher education, Tata McGraw-Hill, 2002.

- [70] B. Murmann, "Thermal noise in track-and-hold circuits: Analysis and simulation techniques," *Solid-State Circuits Magazine, IEEE*, vol. 4, no. 2, pp. 46–54, 2012.
- [71] J. Phillips and K. Kundert, "Noise in mixers, oscillators, samplers, and logic an introduction to cyclostationary noise," in *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000*, pp. 431–438, IEEE, 2000.
- [72] M. Terrovitis and K. Kundert, "Device noise simulation of $\delta\sigma$ modulators," *The Designer's Guide Community (www.designers-guide.org)*, 2004.
- [73] K. Francken and G. G. Gielen, "A high-level simulation and synthesis environment for $\delta\sigma$ modulators," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 22, no. 8, pp. 1049–1061, 2003.
- [74] G. G. Gielen and J. E. Franca, "Cad tools for data converter design: An overview," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 43, no. 2, pp. 77–89, 1996.
- [75] T. Eeckelaert, R. Schoofs, G. Gielen, M. Steyaert, and W. Sansen, "Hierarchical bottom-up analog optimization methodology validated by a delta-sigma a/d converter design for the 802.11 a/b/g standard," in *Proceedings of the 43rd annual Design Automation Conference*, pp. 25–30, ACM, 2006.
- [76] J. Silva, U. Moon, J. Steensgaard, and G. Temes, "Wideband low-distortion delta-sigma adc topology," *Electronics Letters*, vol. 37, no. 12, pp. 737–738, 2001.
- [77] J. Steensgaard, "Nonlinearities in sc delta-sigma a/d converters," in *Electronics, Circuits and Systems, 1998 IEEE International Conference on*, vol. 1, pp. 355–358, IEEE, 1998.
- [78] J. Steensgaard-Madsen, *High-performance data converters*. PhD thesis, The Technical University of Denmark, 1999.
- [79] J. Karki, "Fully-differential amplifiers," *Application Report, sloa054*, 2000.
- [80] F. Khateb, D. Birolek, N. Khatib, and J. Vavra, "Utilizing the bulk-driven technique in analog circuit design," in *Design and Diagnostics of Electronic Circuits and Systems (DDECS), 2010 IEEE 13th International Symposium on*, pp. 16–19, IEEE, 2010.
- [81] N. Krishnapura, "Lecture 46 in analog integrated circuit design," 2012.
- [82] J. Xu, M. Zhao, X. Wu, and X. Yan, "Low voltage low power current mirror ota for sigma-delta modulator," in *Electron Devices and Solid-State Circuits, 2007. EDSSC 2007. IEEE Conference on*, pp. 875–879, IEEE, 2007.
- [83] T.-H. Lin, C.-K. Wu, and M.-C. Tsai, "a 0.8-v 0.25-mw current-mirror ota with 160-mhz gbw in 0.18- μ m cmos," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 54, no. 2, pp. 131–135, 2007.

- [84] J. Silva-Martinez, "Lecture tamu-elen-472," 2008.
- [85] C. C. Enz, E. A. Vittoz, and F. Krummenacher, "A cmos chopper amplifier," *Solid-State Circuits, IEEE Journal of*, vol. 22, no. 3, pp. 335–342, 1987.
- [86] A. Bakker, K. Thiele, and J. H. Huijsing, "A cmos nested-chopper instrumentation amplifier with 100-nv offset," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 12, pp. 1877–1883, 2000.
- [87] G. Léger, A. J. Gines Arteaga, E. J. Peralias Macias, and A. Rueda, "On chopper effects in discrete-time modulators," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 57, no. 9, pp. 2438–2449, 2010.
- [88] I. Bloom and Y. Nemirovsky, "1/f noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation," *Applied physics letters*, vol. 58, no. 15, pp. 1664–1666, 1991.
- [89] D. Siprak, M. Tiebout, N. Zanolla, P. Baumgartner, and C. Fiegna, "Noise reduction in cmos circuits through switched gate and forward substrate bias," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 7, pp. 1959–1967, 2009.
- [90] S. Sutula, J. Pallares Cuxart, J. Gonzalo-Ruiz, F. X. Muñoz-Pascual, L. Teres, and F. Serra-Graells, "A 25- μ w all-mos potentiostatic delta-sigma adc for smart electrochemical sensors,"
- [91] J. Steensgaard, "Bootstrapped low-voltage analog switches," in *Circuits and Systems, 1999. ISCAS'99. Proceedings of the 1999 IEEE International Symposium on*, vol. 2, pp. 29–32, IEEE, 1999.
- [92] M. Van Elzakker, E. Van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9 μ w 4.4 fj/conversion-step 10b 1ms/s charge-redistribution adc," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 244–610, IEEE, 2008.



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