Master's Thesis

Time Domain Electromagnetic (EM) Simulations for IC Packages Modeling

Shubo Yan

Department of Electrical and Information Technology,
Faculty of Engineering, LTH, Lund University, June 2014.

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Department of Electrical and Information Technology
Faculty of Engineering, LTH, Lund University
SE-221 00 Lund, Sweden

Abstract

Because the duration of charged device model (CDM) events is short, CDM-induced damage most often manifests as oxide breakdown. The high current density exists during an electrostatic discharge (ESD) event can cause thermal damage and induce voltages sufficient to damage gate oxides. Effective protection against ESD is critical for high yield and reliability of ICs. It is necessary to study the discharge path to improve the CDM robustness. In this thesis, an accurate and simple model of IC packages under electrostatic discharge (ESD) charged device model (CDM) was presented for the circumstances of using new type of electromagnetic simulations.

To understand the discharge phenomenon and strengthen the protection designs, the accurate and efficient CDM discharge simulation has become very important. Here, the electromagnetic professional (EMPro®) software is adopted in this study. The 3D model of LQFP64 IC package was established and optimized in the EMPro® simulation environment. Then, the LQFP64 package of ICs was also characterized in the actual measurements, i.e. time domain reflectometry (TDR) is applied to extract the parasitics. The simulation model had been updated based on the experimental testing results. And the comparison between the EMPro® simulation results and the testings had been conducted completely. There is a good agreement between the simulation and tested results.

In summary, the feasibility of using the 3D simulation model of IC package based on the EMPro® software was presented in this thesis for LQFP64. Then the parasitics of the LQFP64 package for the lumped elements model are extracted through using the TDR measurement. So the lumped elements parameters of a typical PUT extracted from TDR measurements of the IC packages are obtained. Finally, the extracted lumped circuit is integrated into the model and used to simulate the CDM discharge and compare to actual CDM discharge waveforms measured from these IC packages.

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CHAPTER 1

1 Introduction

1.1 NXP Semiconductors

This project has been sponsored by Foundation Design Intellectual Property (FDIP) department under Foundation Technology unit of Central R&D at NXP Semiconductors in Nijmegen in the Netherlands. NXP Semiconductors, established in 2006 from 50-year experience of Philips Semiconductors, provides high performance mixed-signal and standard product solutions that leverage its leading RF analog, power management, interface, security and digital processing expertise.

With an employee base of about 29,000 from over 25 countries all worldwide, NXP Semiconductors posted total revenue of $ 4.82 billion in 2013. It provides products in eight key application areas namely, automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing through its business units which are high performance mixed signal, identification, automotive and standard products.

The IO/ESD team from the FDIP is responsible for supporting the BLs by designing and qualifying IOs with required Electrostatic Discharge (ESD) and Latch-up protections as well as reviewing chip designs for their ESD robustness in the IOs.

1.2 Objectives of the project

1.2.1 Characterization and Modeling of IC packages

IC packaging not only provides the physical/mechanical support for the device, the package is also responsible for the interconnection between the chip and external terminal (e.g. the printed circuit board, PCB). Without a successful IC packaging process, the chip is not able to become a real product or solution to fulfill the end customer requirement, no matter how good the design and wafer process might be[1]. So, in prediction, IC market will reach $42 billion in 2016[2]. Advancements in IC packaging have allowed the final product to become smaller, cheaper, and thus more

desirable to the final customer. 3D IC technology appears as a platform solution to allow end users to integrate multi-function chips, thereby enabling heterogeneous integration in one package[1]. This imposes challenges for the packaging technologies, which means much more factors should be considered, such as the effect of electrostatic charge, the size of the package, the frequency of operation and the processing technology.

In order to select the right package from different suppliers, semiconductor companies need to check them through modelling and correlating with lab tests. The frequency range of the product is the first thing to be known. Below 1GHz, quasi-static tools can be used, i.e. 2.5D EM planar. 3D Electromagnetic (EM) solvers are needed when the frequency operation exceeds 1GHz. EM solvers are more widely used in the industry today, but 3D EM solvers are more expensive because they are built on complex Maxwell's equation. Sometimes, due to the high license costs of some commercial softwares, e.g. high frequency structural simulator (HFSS®), some companies usually do not have the full license for all applications, so the electromagnetic professional (EMPro®) software is adopted in this project.

The electrostatic discharge (ESD) sensitivity of ICs with respect to the charged-device model (CDM) is strongly dependent on the IC package, the substrate resistivity, and the effectiveness of the ESD protection network. Electrostatic discharge (ESD) is defined as " the rapid, spontaneous transfer of electrostatic charge induced by a high electrostatic field. Usually, the charge flows through a spark between two bodies at different electrostatic potentials as they approach one another "[3]. Many pins of the IC devices are protected against ESD up to a certain level as defined in their quality and reliability specifications. For understanding of the CDM current distribution and for predicting the voltage drop across some CDM sensitive circuit topologies such as cross-domain devices, it is necessary to establish a simple and accurate model for CDM simulation[4]. In order to study the modeling feasibilities of using EMPro® software for IC package simulation, the 3D model of LQFP64 package is adopted in this project. The 3D model of LQFP64 was verified with that under HFSS® simulation environment and also the time-domain reflectometry (TDR) technique.

1.2.2 Measurements on LQFP64 packages

Time Domain Reflectometry as a technique for characterization will be used on LQFP64 package. In this study, the time domain reflectometry (TDR) approach is to extract the actual lumped elements model of the IC

package. The overall TDR system has 42ps rise time, which decides the resolution of the TDR hardware. TDR uses a technique that is comparable to radar: the TDR instrument sends a fast electrical pulse through the pin under test (PUT) and monitors the time to receive reflections. These reflections can correspond to capacitive, inductive, or resistive distortion of the PUT impedance. The resulting waveform is the combination of the incident step and reflections generated when the step encounters impedance deviations from 50 Ohm.

An inductive discontinuity will be visible on a TDR waveform as a spike above the impedance of the surrounding transmission lines, whereas a capacitive discontinuity will be visible as a dip in the impedance profile waveform. The parasitic extraction method described in the previous section has been applied to LQFP64. The lumped circuit extracted by the TDR approach from a PUT of the LQPF64 package of the test case is derived as shown in Figure 6.4.

The parasitics of the LQFP64 package for the lumped elements model are extracted after using the TDR measurement. Here, the scrip code from matlab® software is used for processing the experimental data and plot the voltage waveform. So the lumped elements parameters of a typical PUT extracted from TDR measurements of IC packages are obtained. Then the extracted lumped circuit is integrated into the model and used to simulate the CDM discharge and compare to actual CDM discharge waveforms measured from these IC packages.

CHAPTER 2

2 Packaging

Packing the integrated circuit (IC) chip is an essential step in the manufacturing process because the IC chips are small, fragile, susceptible to environmental damage, and too difficult to handle by the IC users. Hermetically sealed parts are ones where the IC chip is enclosed in a sealed compartment and outside chemicals and gases cannot reach the die. In addition, the package acts as a mechanism to spread apart the connections from the tight pitch on the IC die to the relatively wide pitch required by the Printed Circuit Board (PCB) manufacturer.

2.1 Pad Pitch

The pad pitch on the IC chip is typically 6 mils (152um). This spacing is already much larger than the 0.08 to 0.31 mils pitch of the wiring on the IC chip. However, PCB wiring requires an even larger pitch, usually between 40 and 100 mils. The package acts as a "bridge" between the two sizes, effectively spreading spart the spacing from the IC chip dimensions to the PCB dimensions, as shown in Fig 2.1. Hermetically sealed parts are ones where the IC chip is enclosed in a sealed compartment and outside chemicals and gases cannot reach the die.

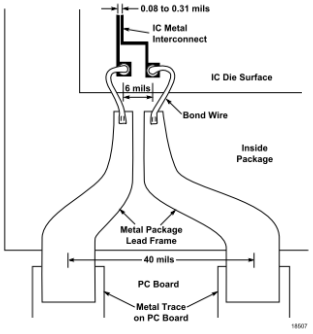

Fig. 1.1 IC Chip to PCB Lead Spacing

2.2 Dual In-Line Packages (DIPs)

The lead configuration consists of two rows of leads, typically both with 100 mil (3.9mm) pitch, as shown in Fig 2.2. The plastic, side-braze and cerdip packages are its hermetic alternatives. Both side-braze and cerdip packages are available with quartz windows in the top for erasable programmable read only memory (EMPROM) devices so the chip can be erased with ultraviolet light.

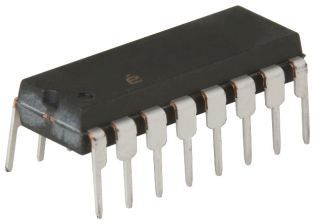

Fig. 2.2 Dual In-Line Packages (DIPs)

2.3 Single In-Line Package (SIPs)

The single in-line package is another alternative to the DIP, as shown in Fig 2.3. It is an IC package that has a single row of leads protruding from the bottom of its body, which is not as popular as the DIP, but has been used for packaging random access memory (RAM) chips and multiple resistors with a common pin.

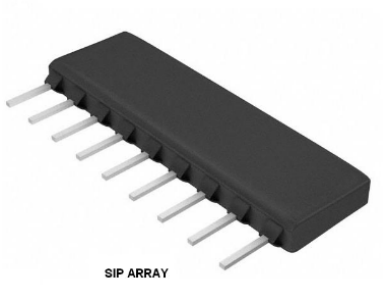

Fig. 2.3 Single In-Line Packages (SIPs)

2.4 Pin Grid Arrays

The pin grid arrays can solve the high pin count IC chip requirements, which cover most of or all of the entire bottom surface of the package, as shown in Fig 2.4. The packages are offered in pin counts from about 100 to 600 pins, and are available with heatsinks to help remove the heat generated

inside the package. This can be a problem with fast clock rate microprocessor chips where the frequent switching generates significant heat.

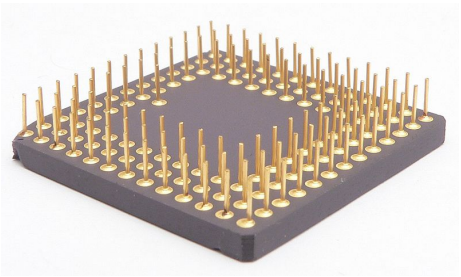

Fig. 2.4 Pin Grid Arrays

2.5 Quad Flat Package

Quad Flat Package that is surface-mounted integrated circuit package with "gull wing" leads extending from each of the four sides, as shown in Fig 2.5. The board space is solved through the use of surface mount packaging. A package related to QFP is PLCC which is similar but has pins with larger pitch.

Fig. 2.5 Quad Flat Package

2.5.1 Low Profile Quad Flat Package (LQFP)

Pins for LQFP packages are numbered counter-clockwise from the index dot, as shown in Fig 2.5.1. Based on the area of deployment and operating considerations, such as power and frequency, the spacing between pins on an LQFP can vary.

Fig. 2.5.1 Low Quad Flat Package (LQFP)

2.5.2 Metric Profile Quad Flat Package (MQFP)

The Metric Quad Flat Package (MQFP) is a surface-mount IC package with gull wing leads on all four sides of the package body, as shown in Fig 2.5.2.

The MQFP comes in different body sizes that range from 10 mm square to 40 mm square. The MQFP leads counts, on the other hand, range from 44 to 304. Typical lead pitch values used by MQFP's range is from 0.55 mm to 0.80 mm. Typical MQFP body thickness values range from 2 mm to 3.5 mm.

Fig. 2.5.1 Low Quad Flat Package (LQFP)

2.6 Plastic Leaded Chip Carrier (PLCC)

The Plastic Leaded Chip Carrier is a four-sided plastic package that has "J" leads around its periphery, as shown in Fig 2.6. These "J" leads occupy less board space than the gull-wing leads that other packages like SOIC have. PLCC packages can either be square or rectangular in shape. The ceramic equivalent of the PLCC is JLCC.

Fig. 2.6 Plastic Leaded Chip Carrier (PLCC)

2.7 Flip Chip Ball Grid Array (FCBGA)

Flip chip ball grid array packages allow for much higher pin count than other package types. In an FCBGA package the die is mounted upside-down (flipped) and connects to the package balls via a substrate that is similar to a printed-circuit board rather than by wires, as shown in Fig 2.7. FCBGA packages allow an array of input-out signals (called Area I/O) to be distributed over the entire die rather than being confined to the die periphery. Also, it can support a high speed double-data rate interface.

Fig. 2.7 Flip Chip Ball Grid Array (FCBGA)

2.8 Fine-Pitch Ball Grid Array (FBGA)

The Fine Pitch Ball Grid Array is a smaller version of the ball grid array package. As in all BGA packages, FBGA's use solder balls that are arranged in a grid or array at the bottom of the package body for external electrical connection. However, the FBGA is near-chip-scale in size, with a

smaller and thinner body than the standard BGA package. As its name implies, it also features a finer ball pitch (smaller distance between balls).

Fig. 2.8 Fine-Pitch Ball Grid Array (FBGA)

2.9 Low Profile Fine-Pitch Ball Grid Array (LFBGA)

The Low-Profile Fine Pitch Ball Grid Array is a smaller version of the ball grid array package. It is basically an FBGA package that has a package height ranging from 1.2 mm and 1.7 mm. It is therefore thicker than the Thin Profile Fine-Pitch Ball Grid Array (TFBGA) and the very thin Profile Fine-Pitch Ball Grid Array (VFBGA).

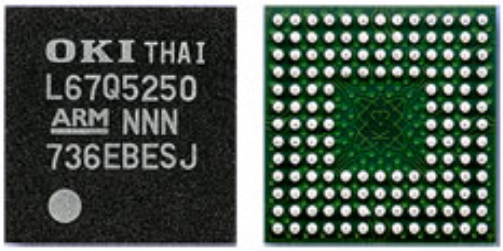

Fig. 2.9 Low Profile Fine-Pitch Ball Grid Array (LFBGA)

CHAPTER 3

3 ESD Basics

3.1 ESD Phenomenon

The phenomenon of electrostatic discharge (ESD) occurs when an electrostatic voltage slowly develops between an object and its surrounding environment, commonly referred to as earth or ground, then spontaneously discharges as an electrical current impulse. ESD is single-event, rapid transfer of electrostatic charge between two objects, usually resulting when two objects at different potentials come into direct contact with each other, which is a transient discharge of static charge that arises from either human handling or machine contact.

Electrostatic charge build-up occurs as a result of an imbalance of electrons on the surface of a material. Such a charge build-up develops an electric field that has measurable effects on other objects at a distance. The process of electron transfer as a result of two objects coming into contact with each other and then separating is known as “triboelectric charging”.

This charging process results in one object gaining electrons on its surface, and therefore becoming negatively charged, and another object losing electrons from its surface and therefore becoming positively charged.

One measure to control the level of charge and electrostatic voltage as well as the magnitude of the current transient is to provide a safe path for the flow and recombination of the charge by means of a moderate surface resistance in the range of some kΩ/sq…MΩ/sq.

If any of these ESD controls fail, the electrostatic voltages can increase, causing spontaneous high-current impulses with a duration in the range of 1ns to 1us, which can either charge the sensitive IC or discharge through it.

3.2 ESD failures and their attributes

Electrostatic Discharge (ESD) is a special type of Electrical Overstress (EOS) mechanism in the form of a single-event, rapid transfer of electrostatic charge between two objects. ESD can destroy a semiconductor

device in many ways, resulting in observable signs of damage or failure attributes. These mechanisms are dielectric or oxide punch through, fusing of a conductor or resistor and junction damage or burn-out.

3.2.1 Dielectric or Oxide Punch through

Dielectric or oxide punch refers to the ESD mechanism involving a voltage pulse that is large enough to rupture an oxide or dielectric layer. This problem is prevalent in MOS circuits because the thin oxide isolating the gate and the channel of the MOS transistor can easily be "punch through" by large voltage spikes. Trends in new fab processes that lean towards thinner oxide layers also aggravate the occurrence of this mechanism.

A typical dielectric punch through event may occur in the following stages:

(1) A high voltage spike occurs between two pins connected to opposite sides of a dielectric layer, in effect applying a large potential difference across the dielectric layer;

(2) The breakdown voltage of the dielectric layer is exceeded by the large potential difference across it;

(3) The dielectric breaks down and starts conducting current;

(4) Adiabatic or localized heating of the dielectric at the point of current conduction occurs;

(5) The conduction site melts down forming a filament that shorts the metal layer above the dielectric (connected to one of the pins) and the metal layer below the dielectric layer (connected to the other pin).

Dielectric punch through is minimized by using adequate ESD protection circuits and prevention of EOS occurrences, such as the inadvertent or random generation of voltage spikes in the circuit.

3.2.2 Conductor / Resistor Fusing

The phrase 'Conductor/Resistor Fusing' literally pertains to a metal line or resistor that acted as a 'fuse', or one that has become open due to excessive current. Such melting of a metal or resistor line is often due to intense heat produced by excessive power dissipation caused by an ESD event that involves a large current flow through the conductor or resistor. Conductor/resistor fusing is also sometimes referred to as 'metal burn-out' or 'resistor burn-out'.

The high power generated during the ESD event is equal to Ie^2R, where Ie is the ESD current and R is the resistance of the metal or resistor line. If this power produces enough localized heat to bring the ESD site's temperature above the melting temperature of the conductor or resistor, then the fusing, meltdown, or burn-out of the conductor/resistor occurs.

Conductor/resistor fusing is often just a secondary mechanism of another ESD failure, such as a dielectric or junction damage that has created a short circuit where large currents can flow to subsequently cause the conductor/resistor line to melt down or burn out.

3.2.3 Junction Damage or Burn-out

Junction damage or burn-out refers to the destruction of a p-n junction due to joule-heating caused by the ESD event, resulting either in the junction's being open or short-circuited. This type of damage also involves joule heating, and is more prevalent in bipolar devices.

Hot spots arise in the junction when it undergoes joule heating, especially in parts where there are non-homogeneities and geometrical shifts. Silicon where these hot spots arise becomes intrinsic in nature, whereby its resistivity goes down as temperature goes up. The reduction in resistivity further sinks more current, increasing the temperature further.

This cycle continues, resulting in a thermal runaway that eventually melts the silicon with the hot spot when its temperature exceeds the melting point of silicon. The silicon meltdown often creates a short across the junction, although high-energy transient ESD events can also result in open junctions.

The power that heats up the junction is equal to Ie^2VBD, where Ie is the ESD current and VBD is the breakdown voltage of the junction. Reverse-biased junctions are more vulnerable to ESD damage than forward-biased ones because its higher breakdown voltage results in a higher power dissipation in the depletion layer, requiring a smaller current to cause the damage.

3.3 ESD Stress Models

Electrostatic discharge (ESD) occurs in a variety of ways, depending on where and how the static charge is accumulated and how the charge build-up is dissipated. A measure of the ability of a device to dissipate this charge while withstanding the high currents is referred to as ESD sensitivity of the device. There are three industry-standard ESD models that define how semiconductor devices are to be tested for ESD sensitivity under different

situations of electrostatic build up and discharge. These are the Human Body Model (HBM), the Charged Device Model (CDM), and the machine Model (MM).

3.3.1 Human Body Model (HBM)

The Human Body Model simulates the ESD phenomenon wherein a charged body directly transfers its accumulated electrostatic charge to the ESD-sensitive (ESDS) device. A common example of this phenomenon in an IC environment is illustrated as following: We assume a charged person approaching a grounded IC, as shown in Fig.3.3.1, which is the most common model. When the air breaks down between the finger and one pin of the IC, the protection structures in the IC turn on and the capacitance of the person is discharged via the IC and the grounded pin into ground.

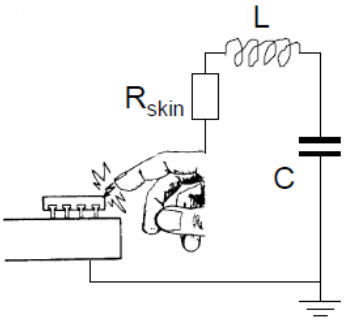

Fig. 3.3.1 Human Body Model (HBM)

Typically, R=1.5 kΩ, C=100 pF and L=7.5μH in the tester of Human Body Model (HBM).The HBM defines the current waveform for the discharge of 100pF capacitor through a 1.5 kΩ resistor, where C stores the charge, R limits the current and L is the effective inductance of the discharge path in a real tester, together with R to determine the rise time.
Without the protection structure, voltage can build up across the gate oxides of a MOS-structure until it breaks down and closes the discharge path.

3.3.2 Machine Model (MM)

The Machine Model originated in Japan as a more severe HBM with intentionally 0 Ω-resistance and a larger capacitance, as shown in Fig. 3.3.2.

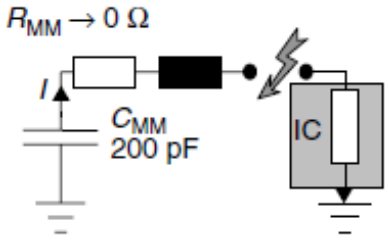

Fig. 3.3.2 Machine Model (MM)

The C_{MM} is defined as 200pF, while R_{MM} is nominally 0 Ω. In a real ESD tester, R_{MM} will be greater than 0 Ω, and during a discharge, the dynamic impedance can be much higher depending on the actual design of the tester. Both models, HBM and MM, involve at least two pins and typically generate power-related failures in pn-junctions.

3.3.3 Charged Device Model (CDM)

Not all ESD events involve the transfer of charge into the device. Electrostatic discharge from a charged device to another body is also a form of ESD, and a quite commonly encountered one at that. A device can accumulate charge in a variety of ways, especially in situations where they undergo movement while in contact with another object, such as when sliding down a track or feeder. If they come into contact with another conductive body that is at a lower potential, it discharges into that body. The Charged Device Model (Fig.3.3.3) can be more destructive than HBM ESD (despite its shorter pulse duration) because of its high current.

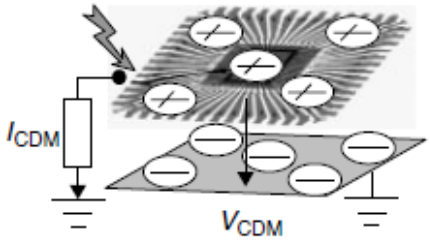

Fig. 3.3.3 Machine Model (MM)

ESD mechanisms in manufacturing and automatic handling are typically associated with a charged piece of equipment, a charged IC-package or the charged conductive parts of the IC itself.

In an IC environment of CDM, the capacitance of the lead frame and chip is charged or discharged, with respect to the environment, as soon as the

electrical breakdown of the residual gap is initiated while it approaches a conductive object at a different electrostatic voltage. In the worst case, the discharge is determined by the capacitance of the device, the inductance of the pin, the resistance of the ionized channel, resulting in an extremely narrow pulse with a high peak current even for voltages around 1kV. In most cases, the voltage drop across protection elements and power bus resistance raises internal gate oxides and causes damage.

CHAPTER 4

4 Electrical Characterization Techniques for IC packages

4.1 Frequency-Domain Measurements

To analyze the high frequency response of an interconnect, parameter sets such as admittance (y), impedance (z), transmission (t), and scattering (s) can be used. The wide use of these parameters sets, based on RF/microwave network theory, can be attributed to both the availability of commercial equipment and, more importantly, the accuracy of the measured results at high frequencies. From the review of the literature, s parameters have become the most popular parameter set used to characterize various interconnects such as packages, planar interconnects, and high density connectors. Although methodologies have been used such as Y parameters and ABCD parameter sets, these parameters have been extracted by converting an s parameter data set.

An s-parameter data set can be acquired through measurements using a network analyzer. A method of measuring the s-parameter of N-port networks is to configure the interconnect as a series of coupled two-port networks. This method simplifies the measurement process and reduces the number of variables to optimize during the extraction process. Equivalent circuit models consisting of capacitance and inductance matrices have been directly extracted from the measured data set. Therefore, the accuracy of the extracted model is directly related to the accuracy of the s-parameter measurements. Interconnects vary in size and physical geometry, so the physical measurements of these is significant. One solution to this problem is the use of microprobe stations. From the literature review, these have proved very useful in the measurement of small dense interconnects. However, if a probe station is not available, a test fixture is required to interface the device under test (DUT) to the coaxial-based environment of the measurement equipment.

In the de-embedded/calibration procedure, the effects of a test fixture or probe station need to be characterized and removed from the measurement result in order to generate the s-parameters for the DUT alone. There are two methods to achieve this: this first is to use calibration structures such as short, open and through that shift the measurement plane from the edge of the instrument measurement plane of the DUT. This is an effective method, and the calibration techniques improve accuracy and simplicity. The second method is to characterize the test fixture and create a parameter set for the fixture. This can be done using electromagnetic (EM) simulation and/or measuring the stand-alone response of the test fixture. These results can be embedded by converting the s-parameter matrix to an ABCD matrix.

4.2 Time-Domain Measurements

A commonly used technique for measuring the high-speed transient performance of an interconnection is time domain reflectometry/transmission (TDR/T). TDR/T employs a step generator and a digital sampling oscilloscope at the input and output of an interconnection to measure the reflection and transmission at different points along it. TDR/T can be either a single-ended, multiport, or differential measurement, depending on the configuration of the input source and the DUT.

An advantage of using TDR/T for interconnect characterization is that the response is separated in time allowing the use of normalization and gating to window out unwanted fixture effects. Compared with frequency domain technique such as s-parameters, time domain based modeling is more intuitive, visual and direct look at the DUT's characteristics. The intuitiveness of TDR has resulted in its wide acceptance for interconnect measurements and modeling work in general, and specifically for electrical modeling packages.

Package modeling techniques using TDR can be easily extended for characterization of other electrically short structures, such as connectors, sockets and multichip modules. Therefore, we use time domain based modeling in the project.

4.3 The Principle of Time Domain Reflectometry

TDR is an echo technique that reveals at a glance the characteristic impedance of the line and both the position and the nature of each discontinuity along the line. In addition, TDR demonstrates whether losses

in a transmission system are series losses or shunt losses. All of this information is immediately available from the oscilloscope's display.

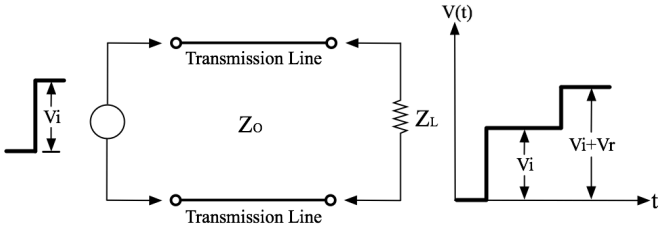

Fig. 4.3 Principle of Time Domain Reflectometry (TDR)

As can be seen from Fig.4.3, the step generator produces a positive-going incident wave that is applied to the transmission system under the test. The step travels down the transmission line at the velocity of propagation of the line. If the load impedance is equal to the characteristic impedance of the line, no wave is reflected and all that be seen on the oscilloscope is the incident voltage step recorded as the wave passes the point on the line monitored by the oscilloscope. However, if a mismatch exists at the load, where ZL is different from ZO, part of the incident wave is reflected. The reflected wave is energy that is not delivered to the load. Therefore, the quality of the transmission system is demonstrated by the ratio of this reflected wave to the incident wave originating at the source. This ratio is called the voltage reflection coefficient ρ, and is also related to the transmission line impedance by the equation:

$$\rho = \frac{V_r}{V_i} = \frac{Z_L - Z_o}{Z_L + Z_o} \qquad \text{(Eq. 4.3.1)}$$

, where V_i is the incident voltage and V_r is the reflected voltage.

Under picoseconds pulse circumstance, an electrical transmission medium can be modeled as shown in Fig. 4.3.1.

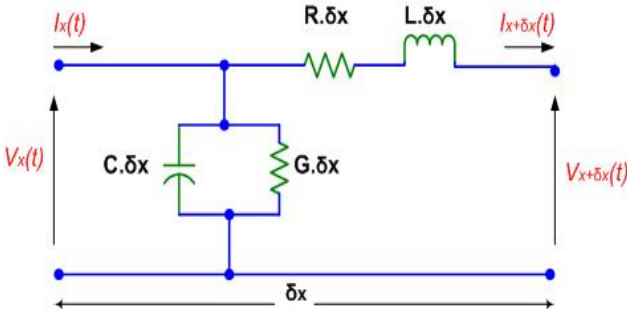

Fig. 4.3.1 Transmission line modeling under picoseconds pulse

Where:
R, conductors resistivity in Ohms/m (series losses)
L, conductors self-inductance in Henrys/m
C, inter-conductor capacity in Farads/m
G, dielectric conductance in Ohms-1/m (dielectric losses)
δx, line element length in meters.

By applying Kirchhoff' s laws to the circuit element (Fig. 4.3.1), we can establish the so-called telegraphers equations (Eq. 4.3.2):

$$\frac{d^2V}{dx^2} = \gamma^2 V = (R + j\omega L)(G + j\omega C)V \qquad \text{(Eq. 4.3.2)}$$

$$\frac{d^2I}{dx^2} = \gamma^2 I = (R + j\omega L)(G + j\omega C)I \qquad \text{(Eq. 4.3.3)}$$

The solutions of the telegraphers equations are defined as (Eq. 4.3.4):

$$V(x,t) = [V_1 e^{-\gamma x} + V_2 e^{+\gamma x}]e^{j\omega t} \qquad \text{(Eq. 4.3.4)}$$

$$I(x,t) = [I_1 e^{-\gamma x} + I_2 e^{+\gamma x}]e^{j\omega t} \qquad \text{(Eq. 4.3.5)}$$

Where γ is the propagation constant and V_1, V_2, I_1, I_2 are constants.
From Eq. 4.3.4 and Eq. 4.3.5, there are incident and reflected waves for both voltage and current.

4.4 Theoretical Study

To understand the principle of Time Domain Reflectometry deeply in different impedance loads, the theoretical derivations have been given by using a more intuitive and easier understood methodology. It will be the basis of the actual measurements.

4.4.1 TDR displays for four different typical loads

(a) Open Termination

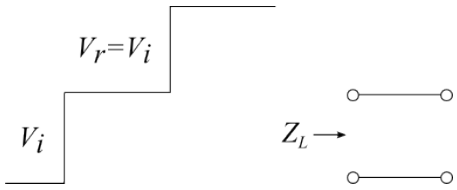

Fig. 4.4.1 (a) Open Termination

From Fig. 4.4.1 (a), we can see that the load impedance Z_L is an infinite impedance. Since the reflection coefficient is

$$\rho = \frac{V_r}{V_i} = \frac{Z_L - Z_o}{Z_L + Z_o} \qquad \text{(Eq. 4.4.1)}$$

We can get $\rho = \frac{V_r}{V_i} = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{\infty - Z_O}{\infty + Z_O} = 1$.

The total voltage waveform from the oscilloscope's display is $2V_r$.

(b) Short Termination

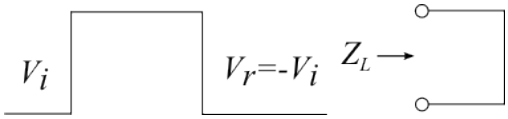

Fig. 4.4.1 (b) Short Termination

As shown in Fig.4.4.1 (b), we can see that the load impedance Z_L is zero (Short Termination).

From Eq. 4.4.1, we can get $\rho = \frac{V_r}{V_i} = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{0 - Z_O}{0 + Z_O} = -1$.

The total voltage waveform from the oscilloscope's display is 0.

(c) Line Termination in $Z_L = 2Z_o$

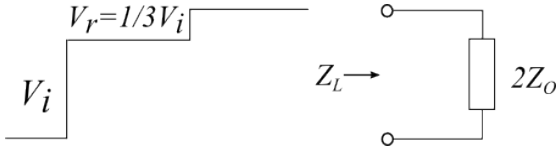

Fig. 4.4.1 (c) Line Termination in $Z_L = 2Z_o$

As can be seen from Fig.4.4.1 (c), the load impedance Z_L is equal to $2Z_O$. From Eq. 4.4.1, we can get $\rho = \frac{V_r}{V_i} = \frac{Z_L - Z_O}{Z_L + Z_O} = \frac{2Z_O - Z_O}{2Z_O + Z_O} = \frac{1}{3}$.

The total voltage waveform from the oscilloscope's display is $\frac{4}{3}V_r$.

(d) Line Termination in $Z_L = 0.5Z_o$

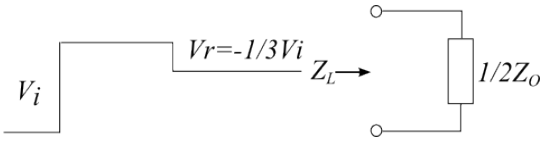

Fig. 4.4.1 (d) Line Termination in $Z_L = 0.5Z_o$

We can see that from Fig.4.4.1 (d), the load impedance Z_L is equal to $0.5Z_O$. From Eq. 1, we can get $\rho = \frac{V_r}{V_i} = \frac{Z_L - Z_O}{Z_L + Z_O} = \frac{0.5Z_O - Z_O}{0.5Z_O + Z_O} = -\frac{1}{3}$.

The total voltage waveform from the oscilloscope's display is $\frac{2}{3}V_r$.

From the above figures, in the case of Z_O that is real, we can get the resistive mismatches reflect a voltage of the same shape as the driving voltage, and the magnitude and polarity of V_r which are determined by the relative values of Z_O and Z_L.

4.4.2 TDR displays for four different basic complex load impedances

These waveforms can be verified by writing the expression for ρ(s) in terms of the specific Z_L for each case. For instance:

$$Z_L = R + sL \qquad \text{(Eq.4.4.2)}$$

$$Z_C = \frac{R}{R + sRC} \qquad \text{(Eq.4.4.3)}$$

Multiplying ρ(s) by $\frac{E_i}{s}$ the transform of a step function of E_i, and then transforming this product back into the time domain to find an expression for $e_r(t)$. The calculation of this procedure is of use, but a simpler methodology is possible without resorting to Laplace transforms. The more direct analysis takes into account the evaluation of the reflected voltage at $t = 0$ and $t = \infty$. For simplicity, we can assume any transition between

these two values to be exponential, where time is chosen to be zero when the reflected wave arrives back at the monitoring point.

(a) Series Resistance-Inductance

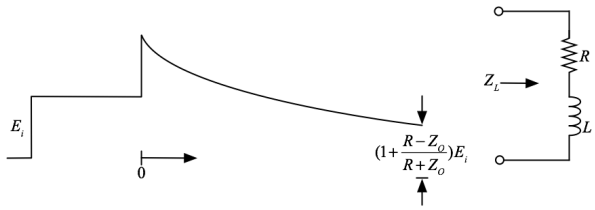

Fig. 4.4.2 (a) Series Resistance-Inductance

As can be seen from Fig.4.4.2 (a), we assume that any transition between $t = 0$ and $t = \infty$ is exponential, where $t = 0$ that means the reflected wave gets back to the monitoring point. At $t = 0$ the reflected voltage is E_i, that is because the inductor will not accept a sudden change in current. It initially looks like an infinite impedance, and the reflection coefficient is equal to 1 at $t = 0$. After that, the current in inductor builds up exponentially and its impedance drops toward zero. At $t = \infty$, the reflected voltage is determined only the value of resistance.

$$E_r = \frac{R - Z_O}{R + Z_O} \times E_i \qquad \text{(Eq.4.4.4)}$$

, where the value of R is larger than that of Z_O, the polarity of E_r is positive and vice versa.

Since the resulting waveform is the combination of the incident step and the reflection, we can get the total voltage is $(1 + \frac{R - Z_O}{R + Z_O}) \times E_i$.

(b) Series Resistance-Capacitance

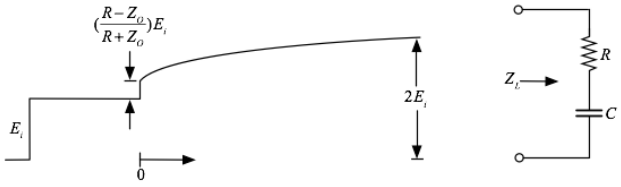

Fig. 4.4.2 (b) Series Resistance-Capacitance

In Fig.4.4.2 (b), since the capacitor will not obtain an instant change in voltage at $t = 0$, the load impedance is only determined by the value of R. According to the Eq. 4.4.1, we can get the reflected voltage at $t = 0$ which

is equal to $(\frac{R-Z_O}{R+Z_O})\times E_i$. After $t=0$, the voltage accumulates exponentially on the capacitor and its impedance rises. The load impedance will be an infinite, which is open circuit at $t=\infty$. The total voltage will be $2E_i$.

(c) Shunt Resistance-Inductance

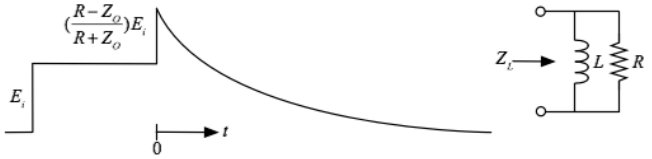

Fig. 4.4.2 (c) Shunt Resistance-Inductance

From Fig.4.4.2 (c), we can see that at $t=0$ the reflected voltage depends on the value of R because of the inductor cannot accept a change in current. The reflected voltage depends on the value of R. After that, the current increases in the inductor and there is a decrease in the impedance until it drops to zero. Finally, the load appears as a short circuit.

(d) Shunt Resistance-Capacitance

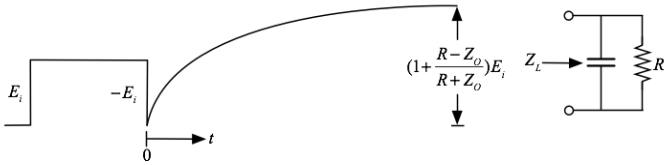

Fig. 4.4.2 (d) Shunt Resistance-Capacitance

In Fig.4.4.2 (d), the reflected voltage is $-E_i$ at $t=0$, since the load initially appears short circuit. After $t=0$, the voltage on the capacitor builds up with the increase of the time. The capacitor is effectively an open circuit at $t=\infty$ and the load is only determined by the value of R when time is infinite. The total voltage can be determined, which is equal to $(1+\frac{R-Z_O}{R+Z_O})\times E_i$.

4.5 Summary of TDR Characteristics

A TDR is a very fast GHz oscilloscope including a fast pulse generator in the picoseconds range. This pulse with an amplitude of usually 200mV is applied to the DUT, and the reflections of that voltage are displayed on the oscilloscope. Therefore, the time axis on that plot corresponds to the physical location of the event in the DUT.

From the above figures, we can get the different characteristics from different terminations. When an open ended one is connected to the TDR output, the resulting oscilloscope reading shows a 200mV amplitude (voltage divider: 50Ω internal resistance and 50Ω characteristic impedance of the line), as long as the impulse is present in the line. Once the open end is reached, there is a jump to 400mV. Otherwise, if the line is shortened at its end, the impulse again sees a 50Ω characteristic impedance (while still in the line), yet disintegrates to 0Ω when hitting the short at the end of the line.

If there is a capacitor between two 50Ω lines, the reflected signal with its level of 200mV (in line 1 in Fig 3.5) will briefly drop down to 0V, 'seeing' the capacitor as a short for the first moment, and then ascend back to 200mV (line 2) with an exponential rise that is proportional to the capacitance value. In case there is an inductor instead of the capacitor, the reflected signal will jump to full 400mV(because the inductor behaves like an open in the first moment) to once again come back to the 200mV level of line 2.

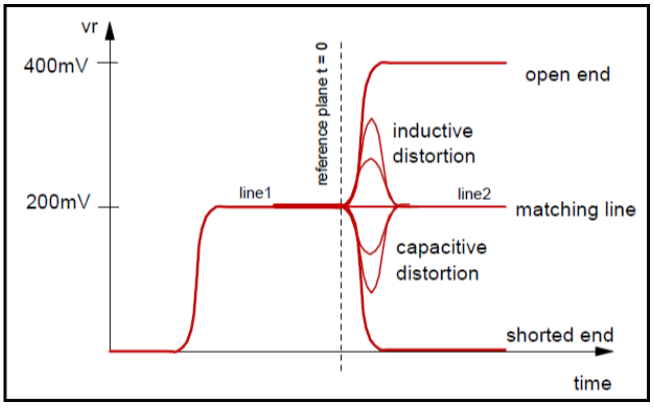

Fig. 4.5 Summary of TDR Characteristics

CHAPTER 5

5 EMPro Simulation Setup

In the development of the robust design of the Charged Device Model (CDM), there is a lack of knowledge of the source the discharge current and its path through the integrated circuit (IC). Circuit simulation, in our project which is EMPro Simulation, can be very useful in helping us access to the internal nodes to determine the path of the CDM discharge current without being distorted by test setup artifacts. EMPro (Electromagnetic Professional) is a three-dimensional full wave electromagnetic solver, which has flexible choice of full wave 3D EM simulation technologies and provides innovative 3D component technology that bridges the 3D EM design environment with the circuit design environment. The accuracy of the simulations in replicating the actual behavior, however, depends on the accuracy of the simulation models.

The integrated circuit (IC) behaves as the source and shapes a part of the discharge path of the CDM current. The capacitance of the IC packages determines the charge on the integrated circuit, and the other parasitics of the package, such as the inductance and resistance from the lead frame and bonding wires, also determine the shape of the CDM waveform.

5.1 LQFP64 Package 3D Model

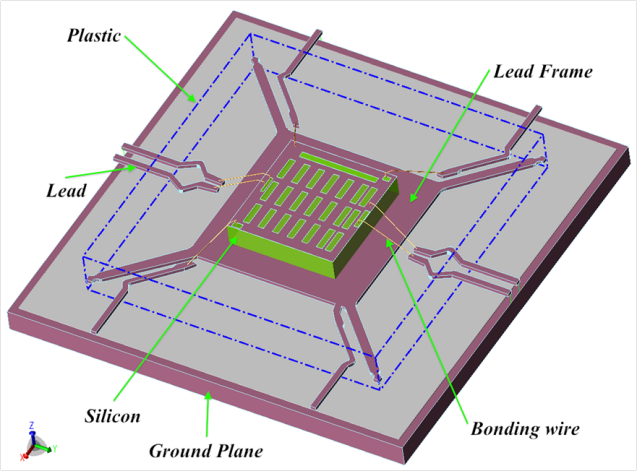

Fig. 5.1 LQFP64 3D Model

A 3D equivalent LQFP64 package of the IC model is built in EMPro simulation environment as shown in Fig 5.1. From Fig 5.1 we see that the components, such as plastic, lead, silicon, bonding wires and lead frame, of LQFP64 package clearly. It is very helpful to analyze the problems of the LQFP64 package in the following actual measurements.

5.2 EMPro Transient Simulation for LQFP64 Packages Setup

Table 1. EMPro Simulation Setup for TDR measurements of IC packages

EMPro Transient Simulation Setup	Setting Value
The Amplitude of Input Step	200 mV
The Rise Time of Input Step	9 ps
Frequency Spectrum	from DC to 62 GHz
Simulation Time	from 0 s to 500 ps

5.3 EMPro Transient Simulation

5.3.1 The bonding wire of the load pin – the Pad Ring, Corner Pin – the Excitation Pin and Middle Pin – the Load pin

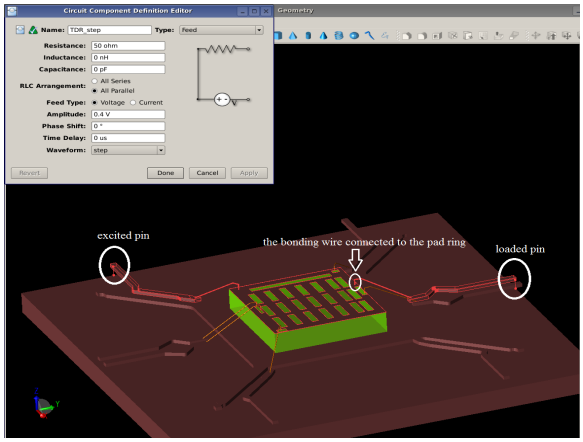

Fig. 5.3.1 (a) LQFP64 3D Model (Pad Ring)

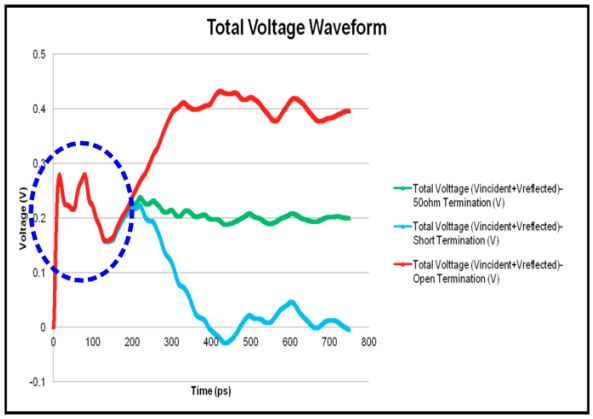

Fig. 5.3.1 (b) The total voltage waveform

As can be seen from Fig 5.3.1 (a), the bonding wire is connected to the pad ring, the corner pin is the excitation pin and the loaded pin is the middle pin. In the simulation, we chose a corner pin and a pin in the middle of package, which can provide us with a sufficient range of inductance and capacitance values for the package under the test. We can use the comparative method

to determine where the parasitics from the package are observed. In this case, we used three different load impedances, 50 ohm, open and short terminations to check the part what we need to analyze. The total voltage waveform is shown in Fig 5.3.1 (a), the green line is the sum of the incident voltage and the reflected voltage when the load pin is connected to 50 Ohm termination. The red shows the summation of the incident voltage and reflected voltage when the load pin connects the open termination that means the impedance is infinite. The blue line is the sum of the incident voltage and reflected voltage of the short termination. From the above analysis, we can get the overlap parts we would like to extract. As can be seen from the blue circle dash line, at the beginning of waveform, the first spike is the characteristics of the inductance because of the bonding wire. And the second spike is due to the inductance of the package and the dip after the second spike that is the capacitance of the die attached of the package. We can use the formulas (6.2.1), (6.2.2) and (6.2.3) to extract the specific parasitics, in our case those are inductance and capacitance.

5.3.2 The bonding wire of the load pin – Silicon, Corner Pin – the Excitation Pin and the Middle Pin – the Load pin

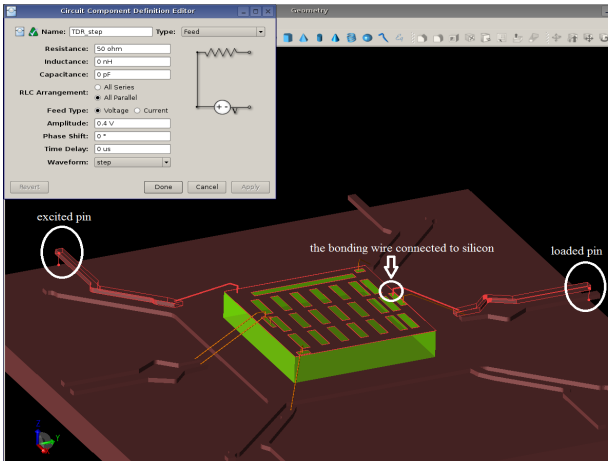

Fig. 5.3.2 (a) LQFP64 3D Model (Silicon)

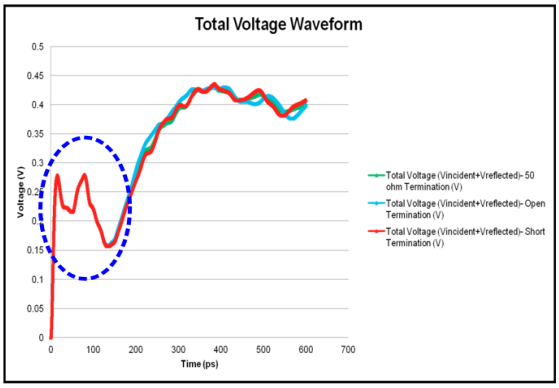

Fig. 5.3.2 (b) The total voltage waveform

As can be seen from Fig 5.3.2 (a), the excitation pin is the corner pin, the load pin is the middle pin and the bonding wire of the load pin is connected to the silicon. We used three different load impedances as the previous cases. Since the silicon is not a conductor, no matter what the loaded pin connected to the impedance, the end of the total voltage waveform is 0.4 V, as shown in Fig 5.3.2 (b). As can be seen from the blue circle dash line, at the beginning of waveform, the first spike is the characteristics of the inductance because of the bonding wire. The second spike is because of the inductance of the package and the dip after the second spike that is the capacitance of the die attached of the package. We can use the formulas (6.2.1), (6.2.2) and (6.2.3) to extract the specific parasitics, in our case those are inductance and capacitance.

5.3.3 The comparison of different connection ways on the bonding wire between the different load impedances

a) 50 Ohm Termination:

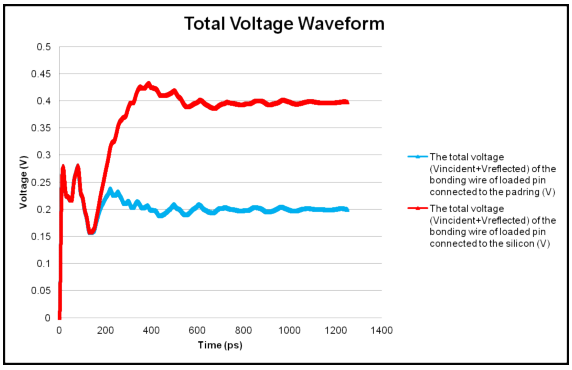

Fig. 5.3.3 (a) The total voltage waveform – the bonding wire connecting to the pad ring and the silicon of the package

As can be seen from Fig 5.3.3 (a), we can find the differences between the bonding wire of the load pin is connected to the silicon and that of the loaded pin which connects to the pad ring. In this case, the load termination is 50 Ohm. The purpose of this figure is to illustrate the differences between the connection of the pad ring and the connection of the silicon.

b) Open Termination:

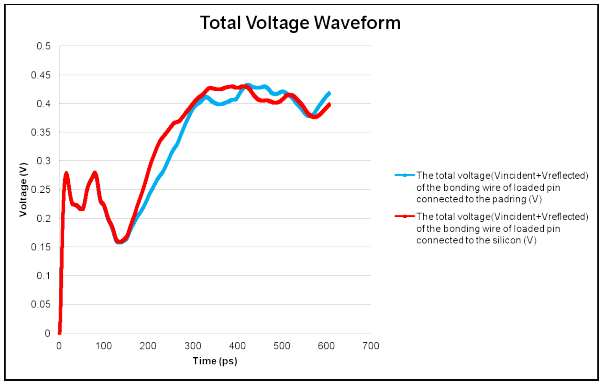

Fig. 5.3.3 (b) The total voltage waveform – the bonding wire connecting to the pad ring and the silicon of the package

As can be seen from Fig 5.3.3 (b), we can find the differences between the bonding wire of the load pin, which is connected to the silicon and that of the loaded pin that connects to the pad ring. In this case, the load termination is open termination. The purpose of this figure is to illustrate the differences between the connection of the pad ring and the connection of the silicon.

c) Short Termination:

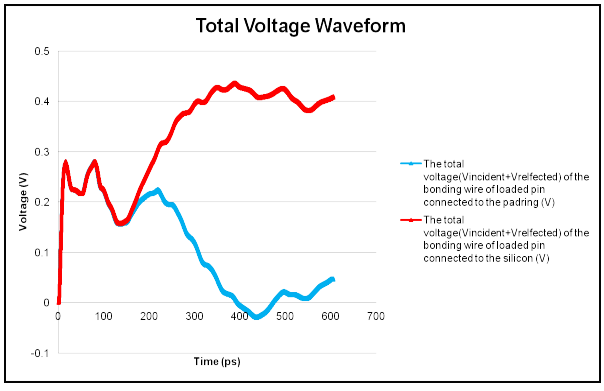

Fig. 5.3.3 (c) The total voltage waveform – the bonding wire connecting to the pad ring and the silicon of the package

As can be seen from Fig 5.3.3 (c), we can find the differences between the bonding wire of the load pin, which is connected to the silicon and that of the loaded pin that connects to the pad ring. In this case, the load termination is short termination. From the above figures 5.3.3 (a), (b) and (c), the impedance of silicon shows that the phenomenon of open termination, as shown by the red line, it is higher than that of the pad ring. The purpose of this figure is to illustrate the differences between the connection of the pad ring and the connection of the silicon.

5.3.4 The comparison of the excited pin connected to the middle pin and the corner pin when the bonding wire of the load pin is connected to silicon.

In order to explore what differences between when the middle pin is the excitation pin and when the corner pin is the excitation pin, we changed the excitation pin to the middle pin and run the simulation to see what the result would be.

a) 50 Ohm Termination:

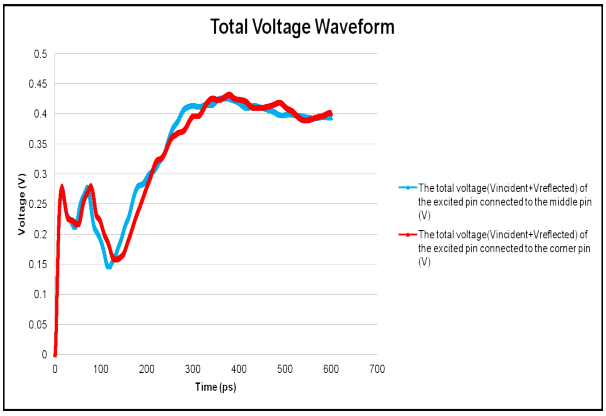

Fig. 5.3.4 (a) The total voltage waveform – the excited pin to the middle pin and the corner pin of the package

In the above Fig 5.3.4 (a), we see the blue line shows the voltage waveform of the excited pin which is connected to the middle pin. The red line is the voltage waveform of the excited pin connected to the corner pin. The purpose of this figure is used to illustrate the differences between the connection of the middle pin and the connection of the corner pin.

b) Short Termination:

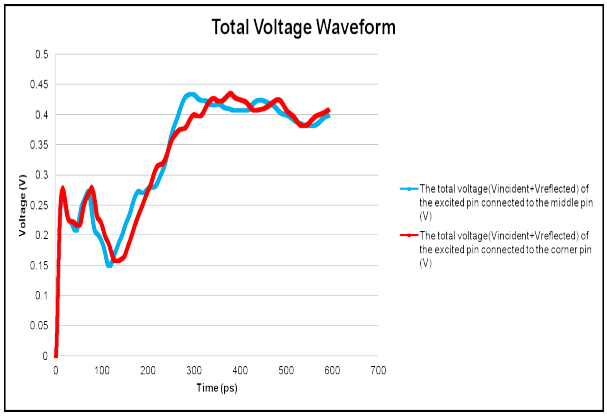

Fig 5.3.4 (b) The total voltage waveform - the excited pin to the middle pin and the corner pin of the package

From the above Fig 5.3.4 (b), we can see the blue line shows the voltage waveform of the excited pin connected to the middle pin. The red line is the voltage waveform of the excited pin that is connected to the corner pin. The purpose of this figure is to illustrate the differences between the connection of the middle pin and the connection of the corner pin.

c) Open Termination:

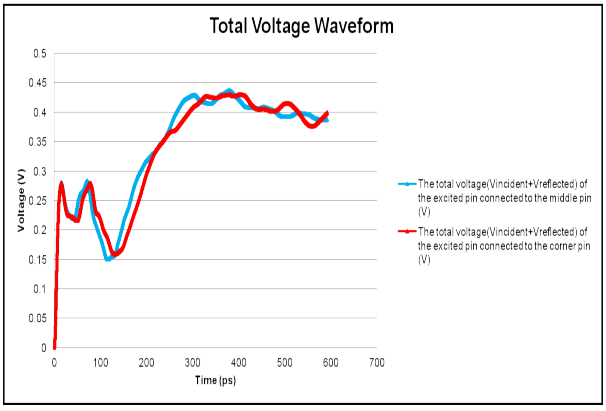

Fig 5.3.4 (c) The total voltage waveform - the excited pin to the middle pin and the corner pin of the package

From the above Fig 5.3.4 (c), we can see the blue line shows the voltage waveform of the excited pin connected to the middle pin. The red line is the voltage waveform of the excited pin connected to the corner pin. The

purpose of this figure is used to illustrate the differences between the connection of the middle pin and the connection of the corner pin.

As can be seen from the above figures 5.3.4 (a), 5.3.4 (b) and 5.3.4 (c), the bonding wire of the load pin is connected to the silicon, no matter what the different load impedances would be. The total voltage is always close to 400mV since the silicon has a very high impedance, which always shows open termination. The blue lines in the above figures are a bit quicker than the red lines, which is because the middle pin has a shorter path than the corner pin.

5.3.5 The comparison of the excited pin connected to the middle pin and the corner pin when the bonding wire of the load pin is connected to the pad ring.

a) 50 Ohm Termination:

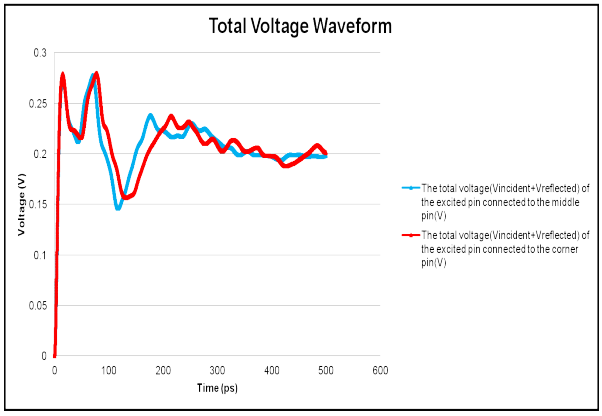

Fig 5.3.5 (a) The total voltage waveform - the excited pin to the middle pin and the corner pin of the package

From the above Fig 5.3.5 (a), we can see the blue line shows the voltage waveform of the excited pin connected to the middle pin. The red line is the voltage waveform of the excited pin connected to the corner pin. The purpose of this figure is to illustrate the difference between the connection of the middle pin and the connection of the corner pin.

b) Short Termination:

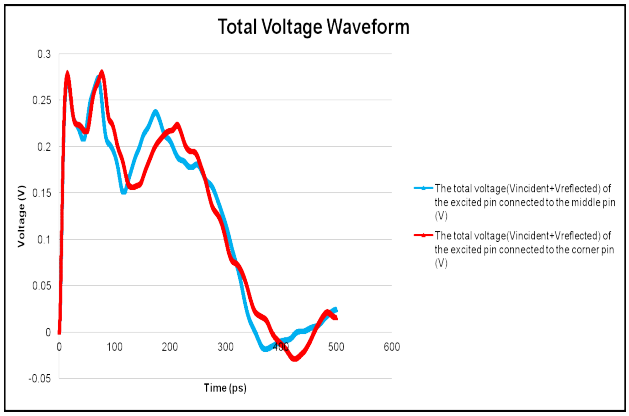

Fig 5.3.5 (b) The total voltage waveform - the excited pin to the middle pin and the corner pin of the package

From the above Fig 5.3.5 (b), we can see the blue line shows the voltage waveform of the excited pin connected to the middle pin. The red line is the voltage waveform of the excited pin connected to the corner pin. The purpose of this figure is to illustrate the differences between the connection of the middle pin and the connection of the corner pin.

c) Open Termination:

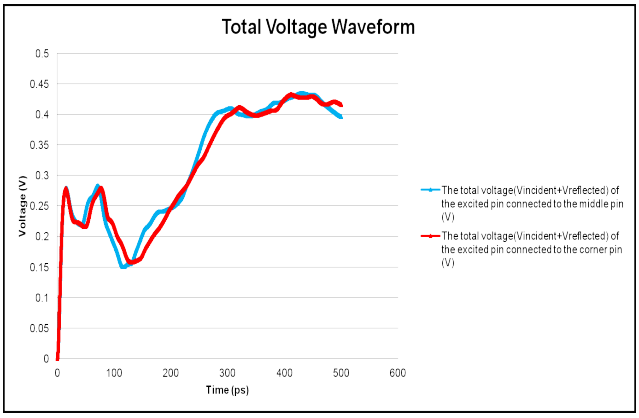

Fig 5.3.5 (c) The total voltage waveform - the excited pin to the middle pin and the corner pin of the package

In the above Fig 5.3.5 (c), we see in blue line shows the voltage waveform of the excited pin connected to the middle pin. The red line is the voltage waveform of the excited pin connected to the corner pin. The purpose of this figure is used to illustrate the differences between the connection of the

middle pin and the connection of the corner pin. As can be seen from the above figures 5.3.5 (a), 5.3.5 (b) and 5.3.5 (c), when the excited pin is connected to the corner pin of the package, it has a longer path than the middle pin of the package. Thus, you see that the red line from the waveform is slower than the blue one.

5.3.6 Conduction current transient simulation

By using EMPro Software, we can get animation results from the simulation. The purpose of doing conduction current transient simulation is to observe the dynamic effects of the current in the package. In order to clearly observe the effects of different components on the current in the package, we have made some different figures to clarify this phenomenon.

a) Lead

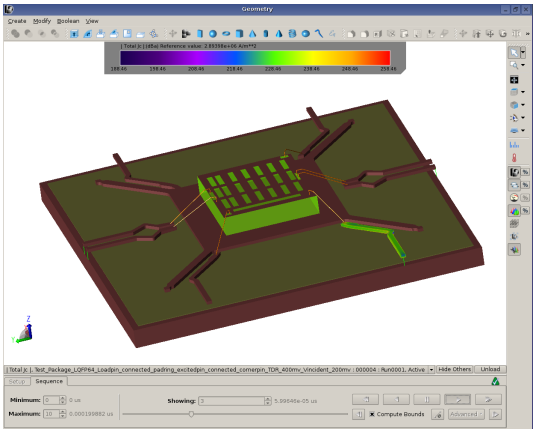

Fig 5.3.6 (a) One lead of the LQFP64 model

b) Bonding wire

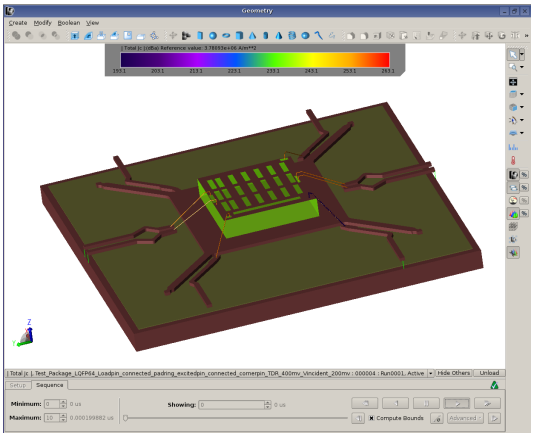

Fig 5.3.6 (b) One bonding wire of the LQFP64 model

We can see from the Fig 5.3.6 (a), the green of the lead shows the density of the current variation. Fig 5.3.6 (b), it shows the variation of the current density of the bonding wire of the package. All the components are displayed in the conduction current transient simulation. The color of the dialog box shows the variation of the current density from low to high.

c) Pad ring

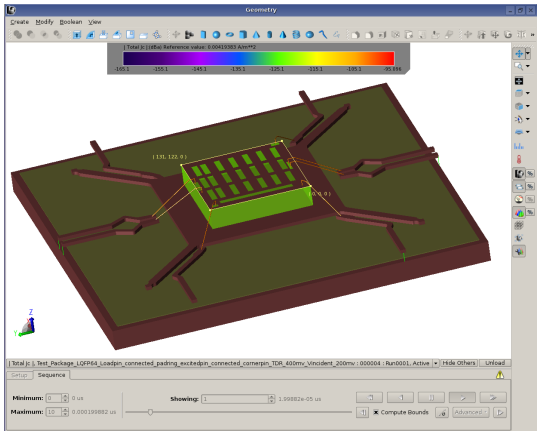

Fig 5.3.6 (c) One pad ring of the LQFP64 model

d) Silicon

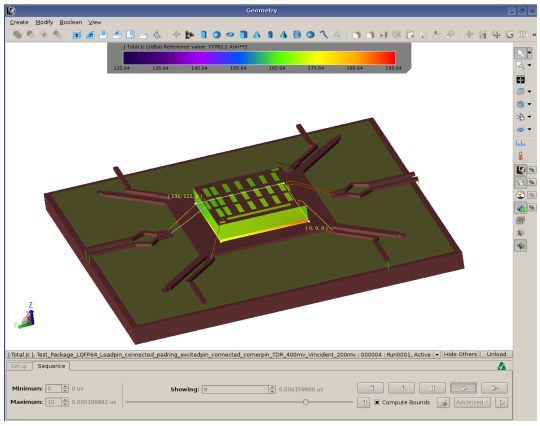

Fig 5.3.6 (d) The silicon of the LQFP64 model

In the Fig 5.3.6 (c), the yellow square frame shows the current density of the pad ring. In Fig 5.3.6 (d), it shows the variation of current density of the silicon in the package. The color of the dialog box shows the variation of the current density from low to high.

e) LQFP64 3D model

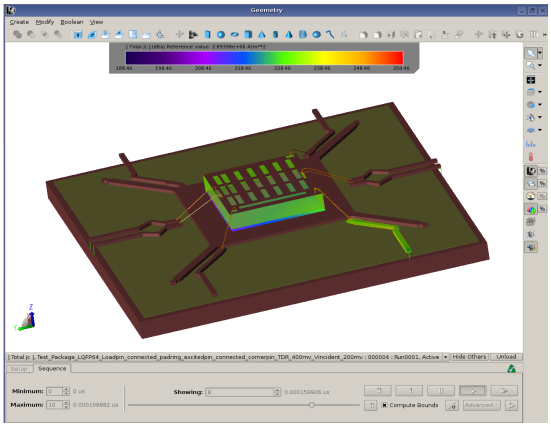

Fig 5.3.6 (e) The LQFP64 3D model in the conduction current transient simulation

As can be seen from the Fig 5.3.6 (e), we can see the variation of the current density of the LQFP64 3D model in the conduction current transient simulation. All the components are displayed in the E-field transient simulation. The color of the dialog box shows the variation of the current density from low to high.

5.3.7 E-field transient simulation

The purpose of doing E-field transient simulation is used to observe the dynamic change of E-field transient simulation in the package. In order to observe clearly the effects of different components on E-field transient simulation in the package, we have made some different figures to clarify this phenomenon.

a) Lead

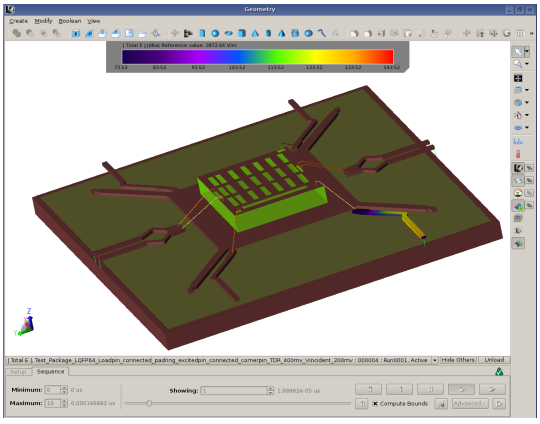

Fig 5.3.7 (a) One lead of the LQFP64 model

b) Bonding wire

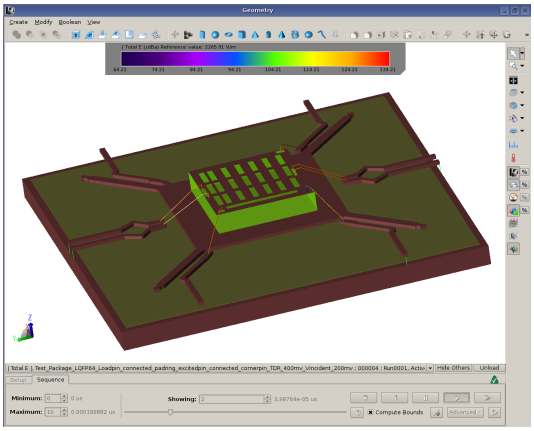

Fig 5.3.7 (b) One bonding wire of the LQFP64 model

From Fig 5.3.7 (a), it shows E-field effect of the lead in the package. From Fig 5.3.7 (b), it shows E-field effect of the bonding wire in the package. The color of the dialog box shows the variation of E-field from low to high.

c) Pad ring

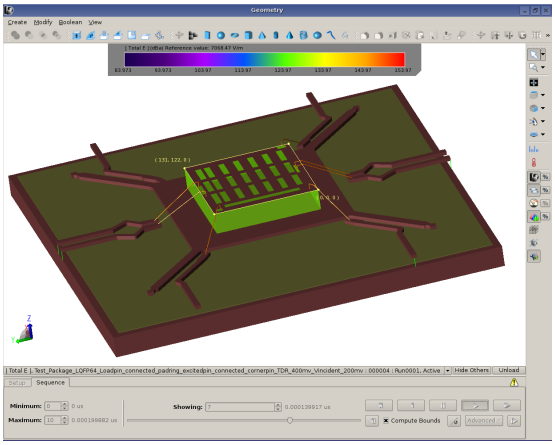

Fig 5.3.7 (c) One pad ring of the LQFP64 model

d) Silicon

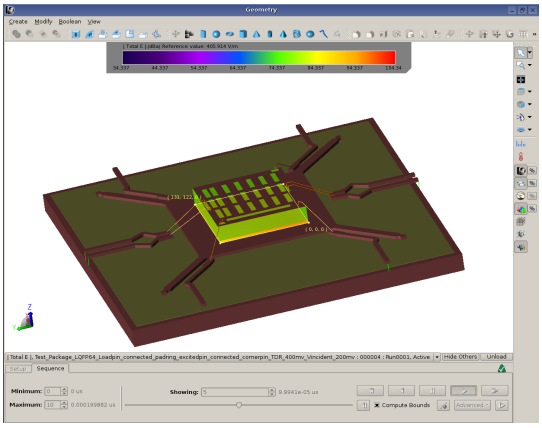

Fig 5.3.7 (d) The silicon of the LQFP64 model

From the Fig 5.3.7 (c), the yellow square frame shows the pad ring of the package. From Fig 5.3.7 (d), it shows E-field of the silicon of the package. The color of the dialog box shows the variation of E-field from low to high.

e) LQFP64 model

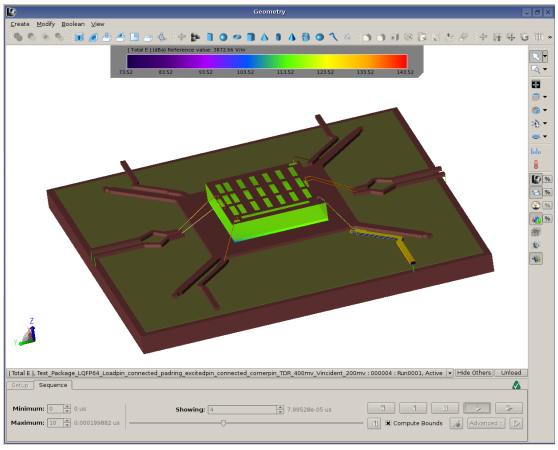

Fig 5.3.7 (e) The LQFP64 3D model in the E-field transient simulation

We can see from the Fig 5.3.7 (e), it shows the E-field of the LQFP64 3D model in the transient simulation. All the components are displayed in the E-field transient simulation. The color of the dialog box shows the variation of E-field from low to high.

5.3.8 H-field transient simulation

The purpose of doing H-field transient simulation is to observe the dynamic change of H-field transient simulation in the package. In order to observe clearly the effects of different components about H-field transient simulation in the package, we have made some different figures to clarify this phenomenon.

a) Lead

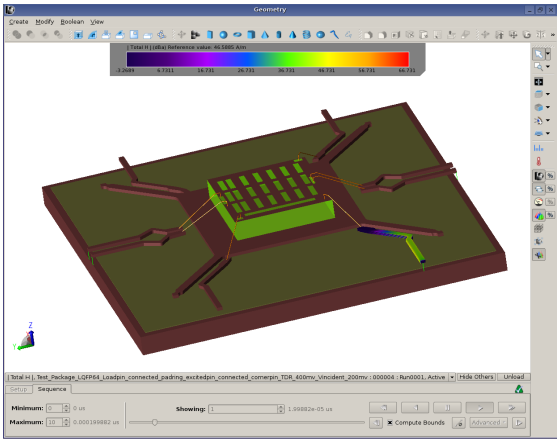

Fig 5.3.8 (a) One lead of the LQFP64 model

b) Bonding wire

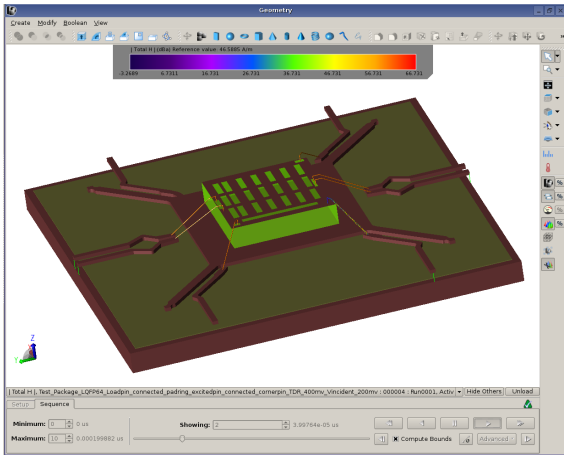

Fig 5.3.8 (b) One bonding wire of the LQFP64 model

We can see from the Fig 5.3.8 (a), the changeable color of lead of the package means H-field effect. From Fig 5.3.8 (b), it shows H-field of the bonding wire of the package.

c) Pad ring

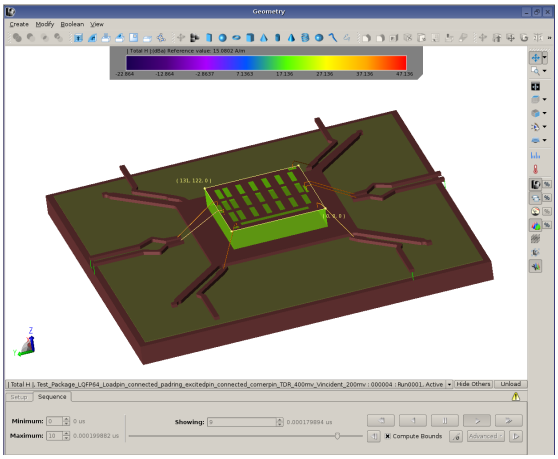

Fig 5.3.8 (c) One pad ring of the LQFP64 model

d) Silicon

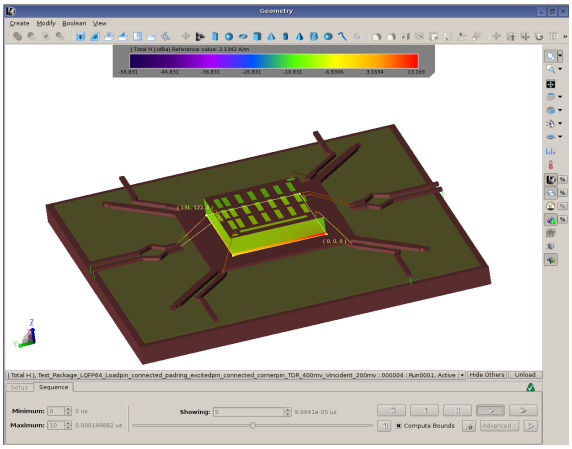

Fig 5.3.8 (d) The silicon of the LQFP64 model

We can see from the Fig 5.3.8 (c), one pad ring of the LQFP64 model of the package means H-field effect. In Fig 5.3.8 (d), it shows H-field of the silicon of the LQFP64 model of the package.

e) LQFP64 model

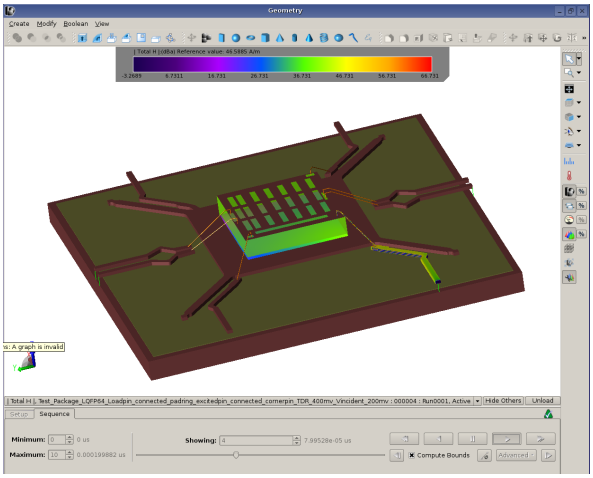

Fig 5.3.8 (e) The LQFP64 3D model in the H-field transient simulation

Fig 5.3.8 (e) shows the LQFP64 3D model in the H-field transient simulation. All the components are displayed in the H-field transient simulation. The color of the dialog box shows the variation of the H-field from low to high.

5.4 Developed a simple model about the conductor in EMPro Simulation

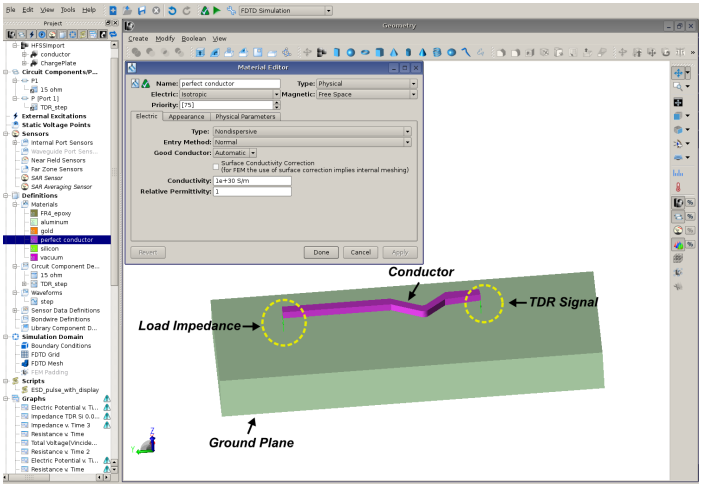

Fig 5.4 The 3D model of the conductor

As can be seen from Fig 5.4, it proves that EMPro Simulation can simulate the passive component. In the actual measurement, there are some

unwanted and unknown effects, not only effects about the lines that connect the passive component. Actually, we do not know what the real effect on the passive components in the actual measurement, such as resistors, inductors and capacitors. Thus, we can use EMPro Simulation to fix the problem and get the real results that we expect. By doing some actual measurements on the passive components, we can use the corresponding results from the EMPro Simulation as a reference to see what the differences between them are.

5.4.1 Comparison of three different resistance terminations in EMPro Simulation and the measurement

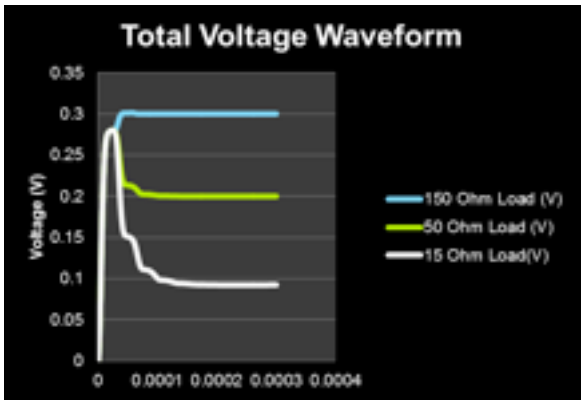

Fig 5.4.1 (a) The results from the EMPro Simulation

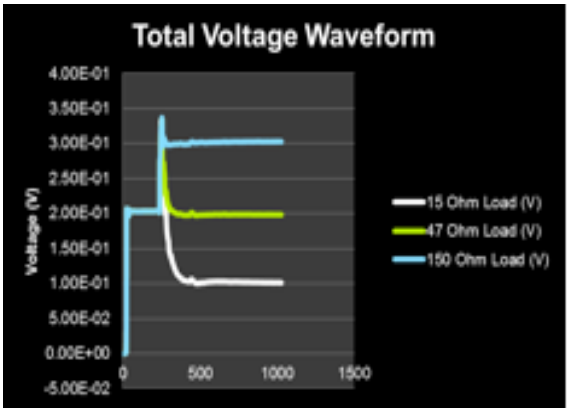

Fig 5.4.1 (b) The results from the actual measurements

The purpose of the comparison of three different resistances is used to check what the results would be between different values of the resistances in the EMPro Simulation and the actual measurements. As can be seen from

the above figures, one is from the EMPro Simulation, as shown in Fig 5.4.1 (a). In this figure, the blue line is 150 Ohm load, the green line is 50 Ohm load and the white line is 15 Ohm. Fig 5.4.1 (b) shows the actual measurement, with 15 Ohm load, 47 Ohm load and 150 Ohm load. In the first figure, there is a spike in the voltage waveform since the inductance is generated when the current goes through the conductor. In the second Fig 5.4.1 (b), it has a time delay since there is a signal interference on the coplanar waveguide board.

5.4.2 Comparison of two different capacitance terminations in EMPro Simulation and the measurement

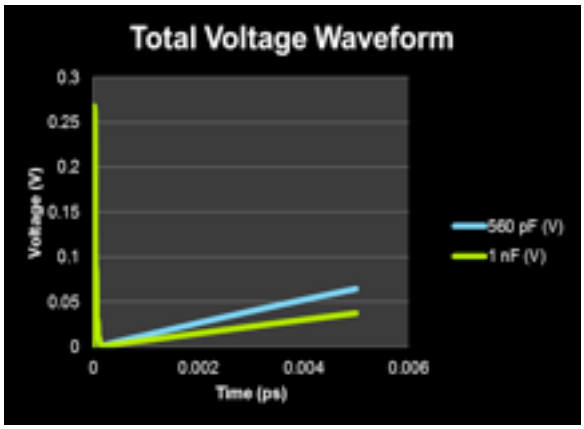

Fig 5.4.2 (a) The results from the EMPro simulation

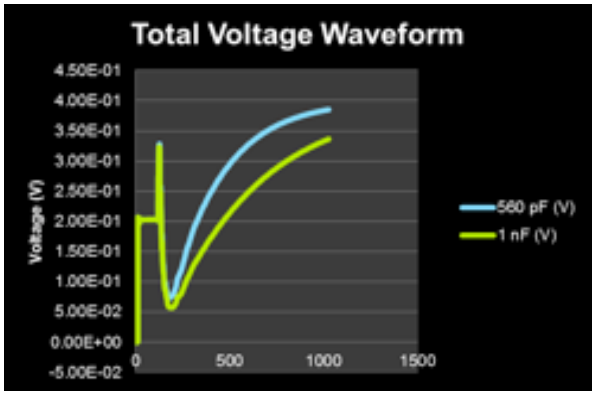

Fig 5.4.2 (b) The results from the actual measurements

The purpose of the comparing two different capacitances is to check what the results would be with different values of the capacitances in the EMPro Simulation and the actual measurements. We can see from Fig 5.4.2 (a) that

the result is from the EMPro Simulation, where the blue line 560 pF and the green line 1 nF. The other one, Fig 5.4.2 (b), is from the actual measurement. In the first figure, there is a spike at the beginning of simulation time in the voltage waveform since the current goes through the conductor that generates the inductance. In the second figure, it has a time delay since there is a signal interference on the coplanar wave guide board.

5.5 Summary

1. IC package characterization is required to accurately simulate the CDM discharge through an IC. The LQFP64 3D model is setup in the EMPro finite difference time domain (FDTD) simulation environment.
2. The differences in the voltage waveform characteristics for the different connections about the load and excitation pins are illustrated by EMPro transient simulation.
3. The animation results of different components on LQFP64 3D model about conduction current, E-field and H-field are simulated.
4. The 3D model of the passive component is developed in the EMPro FDTD simulation environment.

CHAPTER 6

6 LQFP64 Measurements

6.1 Calibrated the precision of the Time Domain Reflectometry equipment

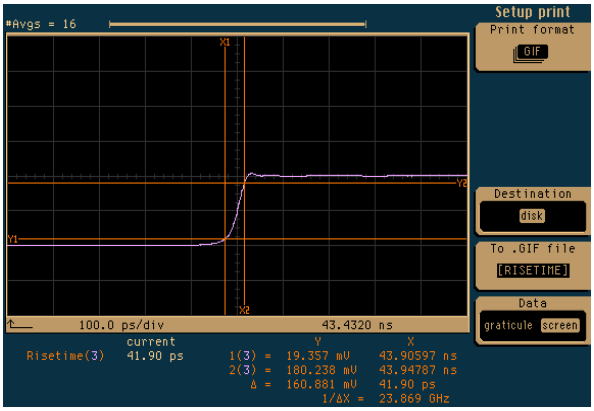

Fig 6.1.1 The Rise Time of the Time Domain Reflectometry Equipment

The above screenshot shows the rise time of the time domain reflectiometry equipment. In order to verify what the degree of precision the Time Domain Reflectometry (TDR) equipment what we used in the measurement can achieve, the method what it illustrates as following is applied. We can use one known 1 nF capacitor to check the precision of TDR system. First of all, we can extract the data from the Time Domain Reflectometry (TDR) so as to calculate the data. The second step is to make comparison between the known value and the measured one.

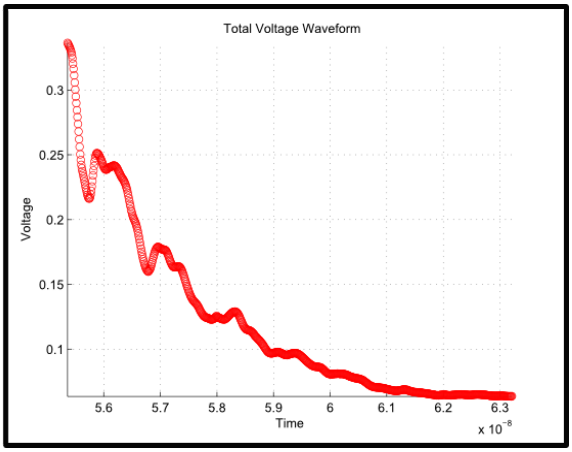

Fig 6.1.2 The total voltage waveform

In Fig 6.1.2, the value from the TDR data is calculated by matlab script. This measured value is calculated from integral function by using matlab script (Appendix – Matlab Script Code). Compared with the 1nF, we can see that there is a good agreement with the measurement results.

6.2 Extracting the parasitics from the voltage waveform of the TDR equipment

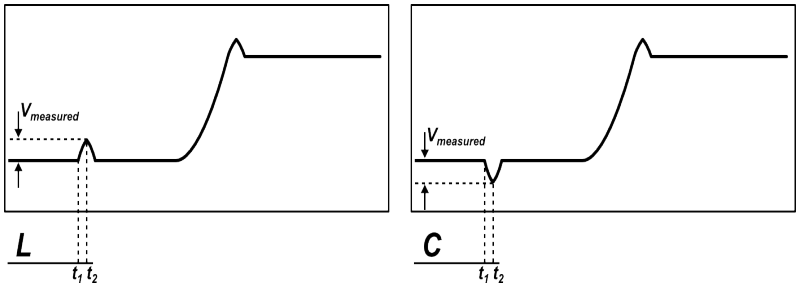

Fig 6.2 The two different cases about extracting the parasitics

Firstly, the variables impedance is calculated:

$$Z_{(t)} = Z_o \times \frac{V_{measure}(t)}{2 \times V_{incident} - V_{measure}(t)} \tag{6.2.1}$$

$$L = \frac{1}{2}\int_{t1}^{t2} Z(t)\,dt = \frac{1}{2} \times Z_o \times \int_{t1}^{t2} \frac{V_{measure}(t)}{0.4 - V_{measure}(t)}\,dt \tag{6.2.2}$$

$$C = \frac{1}{2}\int_{t1}^{t2} \frac{1}{Z(t)}\,dt = \frac{1}{2} \times \frac{1}{Z_o} \times \int_{t1}^{t2} \frac{0.4 - V_{measure}(t)}{V_{measure}(t)}\,dt \tag{6.2.3}$$

6.3 Measuring some specific function pins of the package

The following figure shows the procedures and the results of the measurement. In order to measure some pins of the LQFP64 package, the coplanar waveguide board is used in the lab, as shown in Fig 6.3.1. Data has been collected for all the pins with ground reference for LQFP64 package. The reason for using the coplanar waveguide board is to reduce the electromagnetic interference.

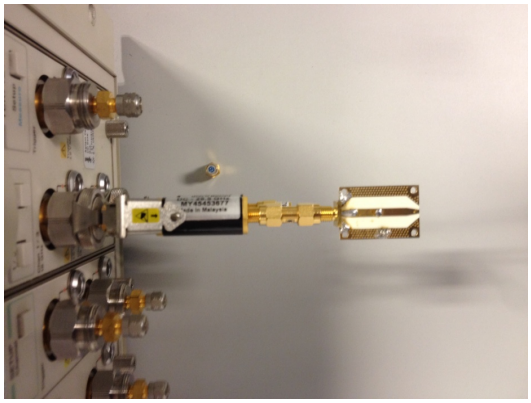

Fig 6.3.1 The coplanar waveguide board measurement

6.3.1 Package Measurement Pin 1 and Pin 8

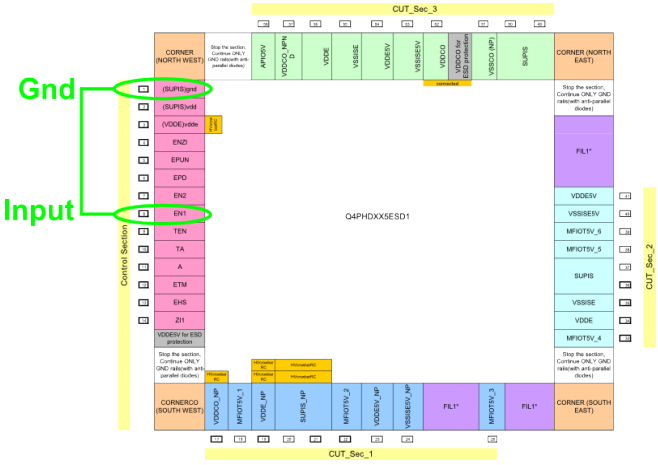

Fig 6.3.2 (a) Pin 1 and Pin 8 in the package schematic

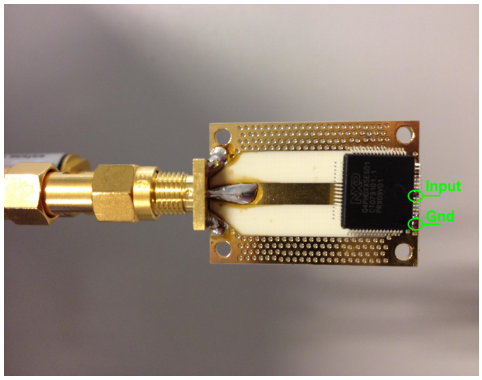

Fig 6.3.2 (b) The Measured Way of the Pin 1 and Pin 8

The Fig 6.3.2 (a) shows the package schematic of LQFP64. In this measurement, we measured the specific pins of Gnd and Input, as shown in Fig 6.3.2 (b) those are Pin 1 and Pin 8. Measuring the Pin 1 and Pin 8 because it has a sufficient range of inductance and capacitance values for the package under the test.

a) The comparison between the measurement and the simulation results

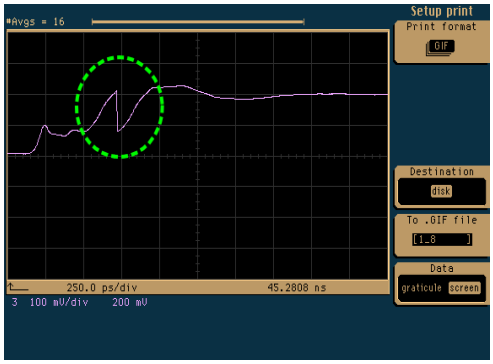

Fig 6.3.3 (a) The Voltage Waveform from TDR Measurement

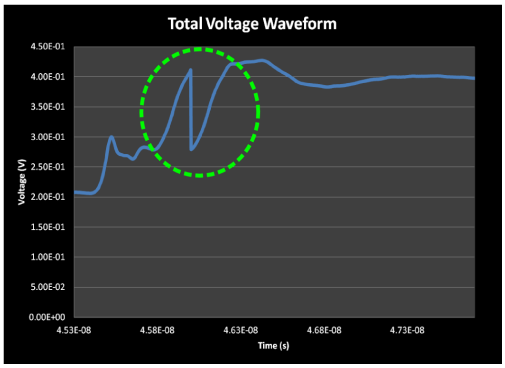

Fig 6.3.3 (b) The Voltage Waveform from EMPro® Simulation

The Fig 6.3.3 (a) shows the voltage waveform from TDR display directly. Fig 6.3.3 (b) is from EMPro Simulation. From both the above figures, we can find the total voltage waveforms of the parasitics of the package from the green dash lines. As can be seen from the green circle dash line, the spike is the characteristics of the inductance because of the bonding wire of the package. The dip after the spike that is the capacitance of the die attached of the package. The comparison between the EMPro® simulation result and the actually tested one had been conducted completely. There is a good agreement between them.

b) Extracting the parasitics of Pin 1 and Pin 8

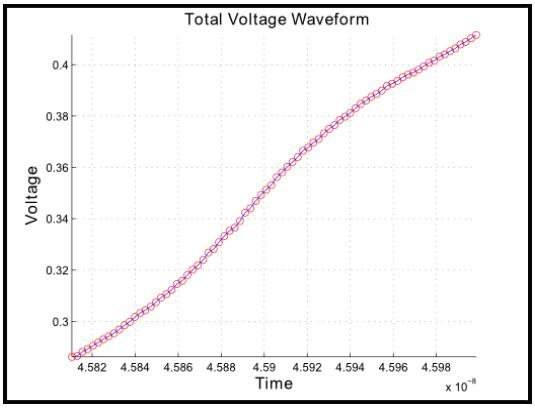

Fig 6.3.4 (a) The inductance parasitics from TDR Data

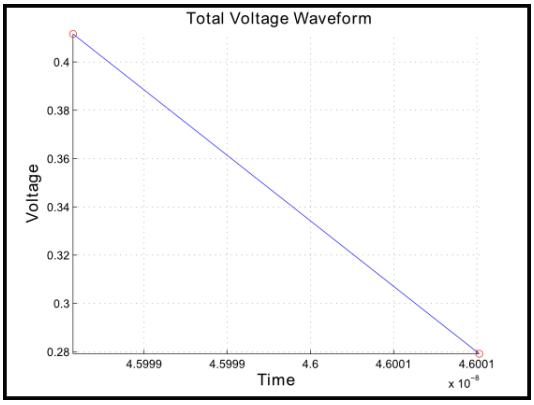

Fig 6.3.4 (b) The capacitance parasitics from TDR Data

From the above Fig 6.3.4 (a) and Fig 6.3.4 (b), the inductance and the capacitance parasitics of pin 1 and pin 8 of the package have been extracted from the measureable data. We used matlab script to get the values of inductance and capacitance that are 65.99 pH and 0.84 pF, respectively.

6.3.2 Package Measurement Pin 1 and Pin 14

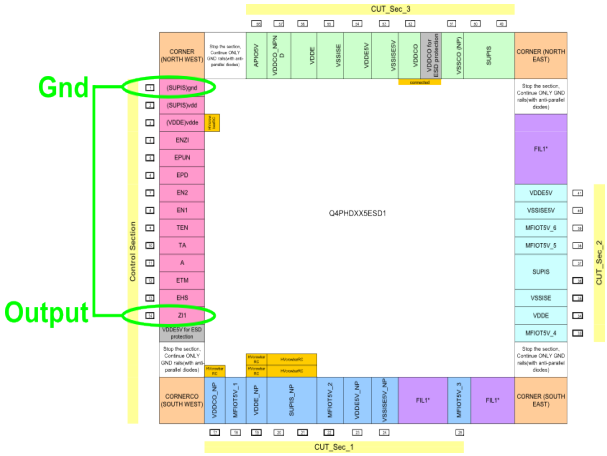

Fig 6.3.5 (a) Pin 1 and Pin 14 in the package schematic

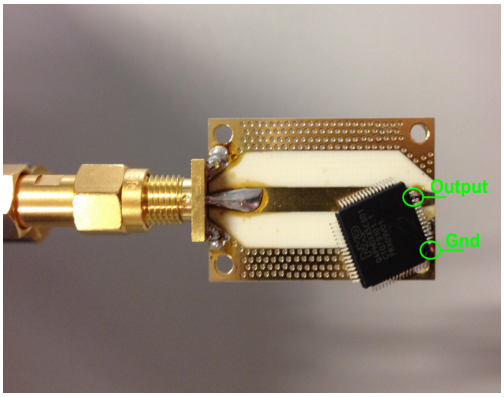

Fig 6.3.5 (b) The Measured Way of the Pin 1 and Pin 14

The Fig 6.3.5 (a) shows the package schematic of LQFP64. In this measurement, we measured the specific pins of Gnd and Output, as shown in Fig 6.3.5 (b) that are Pin 1 and Pin 14. Measuring the Pin 1 and Pin 14 is to get the parasitics of the output of the package under the test.

a) The comparison between the measurement and the simulation results

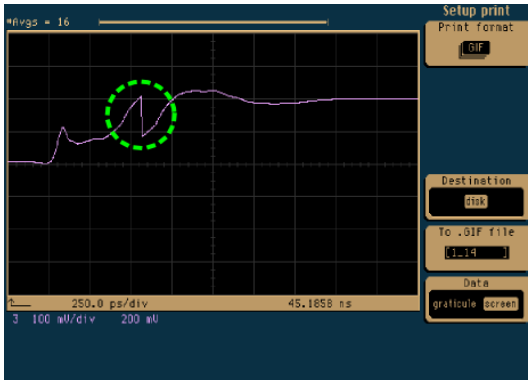

Fig 6.3.6 (a) The Voltage Waveform from TDR Measurement

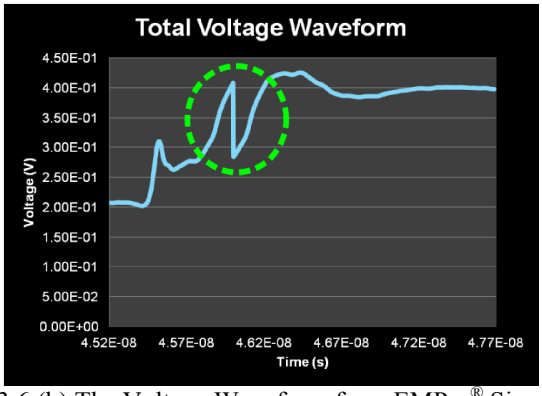

Fig 6.3.6 (b) The Voltage Waveform from EMPro® Simulation

Fig 6.3.6 (a) shows the voltage waveform from TDR display directly. From Fig 6.3.6 (b), we can see the results from EMPro Simulation. From the above figures, we can get the total voltage waveforms of the parasitics of the package from the green dash lines. As can be seen from the green circle dash line, the spike is the characteristics of the inductance because of the bonding wire of the package. The dip after the spike that is the capacitance of the die attached of the package. The comparison between the EMPro® simulation result and the actually tested one had been conducted completely. There is a good agreement between them.

b) Extracting the parasitics of Pin 1 and Pin 14

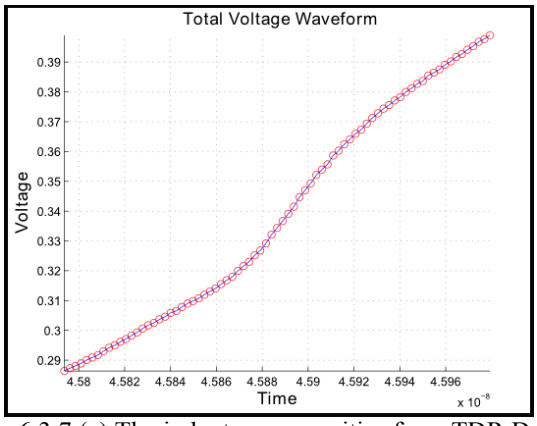

Fig 6.3.7 (a) The inductance parasitics from TDR Data

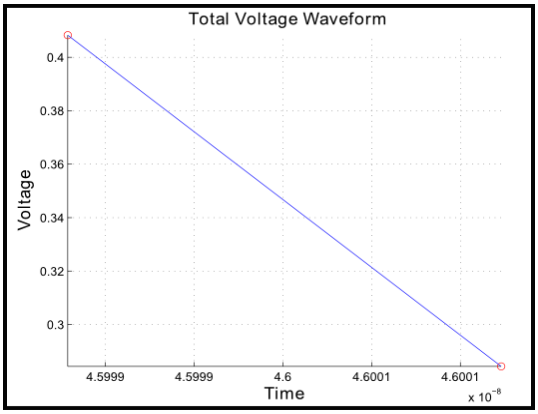

Fig 6.3.7 (b) The capacitance parasitics from TDR Data

From the above Fig 6.3.7 (a) and Fig 6.3.7 (b), the inductance and the capacitance parasitics of pin 1 and pin 14 of the package have been extracted from the measured data. We used matlab script to get the values of inductance and capacitance that are 62.91 pH and 0.85 pF, respectively.

6.3.3 Package Measurement Pin 24 and Pin 17

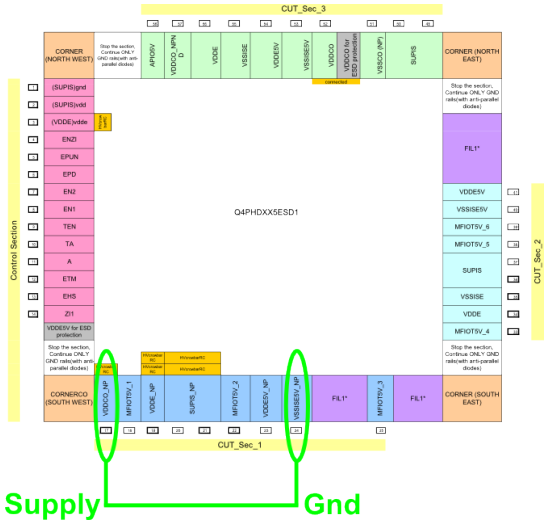

Fig 6.3.8 (a) Pin 24 and Pin 17 in the package schematic

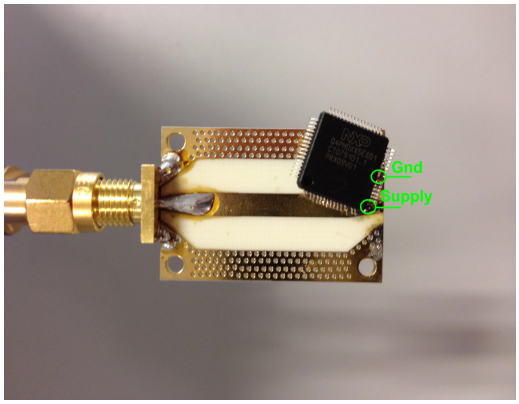

Fig 6.3.8 (b) The Measured Way of the Pin 24 and Pin 17

The Fig 6.3.8 (a) shows the package schematic of LQFP64. In this measurement, we measured the specific pins of Supply and Gnd, as shown in Fig 6.3.8 (b) that are Pin 24 and Pin 17. Measuring the Pin 24 and Pin 17 is to get the parasitics of the supply of the package under the test.

a) The comparison between the measurement and the simulation results

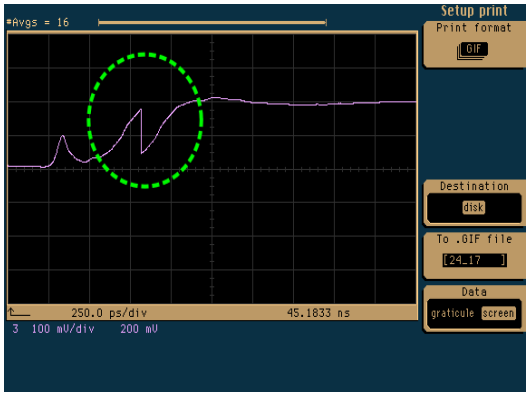

Fig 6.3.9 (a) The Voltage Waveform from TDR Measurement

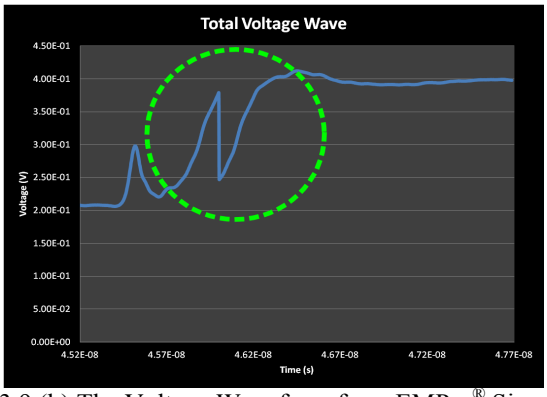

Fig 6.3.9 (b) The Voltage Waveform from EMPro® Simulation

The Fig 6.3.9 (a) shows the voltage waveform from TDR display directly. From Fig 6.3.9 (b), we can see the results from EMPro Simulation. We can get the waveforms of the parasitics of the package from the green dash lines. As can be seen from the green circle dash line, the spike is the characteristics of the inductance because of the bonding wire of the package. The dip after the spike that is the capacitance of the die attached of the package. The comparison between the EMPro® simulation result and the actually tested one had been conducted completely. There is a good agreement between them.

b) Extracting the parasitics of Pin 24 and Pin 17

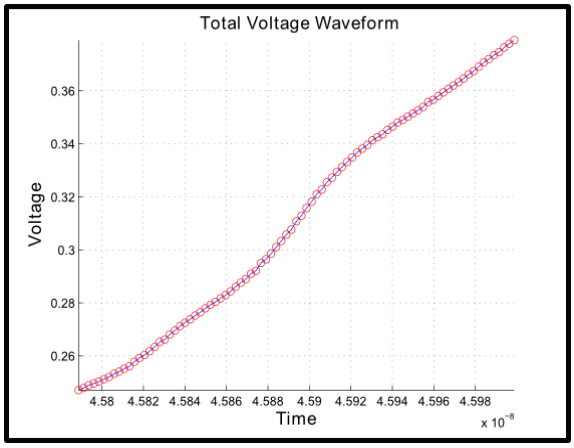

Fig 6.3.10 (a) The inductance parasitics from TDR Data

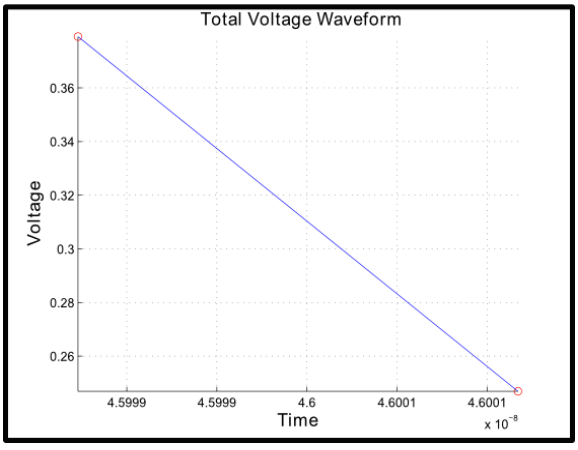

Fig 6.3.10 (b) The capacitance parasitics from TDR Data

In the above figures, the inductance and the capacitance parasitics of pin 24 and pin 17 of the package have been extracted. We used matlab script to get the values of inductance and capacitance that are 65.34 pH and 0.76 pF, respectively.

6.3.4 Package Measurement Pin 37 and Pin 33

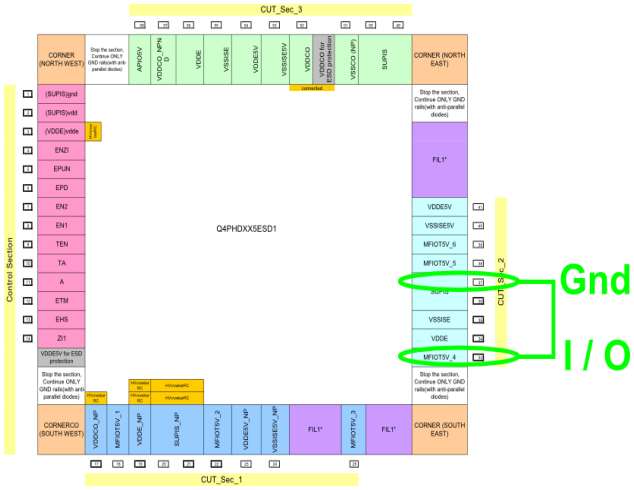

Fig 6.3.11 (a) Pin 37 and Pin 33 in the package schematic

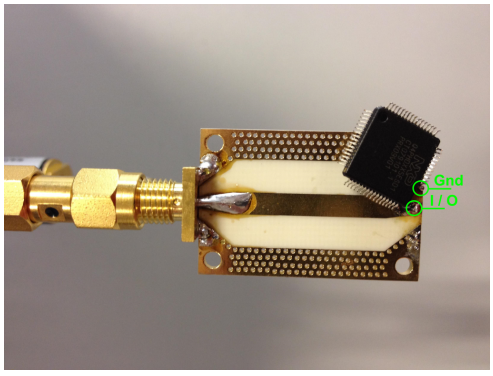

Fig 6.3.11 (b) The Measured Way of the Pin 37 and Pin 33

The Fig 6.3.11 (a) shows the package schematic of LQFP64. In this measurement, we measured the specific pins of Gnd and I/O, as shown in Fig 6.3.11 (b) that are Pin 37 and Pin 33. Measuring the Pin 37 and Pin 33 is to get the parasitics of the supply of the package under the test.

a) The comparison between the measurement and the simulation results

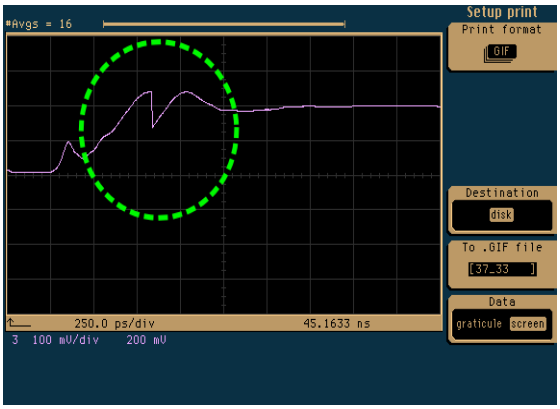

Fig 6.3.12 (a) The Voltage Waveform from TDR Measurement

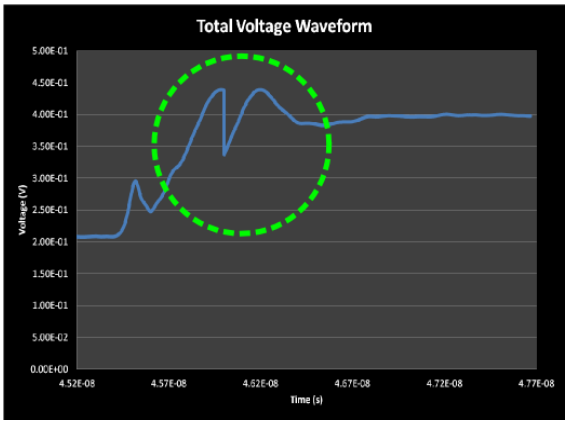

Fig 6.3.12 (b) The Voltage Waveform from EMPro® Simulation

The Fig 6.3.12 (a) shows the voltage waveform from TDR display directly. From Fig 6.3.12 (b), we can see the voltage waveform that is from EMPro Simulation. From the green dash lines, we can get the waveforms of the parasitics of the package. As can be seen from the green circle dash line, the spike is the characteristics of the inductance because of the bonding wire of the package. The dip after the spike that is the capacitance of the die attached of the package. The comparison between the EMPro® simulation result and the actually tested one had been conducted completely. There is a good agreement between them.

b) Extracting the parasitics of Pin 37 and Pin 33

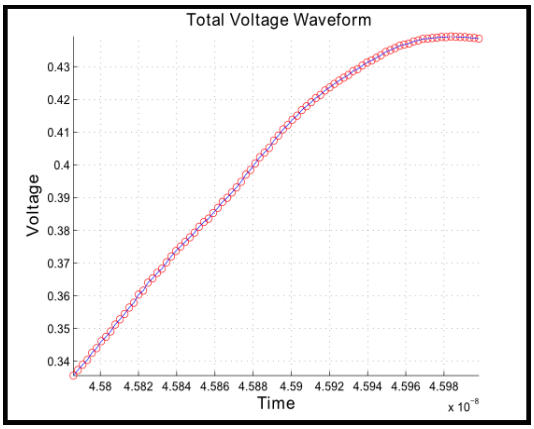

Fig 6.3.13 (a) The inductance parasitics from TDR Data

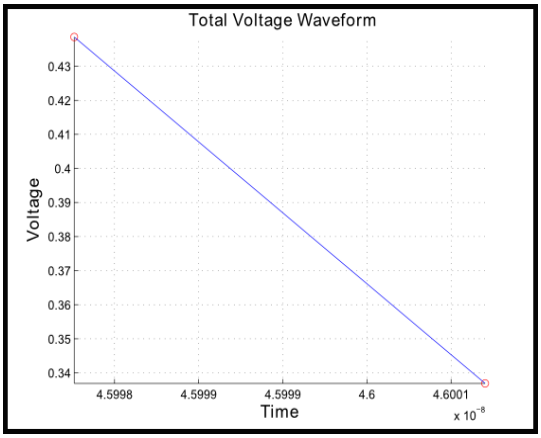

Fig 6.3.13 (b) The capacitance parasitics from TDR Data

In the above figures, the inductance and the capacitance parasitics of pin 37 and pin 33 of the package have been extracted from the measured data. We used matlab script to get the values of inductance and capacitance that are 85.18 pH and 0.95 pF, respectively.

6.3.5 Package Measurement Pin 37 and Pin 41

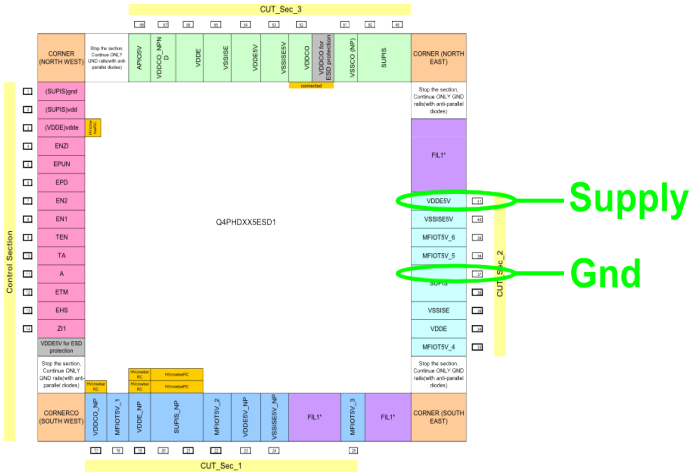

Fig 6.3.14 (a) Pin 37 and Pin 41 in the package schematic

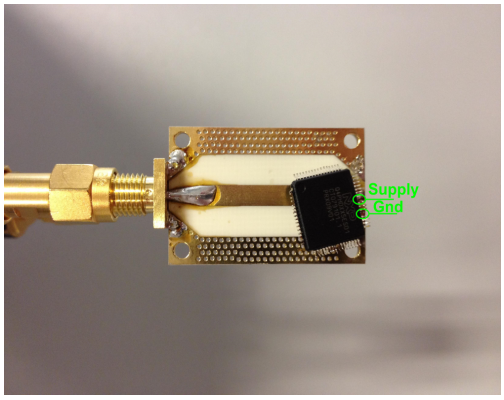

Fig 6.3.14 (b) The Measured Way of the Pin 37 and Pin 41

The Fig 6.3.14 (a) shows the package schematic of LQFP64. In this measurement, we measured the specific pins of Supply and Gnd, as shown in Fig 6.3.14 (b) that are Pin 37 and Pin 41. Measuring the Pin 37 and Pin 41 is to get the parasitics of the supply of the package under the test.

a) The comparison between the measurement and the simulation results

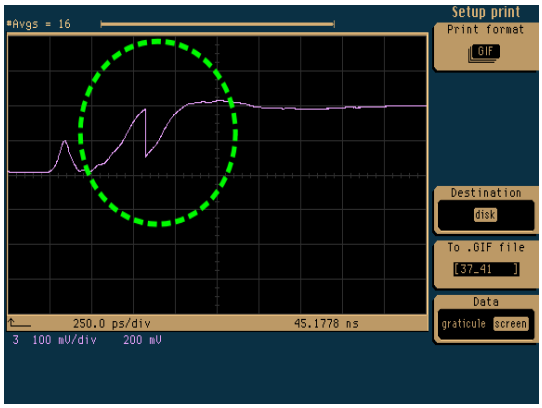

Fig 6.3.15 (a) The Voltage Waveform from TDR Measurement

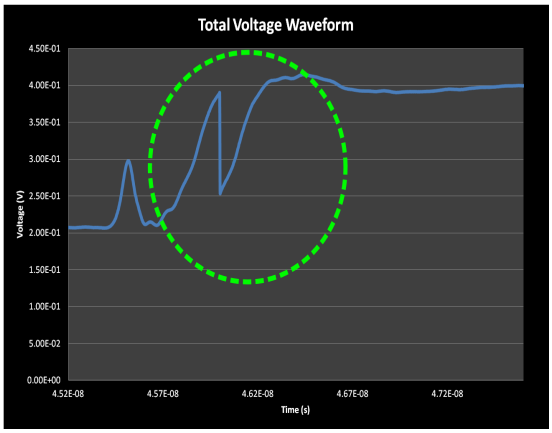

Fig 6.3.15 (b) The Voltage Waveform from EMPro® Simulation

The Fig 6.3.15 (a) shows the voltage waveform from TDR display directly. In Fig 6.3.15 (b), the voltage waveforms that is from the EMPro Simulation. From the green dash line, we can get the waveforms of the parasitics of the package. As can be seen from the green circle dash line, the spike is the characteristics of the inductance because of the bonding wire of the package. The dip after the spike that is the capacitance of the die attached of the package. The comparison between the EMPro® simulation result and the actually tested one had been conducted completely. There is a good agreement between them.

b) Extracting the parasitics of Pin 37 and Pin 41

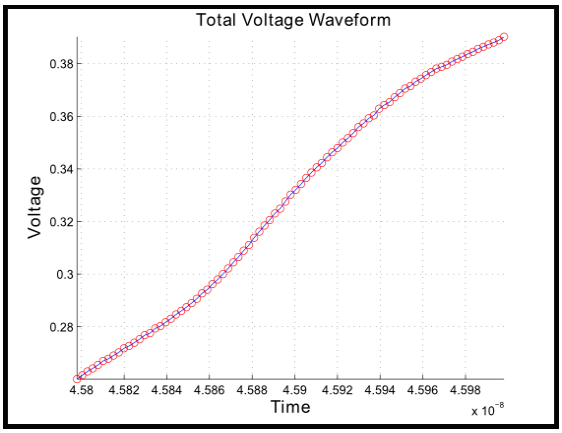

Fig 6.3.16 (a) The inductance parasitics from TDR Data

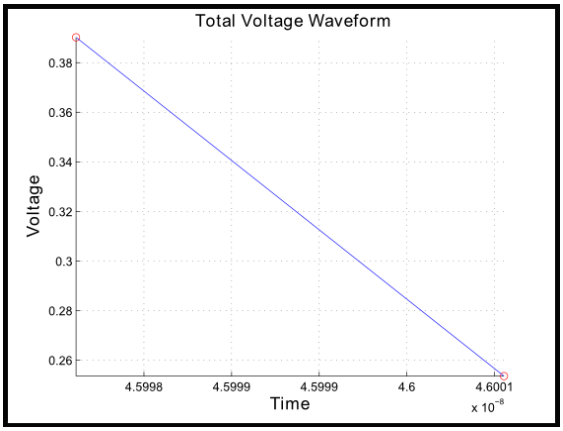

Fig 6.3.16 (b) The capacitance parasitics from TDR Data

From the above figures, the inductance and the capacitance parasitics of pin 37 and pin 41 of the package have been extracted. We used matlab script to get the values of inductance and capacitance that are 65.54 pH and 0.79 pF, respectively.

6.3.6 Package Measurement Pin 55 and Pin 58

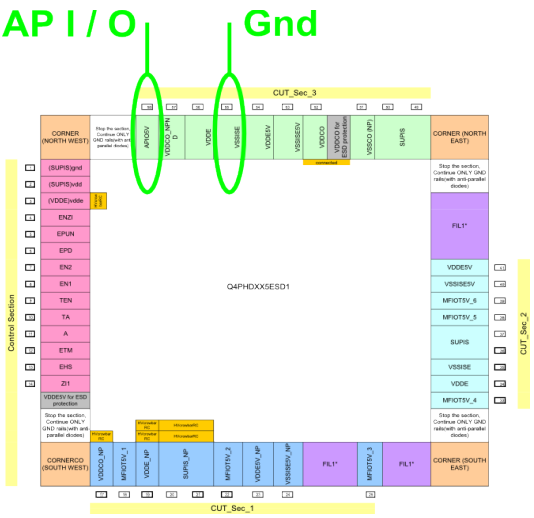

Fig 6.3.17 (a) Pin 55 and Pin 58 in the package schematic

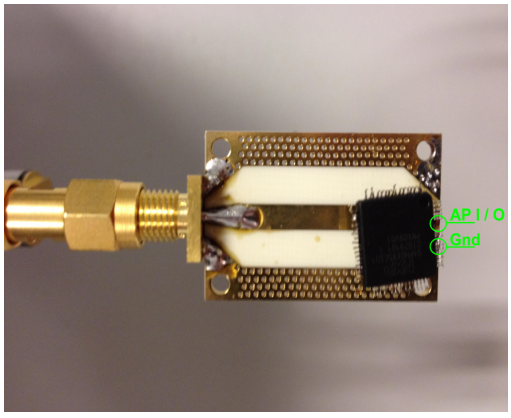

Fig 6.3.17 (b) The Measured Way of the Pin 55 and Pin 58

The Fig 6.3.17 (a) shows the package schematic of LQFP64. In this measurement, we measured the specific pins of API/O and Gnd, as shown in Fig 6.3.17 (b) that are Pin 55 and Pin 58. Measuring the Pin 55 and Pin 58 is to get the parasitics of the supply of the package under the test.

a) The comparison between the measurement and the simulation results

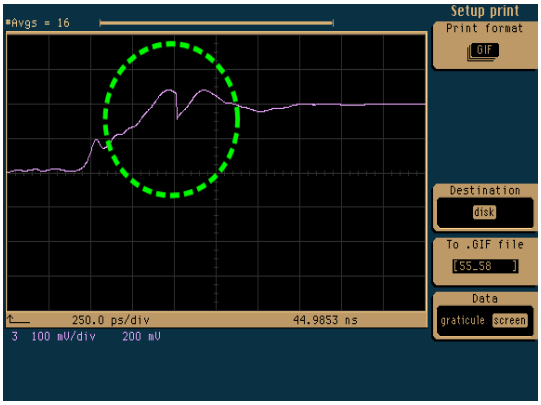

Fig 6.3.18 (a) The Voltage Waveform from TDR Measurement

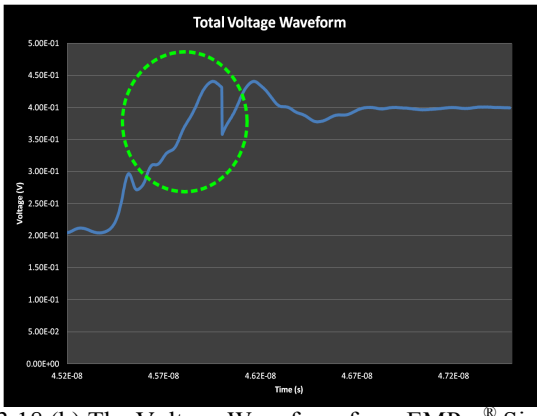

Fig 6.3.18 (b) The Voltage Waveform from EMPro® Simulation

The Fig 6.3.18 (a) shows the voltage waveform from TDR display directly. As shown in Fig 6.3.18 (b) the result is from EMPro Simulation. From the green dash line, we can get the total waveforms of the parasitics of the package. As can be seen from the green circle dash line, the spike is the characteristics of the inductance because of the bonding wire of the package. The dip after the spike that is the capacitance of the die attached of the package. The comparison between the EMPro® simulation result and the actually tested one had been conducted completely. There is a good agreement between them.

b) Extracting the parasitics of Pin 55 and Pin 58

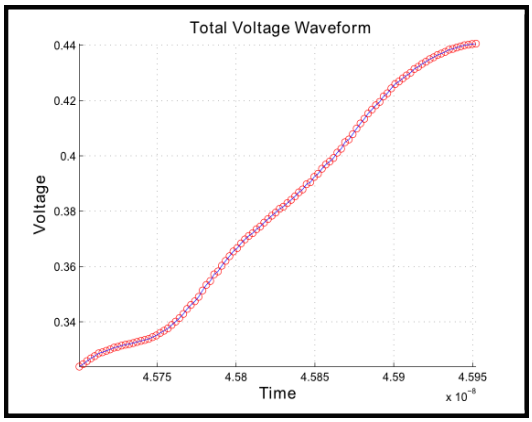

Fig 6.3.19 (a) The inductance parasitics from TDR Data

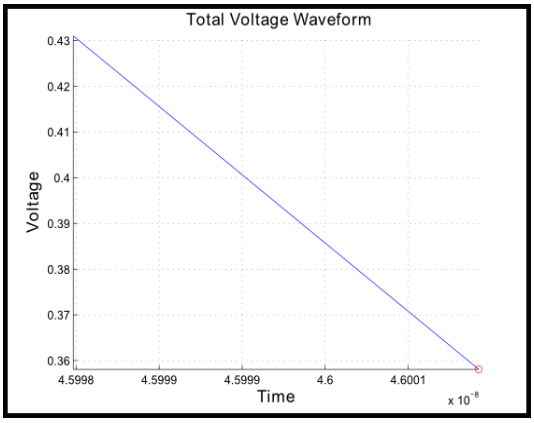

Fig 6.3.19 (b) The capacitance parasitics from TDR Data

From the above figures, the inductance and the capacitance parasitics of pin 55 and pin 58 of the package have been extracted from the measured data. We used matlab scripts to get the values of inductance and capacitance that are 95.84 pH and 0.96 pF, respectively.

6.4 Summary

Table 2. Lumped elements parameters extracted from TDR measurements of IC packages

LQFP64 Package		Extracted lumped elements	
Specific function Pin	**Ground Pin**	**$L_{T-\Pi}$ (pH)**	**C_{Π} (pF)**
Pin 8	**Pin1**	**65.99**	**0.84**
Pin 14	**Pin 1**	**62.91**	**0.85**
Pin 17	**Pin 24**	**65.34**	**0.76**
Pin 33	**Pin 37**	**85.18**	**0.95**
Pin 41	**Pin 37**	**65.54**	**0.79**
Pin 58	**Pin 55**	**95.84**	**0.96**

All in all, the true impedance profile of the pin under test (PUT) can be computed from the TDR waveform actually measured at the input of the oscilloscope TDR sampling head (6.2.1), where Z_o = 50 Ohm is the input impedance of the TDR module head and the characteristic impedance of the TDR probe; $V_{measure}$ =200mV is the incident voltage of the TDR step generator.

From the true impedance profile of the PUT measured with TDR, the LC equivalent model (combined PI and T models) is extracted from inductive spikes and capacitive dips. Table 2 shows the extracted LC model from TDR measurement of LQFP64 package.

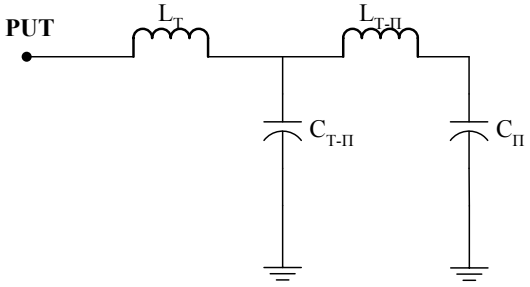

Fig. 6.4. Combined PI and T model of the PUT

The lumped elements of the PUT model (L_T, $L_{T-\Pi}$, $C_{T-\Pi}$, C_π) represent:

(i) the self-inductance of the lead frame for an LQFP64 package

(ii) the self-inductance of the bonding wire

(iii) the equivalent capacitance of the pin due to the package

(iv) the capacitance of the die or the die pad

In this measurement, the self-inductance of the lead frame and the equivalent capacitance of the pin are not taken into account.

CHAPTER 7

7 Conclusions

The project contributed to the development of accurate and simple models of IC packages (LQFP64) under ESD CDM (Charge Device Model) like circumstance, using electromagnetic simulations. During the internship in the Foundation Design Intellectual Property (FDIP) department of Design Platforms Organization at the NXP semiconductors site in Nijmegen, the characterization of packages of ICs by means of time domain reflectometry (TDR) has been successfully worked. Such characterization is needed to enable simulation for Charge Device Model (CDM) testing, one of the standard models for Electrostatic Discharge (ESD). The measurement technique by applying them is used to characterize standard components, such as resistors and capacitors. We applied this technique to characterize actual packages.

In addition, we performed 3D electromagnetic time domain simulations with simulation software, called EMPro. Using a 3D electromagnetic software as a tool for packaging design, it is possible to evaluate the RF performances and investigating different technological solution without the need to physical realize several sample. Parasitics elements associated with package leads and wire bonds have been extracted by means of a lumped equivalent circuit. Several simulation runs with transient and frequency solver were performed in order to determine the most suitable trade off in terms of accuracy, mesh size and simulation time.

Using these methods we were able to establish and verify the correlation between measurements and simulations. We can see clearly that what the differences between the measurements and simulations in the operation environment. We use the coplanar wave guide board to measure the actual package (LQFP64) since it can reduce the electromagnetic interference in some extent compared to the coax cable connection. Also, the accuracy of the measurement is improved through using the coplanar wave guide board. We measured some of the specific pins of the LQFP64 package to extract the capacitance and inductance through using time domain reflectometry (TDR). Time domain reflectometry measures the reflections that result

from a signal traveling through a transmission environment. The TDR instrument sends a pulse through the medium and compares the reflections from the unkown transmission environment to those produced by a standard impedance. The TDR display is the voltage waveform that returns when a fast step signal is propagated down a transmission line. The resulting waveform is the combination of the incident step and reflections generated when the step encounters impedance variations. Compared with frequency domain techniques, time domain based modeling is more intuitive, visual and accurate approach and direct look at the DUT's characteristics.

The methodology developed in this project can be deployed for other IC packages widely used within NXP in order to improve the predictive capability of CDM qualification for NXP products. The TDR approach has proven to give simple and accurate combined T and PI model of the IC packages pins under CDM discharge.

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Appendix

Appendix - Matlab Script Code

1. 1 Extract the capacitance parasitics on the specific pin 1 (SUPIS) Gnd and pin 8 (EN1) Input

```
A = xlsread ('1_8_Data.xlsx','Sheet 1');
x = getcolumn (A(318:319,1:2),1);
y = getcolumn (A(318:319,1:2),2);
c = trapz (x,y)
Z = [ ] ;
for i = 1 :1 :2
    Vmeas = y(i, :);
     Zt = 50*Vmeas/(0.4-Vmeas);
     Yt = 1/Zt;
     Z(end+1,:) = Zt
end
     D = diff (x);
     C = 0.5*Z.*D;
     S = sum(C(:,1))
scatter (x,y,'r');
line(x,y) ;
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth','20','FontSize',14);
title('Total Voltage Waveform','FontWeight','bold','FontSize','14')
```

1. 2 Extract the inductance parasitics on the specific pin 1 (SUPIS) Gnd and pin 8 (EN1) Input

```
A = xlsread('1_8_Data.xlsx','Sheet 1');
x = getcolumn (A(241:318, 1:2),1);
y = getcolumn (A(241:318,1:2),2);
L = trapz (x,y)
Z = [ ] ;
for i=1 :1 :77
     Vmeas = y(i,:);
     Zt = 50*Vmeas/(0.4-Vmeas);
```

```
    Z(end+1,:) = Zt
end
     D = diff(x);
    C = 0.5*Z.*D;
    S = sum (C(:,1))
scatter (x,y,'r');
line(x,y) ;
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylable('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

2.1 Extract the capacitance parasitics on the specific pin 1 (SUPIS) Gnd and pin 14 (ZI1) Output

```
A = xlsread('1_14_data.xlsx','Sheet1');
x = getcolumn(A(357:358,1:2),1);
y = getcolumn(A(357:358,1:2),2);
c = trapz (x,y)
Z = [ ] ;
for i=1 :1 :2
    Vmeas = y(i, :);
    Zt = 50*Vmeas/(0.4-Vmeas);
    Yt = 1/Zt;
    Z(end+1,:) = Zt
end
     D = diff(x);
     C = 0.5*Z.*D;
     S = sum(C(:,1))
scatter(x,y,'r');
line(x,y) ;
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylable('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

2.2 Extract the inductance parasitics on the specific pin 1 (SUPIS) Gnd and pin 14 (ZI1) Output

```
A = xlsread('1_14_Data.xlsx','Sheet1');
x = getcolumn(A(273:349,1:2),1);
y = getcolumn(A(273:349,1:2),2);
L = trapz (x,y)
Z = [ ];
for i=1:1:76
   Vmeas = y(i,:);
   Zt = 50*Vmeas/(0.4-Vmeas);
   Z(end+1,:)= Zt
end
   D = diff(x);
   C = 0.5*Z.*D;
   S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

3.1 Extract the capacitance parasitics on the specific pin 24 (VSSISE5V_NP) Gnd and pin 17 (VDDCO_NP) Supply

```
A = xlsread('24_17_Data.xlsx','Sheet1');
x = getcolumn(A(358:359,1:2),1);
y = getcolumn(A(358:359,1:2),2);
c = trapz (x,y)
Z = [ ];
for i=1:1:2
   Vmeas = y(i,:);
   Zt = 50*Vmeas/(0.4-Vmeas);
   yt = 1/Zt;
   Z(end+1,:)= Zt
end
   D = diff(x);
   C = 0.5*Z.*D;
   S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
```

```
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

3.2 Extract the inductance parasitics on the specific pin 24 (VSSISE5V_NP) Gnd and pin 17 (VDDCO_NP) Supply

```
A = xlsread('24_17_Data.xlsx','Sheet1');
x = getcolumn(A(272:358,1:2),1);
y = getcolumn(A(272:358,1:2),2);
L = trapz (x,y)
Z = [ ];
for i=1:1:86
   Vmeas = y(i,:);
   Zt = 50*Vmeas/(0.4-Vmeas);
   Z(end+1,:)= Zt
end
   D = diff(x);
   C = 0.5*Z.*D;
   S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

4.1 Extract the capacitance parasitics on the specific pin 37 (SUPIS) Gnd and pin 33 (MFIOT5V_4) I/O

```
A = xlsread('37_33_Data.xlsx','Sheet1');
x = getcolumn(A(366:367,1:2),1);
y = getcolumn(A(366:367,1:2),2);
c = trapz (x,y)
Z = [ ];
for i=1:1:2
   Vmeas = y(i,:);
   Zt = 50*Vmeas/(0.4-Vmeas);
   yt = 1/Zt;
   Z(end+1,:)= Zt
end
```

```
   D = diff(x);
   C = 0.5*Z.*D;
   S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

4.2 Extract the inductance parasitics on the specific pin 37 (SUPIS) Gnd and pin 33 (MFIOT5V_4) I/O

```
A = xlsread('37_33_Data.xlsx','Sheet1');
x = getcolumn(A(279:366,1:2),1);
y = getcolumn(A(279:366,1:2),2);
L = trapz (x,y)
Z = [ ];
for i=1:1:87
   Vmeas = y(i,:);
   Zt = 50*Vmeas/(0.4-Vmeas);
   Z(end+1,:)= Zt
end
   D = diff(x);
   C = 0.5*Z.*D;
   S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

5.1 Extract the capacitance parasitics on the specific pin 37 (SUPIS) Gnd and pin 41 (VDDE5V) Supply

```
A = xlsread('37_41_Data.xlsx','Sheet1');
x = getcolumn(A(360:361,1:2),1);
y = getcolumn(A(360:361,1:2), 2);
c = trapz (x,y)
Z = [ ];
for i=1:1:2
```

```
    Vmeas = y(i,:);
    Zt = 50*Vmeas/(0.4-Vmeas);
    yt = 1/Zt;
    Z(end+1,:)= Zt
end
    D = diff(x);
    C = 0.5*Z.*D;
    S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

5.2 Extract the inductance parasitics on the specific pin 37 (SUPIS) Gnd and pin 41 (VDDE5V) Supply

```
A = xlsread('37_41_Data.xlsx','Sheet1');
x = getcolumn(A(278:360,1:2),1);
y = getcolumn(A(278:360,1:2),2);
L = trapz (x,y)
Z = [ ];
for i=1:1:82
    Vmeas = y(i,:);
    Zt = 50*Vmeas/(0.4-Vmeas);
    Z(end+1,:)= Zt
end
    D = diff(x);
    C = 0.5*Z.*D;
    S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

6.1 Extract the capacitance parasitics on the specific pin 55 (VSSISE) Gnd and pin 58 (APIO5V) API/O

```
A = xlsread('55_58_Data.xlsx','Sheet1');
```

```
x = getcolumn(A(439:440,1:2),1);
y = getcolumn(A(439:440,1:2), 2);
c = trapz (x,y)
Y = [ ];
Z = [ ];
for i=1:1:2
   Vmeas = y(i,:);
   Zt = 50*Vmeas/(0.4-Vmeas);
   yt = 1/Zt;
   Y(end+1,:) = yt
   Z(end+1,:) = Zt
end
   D = diff(x);
   C = 0.5*Y.*D;
   S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
grid on
axis tight
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

6.2 Extract the inductance parasitics on the specific pin 55 (VSSISE) Gnd and pin 58 (APIO5V) API/O

```
A = xlsread('55_58_Data.xlsx','Sheet1');
x = getcolumn(A(317:420,1:2),1);
y = getcolumn(A(317:420,1:2),2);
Z = [ ];
for i=1:1:103
   Vmeas = y(i,:);
   Zt = 50*Vmeas/(0.4-Vmeas);
   Z(end+1,:) = Zt
end
   D = diff(x);
   C = 0.5*Z.*D;
   S = sum(C(:,1))
scatter(x,y,'r');
line(x,y);
grid on
axis tight
```

```
xlabel('Time','FontWeight','bold','linewidth',20,'FontSize',14);
ylabel('Voltage','FontWeight','bold','linewidth',20,'FontSize',14);
title ('Total Voltage Waveform','FontWeight','bold','FontSize',14)
```

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