Power and Performance Tradeoff in LTE Receiver Chains

Master Thesis

Muris Sarajlić

Lund University

A thesis submitted for the degree of

Master of Science

September 2013

Acknowledgements

First and foremost, I would like to express my sincere appreciation to Professor Ove Edfors for giving me the opportunity to do this master thesis work under his supervision.

A special word of thanks goes also to professors and PhD students at the Analog RF, Data Converters and Frequency Synthesis and Digital ASIC groups at the department of EIT: Professor Pietro Andreani, PhD students Anders Nejdel, Mohammed Abdulaziz, Xiaodong Liu and others for providing me with valuable insights and helpful advice.

I would also like to thank my friends and study colleagues for all the priceless moments we had together, both in school and outside of it. Thanks for all the trips, parties, fikas and long lunches. I hope we will meet again somewhere!

Last but not least, for my parents and my girlfriend Erna: thank you for your love and support. Although you are far away, at every moment I feel like you are right next to me. I love you.

Abstract

The continuous development and expansion of mobile systems puts increased demand on the mobile receiver designers to deliver circuits that will provide high bitrates, while at the same time the power consumption and battery life should be kept at reasonable levels, and ideally should not increase. Classical radio receiver design techniques are proving hard to meet these conflicting requirements, opening doors for introducing new and different means of designing high performance, high power-efficient receiver circuits.

Following this, newer radio receiver circuits are utilizing today's cheap, fast and power-efficient digital circuits for *digital assistance* and *digital control* of receiver blocks. This thesis focuses on the techniques of digital control and presents a basic investigation of radio receiver block properties that leads to a digital control strategy. The basic idea of digitally controlled radio receivers is to adapt the overall analog and digital processing quality to the current channel properties, with the final goal of saving power. If the receiver is operating in a channel with good quality, then it might be possible to reduce the processing quality of the receiver (introduce more thermal noise, allow increased distortion due to nonlinearity, etc.) by tuning certain parameters of receiver blocks; the output performance should not deteriorate in the process. Power savings then come as the result of decreasing the processing effort of the receiver.

In order to determine the right combination of tunable parameters of receiver blocks that will keep the overall performance above a certain threshold while at the same time consuming least power, two things need to be determined: how does the change of the parameter affect the overall performance, and how does it reflect on the power consumption.

This thesis first investigates appropriate ways of modeling the effects of RF impairments and then finds a way to connect the tunable block parameters through RF impairments with the overall performance; this is accomplished by determining the Error Vector Magnitude (EVM) of each RF impairment source, calculating the total receiver EVM and using the information about thermal noise and EVM to determine the Signal-to-Noise-and-Distortion ratio (SNDR) which serves as the overall channel quality indicator. After this, the behaviour of individual blocks of the direct-conversion receiver is analyzed in terms of a functional dependence between the value of tunable block parameters and power consumption; the analysis is performed through analyzing the tradeoffs between power consumption and performance for each block, as well as for the entire receiver. Finally, using the knowledge about the power and performance behaviour of blocks due to the tuning of block parameters, a simple strategy of digital control is proposed and supported by initial calculations, which show that power consumption savings are possible when using a channel-adaptive, digitally tunable receiver.

Table of Contents

1 Introduction

1.1 Background

In recent years, the world has witnessed an incredibly fast development of mobile phone systems and devices; by observing only the communication part, a multifold increase in transmission bitrates enabled support for an increased number of services and finally enabled a multifold increase in overall quality of user experience. Current 4G - LTE (Long Term Evolution) systems are designed to provide maximum downlink and uplink bitrates of 100 Mbps and 50 Mbps, respectively, whereas the LTE-Advanced (LTE-A) systems, which are currently in development, should provide transmission bitrates of 1 Gbps in the downlink and 500 Mbps in the uplink ("downlink" and "uplink" are referred to the user equipment - mobile device). Increased bitrates inevitably cause an increase in power consumption in receiver circuits, which reduces the battery life of the mobile device. Therefore, there is a big challenge imposed on transceiver designers to deliver power-efficient analog and digital circuits that will still have processing power needed to support the nominal bitrates.

Luckily, the development of mobile systems ran in parallel to the development of digital circuit technology, which has seen a continuous reduction of the size of fundamental components - integrated transistors, as well as an increase of processing speed. This development not only serves to support the increased demand on processing power in the digital domain, but can also be cleverly used to improve the performance of integrated analog blocks of the receiver. This can be implemented in two ways:

- By using digital signal processing techniques to correct errors induced in the analog part of the receiver: this can be done either in the analog part - at the place of the error generation ("clean RF" approach) or in a special block for digital correction of impairments situated at the front of the digital baseband part of the receiver (the "dirty RF" approach);
- By designing analog receiver blocks to be reconfigurable and digitally tunable. Values of one or several parameters of an analog block are allowed to change during operation, thus affecting the peformance and power consumption of the block. The idea is to adjust the performance of the block to current overall performance requirements, *e.g.* reduce its performance quality if a high quality is not needed; due to inherent tradeoffs between power consumption and performance quality for the blocks, a reduction of performance quality would directly result in savings in power consumption. Analog blocks would be controlled by an external digital global controller which uses the information about current performance requirements to set the tunable parameters of analog blocks to proper values.

Receiver design employing digital control can go one step further, so the controller not only controls analog, but also *digital* blocks, because there is room for benefitting from power/performance tradeoffs in the digital domain also.

Determining the proper values for tunable parameters of analog and digital blocks is not a trivial task. Reconfiguring one block might influence the performance of other blocks, so we always have to have the insight in how the *overall* receiver chain performance is influenced by tuning one

parameter. Furthermore, it might be possible to save more power by reconfiguring one block than by reconfiguring some other block. It is obvious that the values of tunable parameters are obtained by solving an *optimization* problem.

This optimization problem can be formulated with the help of a generic model of the radio receiver chain given in Figure 1.

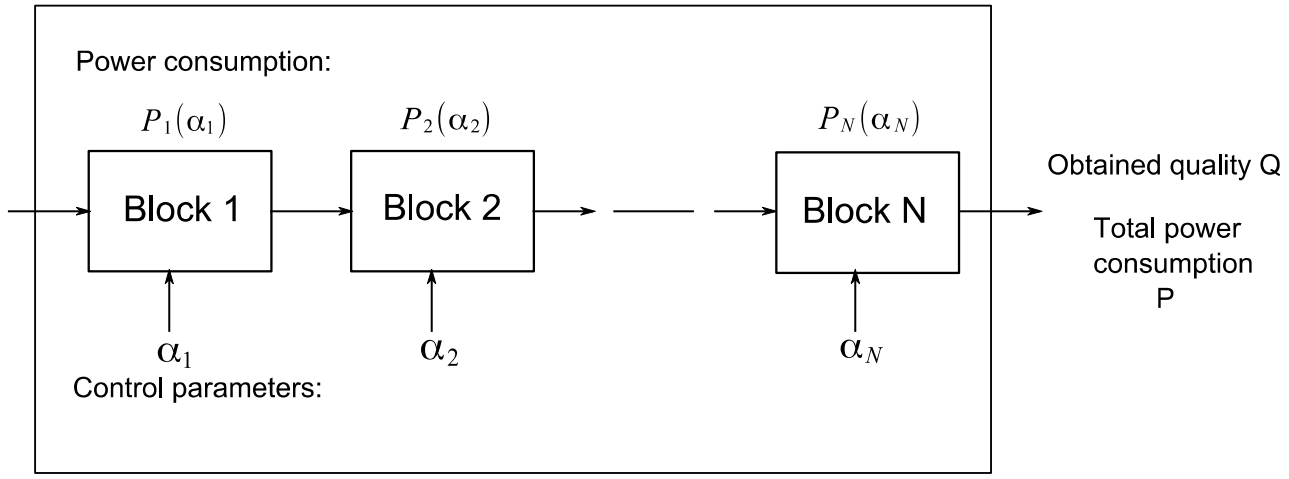

Figure 1: Generic receiver chain model

The parameter α_k is used to tune the performance and power consumption of each block. It can be assumed that the overall power consumption is the sum of power consumptions of individual blocks

$$P(\alpha_1, \alpha_2, \ldots \alpha_N) = \sum_{k=1}^{N} P_k(\alpha_k) \quad . \qquad (1.1)$$

The overall performance quality (measured as BER, BLER, or in terms of equivalent SNR, or other performance indicators) is a function of tunable parameters α_k that is generally more complex than a simple linear combination of performance quality for each individual block. This is due to the heavy influence that certain block parameters exert on the performance of other blocks. The overall performance is also a function of external variables, like interference and fading that can be subsumed in an enviroment variable Θ, so $Q = Q(\alpha_1, \alpha_2, \ldots \alpha_N, \Theta)$. The task of finding the optimal vector of parameters $[\alpha_1, \alpha_2, \ldots \alpha_N]_{opt}$ is then the task of solving the optimization problem

$$\begin{aligned} &\textit{minimize} && P(\alpha_1, \alpha_2, \ldots \alpha_N) \\ &\textit{subject to} && Q(\alpha_1, \alpha_2, \ldots \alpha_N, \Theta) \geqslant Q_{bound} \quad , \end{aligned} \qquad (1.2)$$

where Q_{bound} is a bounding value for the overall performance.

1.2 Thesis goals

The objectives of this master thesis work are:

1. Finding the appropriate tunable parameters for each block of the receiver chain;
2. Analyzing the influence tunable parameters have on power consumption and performance quality of the chosen block;
3. Establishing the connections between individual parameters that will determine the overall

performance quality Q;

4. Using the information obtained under steps 1 - 3, setting up a framework for solving the optimization problem (1.2). Power consumption and performance quality models found under 2. and 3. should be tractable - have reasonable complexity that will enable relatively simple solving of the optimization problem, while at the same time the precision of the model should not be reduced;
5. Solving the optimization problem (1.2) by using the developed framework and proving that power consumption can be reduced by adapting the receiver blocks to the demands for performance quality.

1.3 Thesis outline

This thesis work has the following outline:

- **Chapter 2** presents an analysis of RF impairments and their models. Also, the Error Vector Magnitude (EVM) is introduced as a unifying model of RF impairments' impact on the overall performance quality of the receiver system; this provides a tractable (and at the same time reasonably accurate) model of the quality function Q from (1.2);
- **Chapter 3** describes the functionality and design of the analog blocks of the receiver chain, lists the possible tunable parameters of these blocks and analyzes their impact on power consumption and performance;
- **Chapter 4** provides the same type of analysis given in Chapter 3, but applied to the mixed-signal and digital parts of the receiver;
- **Chapter 5** gives a concise overview of information gathered about tunable parameters and local and global power/performance tradeoffs;
- In **Chapter 6,** the EVM - based framework is applied to calculate the tunable parameters of a channel-adaptive receiver; this receiver is compared in terms of power consumption with a non-adaptive design.
- Finally, **Chapter 7** gives a conclusion of the work, as well as possible improvements and guidelines for future work.

2 Overview of RF Impairment Modeling

Real-life radio receivers suffer from performance degradation caused by thermal noise, as well as various signal degradations caused by component and system imperfections. This chapter will give a brief overview of these degradations, analyze their impact on multicarrier systems and introduce a unifying approach of measuring their effect.

2.1 RF impairments

2.1.1 Thermal noise

Thermal noise is generated by resistive components inside receiver blocks and is caused by the chaotic movement of electrons. The power of thermal noise is given by

$$P_n = kTB \quad , \tag{2.1}$$

where k is Boltzmann's constant, T is the temperature in Kelvins and B the bandwidth of the device.

A measure of the influence of thermal noise on the SNR degradation is the *noise figure F*, defined as

$$F = \frac{SNR_{\text{in}}}{SNR_{out}} \quad . \tag{2.2}$$

For a cascade of noisy blocks with gains G_i and noise figures F_i, the equivalent noise figure for the cascade is given by the *Friis' formula*

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_N - 1}{G_1 G_2 \cdots G_{N-1}} \quad . \tag{2.3}$$

The total noise figure enables us to represent the noise generated in the whole receiver by a single noise source with power equal to

$$P_{n,total} = kTBF_{total} \quad . \tag{2.4}$$

2.1.2 Nonlinearity

Although modeled as linear when dealing with input signals of small amplitude, most receiver blocks actually exhibit nonlinear behaviour with arbitrary levels of input signals. Significant causes of nonlinearity are saturation of active electronic elements and component mismatch.

One of the commonly used ways to represent nonlinearities is by using the polynomial

input-output model [1]:

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \quad . \tag{2.5}$$

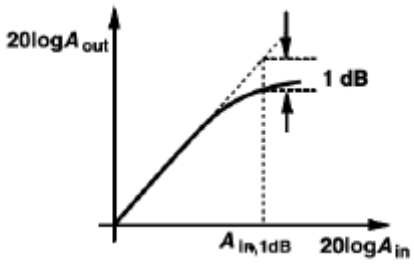

Figure 2: 1 dB compression point ([1])

A majority of RF devices of interest has a so-called "compressive" characteristic with $\alpha_3 < 0$. This means that the amplitude gain *decreases* with the increase of the input signal amplitude A, or as it is popularly put, the device "goes into compression" for sufficiently high input signal levels (or powers). The compression is characterized by the *1 dB compression point* $(CP_{1\text{dB}})$ - the input signal power for which the actual output deviates from the linear one for 1 dB. It can be shown that (for a single sinusoidal tone at the output) the input signal amplitude at the 1 dB compression point is

$$A_{CP1dB} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|} \tag{2.6}$$

A phenomenon analogous to compression occurs when the wanted signal is joined by a strong interferer. In the case of a compressive nonlinear device, the interferer will reduce the gain, effectively "drowning" the wanted signal. This phenomenon is called "desensitization" or "blocking", and therefore a more common term for a single interferer in RF parlance is "blocker".

If the single-tone interferer is substituted by an amplitude-modulated signal, the wanted signal modulates this signal (and additionally broadens its spectrum), so in the end the interferer and wanted signal spectra overlap. This phenomenon is called "cross-modulation".

Next we analyze the situation when the signal is accompanied not by one, but by two interferers (a very common situation in real-life radio systems). The interferer tone pair can be modeled as $x(t) = A_1 \cos(\omega_{\text{int},1} t) + A_2 \cos(\omega_{\text{int},2} t)$. The ouput of the nonlinear device (2.5) contains, other than the components at frequencies $\omega_{\text{int},1}$ and $\omega_{\text{int},1}$, a DC component and 10 additional components at various frequencies., given in Figure 3.

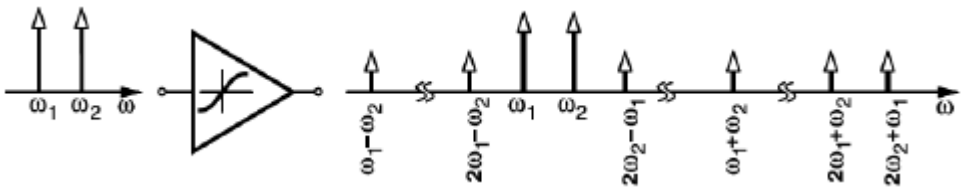

Figure 3: Various intermodulation products of the two interferers [1]

Of all the intermodulation products created by the linearity, the ones sitting at frequencies $(\omega_{\text{int},2} - 2\omega_{\text{int},1})$ and $(\omega_{\text{int},1} - 2\omega_{\text{int},2})$ (the so-called "third-order intermodulation products", or IM3) present the highest danger to the wanted signal: if the wanted signal has, *e.g.* frequency $\omega_0 = 2\omega_{\text{int},1} - \omega_{\text{int},2}$, one of these newly created frequency components will directly interfere with

it. This scenario is not at all uncommon in real-life radio systems.

A measure of the level of influence the third-order nonlinearities have in the system is the *third-order intercept point* (IP3). The input IP3 is defined as the input signal level for which the system output (clear of any influence of nonlinearities) is equal to the IM3, and is calculated as

$$A_{IIP3}=\sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.7}$$

The device goes into saturation long before the A_{IIP3}, so it is not a directly measurable value. It can be shown that A_{CP1dB} is about 10 dB lower than A_{IIP3}.

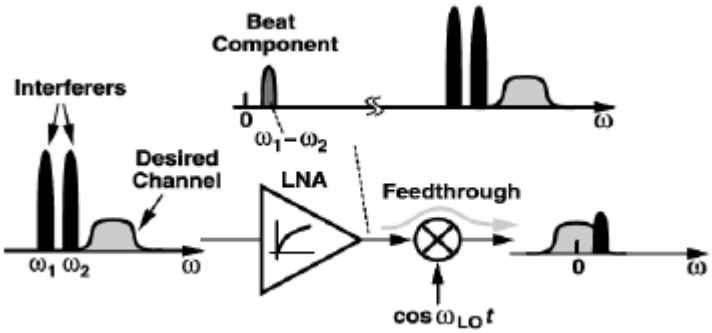

Figure 4: Impact of IM2 on the direct-conversion receiver [1]

In addition to IM3, direct-conversion receivers are vulnerable to IM2. The description of this influence is somewhat more involved than the simple mixing effect of IM3. As it is described in [1], the imbalance between the mixers in the I and Q branches of the receiver can cause a DC component to accompany the carrier frequency tone, thus allowing any baseband frequency content to pass "through" the mixer without altering its carrier frequency. On the other hand, if the two interferers are close in frequency, their order - two intermodulation product (IM2) at $(\omega_{\text{int},1}-\omega_{\text{int},2})$ falls into the baseband, and combined with mixer mismatch can interfere with the downconverted wanted signal. This scenario is described in Figure 4.

The measure of impact of the IM2 is the *second-order intercept point* (IP2), defined as the input level for which the IM2 is equal to the distortion-free input, and calculated simply as

$$A_{IIP2}=\frac{\alpha_1}{\alpha_2} \tag{2.8}$$

A phenomenon observed when analysing the effects of nonlinearities in frequency domain is *spectral regrowth*. To describe it, it is best to consider the polynomial nonlinearity model and an arbitrary lowpass input signal $x_L(t)$. Assuming just the third-order nonlinearity, the output of a nonlinear system in the time domain can be written in the form [2]

$$y_L(t)=x_L(t)+\alpha_3 x_L^2(t)x_L^*(t)\ , \tag{2.9}$$

where subscript *L* denotes that the signal is lowpass (baseband), and * in the superscript denotes the complex conjugate. If we assume $x(t)$ is deterministic, the frequency-domain version of (2.9) is

$$Y_L(f)=X_L(f)+\alpha_3 X_L(f)*X_L(f)*X_L^*(-f)\ , \tag{2.10}$$

where the operator $*$ denotes convolution. As the spectrum of the signal is convoluted with itself, the signal experiences a broadening of the spectrum (signal power leaks into adjacent bands).

The coefficients of the polynomial nonlinearity model are usually hard to obtain from measurement. Based on the observation that the nonlinearity depends only on the input signal amplitude (not the phase) [2], two metrics are introduced that describe the mapping from input

amplitude to output amplitude and to output phase. These metrics are called AM-to-AM and AM-to-PM characteristics, respectively. For a complex baseband signal, $x_L(t)=a_L(t)e^{j\phi(t)}$, the AM-AM characteristic can be denoted as $f(a_L(t))$ and the AM-PM as $g(a_L(t))$. The total output signal can then be expressed as

$$y_L(t)=f(a_L(t))e^{j(\phi(t)+g(a_L(t)))} \tag{2.11}$$

Some parameters of these functions can be determined by measurements, and then the complete characteristics are derived empirically from the measurement results.

It has been observed ([3], [4], [5]) that the effects nonlinearities have on the OFDM signal exhibit themselves as a rotation and attenuation of the signal constellation, plus an addition of a noise term. If we observe this influence through the AM-AM/AM-PM model of the nonlinearity, we can conclude that:

- The rotation of the constellation comes from the AM-PM characteristic. If $g(a_L(t))=0$, there is no rotation. This is the case for some very common nonlinear models, like the baseband polynomial model for a nonlinear device without memory [6], as well as hard and soft limiter models.
- The attenuation and noise factor are due to the AM-AM characteristic. The subcarriers produce intermodulation products that interfere with other subcarriers, causing intercarrier interference (ICI), which appears in the constellation diagram in the form of noise "clouds" around constellation points.

In [5], these effects have been expressed in a form of a mathematical model, and the validity of this model has been proven. The model can be formulated as

$$Y_k=\mu_{NL}X_k+D_{k,NL}\ , \tag{2.12}$$

where Y_k and X_k are the received and sent OFDM symbols for the *k*th subcarrier respectively, μ_{NL} is a complex gain factor not depending on the subcarrier index (describing the attenuation and rotation of the whole constellation) and $D_{k,NL}$ is a nonlinear distortion (NLD) noise term; the NLD noise is not correlated with the signal at the nonlinear device input. For a large number of subcarriers *N,* this noise can be assumed to be complex Gaussian. Analytical expressions for μ_{NL} and the variance of $D_{k,NL}$, σ^2_{NL} expressed via AM-AM and AM-PM characteristics are given in [5].

Using the MATLAB code from [2], the influence of a third-order nonlinearity on an OFDM system using QPSK is demonstrated and shown in Figure 5. The IIP3, expressed as a power measure on a 50 ohm load, is equal to -5 dBm.

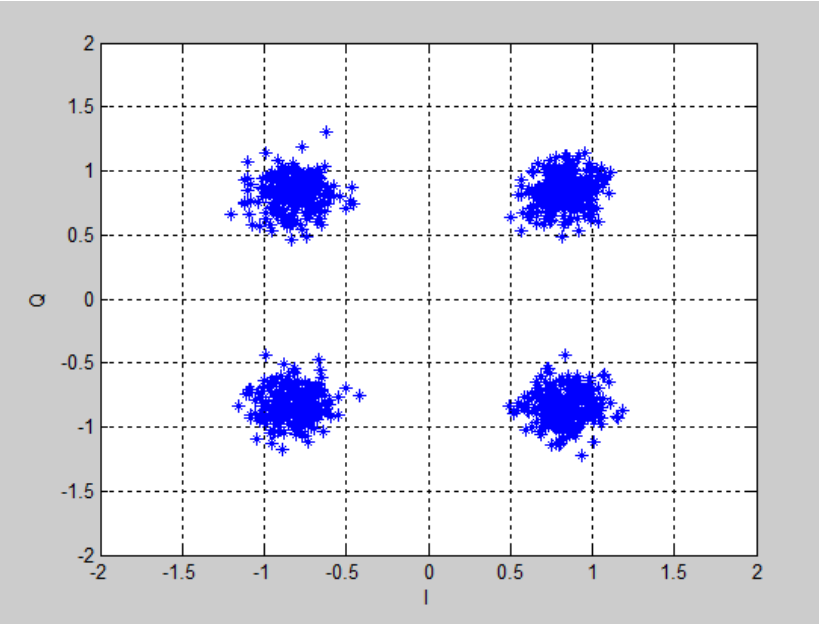

Figure 5: Influence of a third-order nonlinearity on the OFDM system

As said before, the third-order memoryless polynomial nonlinarity model does not introduce any phase shift and therefore there is no observed rotation of the constellation. There is, however, an attenuation (the constellation gets "compressed" - its points come closer together.

2.1.3 Carrier frequency offset (CFO)

In direct conversion receivers, CFO is defined as the offset between the local oscillator frequency and the carrier frequency. For an OFDM signal, the CFO exhibits itself as a phase shift common to all subcarriers (rotation of the constellation), plus a noise-like additive component coming from intercarrier interference (FCO causes a loss of orthogonality between subcarriers).

2.1.4 Sampling clock offset

All clocks and local oscillators in a receiver usually use a single reference oscillator (crystal oscillator). Therefore, any drift of the crystal oscillator that causes the CFO will also cause a sampling clock offset in the ADC. The impact of the sampling clock offset on an OFDM signal is similar to the one CFO has, with additional amplitude distortion.

2.1.5 Local oscillator leakage - DC offset

Due to imperfections of integrated electronic components and on-chip manufacturing process, a certain amount of local oscillator signal "leaks" to other parts of the analog front-end. One part of the leaked signal goes through the antenna, causing desensitization of the nearby receivers operating in the same band. It can also bounce off neighboring objects, get received and downconverted to baseband; because of relative movement of the receiver, this can result in a *slowly time-varying DC offset*. Another part of the leaked signal returns towards the mixer and mixes with itself, creating a *static DC offset* component that interferes with the downconverted

wanted signal. This offsets the signal at the input of the ADC, reducing its dynamic range [2].

2.1.6 I/Q imbalance

If the I and Q branches of the direct conversion receiver don't have same gains and/or phases, we say that I/Q imbalance occurs. There are three main causes of the I/Q imbalance [1]:

- errors in the 90° phase shift circuit
- mismatch of the mixers
- mismatch of baseband components (baseband filters and ADCs)

It can be shown that, due to I/Q imbalance, the baseband signal gets scaled and interferes with a scaled complex conjugate version of itself. If observed in frequency domain

$$X_{LP}(f)=\alpha_R X_L(f)+\beta_R X_L^*(-f) \tag{2.13}$$

we see this implies that the positive part of the spectrum overlaps with the scaled negative ("mirrored") part of itself. This effect is observed equally in single- and multicarrier systems; in multicarrier systems this implies overlapping of a subcarrier with a "mirrored" subcarrier.

2.1.7 Phase noise

Local oscillator frequency in real-life receivers is not a pure sine wave. The local oscillator exhibits random changes of the instantaneous frequency, which is equivalent to a random phase shift. The local oscillator signal can therefore be modeled as

$$x_{osc}(t)=e^{j2\pi f_c t}e^{j\phi(t)} \tag{2.14}$$

where $\phi(t)$ is the phase noise process. Phase noise can be also described as a *random phase modulation* of the signal of the local oscillator, which transfers directly to a random phase modulation of the wanted signal. The received baseband signal is thus

$$y_L(t)=x_L(t)e^{j\phi(t)} \tag{2.15}$$

Phase noise is usually characterized by its one-sided power spectral density (PSD) $L_\phi(f)$. For free-running oscillators, the phase noise is modeled as a Wiener process with a Lorentzian PSD ([1], [7], [8]). However, most receivers use phase locked loop (PLL)-based frequency synthesizers for downconversion, and the PSD in PLL is a rather intricate function of various white and colored noise sources in the voltage-controlled oscillator (VCO) and the reference cristal oscillator (CO), as well as the transfer function of the PLL ([1], [7], [8]). An example of a resulting phase noise "mask" is shown in Figure 6.

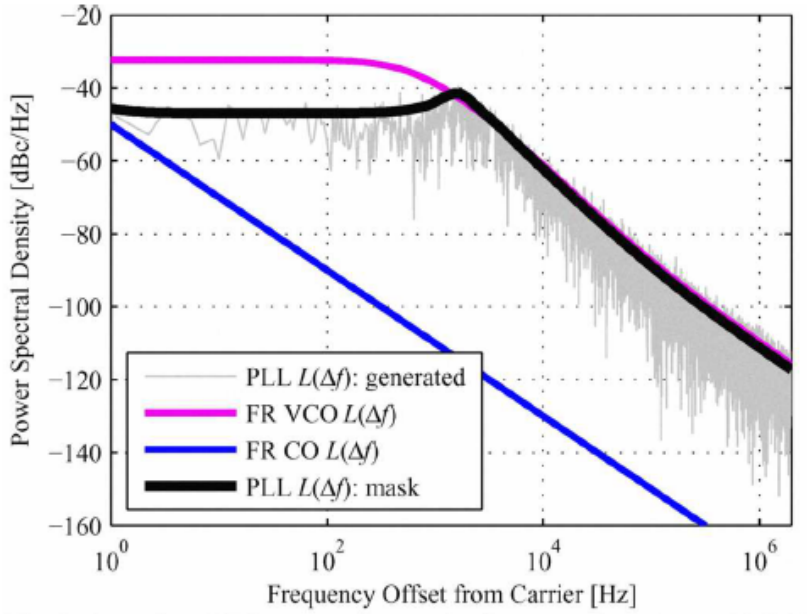

Figure 6: An example of a PLL phase noise mask, together with free-running VCO and CO PSDs shown for comparison [7]

The measured phase noise PSD is expressed relative to the carrier power.

The total power of the phase noise is

$$\sigma_{\phi}^{2}=2\int_{0}^{f_B} L_{\phi}(f)\,df \quad , \tag{2.16}$$

where f_B is the receiver bandwidth (determined by the baseband channel select filter).

The effect of phase noise in OFDM systems has been analyzed in [9] and [10]. Following the analysis presented in these papers, we can first start by recognizing the time - domain symbols at the OFDM modulator output as

$$x_n=\sum_{k=0}^{N-1} X_k e^{j2\pi\frac{k}{N}n} \quad , \tag{2.17}$$

where X_k are frequency-domain data symbols. To simplify things, the channel is considered flat and with unity gain. Only the influence of phase noise is considered, and the received samples affected by the PN are then given as

$$r_n=x_n e^{j\phi(n)} \tag{2.18}$$

where $\phi(n)$ is the sampled phase noise process $\phi(t)$. The OFDM demodulator performs the DFT, generating

$$Y_k=\frac{1}{N}\sum_{m=0}^{N-1} r_m e^{-j2\pi\frac{m}{N}k} \quad . \tag{2.19}$$

Assuming that $\phi(n)$ is small (a valid assumption for most state-of-the-art frequency synthesizers), we have

$$e^{j\phi(n)}\approx 1+j\cdot\phi(n) \quad . \tag{2.20}$$

Using this assumption, we obtain

$$Y_k = X_k + \frac{j}{N}\sum_{r=0}^{N-1} X_r \sum_{m=0}^{N-1} \phi(m) e^{j2\pi\frac{(r-k)}{N}m} = X_k + E_k \quad , \qquad (2.21)$$

which implies that the received symbol is equal to the sent symbol, plus an error term E_k . This error term is analyzed for two cases:

- when r = k:

$$E_k = j\, X_k \Phi \qquad (2.22)$$

with Φ being the average of the phase noise across all the samples:

$$\Phi = \frac{1}{N}\sum_{n=0}^{N-1} \phi(n) \qquad (2.23)$$

We can conclude that all subcarriers experience the same amount of phase shift (from (2.20), (2.21) and (2.22), $Y_k = X_k + jX_k\Phi = X_k(1 + j\Phi) \approx X_k e^{j\Phi}$) equal to Φ . This phase shift is referred to as the *common phase error* (CPE). As OFDM-based systems like LTE employ pilot-based channel estimation and equalization schemes, CPE is removed - to a certain extent - in the process of channel equalization.

- when $r \neq k$:

$$E_k = ICI_k = \frac{j}{N}\sum_{\substack{r=0,\\ r\neq k}}^{N-1} X_r \sum_{n=0}^{N-1} \phi(n) e^{j2\pi\frac{(r-k)}{N}n} \qquad (2.24)$$

As it can be read from this expression, symbols from every subcarrier (multiplied by a complex gain factor) interfere with each of the remaining subcarriers. Phase noise therefore introduces a loss of orthogonality between subcarriers, or ICI.

If the phase noise is narrowband compared to the subcarrier bandwidth (its samples are very correlated, if we observe them in time domain) then it doesn't change much across one set of *N* samples and $\Phi \neq 0$. This means that CPE is the dominant error mechanism for narrowband phase noise. CPE can be removed in the process of pilot-assisted channel estimation and equalization (same as in the case of carrier frequency offset).

On the other hand, if the phase noise is broadband, it is fairly uncorrelated across the set of *N* samples and it averages out to 0, $\Phi \approx 0$. This means that for broadband phase noise CPE is negligible and ICI is the dominant error mechanism.

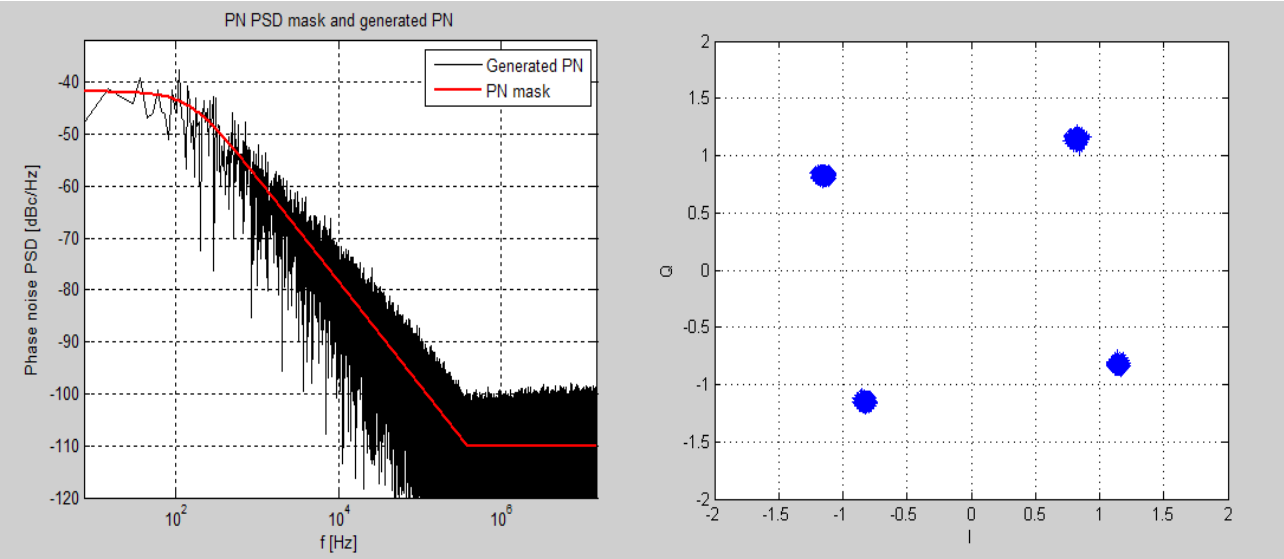

Figure 7: Phase noise spectrum (left) and a QPSK constellation diagram (right): PN 3 dB bandwidth = 150 Hz

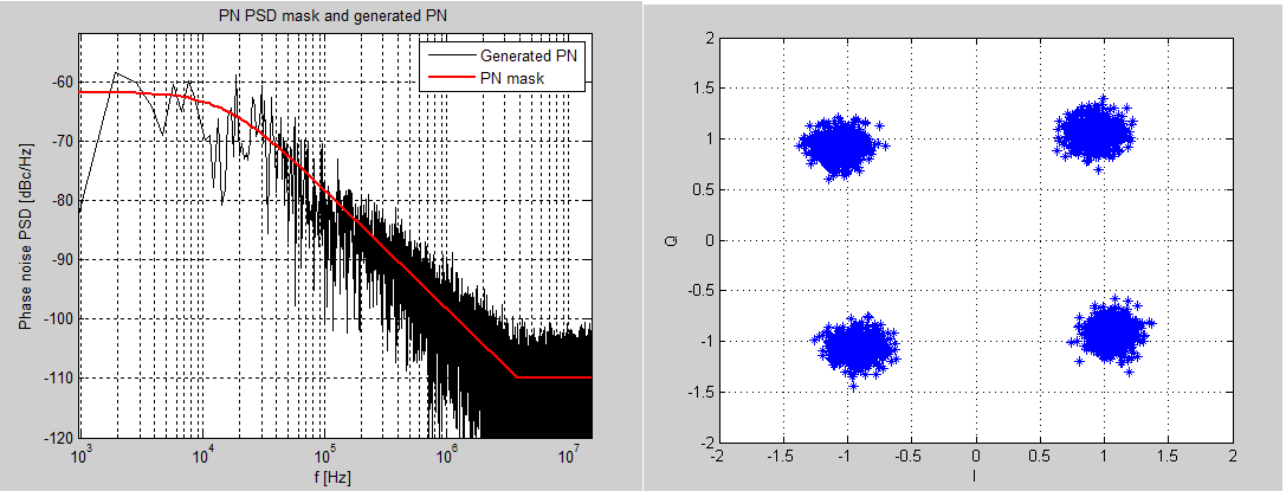

Figure 8: Phase noise spectrum (left) and a QPSK constellation diagram (right): PN 3 dB bandwidth = 15 kHz

The presented conclusions are illustrated in the Figures 7 and 8. The simulation of the phase noise effect in multicarrier system was done in MATLAB, using the code provided in [2]. The number of subcarriers was $N = 2048$ and the sampling frequency $F_s = 30.72\ MHz$, corresponding to the highest channel bandwidth of LTE. The total integrated phase noise is the same for both scenarios, equal to -15 dBc. The chosen spectral mask has a Lorentzian shape for low and medium frequencies and a noise floor for higher frequencies. The 3 dB bandwidth of the PN in the first case is 150 Hz, and in the second case 15 kHz.

When a receiver has a noisy local oscilator and a strong out-of-band interferer, the oscillator mixes with the wanted signal as well as the interferer. Aside from a randomly phase modulated wanted signal, this also results in spreading the noisy "skirt" of the modulated interferer across the bandwidth of the wanted signal, reducing the total SNR. This phenomenon is known as *reciprocal mixing*.

2.1.8 Quantization noise and clipping

Errors due to quantization and clipping are introduced in the analog-to-digital converter (ADC), the device that serves as a bridge between analog and digital domains of the receiver. This device takes an analog signal and discretizes it both in time (by sampling at discrete time instants) and in amplitude (by mapping a continuous value of the amplitude to the nearest discrete quantization level). The number of quantization levels depends on the number of quantization bits n and is finite, implying that all signal levels outside of the range $(-A_{max}, A_{max})$ are assigned to the outermost quantization levels, introducing distortion due to the clipping of the signal. Errors due to quantization can be modeled as additive, white noise uniformly distributed over $[-q/2, q/2]$, where q is the quantization step size:

$$q = \frac{2A_{max}}{2^n - 1} \tag{2.25}$$

The mean value of quantization noise is 0, and the quantization noise variance is

$$\sigma_e^2 = \frac{q^2}{12} \quad . \tag{2.26}$$

Combining with the expression for q, we get

$$\sigma_e^2 = \frac{A_{max}^2}{3(2^n - 1)^2} \approx \frac{A_{max}^2}{3 \cdot 2^{2n}} \quad , \tag{2.27}$$

with the approximation being valid for $n > 3$.

An important performance metric of ADCs is the *dynamic range* DR, measured with a sinusoidal input signal and defined as

$$DR = \frac{A_{max}^2}{2P_N} \quad , \tag{2.28}$$

where P_N is the general quantization noise power (can be different from the pure quantization noise variance because quantization noise can be shaped and filtered). DR for an ideal Nyquist - rate ADC is given as [44]

$$DR \approx 6.02n + 1.76 [dB] \tag{2.29}$$

We can now define another ADC performance metric, namely the *ideal effective number of bits* (ENOB) as the bit precision of an ideal Nyquist-rate ADC having the dynamic range DR:

$$ENOB_{id} = \frac{DR(dB) - 1.76}{6.02} \tag{2.30}$$

In a real-world ADC, thermal noise and distortion will also affect the performance and have to be taken into account. The ENOB for a real-world ADC is therefore defined by taking the SNDR (signal-to-noise-and-distortion ratio) into account:

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02} \tag{2.31}$$

and this definition of ENOB is the one most commonly used in characterizing ADCs.

Quantization and clipping in OFDM systems can be assumed to have the effect of additive noises with non-Gaussian distributions. The received OFDM symbol is therefore

$$Y_k = X_k + N_k^q + N_k^c \tag{2.32}$$

where N_k^q and N_k^c are quantization and clipping noise terms with variances σ_q^2 and σ_c^2 .

2.2 Error vector magnitude

Error vector magnitude (EVM) emerged as a standard performance measure in the analysis and synthesis of RF receiver systems. Using EVM, it is possible to quantify the level of degradation that a certain RF impairment introduces in the signal, to compare these levels of degradation and, using certain assumptions, to combine them in a "degradation budget" calculation for the whole receiver chain - properties not readily obtainable from using BER simulation curves. Although the EVM was traditionally used as a performance measure for the transmitted signals, its attractive properties (and especially the one offering the possibility of creating an EVM budget) point out to EVM as a performance indicator of choice used in the power-optimized RF receiver design.

For a set of N measured symbols with a single modulation scheme being used during the measurement period, the EVM is defined as [11]

$$EVM = \sqrt{\frac{\frac{1}{N}\sum_{k=1}^{N}|Y_k - X_k|^2}{\frac{1}{N}\sum_{k=1}^{N}|X_k|^2}} \tag{2.33}$$

where Y_k are the received symbols (constellation points) and X_k are the ideal received symbols (without the influence of signal degradation or noise). The quantity $1/N\sum_{k=1}^{N}|Y_k - X_k|^2$ can be recognized as the mean error vector power ($|Y_k - X_k|$ is the distance between the distorted and ideal constellation points, or an error vector) and the quantity $1/N\sum_{k=1}^{N}|X_k|^2$ is the mean reference signal power P_S .

If the distortion can be modeled as an uncorrelated additive noise term D_k with variance σ_{dist}^2

$$Y_k = X_k + D_k \tag{2.34}$$

the EVM can be simply expressed as [12]

$$EVM \approx \sqrt{\frac{\sigma_{dist}^2}{Ps}} = \frac{1}{\sqrt{SNR}} \tag{2.35}$$

The uncorrelated additive noise model of the distortion allows for a very simple and elegant way of combining the EVMs related to different distortion sources into a total EVM. If we assume that there are K distortion sources in the receiver chain, that the distortions can be modeled as AWGN and that there is no correlation between individual distortion sources, we have [13]:

$$EVM_{total}^2 = \frac{\sigma_{dist,total}^2}{P_S} = \frac{\sum_{k=1}^{K} \sigma_{dist,k}^2}{P_S} = \sum_{k=1}^{K} EVM_k^2 \quad , \tag{2.36}$$

or simply

$$EVM_{total} = \sqrt{\sum_{k=1}^{K} EVM_k^2} = \sqrt{\sum_{k=1}^{K} \frac{1}{SNR_k}} \quad . \tag{2.37}$$

The effects of a large number of RF impairments can be cancelled or compensated in the receiver. This is achieved by using two possible approaches:

- Using DSP algorithms for estimation and correction of the errors induced in the RF. The processing takes place in digital baseband, right before the baseband MIMO-OFDM detection block. This approach is referred to as "dirty RF" (the analog signal is left "dirty" and "cleaned" only in the digital baseband)
- Using DSP algorithms and digital tuning of the parameters of analog blocks to correct/cancel/reduce the RF impairment effects *at the spot*, in the very analog block where they are generated. This is the so-called "clean RF" approach (the RF signal is "cleaned" already in the analog domain and arrives "clean" to the digital baseband).

A number of "dirty RF" algorithms have been developed for use in OFDM systems. They mostly target the deterministic or time-invariant RF impairments (carrier frequency offset, DC offset, I/Q imbalance and sampling clock offset). Some of these algorithms are presented in [14], [15], [16] to list only a few. Some "dirty RF" algorithms are also described in [2].

With the final goal of reducing the complex and intricate set of RF impairment effects in the receiver to a tractable one that can be used in a simple power-performance tradeoff analysis, we introduce a series of assumptions. These assumptions will be used later in the derivation of the EVM for the entire receiver chain.

- It is assumed that the effects of the four deterministic RF impairments are corrected by "dirty RF"; thus, the remaining distortion comes from phase noise, nonlinearities and quantization/clipping.
- In OFDM systems using pilot symbols for channel estimation and synchronization (LTE being one of these systems), the compensation of the common phase rotation and/or attenuation due to PN and nonlinear compression comes as a by-product of frequency-domain channel estimation and equalization (baseband channel estimator sees and corrects the overall constellation rotation and attenuation due to the transmission channel, PN and compression). Additional compensation of the attenuation caused by nonlinearities can be performed by the automatic gain control (AGC) in the analog RF part of the receiver. The AGC senses the instantaneous power level and acts on it with a final goal of delivering a constant power level at the input of the ADC. This way the power variations due to compression get compensated together with other channel power variations.

This then leaves us just with the additive noise due to PN, quantization/clipping and compression. (We can additionally assume for now that out-of-band blockers are not present; this leaves the connected effects, like desensitization, reciprocal mixing and noise folding in the ADC out of the analysis. However, a more thorough analysis will have to deal with blocker-induced effects because blockers are an omni-present and serious problem). The overall RF impairment influence of the performance can then be simply calculated using (2.37).

We now turn to analyzing the EVMs for the most critical RF impairments.

2.2.1 EVM of phase noise

For the derivation of EVM for the phase noise, we first assume perfect channel estimation and ZF equalization in the receiver; this will perfectly derotate the signal constellation, rendering CPE = 0. Using (2.21), (2.22) and (2.24), the received symbol Y_k can be written as

$$Y_k \approx X_k e^{j\Phi} + ICI_k \tag{2.38}$$

and the equalized received symbol is then

$$Y_k^{(e)} \approx X_k + ICI_k e^{-j\Phi} \quad . \tag{2.39}$$

This leaves us just with ICI, which can be modeled as complex, circularly symmetric Gaussian noise (if the number of subcarriers N is large enough). Following the derivation in [17], the power of the "ICI noise" is

$$P_{ICI} = var\left\{ e^{-j\Phi} e^{j\pi/2} \frac{1}{N} \sum_{\substack{r=0,\\ r\neq k}}^{N-1} X_r \sum_{n=0}^{N-1} \phi(n) e^{j2\pi \frac{(r-k)}{N} n} \right\} = var\left\{ \sum_{\substack{r=0,\\ r\neq k}}^{N-1} X_r \sum_{n=0}^{N-1} \phi(n) e^{j2\pi \frac{(r-k)}{N} n} \right\} \tag{2.40}$$

because $var(cX) = |c|^2 var(X)$. P_{ICI} is then found to be

$$P_{ICI} = P_S \frac{N-1}{N} \sigma_\phi^2 \tag{2.41}$$

where P_S is the OFDM signal power.

Although papers [9], [10] and [17] do not derive the EVM of the phase noise explicitly, it can be derived easily. By assuming a large number of subcarriers and combining (2.16), (2.35) and (2.41) we get an approximate expression for the EVM of phase noise as

$$EVM_{PN} \approx \sqrt{\sigma_\phi^2} = \sqrt{2 \int_0^{f_B} L_\phi(f)\, df} \tag{2.42}$$

The influence of phase noise was simulated with the phase noise model provided in [2], for a 100 kHz PLL loop bandwidth and a system bandwidth of 3.84 MHz. The results are given in Figure 9.

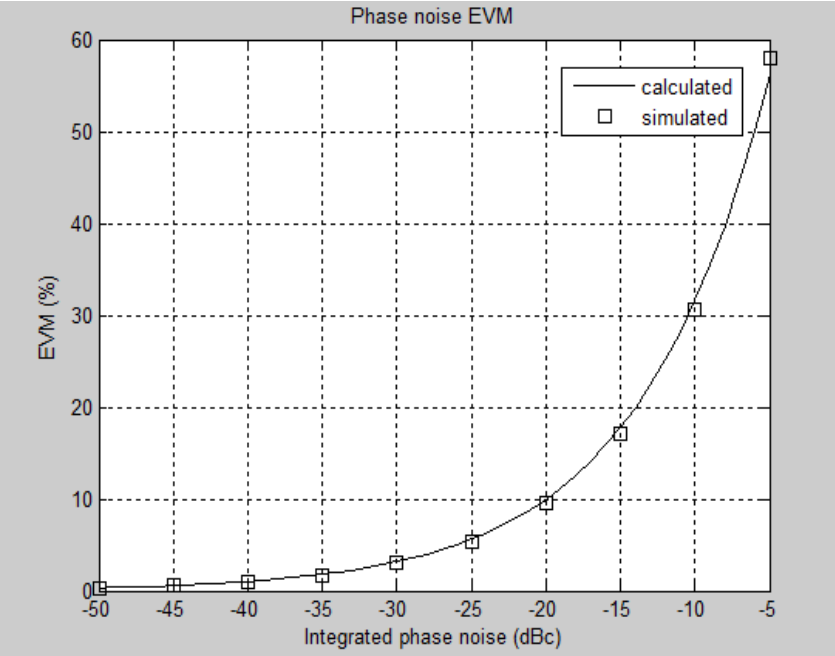

Figure 9: EVM of phase noise, calculated and simulated

2.2.2 EVM of nonlinearities

The derivation of the EVM due to nonlinearity given here is the original contribution of this thesis work, based on the results derived in [18].

In the analysis of the EVM in nonlinear systems, we focus on the polynomial baseband model of nonlinearities, given in discrete time. The input-output K-order characteristic of such a system is [18], [19]

$$y_n = \sum_{k=1}^{K} \alpha_k x_n |x_n|^{k-1} \tag{2.43}$$

As it was pointed out before, the overall effect of nonlinearities on an OFDM signal can be described by joint compression of the signal constellation and addition of (approximately Gaussian) noise, the latter coming from subcarrier ICI. The signal at the FFT output can then be modeled by (2.38).

In order to determine the overall influence of nonlinearity in a real-life system, we must recall that in real-life systems there is an AGC device (usually sitting at the end of the analog part of the chain) that ideally delivers a constant power level to the ADC; if it senses any perturbation of the signal power, it fights to cancel it. If any power loss is left uncompensated, it will be compensated in the digital domain by channel equalization (we can think of the AGC as an analog-domain equalization, if we consider a flat fading channel). In this respect, the compensation of the compression has to be regarded as a phenomenon that is inherent to the nonlinearity and needs to be taken into concern when analyzing the effects of nonlinearity.

The nonlinearity model can be rewritten as

$$Y_k = \mu_{NL} X_k + D_{k,NL} = \alpha_1 \cdot \gamma X_k + D_{k,NL} \quad , \tag{2.44}$$

where α_1 is the small-signal gain (uncompressed) and γ models the compression

effect.

The block diagram of the system with compression compensation is given in Figure 10.

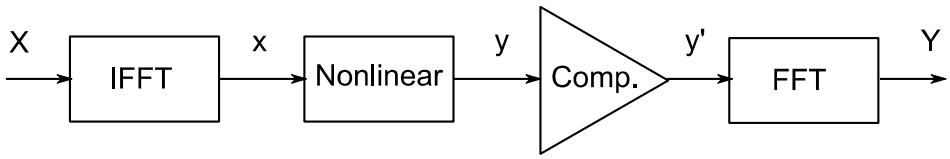

Figure 10: Nonlinearity with compensation

The mathematical model of the system is (only taking into account only the third order nonlinearity):

$$x = IFFT(X)$$
$$y = \alpha_1 x + \alpha_3 x|x|^2$$
$$y' = G \cdot y$$
$$Y = FFT(y') = G \cdot IFFT(y) = G \cdot \mu \cdot X + G \cdot D_{NL} \tag{2.45}$$

Since $G = 1/\gamma$, finally we have

$$Y = \alpha_1 \cdot X + G \cdot D_{NL} \quad . \tag{2.46}$$

In [18], it was found that

$$\gamma = 1 + \frac{\alpha_3}{\alpha_1} \frac{P}{N} \quad , \tag{2.47}$$

$$\sigma_{NL}^2 = 3|\alpha_3|^2 \frac{P^3}{N^2} \quad , \tag{2.48}$$

where P is the power of the pre-IFFT signal X and $P_{\text{in}} = P/N$ is the power of the signal *x,* coming after IFFT. For determining the EVM, we must determine the power of the distortion P_{dist} and the reference power P

$$P_{dist} = G^2 \cdot \sigma_{NL}^2 = \frac{1}{\gamma^2} 3|\alpha_3|^2 \frac{P^3}{N^2} \tag{2.49}$$

and since we are expecting the signal X with small-signal amplification, the reference output constellation should have the power

$$P_{ref} = \alpha_1^2 \cdot P \tag{2.50}$$

It should be observed that the compensation is not taken into concern when calculating P_{ref} since it is inherent to the nonlinearity, as explained before. The EVM is now found to be

$$EVM = \sqrt{\frac{P_{dist}}{P_{ref}}} = \sqrt{3\left(\frac{\alpha_3}{\alpha_1}\right)^2 \frac{P_{\text{in}}^2}{\gamma^2}} \tag{2.51}$$

which after little manipulation becomes

$$EVM = \frac{4 \cdot P_{\text{in}}}{\sqrt{3}\, A_{IIP3}^2 - \frac{4\sqrt{3}}{3} P_{\text{in}}} \quad . \tag{2.52}$$

This model was put to the test in MATLAB, where a nonlinear device with IIP3 = 10 dBm

was simulated with an input OFDM signal of varying power. The results are given in Figure 11.

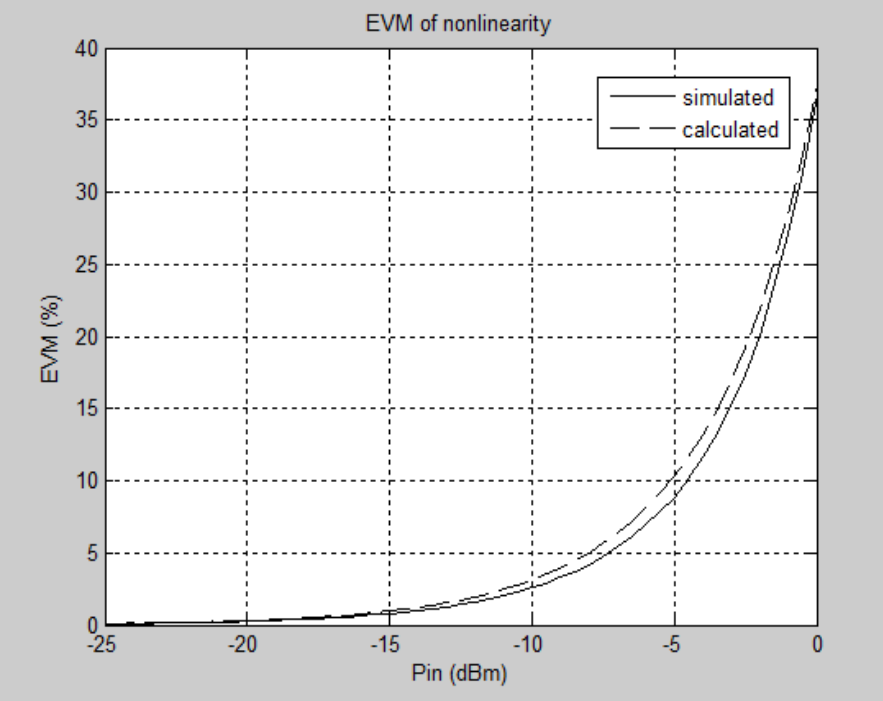

Figure 11: Nonlinearity EVM, simulated and calculated

2.2.3 EVM of quantization and clipping

The joint EVM of quantization and clipping is derived based on the expressions for the power of quantization and clipping distortions that are well-known in literature (for the purposes of this derivation, the expression for the power of clipping distortion is found in [20]).

The effects of quantization and clipping in OFDM systems are defined in terms of the *input backoff* (IBO), defined as

$$\rho_{ADC} = \frac{A_{max}^2}{P_{\text{in}}} \tag{2.53}$$

where P_{in} is the power of the post-IFFT (time-domain) OFDM signal. The power of the clipping distortion is shown to be [20]

$$\sigma_c^2 = 2\left(P_{\text{in}} + A_{max}^2\right) Q\left(\frac{A_{max}}{\sqrt{P_{\text{in}}}}\right) - 2\,A_{max}\sqrt{\frac{P_{\text{in}}}{2\pi}}\,e^{-\frac{A_{max}^2}{2P_{\text{in}}}} \quad . \tag{2.54}$$

If the quantization noise power $\sigma_q^2 = \sigma_e^2$ is found from (2.27), the total EVM is

$$EVM_{c,q} = \sqrt{\frac{\sigma_c^2 + \sigma_q^2}{P_{\text{in}}}} = \sqrt{2\left(1+\rho_{ADC}\right)Q\left(\sqrt{\rho_{ADC}}\right) - \sqrt{\frac{2\rho_{ADC}}{\pi}}\,e^{-\frac{\rho_{ADC}}{2}} + \frac{\rho_{ADC}}{3\cdot\left(2^n-1\right)^2}} \tag{2.55}$$

where *Q(x)* is the Q-function.

The EVM of a regular Nyquist ADC with bit resolutions 6, 8, 10, 12 and 14 and as a function of input backoff is plotted in Figure 12.

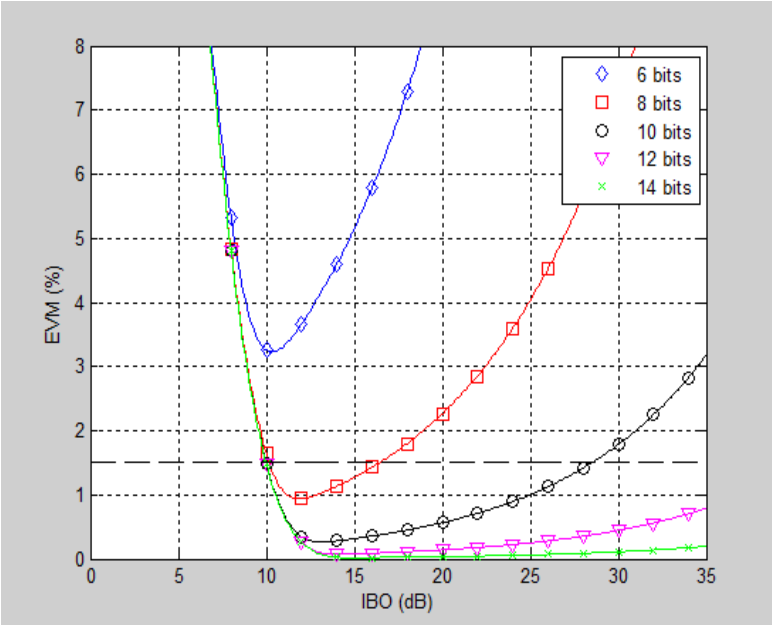

Figure 12: EVM as a function of input backoff (IBO) for ADCs with different bit resolutions

As it can be seen from Figure 12, for a very large input signal power P_S (small IBO) the clipping is very intense and EVM is large. As P_S decreases, the EVM reaches its minimum. For a very small P_S, the effective number of bits used in the quantization of the signal is small and so EVM increases again. Thus, the errors due to clipping dominate the area left of the minimum, and quantization noise dominates to the right of the minimum.

If we assume that an ideal AGC precedes the ADC, then the working point of the AGC is always at the minimum value of the EVM curve for a particular bit resolution. In ADC design, for a given EVM specification (like EVM = 1.5%, given as a dashed black line in Figure 12), we then choose the bit resolution that has its minimum below the target EVM. As it can be seen from the plot, we are usually allowed to have a *range* of IBO values, allowing for a non-ideal (simpler) AGC.

2.2.4 Calculation of EVM for a cascade of impairments

As another original contribution of this thesis, the expressions relating to the power of phase noise, nonlinearity and quantization/clipping distortions, found in [17], [18] and [20], are going to be applied on a specific receiver topology, resulting in the overall RF impairment EVM for that topology. The theory is compared with simulation results.

So far, we have analyzed the influence individual RF impairments have on the OFDM signal. In the analysis and design of real systems, however, there is a need to determine the total EVM for a cascade of blocks, where each block contains one or more sources of RF signal distortion coming from impairments. Due to the interaction between different impairment effects in the cascade, the complexity of an accurate theoretical expression for the EVM blows up with the number of blocks taken into account. This work, on the other hand, aims at finding useful system performance models that will give reasonable precision with reduced description complexity.

In order for the analysis to yield usable theoretical description, two important assumptions need to be made:

1. The phase rotation of the constellation due to CPE and the compression of the constellation due to nonlinearities are compensated with AGC, with equalization or jointly by both. Therefore, the final joint effect of RF impairments is a sum of noise-like components;

2. With 1. satistfied, we assume these noise-like components to be Gaussian and independent. The overall distortion power $P_{dist,total}$ is then calculated as the sum of powers of K individual distiortions:

$$P_{dist,total} = P_{dist,1} + P_{dist,2} + \ldots + P_{dist,K} \tag{2.56}$$

The validity of these assumptions is going to be put on test in a receiver chain model. The block diagram of the model is shown in Figure 13.

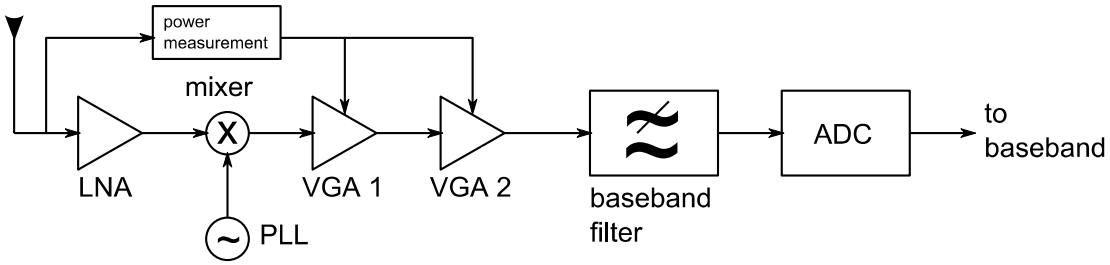

Figure 13: Block diagram of the receiver chain

LNA, VGAs, mixer and the baseband filter can quickly be recognized as sources of nonlinearity, PLL as the source of the phase noise and ADC of the quantization and clipping distortion. All of the elements also generate thermal noise; the equivalent thermal noise for the chain can be calculated using formulas (2.3) and (2.4) and then be referenced at the input of the chain, right after the antenna. This noise can also be assumed independent from other distortions. The block diagram of the RF impairment model of the chain (needed for calculating the input - output characteristic) is given in Figure 14.

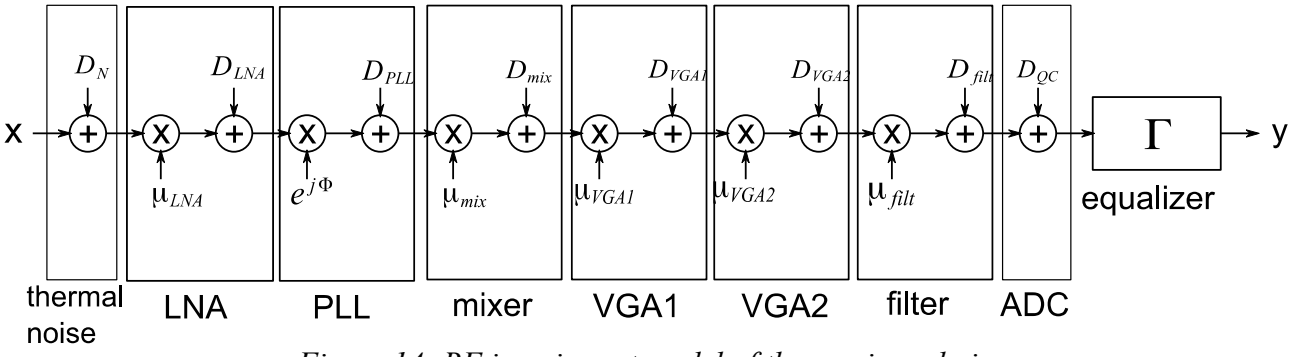

Figure 14: RF impairment model of the receiver chain

Compressed signal gains $\mu_{LNA}, \mu_{mix}, \mu_{VGA1}, \mu_{VGA2}, \mu_{filt}$ of their respective elements are given by $\alpha_1 + \alpha_3 \cdot P_{block}$, where P_{block} is the input power to the block:

$$\mu_{LNA} = \sqrt{G_{LNA}} + \alpha_{3\mathrm{LNA}} \cdot \frac{P}{N} \quad ,$$

$$\mu_{mix} = \sqrt{G_{mix}} + \alpha_{3\mathrm{mix}} \cdot \frac{\mu_{LNA}^2 P}{N} \quad ,$$

$$\mu_{VGA1} = \sqrt{G_{VGA1}} + \alpha_{3\mathrm{VGA1}} \cdot \frac{\mu_{LNA}^2 \mu_{mix}^2 P}{N} \quad ,$$

$$\mu_{VGA2} = \sqrt{G_{VGA2}} + \alpha_{3\mathrm{VGA2}} \cdot \frac{\mu_{LNA}^2 \mu_{mix}^2 \mu_{VGA1}^2 P}{N} \quad ,$$

$$\mu_{filt}=\sqrt{G_{filt}}+\alpha_{3\mathrm{filt}}\cdot\frac{\mu_{LNA}^2\mu_{mix}^2\mu_{VGA1}^2\mu_{VGA2}^2P}{N} \quad . \tag{2.57}$$

A few further observations about the model: the small - signal gains α_1 can be substituted by $\sqrt{G}$, where G is the corresponding power gain of the block. Furthermore, P models the constellation power before the IFFT and it is assumed that there is no loss in the channel, *i.e.* channel gain is 1. Any channel losses would have to be incorporated in the pre-IFFT constellation power.

The terms $D_{LNA}, D_{mix}, D_{VGA1}, D_{VGA2}, D_{filt}$ are the "noise" components of the nonlinear distortion, whose power is given by the expressions

$$\begin{aligned}
\sigma_{LNA}^2&=3|\alpha_{3\mathrm{LNA}}|^2\frac{P^3}{N^2}=3|\alpha_{3\mathrm{LNA}}|^2P_{\mathrm{in}}^3\cdot N \quad ,\\
\sigma_{mix}^2&=3|\alpha_{3\mathrm{mix}}|^2\mu_{LNA}^6P_{\mathrm{in}}^3\cdot N \quad ,\\
\sigma_{VGA1}^2&=3|\alpha_{3\mathrm{VGA1}}|^2\mu_{LNA}^6\mu_{mix}^6P_{\mathrm{in}}^3\cdot N \quad ,\\
\sigma_{VGA2}^2&=3|\alpha_{3\mathrm{VGA2}}|^2\mu_{LNA}^6\mu_{mix}^6\mu_{VGA1}^6P_{\mathrm{in}}^3\cdot N \quad ,\\
\sigma_{filt}^2&=3|\alpha_{3\mathrm{filt}}|^2\mu_{LNA}^6\mu_{mix}^6\mu_{VGA1}^6\mu_{VGA2}^6P_{\mathrm{in}}^3\cdot N \quad ,
\end{aligned} \tag{2.58}$$

where $P_{\mathrm{in}}=P/N$ is the post-IFFT power, or the power at the receiving antenna.

Additionally, $e^{j\Phi}$ is the phase rotation due to the CPE caused by phase noise.

An important note about VGAs and equalization: by examining Figure 13, it can be observed that VGA gains are adjusted using the input signal information from the input of the antenna. The analog part of the receiver in this setup is not aware of possible signal compression by nonlinear elements, and hence the compensation of compression is not done by VGAs. This compensation, together with the derotation of the constellation, is done by the equalizer. Assuming flat fading and perfect channel estimation, the voltage gain Γ of the zero forcing equalizer is

$$\Gamma=\frac{e^{-j\Phi}}{\gamma_{LNA}\gamma_{mix}\gamma_{VGA1}\gamma_{VGA2}\gamma_{filt}} \quad . \tag{2.59}$$

The input-output characteristic of the system shown in Figure 13 is then given by

$$\begin{aligned}
y=(&\mu_{LNA}e^{j\Phi}\mu_{mix}\mu_{VGA1}\mu_{VGA2}\mu_{filt}x\\
&+\mu_{LNA}e^{j\Phi}\mu_{mix}\mu_{VGA1}\mu_{VGA2}\mu_{filt}D_N\\
&+e^{j\Phi}\mu_{mix}\mu_{VGA1}\mu_{VGA2}\mu_{filt}D_{LNA}\\
&+\mu_{mix}\mu_{VGA1}\mu_{VGA2}\mu_{filt}D_{PLL}\\
&+\mu_{VGA1}\mu_{VGA2}\mu_{filt}D_{mix}\\
&+\mu_{VGA2}\mu_{filt}D_{VGA1}\\
&+\mu_{filt}D_{VGA2}+D_{filt}+D_{QC})\cdot\Gamma
\end{aligned} \tag{2.60}$$

which can then be expressed as

$$
\begin{aligned}
y = {} & \alpha_{LNA}\alpha_{mix}\alpha_{VGA1}\alpha_{VGA2}\alpha_{filt}\,x \\
& + \alpha_{LNA}\alpha_{mix}\alpha_{VGA1}\alpha_{VGA2}\alpha_{filt}\,D_N \\
& + \alpha_{mix}\alpha_{VGA1}\alpha_{VGA2}\alpha_{filt}\frac{D_{LNA}}{\gamma_{LNA}} \\
& + \alpha_{mix}\alpha_{VGA1}\alpha_{VGA2}\alpha_{filt}e^{-j\Phi}\frac{D_{PLL}}{\gamma_{LNA}} \\
& + \alpha_{VGA1}\alpha_{VGA2}\alpha_{filt}e^{-j\Phi}\frac{D_{mix}}{\gamma_{LNA}\gamma_{mix}} \\
& + \alpha_{VGA2}\alpha_{filt}e^{-j\Phi}\frac{D_{VGA1}}{\gamma_{LNA}\gamma_{mix}\gamma_{VGA1}} \\
& + \alpha_{filt}e^{-j\Phi}\frac{D_{VGA2}}{\gamma_{LNA}\gamma_{mix}\gamma_{VGA1}\gamma_{VGA2}} \\
& + e^{-j\Phi}\frac{D_{filt}}{\gamma_{LNA}\gamma_{mix}\gamma_{VGA1}\gamma_{VGA2}\gamma_{filt}} \\
& + e^{-j\Phi}\frac{D_{QC}}{\gamma_{LNA}\gamma_{mix}\gamma_{VGA1}\gamma_{VGA2}\gamma_{filt}}
\end{aligned}
\tag{2.61}
$$

The distortion power for the nonlinearities is given by:

$$
\begin{aligned}
P_{dist,LNA} &= \frac{\alpha_{mix}^2\alpha_{VGA1}^2\alpha_{VGA2}^2\alpha_{filt}^2\sigma_{LNA}^2}{\gamma_{LNA}^2} = \frac{\alpha_{mix}^2\alpha_{VGA1}^2\alpha_{VGA2}^2\alpha_{filt}^2 3\left|\alpha_{3\mathrm{LNA}}\right|^2 P_{\mathrm{in}}^3\cdot N}{\gamma_{LNA}^2}\,, \\
P_{dist,mix} &= \frac{\alpha_{VGA1}^2\alpha_{VGA2}^2\alpha_{filt}^2\sigma_{mix}^2}{\gamma_{LNA}^2\gamma_{mix}^2} = \frac{\alpha_{VGA1}^2\alpha_{VGA2}^2\alpha_{filt}^2 3\left|\alpha_{3\mathrm{mix}}\right|^2\mu_{LNA}^6 P_{\mathrm{in}}^3\cdot N}{\gamma_{LNA}^2\gamma_{mix}^2}\,, \\
P_{dist,VGA1} &= \frac{\alpha_{VGA2}^2\alpha_{filt}^2\sigma_{VGA1}^2}{\gamma_{LNA}^2\gamma_{mix}^2\gamma_{VGA1}^2} = \frac{\alpha_{VGA2}^2\alpha_{filt}^2 3\left|\alpha_{3\mathrm{VGA1}}\right|^2\mu_{LNA}^6\mu_{mix}^6 P_{\mathrm{in}}^3\cdot N}{\gamma_{LNA}^2\gamma_{mix}^2\gamma_{VGA1}^2}\,, \\
P_{dist,VGA2} &= \frac{\alpha_{filt}^2\sigma_{VGA2}^2}{\gamma_{LNA}^2\gamma_{mix}^2\gamma_{VGA1}^2\gamma_{VGA2}^2} = \frac{\alpha_{filt}^2 3\left|\alpha_{3\mathrm{VGA2}}\right|^2\mu_{LNA}^6\mu_{mix}^6\mu_{VGA1}^6 P_{\mathrm{in}}^3\cdot N}{\gamma_{LNA}^2\gamma_{mix}^2\gamma_{VGA1}^2\gamma_{VGA2}^2}\,, \\
P_{dist,filt} &= \frac{\sigma_{filt}^2}{\gamma_{LNA}^2\gamma_{mix}^2\gamma_{VGA1}^2\gamma_{VGA2}^2\gamma_{filt}^2} = \frac{\alpha_{filt}^2 3\left|\alpha_{3\mathrm{filt}}\right|^2\mu_{LNA}^6\mu_{mix}^6\mu_{VGA1}^6\mu_{VGA2}^6 P_{\mathrm{in}}^3\cdot N}{\gamma_{LNA}^2\gamma_{mix}^2\gamma_{VGA1}^2\gamma_{VGA2}^2\gamma_{filt}^2}\,.
\end{aligned}
\tag{2.62}
$$

The analysis of distortion power for the PLL and for ADC needs to be undertaken carefully.

Following the analysis in [17] and according to (2.41), the power of the ICI distortion due to phase noise is

$$
P_{ICI,single} = P_S\sigma_\phi^2\,, \tag{2.63}
$$

where P_S is the power of the pre-IFFT (frequency-domain) OFDM signal. If a certain (compressed) gain μ_{LNA} precedes the entry point of the PLL signal in the chain, this needs to be incorporated in P_S. Therefore, ICI distortion power in the chain is equal to

$$
P_{dist,PLL} = P_{ICI,chain} = \mu_{LNA}^2 P_S\sigma_\phi^2\,. \tag{2.64}
$$

Clipping noise power is expressed in terms of an input backoff (IBO) denoted by ρ. In an ideal receiver chain, without compression and with ideal AGC settings, this IBO is set to the optimum value for the particular bit resolution (corresponding to bottom points of the curves in Figure 12). It we are to track the joint effect of quantization, clipping and nonlinearities, it is then convenient to define an optimum clipping noise for the optimal backoff:

$$\sigma_{c,opt}^2 = 2\left(P_{opt} + A_{max}^2\right) Q\left(\frac{A_{max}}{\sqrt{P_{opt}}}\right) - 2\,A_{max}\sqrt{\frac{P_{opt}}{2\pi}}\,e^{-\frac{A_{max}^2}{2P_{opt}}} \quad , \qquad (2.65)$$

with $P_{opt} = \alpha_{LNA}^2 \alpha_{mix}^2 \alpha_{VGA1}^2 \alpha_{VGA2}^2 \alpha_{filt}^2 P_{\text{in}}$. If we now consider the effects of compression, it is obvious that the power of the signal at ADC input is not longer going to give the optimal backoff: it is reduced so the backoff is increased.

Let's define, for convenience, a power compression coefficient *K:*

$$K = \gamma_{LNA}^2 \gamma_{mix}^2 \gamma_{VGA1}^2 \gamma_{VGA2}^2 \gamma_{filt}^2 \quad . \qquad (2.66)$$

Then the input power to the ADC is equal to $K \cdot P_{opt}$ and the clipping noise power for this case is calculated as

$$\sigma_{c,comp}^2 = 2\left(K \cdot P_{opt} + A_{max}^2\right) Q\left(\frac{A_{max}}{\sqrt{K \cdot P_{opt}}}\right) - 2\,A_{max}\sqrt{\frac{K \cdot P_{opt}}{2\pi}}\,e^{-\frac{A_{max}^2}{2K \cdot P_{opt}}} \quad . \qquad (2.67)$$

The expressions for the nonlinearity and PLL distortions have been derived for the entire OFDM system, *i.e.* they consider that the power of the signal is increased *N* times in the FFT block. Quantization and clipping noise expressions, however, do not consider this, and as a result, the proper expression for the power of the joint quantization and clipping noise would be

$$\sigma_{QC}^2 = N\left(\sigma_{c,comp}^2 + \sigma_q^2\right) \qquad (2.68)$$

and the power of the distortion

$$P_{dist,QC} = \frac{\sigma_{QC}^2}{K} = \frac{1}{K} N\left(\sigma_{c,comp}^2 + \sigma_q^2\right) \quad . \qquad (2.69)$$

A proper definition of the reference power is essential for finding the correct EVM. The reference power for the chain is defined as the signal power that is expected at the FFT output when there are no RF impairments present, *i.e.* with just the small-signal gains. This power is equal to

$$P_{ref} = \alpha_{LNA}^2 \alpha_{mix}^2 \alpha_{VGA1}^2 \alpha_{VGA2}^2 \alpha_{filt}^2 P = \alpha_{LNA}^2 \alpha_{mix}^2 \alpha_{VGA1}^2 \alpha_{VGA2}^2 \alpha_{filt}^2 P_{\text{in}} \cdot N \quad . \qquad (2.70)$$

Individual EVMs for different impairment sources are then calculated as follows:

$$EVM_{LNA} = \sqrt{\frac{P_{dist,LNA}}{P_{ref}}} = \sqrt{3\left(\frac{\alpha_{3\text{LNA}}}{\alpha_{LNA}}\right)^2 \frac{P_{\text{in}}^2}{\gamma_{LNA}^2}} \quad ,$$

$$EVM_{PLL} = \sqrt{\frac{P_{dist,PLL}}{P_{ref}}} = \sqrt{\sigma_\phi^2} \quad ,$$

$$EVM_{mix} = \sqrt{\frac{P_{dist,mix}}{P_{ref}}} = \sqrt{3\left(\frac{\alpha_{3\text{mix}}}{\alpha_{mix}}\right)^2 \frac{\left(\mu_{LNA}^2 P_{\text{in}}\right)^2}{\gamma_{mix}^2}} \quad ,$$

$$EVM_{VGA1} = \sqrt{\frac{P_{dist,VGA1}}{P_{ref}}} = \sqrt{3\left(\frac{\alpha_{3\text{VGA1}}}{\alpha_{VGA1}}\right)^2 \frac{\left(\mu_{LNA}^2 \mu_{mix}^2 P_{\text{in}}\right)^2}{\gamma_{VGA1}^2}} \quad ,$$

$$EVM_{VGA2} = \sqrt{\frac{P_{dist,VGA2}}{P_{ref}}} = \sqrt{3\left(\frac{\alpha_{3\text{VGA2}}}{\alpha_{VGA2}}\right)^2 \frac{\left(\mu_{LNA}^2 \mu_{mix}^2 \mu_{VGA1}^2 P_{\text{in}}\right)^2}{\gamma_{VGA2}^2}} \quad ,$$

$$EVM_{filt}=\sqrt{\frac{P_{dist,filt}}{P_{ref}}}=\sqrt{3\left(\frac{\alpha_{3filt}}{\alpha_{filt}}\right)^2\frac{\left(\mu_{LNA}^2\mu_{mix}^2\mu_{VGA1}^2\mu_{VGA1}^2P_{in}\right)^2}{\gamma_{filt}^2}}\quad,\qquad(2.72)$$

For the ADC, the P_{ref} is more conveniently expressed as

$$P_{ref}=K\cdot P_{opt}\cdot N\cdot\frac{1}{K}=N\cdot P_{opt}\quad.\qquad(2.73)$$

The EVM for the ADC is then

$$EVM_{ADC}=\sqrt{\frac{P_{dist,QC}}{P_{ref}}}=\sqrt{\frac{\frac{1}{K}N\left(\sigma_{c,comp}^2+\sigma_q^2\right)}{N\cdot P_{opt}}}$$
$$EVM_{ADC}=\sqrt{2\left(1+\frac{\rho_{opt}}{K}\right)Q\left(\sqrt{\frac{\rho_{opt}}{K}}\right)-\sqrt{\frac{2\rho_{opt}}{K\pi}}e^{-\frac{\rho_{opt}}{2K}}+\frac{\rho_{opt}}{3K\cdot\left(2^n-1\right)^2}}\quad.\qquad(2.74)$$

Finally, the EVM of the thermal noise is calculated simply as $EVM_n=\sqrt{P_n/P_{in}}$.

The total EVM for the entire chain is then calculated as

$$EVM_{total}=\sqrt{EVM_{LNA}^2+EVM_{PLL}^2+EVM_{mix}^2+EVM_{VGA1}^2+EVM_{VGA}^2+EVM_{filt}^2+EVM_{ADC}^2+EVM_n^2}\qquad(2.75)$$

The described model has been put to test in MATLAB, with a couple of characteristic use cases:

- **Use case 1:** Parameters of the blocks (gains, linearity) are fixed and input power changes. The parameters are given in Table 1:

Block	Parameter values
LNA	G = 10 dB, IIP3 = 10 dBm
PLL	Integrated phase noise = -43.86 dBc; the rest is same as in the simulation of 2.1
Mixer	G = 5 dB, IIP3 = 5 dBm
VGA1	G = 10 dB, IIP3 = 15 dBm
VGA2	G = 15 dB, IIP3 = 20 dBm
Baseband filter	G = 5 dB, IIP3 = 20 dBm
ADC	ENOB = 6, optimal IBO = 10.5 dB
Thermal noise	P_n = -90 dBm

Table 1: Parameter values for the simulation of use case 1 of the receiver chain

The input power is swept from -60 to -30 dBm. Simulated and calculated EVM are given in Figure 15.

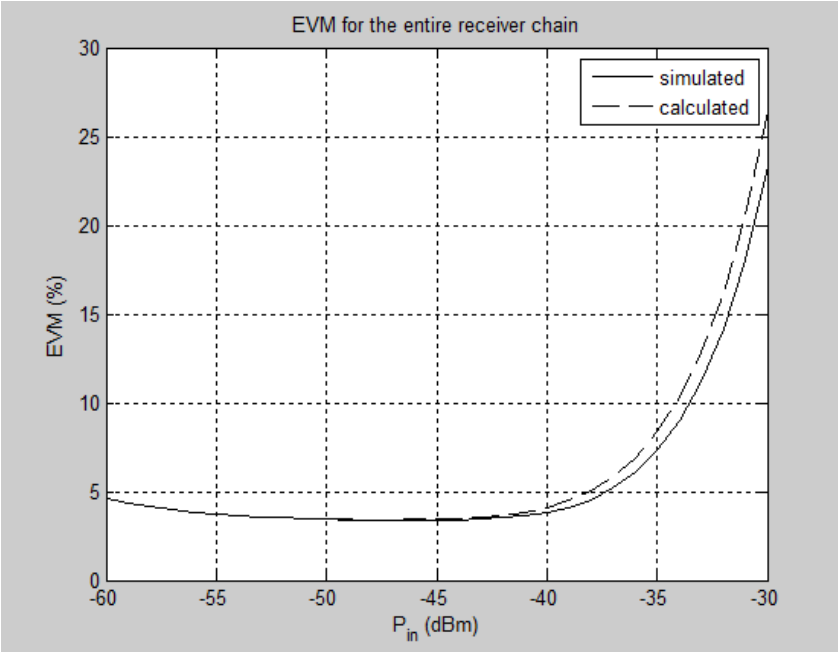

Figure 15: Simulated and calculated EVM for the entire receiver chain, use case 1

It can be observed that the theory gives an accurate estimate of the actual EVM.

- **Use case 2:** Input power is fixed at -30 dBm and filter IIP3 is swept. The remaining parameters are same as in use case 1.

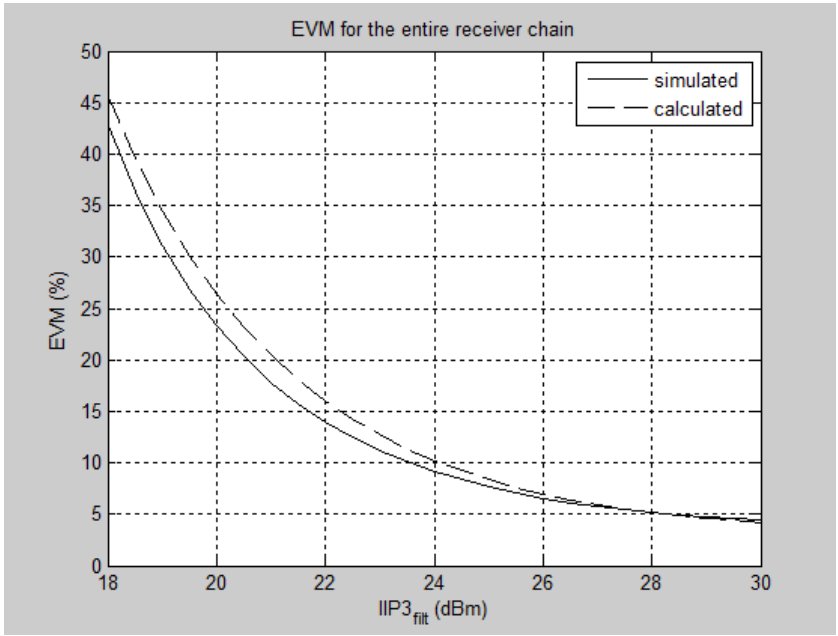

Figure 16: Simulated and calculated EVM for the entire receiver chain, use case 2

- **Use case 3:** Input power is fixed at -30 dBm and VGA2 IIP3 is swept. The remaining parameters are same as in use case 1.

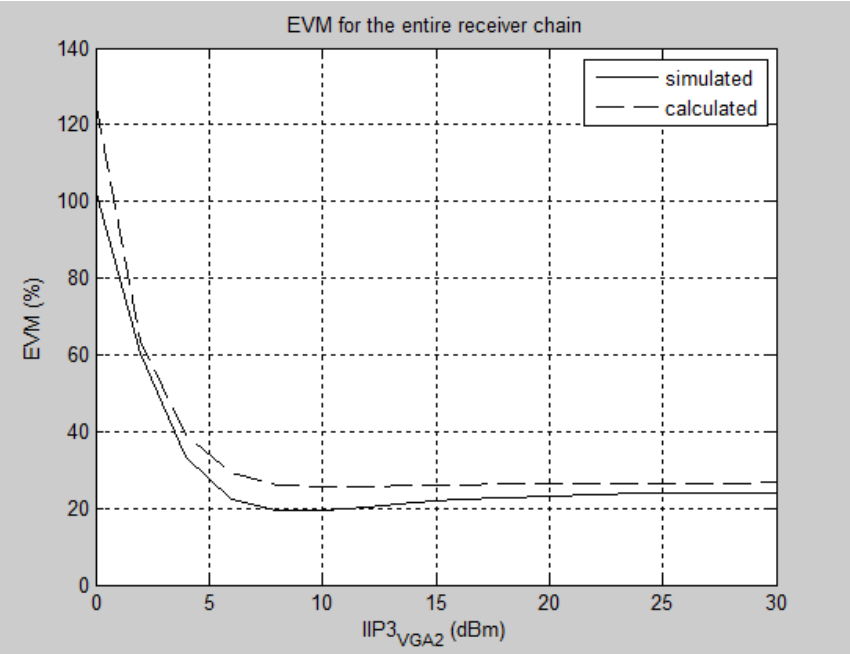

Figure 17: Simulated and calculated EVM for the entire receiver chain, use case 3

Plots for use cases 2 and 3 also confirm that the model gives a reasonably good approximation of the EVM (and it's always an overestimate).

2.2.5 EVM as means of calculating SNR degradation and signal-to-noise-and-distortion ratio (SNDR)

When analyzing the overall effects that the receiver chain has on the received signal, it is useful to separate the influence of thermal noise from the influence of other RF impairments (nonlinearity, phase noise...):

- The ratio of signal power to thermal noise power is the signal-to-noise ratio (SNR)
- The ratio of signal power to the sum of the power of thermal noise and other distortions is the signal-to-noise-and-distortion ratio (SNDR)

In the end, it's the effect of the SNDR that determines the quality of detection at the baseband and thus the overall performance of the system. Therefore, the SNDR has to be quantified. Figure 18 shows the noise and distortion budget diagram.

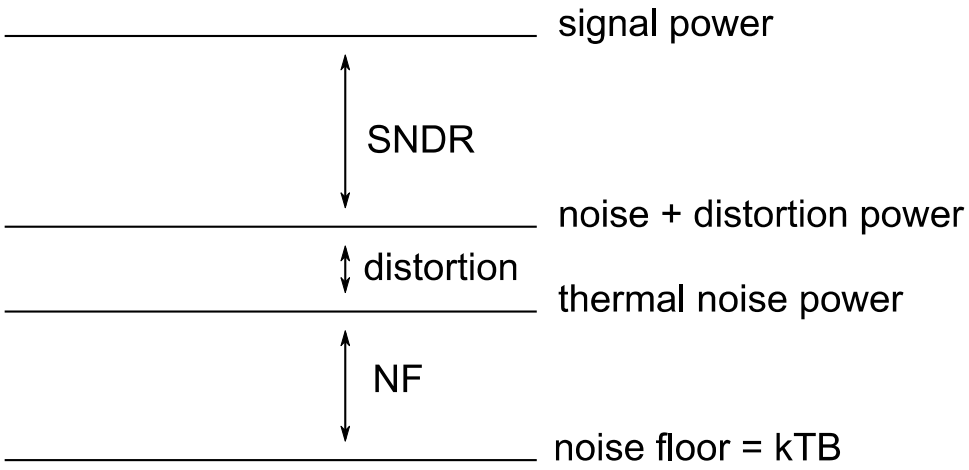

Figure 18: Noise and distortion budget diagram

One possible way of determining the SNDR is with the help of the EVM. First, it is assumed that the effect of all RF impairments can be modeled as white noise; this can hold for multicarrier systems that use equalization, as described in section 2.2.4. If we denote signal power with *S*, the total thermal noise power by *N* and total distortion power as *M*, SNDR is determined simply as

$$SNDR = \frac{S}{N+M} \tag{2.76}$$

If we recognize that $EVM_{total}^2 = M/S$ and $SNR = S/N$, then we can write

$$\frac{1}{SNDR} = \frac{1}{SNR} + EVM_{total}^2 , \tag{2.77}$$

or finally

$$SNDR = \frac{SNR}{1 + EVM_{total}^2 \cdot SNR} . \tag{2.78}$$

With an SNR determined from (2.4) and EVM_{total} defined as

$$EVM_{total} = \sqrt{EVM_{LNA}^2 + EVM_{PLL}^2 + EVM_{mix}^2 + EVM_{VGA1}^2 + EVM_{VGA}^2 + EVM_{filt}^2 + EVM_{ADC}^2} \tag{2.79}$$

(not counting the effects of thermal noise, because it is separately accounted for by SNR), it is then possible to determine the SNDR.

3 Direct Conversion Receiver - Analog Front End

3.1 Introduction

In recent years, RF receivers based on the direct-conversion principle have began to dominate in the realm of cellular chipset design. Figure 19 shows a direct conversion receiver (DCR) without the initial band-pass filter.

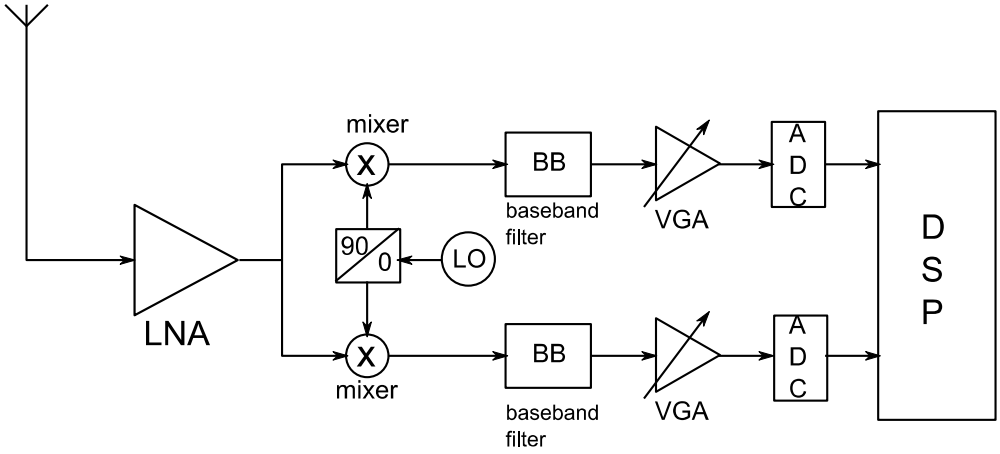

Figure 19: Direct conversion receiver (without the surface-acoustic-wave filter)

DCRs convert the signal from passband to baseband in a single step, by mixing the signal with a tone which has the frequency equal to the center frequency of the signal. Since the transmitted information is encoded in the two sidebands of the signal, these two sidebands have to be preserved and separated for successful detection; this explains the I and Q branches of the DCR.

Some benefits of DCRs are [21]:

- No need for bulky off-chip components like image-reject or IF filters;
- The entire receiver fits onto one chip;
- Only one local oscillator is needed;
- Image frequency issue, present in heterodyne receivers, is not encountered in DCRs;
- Channel-select filter is a simple baseband filter.

However, there are also some issues related specifically to DCRs:

- DC offset due to LO leakage;
- I/Q imbalance problem;
- Problems with even-order distortion;
- Pronounced flicker (low-frequency) noise.

All of the named issues that impair the performance of DCRs can be treated by clever analog designs, employing analog impairment cancellation schemes right at the point of the impairment

(the so-called "clean RF" approach). In recent years, the advances in digital design have also made possible that the listed issues be resolved in the digital domain by employing digital signal processing algorithms ("dirty-RF" approach).

This chapter deals with the analog part of the DCR. The analog-to-digital conversion (mixed-signal part) and digital baseband are overviewed in subsequent chapters.

3.2 Low noise amplifier

The LNA represents the first stage of a radio receiver, and owing to this sensitive position it exerts a significant impact on the overall system performance. Therefore, much care needs to be invested in the design of the LNA. Important parameters in the LNA design are:

- **Noise figure (NF)**. From the Friis' formula, the noise figure of the LNA directly adds to the overall noise figure of the receiver. The input stage of the LNA is the main contributor to its NF.
- **Gain.** Again from the Friis' formula, the gain of the LNA has to be sufficiently high so it supresses thermal noise coming from subsequent stages (especially the one coming from the downconversion mixer). However, if the gain is chosen too large, it raises the input signal level too high - too early in the receiver chain; this emphasizes the nonlinearity of the subsequent stages.
- **Input return loss (matching).** For maximum effectiveness, the antenna is designed for a real terminating impedance (usually 50 ohm). Therefore, the input impedance of the LNA should be equal to this impedance, otherwise, a certain amount of input power is reflected at the LNA input back to the antenna.
- **Linearity.** Except for occasional peaks, the power of the wanted signal at the input of the LNA is rather small so, with regards to just the wanted signal, LNA will rarely go into compression. The issues with the LNA linearity arise when there is a strong blocking signal at its input (typically a leaked transmit signal; for a typical Tx power level of 30 dBm and duplexer isolation of 50 dB, the blocker is at -20 dBm). This imposes an increased demand for LNA linearity, and for the linearity of subsequent stages as well.

LNA topologies can be divided into two major groups: LNAs with a common-source (CS) input stage, and LNAs with a common-gate (CG) input stage.

CG designs are shown [1] to be broadband, *i.e.* their gain and matching are relatively constant over a wider range of frequencies. Compared with CS topologies, the matching is better (input return loss is lower). CG also provide a higher NF than CS topologies, but their NF is independent of frequency.

CS designs offer a smaller gain and matching bandwidth, with the input return loss being higher compared to CG. CS, on the other hand, offer an overall smaller NF which is, however, frequency dependent.

We therefore see that the choice of the topology-CG or CS-entails a tradeoff between noise, input matching and supported bandwidth: if a higher noise floor can be allowed in the design, the CG should be used (giving a larger badwidth and better matching), but if the demand on the noise floor is strict, it's better to choose the CS (with a lower bandwidth and poorer matching).

3.2.1 Tunability and its impact on the overall system performance

LNAs in modern multistandard radio receivers have to be designed to support multiple bands (inside one standard, or for different standards), *i.e.* their central frequency of operation needs to be tunable. Also, the LNA should support some kind of power tunability that would trade performance for power. Classical radio receivers use an LNA in CS topology with inductively degenerated input. The operating frequency of this LNA design proves to be very difficult to tune (tuning it also tunes the NF), and the power tuning is difficult as well (due to interdependence between the noise, linearity and input matching of the amplifier).

Paper [22] introduces a general LNA design that is shown to support both frequency and power tunability in a very efficient way. This design is chosen for demonstration of the connections between the parameters of the LNA (listed above) and power consumption.

The said LNA design is a CG topology with general series and shunt feedbacks, represented by feedback coefficients F_1 and F_2 and shown in Figure 20.

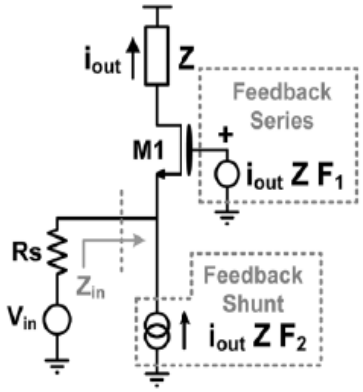

Figure 20: LNA in CG topology with generalized series and shunt feedbacks [22]

As shown later, all parameters of interest in the LNA, together with power consumption, can be tuned via feedback coefficients F_1 and F_2 .

A general reason for trading the gain, NF or linearity of the LNA with power is to adjust them to the current channel quality and performance requirements; for *e.g.* relaxed performance (throughput) requirements of the system and modest channel conditions, we can allow more signal degradation and the parameters of the LNA are tuned to support the allowed degradation, inevitably decreasing the power consumption. A more subtle description of the need for parameter tunability can be given if we consider possible combinations of signal, noise and interferer power at the input of the LNA. If the noise level is considered constant and we assume we are keeping the performance quality at a certain "modest" level constant, then we can distinguish between four cases of interest, illustrated in Figure 21 [23]:

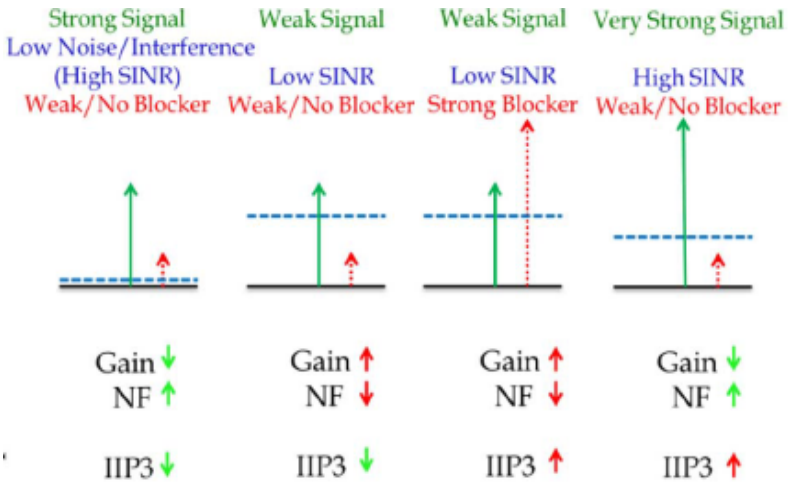

Figure 21: Four combinations of input signal power, SNR and interferer level [23]

a) A strong input signal, high SNR and a weak blocker: in this case, there is room for potential SNR reduction so the gain can be low and the noise floor high; since the linearity is not an issue, the IIP3 can also be low;

b) A weak input signal, low SNR and a weak blocker: here the SNR needs to be improved, so the gain needs to be high, NF low and IIP3 low, since there is no nonlinearity threat;

c) A weak signal, a low SNR and a strong blocker: this is the case with the worst channel conditions. In order to have a certain "modest" level performance, the SNR needs to be increased and the nonlinearities coming from the interferer reduced, so the gain needs to be high, NF low and the IIP needs to be high;

d) An extremely strong input signal, high SNR and a weak blocker; here, the linearity coming from a strong input signal is the main issue. Therefore, the IIP3 needs to be increased to reduce the distortion. Since a modest SNR is needed, gain can be low and NF high.

As it can be seen, tuning of the SNR always implies changes in gain and NF that have opposite "signs", so it is enough for them to be perfectly coupled and then we can consider just one of them (*e.g.* gain). On the other hand, the requirements for tuning the IIP3 do not always follow the tuning requirements of the gain, and for a complete control over the performance tuning the gain/NF and IIP3 controls need to be decoupled (independent).

We start our analysis of tunability of LNA parameters and its connection to the power consumption, based on results from [22], by making two assumptions. The first one is that the input impedance Z_{in} of the LNA is always matched to the antenna impedance R_S, so that power reflection at the LNA input is zero. The other assumption is that the overdrive voltage V_{OV} of the input MOS transistor M1 is held constant. Then it is shown that the tuning of the gain and IIP3 of the LNA can be decoupled; feedback coefficient F_1 tunes the IIP3 (gain is independent of F_1) and F_2 tunes the gain (IIP3 is independent of F_2).

The condition $Z_{\text{in}} = R_S$ implies that the transconducance of M1 is [22]

$$g_m = \frac{1}{R_S - (F_1 + F_2 R_S) R_P} \tag{3.1}$$

R_P is the value of the load impedance (tank circuit) Z at the resonance frequency.

Values of feedback coefficients F_1 and F_2 are constrained by two conditions: the first one is that the transconductance of M1 should be finite, and the other one is that the LNA circuit is stable. The two constraints related to these conditions are then given as [22]

$$\frac{R_P}{R_S}F_1 + R_P F_2 < 1$$
$$R_P F_2 < 1 \tag{3.2}$$

Voltage gain of the LNA is given as [22]

$$G_v = \frac{R_P}{2R_S(1 - F_2 R_P)} \tag{3.3}$$

and the power gain is then

$$G_{dB} = 20\log(G_v) \tag{3.4}$$

It can be observed that the gain depends solely on F_2; for F_2 satisfying the constraints (3.2), an increase in F_2 brings an increase in the gain.

Next, the noise figure is analyzed (assuming noiseless feedback networks and under the condition of perfect input matching). It is found that NF depends both on F_1 and F_2 [22]:

$$NF = 1 + \gamma\left(1 - \frac{R_P F_1}{R_S} - F_2 R_P\right) + \frac{R_S}{R_P}\left(2 - \frac{R_P F_1}{R_S} - F_2 R_P\right)^2 \tag{3.5}$$

where γ is a factor related to MOS transistor physical properties (typical value is 2/3).

Finally, an analysis of the influence of feedback on linearity shows that, with constant overdrive, the linearity (IIP3) is not affected by F_2. In that case, the IIP3, dependent on F_1 only, is given as [22]

$$IIP3_{F_1} = \frac{16V_{OV}^2(2 + \theta V_{OV})^2}{3R_S}\left|1 + \frac{F_1 g_m R_P}{1 + R_S g_m}\right|^3, \tag{3.6}$$

where θ is a fitting parameter.

Taking into account that the transconductance g_m is determined by feedback coefficients and that the overdrive voltage V_{OV} is constant, the drain voltage is equal to

$$I_D = \frac{g_m V_{OV}}{2}. \tag{3.7}$$

The framework given by this LNA design enables that the LNA parameters determining the performance/signal degradation, given by (3.3), (3.5) and (3.6) can be mapped to drain current via feedback coefficients F_1 and F_2 and expressions (3.1) and (3.7). The drain current can finally be mapped to the power consumed by the circuit simply as

$$P = I_D V_{DD} \tag{3.8}$$

where V_{DD} is the supply voltage.

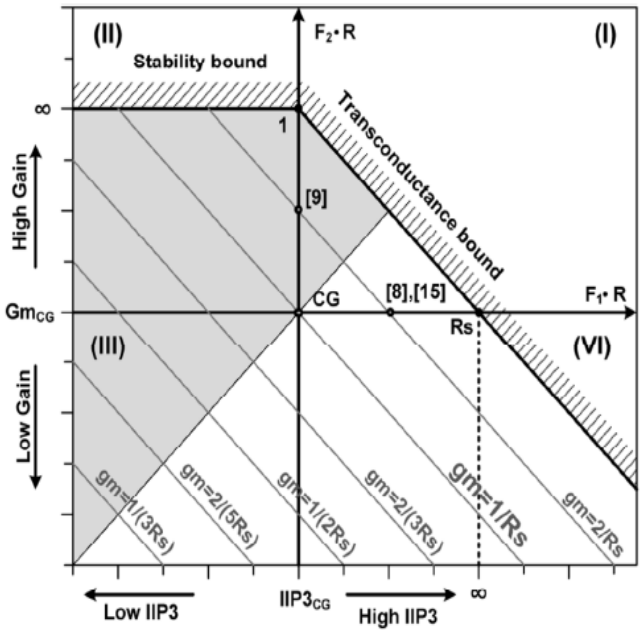

Figure 22: LNA parameters represented in the feedbacks plane [22]

A diagram of LNA parameters given in the "feedbacks plane" is taken from [22] and can serve as an illustration of the qualitative relations between LNA parameters and power consumption and give insight into power/performance tradeoffs.

Constant g_m lines can be used to represent the power consumption (the connection given by (3.7) and (3.8)). It can be seen from Figure 22 that an increase in IIP3 costs in terms of power consumption, and that a higher gain also means higher power consumption. These two can be tuned orthogonally to each other. It can also be seen that a simultaneous increase in gain and IIP3 (needed, for instance, for the case c) of channel conditions represented above) costs more in power than individual increases of gain or power. We can then assume that case a) will be the least demanding in terms of power, case c) the most demanding and that cases b) and d) are somewhere in the middle.

Let us now analyze both qualitative and quantitative relations between LNA parameters and drain current (equivalent to power consumption) by using the expressions (3.1) - (3.7). Three characteristic cases will be considered:

1. Constant gain
2. Constant IIP3
3. Constant NF

Circuit parameter values are given in Table 2. The values of θ and V_{OV} are chosen so that the IIP3 of the pure CG LNA (without any feedback applied) is 6 dBm (after a typical value presented in [22]).

Parameter	Value
R_S	50 ohm
R_P	500 ohm
γ	2/3
θ	0.9 V^{-1}
V_{OV}	93 mV

Table 2: Circuit parameter values for the quantitative representation of LNA gain, NF and IIP3

Case 1: Constant gain.

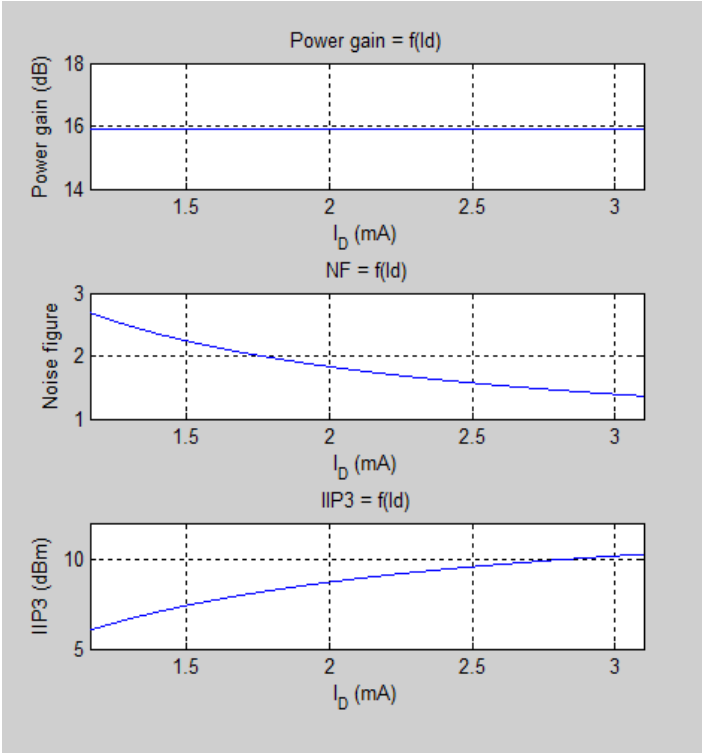

Figure 23: LNA gain, NF and IIP3 for variable F1, constant F2

As it can be seen, if the gain is kept constant, a reduction in power/current consumption implies both reduced linearity and increased noise figure.

Case 2: Constant IIP3.

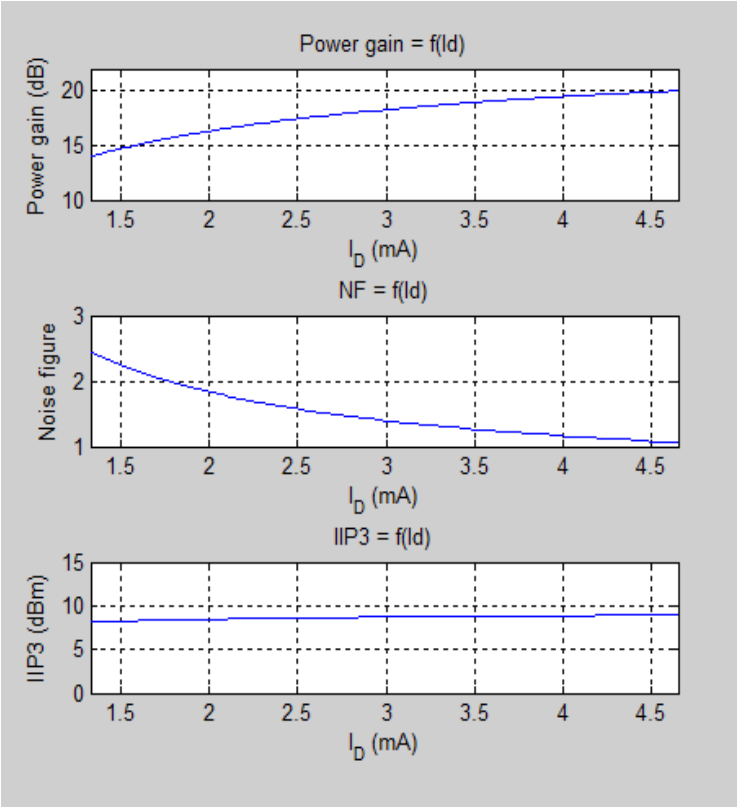

Figure 24: LNA gain, NF and IIP3 for variable F2, constant F1

(Note: the IIP3 in this amplifier model should ideally be independent from F_2 , or rather, it is constant if F_1 is constant. However, more detailed analysis shows that it is not entirely independent from F_2). It is observed that for a "constant" IIP3 and reduced power consumption, NF is increased and gain is reduced.

Case 3: Constant NF (constant power consumption)

It is possible to balance the values of F_1 and F_2 so as to keep the power consumption constant. As a consequence, the NF also remains constant, and gain and IIP3 change.

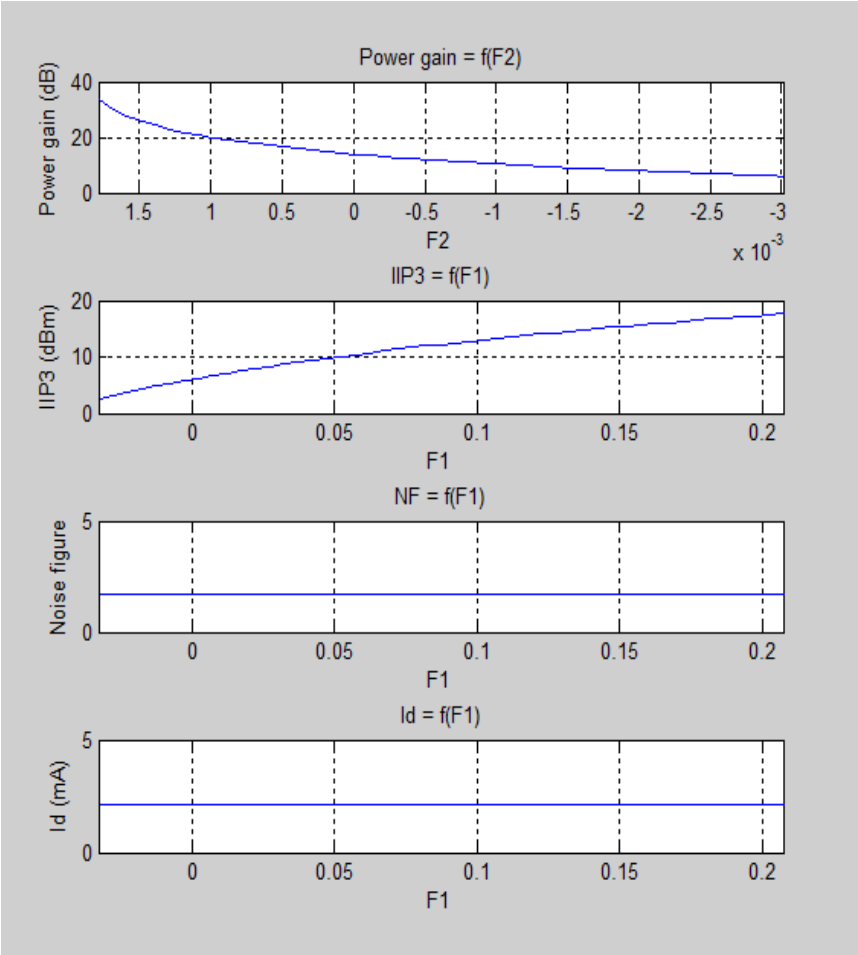

Figure 25: LNA gain, IIP3, NF and Id for an LNA design with Id = const

For a constant NF, the gain and IIP3 have opposite trends: a decrease in gain is followed by an increase in linearity.

In [22], an actual implementation of the presented general design is offered, where F_1 is a combination of feedback tunable capacitors and F_2 is a transconductance of a MOS transistor. It is reported that, due to non-idealities introduced by the active feedback F_2 and due to the effect of all noise sources and non-idealities not taken into consideration when deriving the general models, the NF is 0.5 higher than the calculated one, and IIP3 is 4 dB lower than the calculated one.

Similar quantitative relations between LNA parameters are reported in the tunable LNA design presented in [23]. The design is of a CS LNA with gain and IIP3 orthogonally tunable by two different bias currents; the design does not incroporate any input matching constraint. The measurement results show that an increase in current consumption simultaneously improves the input matching, reduces the NF and increases the gain. An increase in current consumption also leads to increased IIP3.

It can be concluded that, for LNAs with independently tunable gain and linearity, an increase in current consumption delivers a higher gain, reduced NF and increased linearity.

3.3 Frequency synthesizers

The task of the frequency synthesizer is to generate a clear carrier tone that will be mixed with the incoming signal with the goal of reconverting it to baseband. The amount of spurs, noise, etc. in the generated tone's frequency needs to be reduced to minimum; furthermore, the synthesizer must be able to generate a finite number of different carrier frequencies corresponding to different frequency bands and specific frequencies inside particular bands.

3.3.1 Voltage-controlled oscillator (VCO)

Building of a frequency synthesizer begins with a voltage-controlled oscillator (VCO). The basis of a VCO is a simple oscillator - a circuit that is built as a positive-feedback system that sustains a self-oscillating behaviour. Another view of oscillators is of a lossy LC tank in which the energy for sustaining the oscillations is injected by an active circuit [1]. It is shown that a series connection of two tuned amplifiers (alternatively given in the form of a cross-coupled structure) can provide positive feedback and thus generate oscillations at its output.

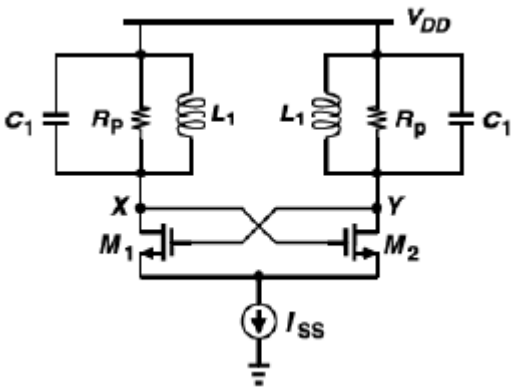

Figure 26: A cross-coupled oscillator with a tail current supply [1]

The biasing of the active elements is provided by the tail current I_{SS}. This current determines the amplitude of the output oscillations; a larger oscillation amplitude implies more abrupt switching in the mixer, which reduces noise and also increases the conversion gain of the mixer.

A VCO can be constructed by using the circuit from Figure 26 as its basis; we just add to this a pair of varactors and an external voltage control for the varactors. Thus the voltage control signal tunes the capacity of the varactors, which tunes the resonance frequency of the circuit.

Resistor R_p in the cross-coupled oscillator model generally describes the resistance of the inductors (on the order of tens of ohms). Due to the presence of R_p, dynamical tuning of the bias current (in order to control the power consumption) is not so straightforward; by tuning the tail current, the voltage drops that are generated across R_p will exert themselves over the varactors, thereby changing the output frequency and effectively frequency modulating the output, creating unwanted frequency spurs.

Phase noise in VCOs depends on the quality factor Q of the LC tank in the oscillator, the noise injected in different parts of the oscillator, time instants when the noise is injected and the

carrier power. Thermal noise sources in the VCO (transistors and the tank resistance) generate a phase noise with spectral density (at a frequency offset of $\Delta\omega$) equal to [1]

$$S(\Delta\omega)=\frac{\pi^2}{R_p}\frac{kT}{I_{SS}^2}\left(\frac{3}{8}\gamma+1\right)\frac{\omega_0^2}{4Q^2\Delta\omega^2} \qquad (3.9)$$

where Q is the quality factor of the oscillator.

It is important to note that the spectral density of this so-called "$1/f^2$" noise is inversely proportional to the square of the tail current. When the tail current has increased to a certain level, the transistors (one of them, or both) enter the triode region; this degrades (decreases) the Q. As seen from (3.9) this will cancel the effect of increasing the tail current; so we can conclude that, after a certain point, an increase in tail current yields a very modest or zero reduction of the phase noise.

In addition to thermal noise, the flicker noise of MOS transistors also generates phase noise; the spectral density of this contribution is inverse proportional to $\Delta\omega^3$ and this is the "$1/f^3$" part of the phase noise spectrum. Therefore, the PSD of VCO phase noise can roughly be divided into $1/f^3$ and $1/f^2$ parts, generated by flicker and thermal noise, respectively.

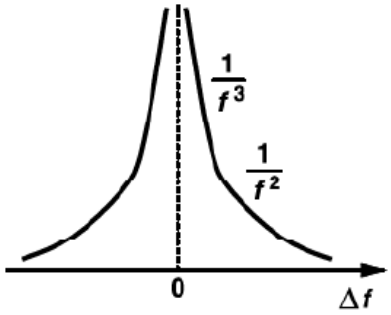

Figure 27: A general PSD of the VCO phase noise [1]

3.3.2 The phase locked loop (PLL) concept

The basic PLL consists of an ideal phase/frequency reference signal source, a phase detector (PD) that determines the difference in phases of the signals presented at its input ports, a lowpass filter and a VCO, as shown in Figure 28

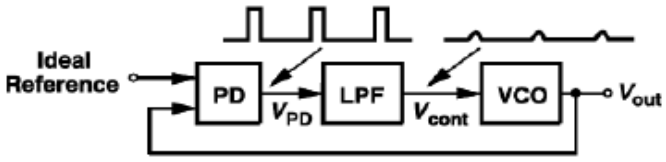

Figure 28: A basic PLL [1]

PD generates pulses with width proportional to the phase difference of the inputs; these pulses are smoothed out by a LPF. The output of the LPF is then a DC signal proportional to the phase difference. This signal is then used to tune the frequency of the VCO.

A more involved PLL design (the one that most of the PLLs implemented in practice are

based on) is a Type-II PLL (or charge-pump PLL).

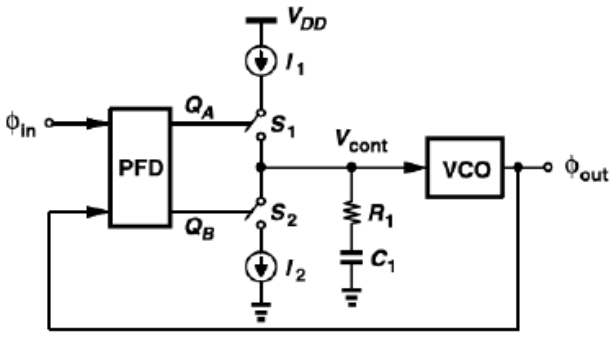

Figure 29: Charge-pump PLL [1]

A charge-pump PLL consists of:

- A phase-frequency detector (PFD) - this block detects a frequency difference between the reference signal and the VCO signal and then acts on the frequency of the VCO, pushing it towards the reference frequency; after the two frequencies are sufficiently close, the block acts like a phase detector, acting further on the VCO to lock the phases
- A charge pump - this device introduces a pole in the transfer function of the PLL and enables simultaneous frequency spur filtering (for a better phase noise performance) and control of the ripple of the locking transient process.
- A lowpass filter that enables the control of the loop bandwidth and transient process
- A VCO

A **frequency-multiplying** PLL will have a divider of M in its feedback path; this makes VCO oscillate at $f_{out} = M \cdot f_{ref}$. The PLL can thus generate a wide set of equidistant carrier frequencies equal to integer multiples of the reference frequency, which enables its use as a local oscillator for practical radio applications.

The PLL shapes the phase noises of the frequency reference and of the VCO. VCO phase noise in the PLL is shaped by a **high-pass** characteristic; the phase noise of the reference is **low-pass** filtered by the PLL transfer charactersitic. The two characteristics share the same poles. The effect of the PLL on the phase noise of the VCO is similar to the high-pass shaping of quantization noise in the sigma-delta ADC.

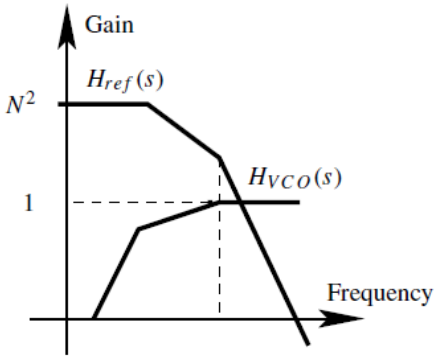

Figure 30: Transfer functions of reference and VCO phase noises in the PLL [2]

With the VCOs exhibiting a PSD which is a combination of α/f^3 and β/f^2 parts (which is then high-pass filtered by the PLL) and frequency references usually having a flat phase noise PSD (which is low-pass filtered in the PLL), the shape of the overall phase noise PSD for the entire PLL becomes dependent on the coefficients α and β, the PSD of the reference and the position of the poles of the PLL transfer function. The total reference phase noise (the integral of the PSD) increases with the loop bandwidth; in contrast, the total phase noise of the VCO reduces with the increase in loop bandwidth. Therefore, the loop bandwidth is used to trade the reference PN with VCO PN. Loop bandwidth also determines the settling time and ripple of the phase/frequency locking; to ensure successful locking, it should be chosen to be much smaller than the channel (system) bandwidth. It can be concluded that the overall phase noise PSD of the PLL is a rather involved function of phase noise PSDs of the reference and VCO and the loop transfer function.

A simplified model of the PLL phase noise PSD assumes that the value of the loop bandwidth is set so the PSD can be divided in two parts:

- A flat part up until the loop bandwidth, dominated by the reference phase noise (the $1/f^3$ noise of the VCO is here cancelled by the high-pass filtering),
- A β/f^2 part due to the combination of low-pass filtering of reference PN and the $1/f^2$ noise of the VCO which is not affected by high-pass filtering.

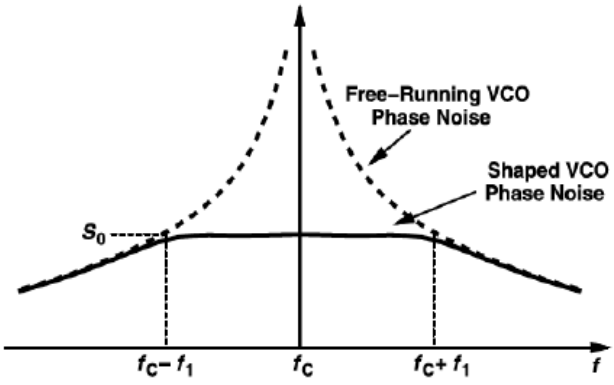

Figure 31: A simplified PLL phase noise PSD [1]

This simplified PLL phase noise PSD is shown in Figure 31. Here it is additionally assumed that the total phase noise PSD is dominated by the shaped PN of the VCO.

3.3.3 The all-digital phase-locked loop (ADPLL)

Based on the premise that, for electronic circuits built in the deep-submicron CMOS technology, the time-domain resolution of digital signals is superior to the voltage resolution of analog signals, the current trend in the analog RF design has been to substitute the traditional analog blocks with equivalent digital blocks, whenever possible to do so. One of the results of these efforts was the design of the ADPLL [24], [25], [26]. The essence of ADPLL is to take the charge-pump/type II PLL and replace the PFD/charge pump pair with an aritmetic phase detector and a time-to-digital converter (TDC), the analog filter with a digital one and the VCO with a digitally-controlled oscillator (DCO).

- In the initial ADPLL design [26], the integer part of the phase difference between the reference and the output signal is calculated by accumulation and subtraction;
- The digital signal corresponding to the total phase difference between the reference and

output is filtered by a digital lowpass filter, with the same function as its analog counterpart in analog PLLs;

- The digital signal produced by the loop filter is used to control the DCO; the frequency is tuned by applying the digital signal to a controllable bank of capacitors/varactors.

3.3.4 Tunability and its impact on the overall system performance

The main effect of the local oscillator on system performance is through phase noise. If we concentrate on ADPLL, there is one external source of phase noise and two internal ones. The external phase noise source is, as in the analog PLL, the reference signal source. The internal phase noise comes from the quantization noise of the TDC (due to TDCs finite time resolution) and also from the DCO.

The finite resolution of the TDC causes a quantization error in the calculation of the phase difference between the output signal and the reference signal; this error is thus directly converted to phase noise at the output of the ADPLL. The spectrum of this phase noise can be considered flat, with the PSD given by [25]

$$L = \frac{(2\pi)^2}{12}\left(\frac{\tau_{TDC}}{T_{DCO}}\right)^2 \frac{1}{F_{REF}} \tag{3.10}$$

where τ_{TDC} is the time resolution of the TDC, $1/T_{DCO}$ is the output frequency of the ADPLL and F_{REF} is the reference frequency.

The TDC phase noise dominates the PLL phase noise spectrum up to the loop bandwidth. If we refer to older TDC designs, like [27], τ_{TDC} is equal to the delay of CMOS inverters which is on the order of tens of ps, and can be considered proportional to C/I_{bias}, where C is the parasitic capacitance of the inverter and I_{bias} its bias current. Therefore, the TDC phase noise level can be, at least in theory, tuned by the bias currents of CMOS inverters. Newer TDC designs employ more advanced techniques, such as linear Vernier, gated -Vernier and 2D-Vernier inverter lines ([28], [29]), which employ the difference between different inverter types to produce an overall time resolution on the order of ps. Other than offering superior phase noise performance compared to linear delay line TDCs, these designs offer remarkably small power consumption, occupying only a few percent of the total power consumption of the whole PLL [29], and thus the development of designs which would feature power scalability of TDCs seems like a useless effort.

On the other hand, by analyzing actual ADPLL designs, the DCO sticks out as a main power consumer; it is also the dominant source of phase noise outside the loop bandwidth. By analyzing (3.9), we see that the level of phase noise PSD for the cross-coupled oscillator can be decreased by increasing the tail current (this analysis deserves a cautios approach, however. As pointed out before, the increase in bias current affects the Q factor of the LC tank. Also, the newly generated voltage drop across the tank resistance affects the voltage controlling the varactors, and thus the tank resistance has to be tuned together with the bias current. The result is a 3 dB improvement of phase noise with a 3 dB increase of consumed power, as analyzed in Example 8. 38 in [1]).

When dynamical tuning of power consumption/phase noise is performed in a DCO, it is of interest to keep the figure of merit (FOM) of the oscillator constant. The FOM is usually defined as [30]

$$FOM = -L(\Delta\omega) + 20\log\left(\frac{\omega}{\Delta\omega}\right) - 10\log(P_{mW}) \tag{3.11}$$

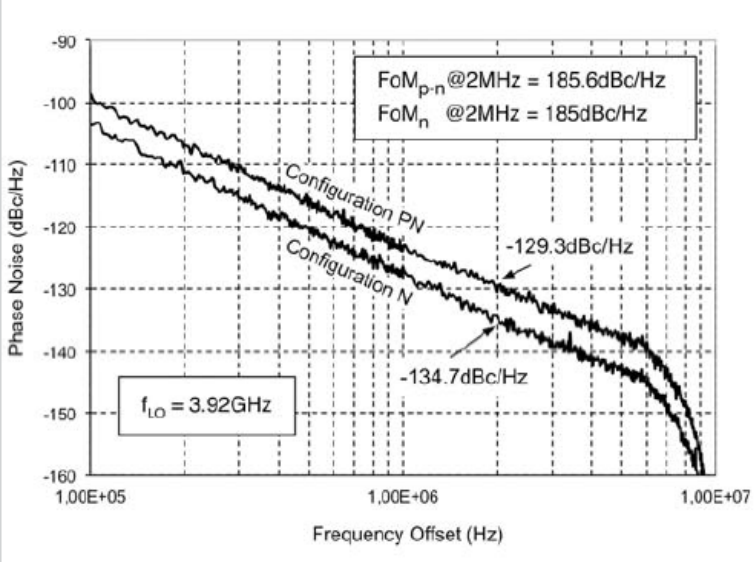

Figure 32: Measured phase noise for the two-step power tuning of the DCO [31]

where $L(\Delta\omega)$ is phase noise PSD value at the frequencu offset of $\Delta\omega$ and ω is the output frequency. P_{mW} is the power consumption in milliwatts. If it is possible to keep the FOM constant while tuning the power, then power and phase noise have a linear-in-dB relationship with slope 1. The DCO design in [31] manages to implement a two-stage tuning of power and phase noise while keeping the FOM constant by essentially switching between two DCO topologies. For a four-fold increase in power consumption when switching from one topology to another, there is a theoretical 6 dB improvement of the phase noise (the measured one is 5.4 dB, very close to the theoretical value). It is reasonable to assume a very simple ADPLL design which would incorporate this DCO. As DCO is a dominant phase noise source outside of the loop bandwidth, this part of the phase noise PSD for the PLL can be copied from Figure 32. With a loop bandwidth of 100 kHz making an ideal balance of DCO and TDC/reference phase noises, the phase noise PSD inside the loop band can be assumed flat and attaining the values of -98 dBc and -104 dBc for the "low-power" and "high-power" ADPLL configurations, respectively.

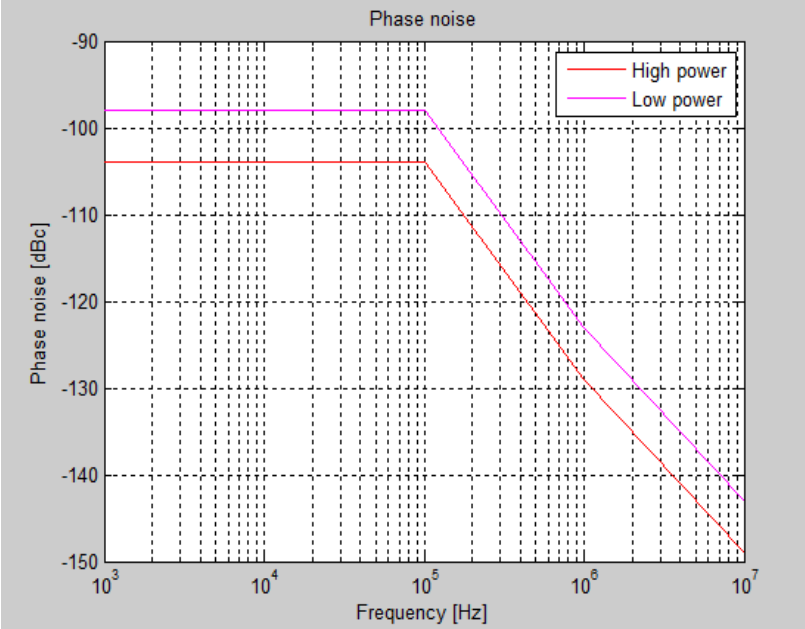

Figure 33: Phase noise PSD of a simple two-step power-scalable ADPLL

Phase noise PSD of this simple ADPLL design is given in Figure 33. If the power consumption budget from a standard ADPLL design like the one in [29] is retained, where 9 mW are consumed by the digital circuitry and the rest is consumed by the DCO, we can assign a power consumption of 18 mW to the low-power and 45 mW to the high-power configuration of the ADPLL.

Turning on the high-power mode of the ADPLL can occur *e.g.* when a high throughput has to be supported, or the SNR is too low and the noise floor coming from the phase noise has to be lowered. Also, in the presence of a strong blocker, reciprocal mixing can raise the noise floor significantly and thus the receiver can react by turning on the high-power mode. Once the blocker is gone, the receiver can return back to low-power mode and save power.

3.4 Downconversion mixer

The task of the downconversion mixer in the direct-conversion receiver is to map the wanted signal from passband to baseband by using the signal from the local oscillator. This is (conceptually) done by *multiplying* the oscillator sinusoidal signal (having a frequency f_c) and the wanted signal. Mixers have two input ports: RF port and LO port, and one output port - the baseband port.

The usual implementation of mixers is the one of a balanced pair of switches (represented in Figure 34).

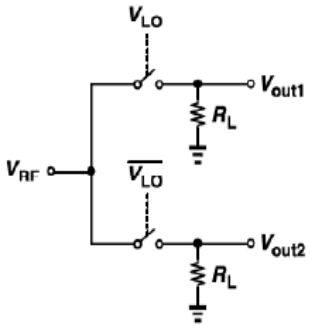

Figure 34: Mixer as a balanced pair of switches [1]

Signals V_{LO} and $\bar{V}_{LO}$ are ideally rectangular pulse trains opposite to each other: when V_{LO} is "high", $\bar{V}_{LO}$ is "low" and vice versa. This mixer configuration is the *single-balanced* configuration; there is also a *double-balanced* configuration where the input has split polarity as well.

The choice of square pulses over a pure sinusoidal carrier is justified by a larger conversion gain offered by the square pulses. The actual downconversion itself is performed through the first harmonic of the square pulse train; input signal spectrum replicas generated by higher harmonics of the square wave are safely filtered out by the baseband filter.

Mixer implementations can be broadly categorized into *passive* and *active* ones.

Passive mixers: in this mixer implementation, MOSFETs are used just as switches, not as amplifying devices. Usually, a single-balanced configuration is used, and load resistors R_L are substituted by capacitors; this particular configuration is referred to as the *sampling mixer*. The sampling single-balanced mixer can be shown to offer a conversion gain of 1.48 dB, and the sampling double-balanced mixer has the conversion gain of $2/\pi \approx -4\,dB$ [1]. Since this gain is too small to supress the noise coming from subsequent stages, usually a differential amplifying stage is attached to the passive mixer output, thus increasing the overall conversion gain [1]; another option is to have an LNA with a larger gain [32].

Active mixers lump together the mixing and amplifying stages into one block; this block performs voltage-to-current conversion, current switching and current-to-voltage conversion, thus performing mixing and amplification simultaneously [1]. A classical active mixer design is the cross-coupled differential design-Gilbert cell [33].

3.4.1 Tunability and its impact on the overall system performance

Main performance parameters of downconversion mixers are *conversion gain, noise figure* and *linearity*. Passive mixers generally offer a larger IIP3/ CP_{1dB} than active mixers, with noise figures being roughly the same [32]. One benefit of passive mixers is that they don't suffer from low-frequency flicker noise; another benefit is that they don't consume any DC power. Their drawback is a negative or very small conversion gain which needs to be compensated in preceding or subsequent stages (this is where then the saved power is spent). For proper switching, maximum conversion gain and minimum noise, passive mixers demand a full-rail signal from the local oscillator; this is another power investment drawn by passive mixers elsewhere in the receiver. Effectively being switching networks, passive mixers cannot be subject to any reconfigurability or dynamic power/performance control.

Active mixers, however, can be made tunable. Following the analysis in [33], the conversion gain (voltage) and IIP3 of a double-balanced Gilbert cell (shown in Figure 35) can be expressed with (3.12) and (3.13) respectively [33]:

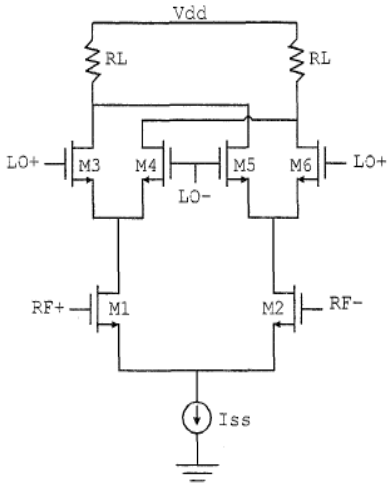

Figure 35: Double-balanced Gilbert cell [33]

$$A_v = \sqrt{K\, I_{SS}}\, R_L \frac{2}{\pi} \quad , \tag{3.12}$$

$$IIP3 \approx \sqrt{\frac{32\, I_{SS}}{3K}} \quad , \tag{3.13}$$

with $K = \mu_n C_{ox} W/L$. It appears that wasting some power and increasing the tail current I_{SS} will bring the double benefit of increasing the conversion gain and improving linearity; however, with a constant V_{DD} , the voltage drop over R_L will decrease the voltage headroom available for output signal swings, thus actually *reducing* the linearity. This is a common issue in power-tunable amplifier structures, and is resolved by isolating the tunable bias from load resistors [34]. One possible solution is injecting the needed additional bias current at the drains of M1 and M2 (the so-called "charge injection method", [33]). There is, however, some additional thermal noise injected with the independent bias currents, so some additional features need to be added to cancel this noise.

3.5 Channel select filters

After the downconverting mixer, the signal spectrum consists of the wanted signal component in the baseband, a copy of the wanted signal centered at $2f_c$ and numerous out-of-band interference signals. The wanted baseband signal is then isolated from unwanted components by using a low-pass filter - the *channel select filter* with an aggressive stopband attenuation.

3.5.1 Filter types

There are four filter types that are commonly implemented in actual analog (as well as digital) filter designs [35]: Butterworth, Chebyshev type I, Chebyshev type II and elliptical. All these filter types trade the amount of passband ripple in the amplitude characteristic for the

sharpness of the cutoff between passband and stopband.

- **Butterworth filter** has a totally flat passband (zero ripple). This is paid for by the worst cutoff among the listed filter types;
- **Chebyshev type I** has a certain amount of ripple in the passband and zero ripple in passband; this amount of ripple can be determined in the filter design process. The cutoff is sharper than in Butterworth filters;
- **Chebyshev type II** (or **inverse Chebyshev**) has a certain amount of predetermined ripple in the stopband and zero ripple in passband;
- Finally, the **elliptic filter** has predetermined ripple both in passband and stopband and the sharpest cutoff among the listed filter types.

The cutoff sharpness in all filter types increases with the filter order. Amplitude characteristics of different filter types are given in Figure 36, with frequency on the x-axis and the amplitude of the transfer function on the y-axis.

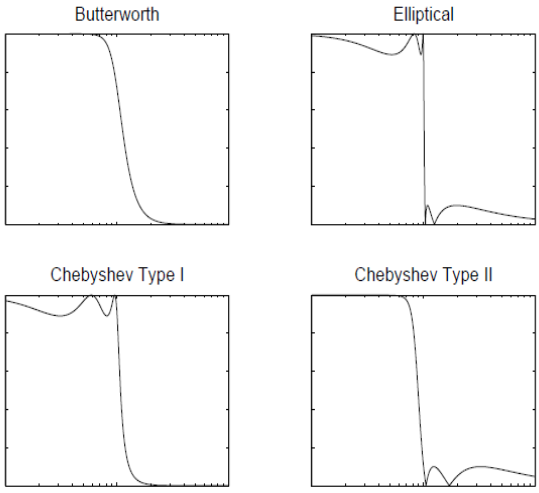

Figure 36: Common types of lowpass filters [35]

3.5.2 Filter implementations

Traditionally, analog filters have been implemented in the form of an LC (inductor and capacitor) ladder. These passive ladder designs can be implemented using discrete inductors and capacitors, by mechanical resonance in cristals or by using acoustic waves in ceramic materials [35]. When it comes to implementation in integrated circuits, analog designs using discrete elements can be implemented with only partial functionality. Analog filters in integrated circuits are therefore usually implemented with active electronic elements.

There are different "flavours" of active analog integrated filters. One of them is the *active-RC* filter; the fundamental cell/stage of such a filter is an RC network surrounding an op-amp. The amplitude characteristic of such a filter is determined by R and C elements, which can be made

discretely or continuously tunable in order to support a variable filter bandwidth; channel select filters with variable bandwidth are needed in radio receivers that are supposed to support multiple standards and operation modes. Tunability in active-RC filters is usually implemented by using a variable resistor. A benefit of active-RC filters that use op-amps is their high linearity. A drawback is that op-amps need to have a bandwidth that is much larger than the filter cutoff frequency, leading to increased power consumption.

Another line of active analog integrated filters is based on an OTA driving a load capacitance - a simple OTA integrator; these filters are referred to as G_m-C or OTA-C filters. The amplitude characteristic of G_m-C filters is determined by the value of the OTA transconductance g_m .

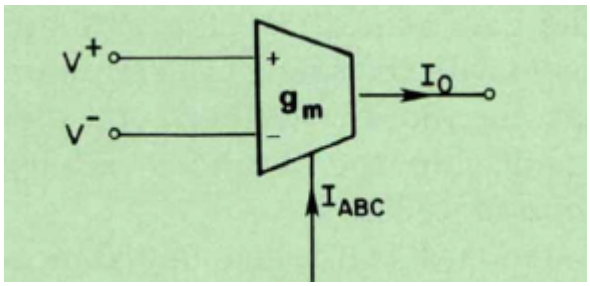

Figure 37: A general OTA [36]

As it can be seen from Figure 37, g_m can be directly tuned by changing the bias current I_{ABC} , with which it is directly proportional. $g_m=h\,I_{ABC}$ for an OTA using MOSFETs in weak inversion; $g_m=h\sqrt{I_{ABC}}$ when MOSFETs are in saturation. h is a proportionality constant depending on temperature and device geometry. The benefit of G_m-C filters is their reduced power consumption compared to active-RC filters; the drawback is their reduced linearity.

A hybrid between these two types is the active-RC filter with an OTA instead of the op-amp.

3.5.3 Tunability and its impact on the overall system performance

Filter cutoff frequency (pole/zero positions) can be tuned by *changing the values of variable resistors and capacitors*. A filter design which is, among other things, capable of continuously tuning the cutoff frequency is described in [37].

As the filter bandwidth increases, the power consumption increases as well. To reduce the power consumption at high bandwidths, *the bias currents of opamps/OTAs are reduced*. This technique is also implemented in [37]. Reduced bias currents/reduced power, however, also reduce the linearity of the filter. This is shown in Figure 38.

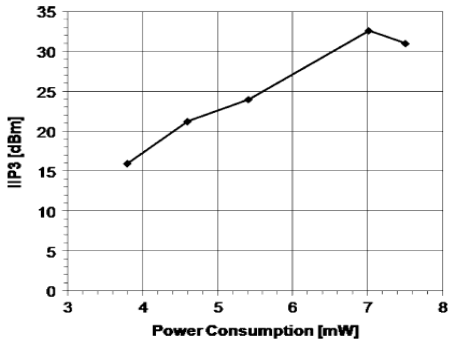

Figure 38: Filter IIP3 as a function of power consumption in the low frequency mode (measurement results of the design in [37])

We conclude that the power can be tuned either to compensate for frequency tuning (if we disregard the linearity criteria), or to tune the linearity of the filter according to performance requirements.

A similar power/performance driven tuning scheme is presented in [38]. Here, a special circuit detects the presence and level of the out-of-band blockers, and *increases tail currents of class-AB opamps in the filter in order to increase the linearity* and reduce the influence of the blockers. From the results given in [38], for an opamp used in a negative feedback loop the IIP3 is proportional to the 1.25th power of the bias/tail current [38]

$$IIP3 \propto I_{CNT}^{1.25} \quad , \tag{3.14}$$

where I_{CNT} is the tail current of the differential transistor pair at the opamp input.

Another way of adaptive treatment of blockers is by changing the stopband selectivity: for a given blocker level, reduced selectivity in the stopband means a more pronounced influence of the blocker (*e.g.* a higher level of compression). Selectivity can also adjust to the blocker level: to maintain the performance level, a larger blocker level would ask for increased selectivity. Stopband selectivity can be adjusted by *changing the filter order* - selectivity is reduced by reducing the order of the filter. As total power consumption of the filter grows linearly with the filter order, reducing the order implies a reduction in power consumption. Stopband selectivity adjustment by changing the filter order is implemented in [39].

With filters being complex, multi-stage electronic circuits, it is hard to describe general relations between performance indicators (noise figure, linearity) and power consumption because they are highly design-dependent. Some general trends can, however, be observed by analyzing **figures-of-merit** (FoM). A popular FoM for analog filters is defined as [40]

$$FoM = \frac{power\ consumption}{order \cdot SFDR \cdot bandwidth} [J] \tag{3.15}$$

where SFDR is the (normalized) spurious-free dynamic range, defined as

$$SFDR = \left(\frac{IIP3}{P_n} \right)^{\frac{2}{3}} \tag{3.16}$$

with P_n being the integrated phase noise power and IIP3 being expressed in power units (both dissipated over a 50 ohm resistor). Obivously, the principle "the less, the better" is applied to this FoM. If a design goal is set out - that FoM remains constant with parameter change and filter reconfiguration - it can be observed how changes in different performance parameters affect the

power consumption.

Three different power/performance tuning scenarios can be defined with a constant target FoM of 0.2 pJ (corresponding to state-of-the-art filters, like the one presented in [53]) and integrated noise, IIP3 and filter order being tuned in each of the scenarios (with one parameter changing and other two being constant). The parameters of scenarios are given in Table 3.

Scenario No.	1	2	3
Bandwidth [MHz]	10	10	10
FoM [pJ]	0.2	0.2	0.2
IIP3 [dBm]	10	from 0 to 20	10
Noise voltage density [$nV/\sqrt{Hz}$]	from 10 to 100	50	50
Filter order	5	5	from 3 to 7

Table 3: Channel filter reconfiguration scenarios

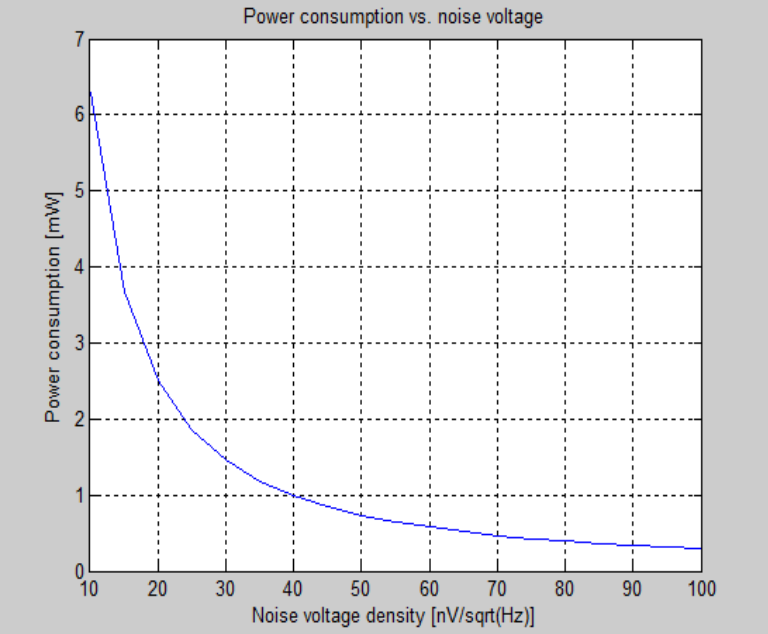

Figure 39: Power consumption as a function of noise voltage in scenario No. 1

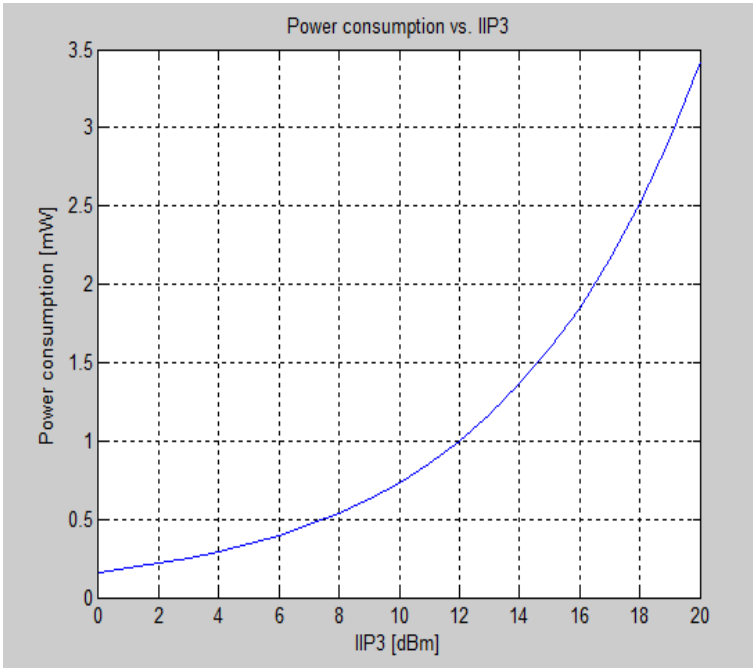

Figure 40: Power consumption as a function of IIP3 in scenario No. 2

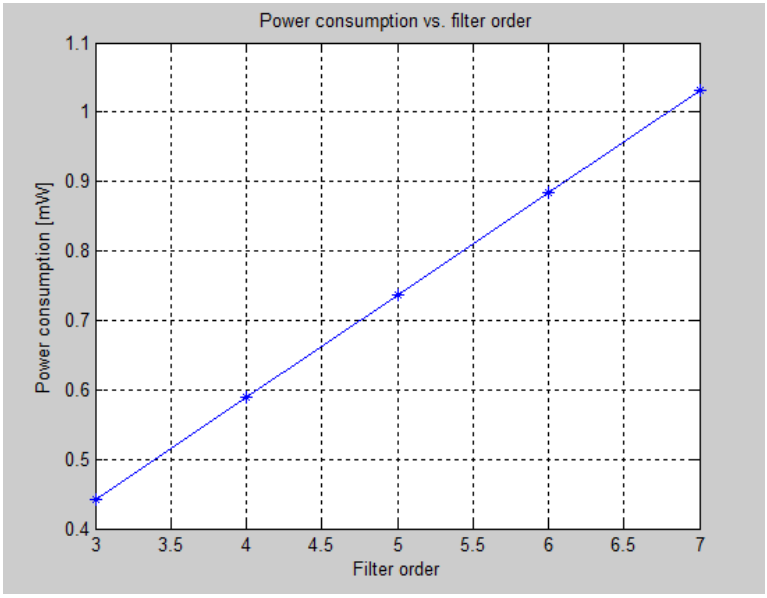

Figure 41: Power consumption as a function of filter order in scenario No. 3

3.6 Variable gain amplifier (VGA)

Due to small- and large-scale fading, the instantaneous power of the received signal experiences large swings, sometimes covering several orders of magnitude. These changes do not usually affect the analog parts of the receiver (with the exception of the maximum value of the received power which directly affects the signal distortion and puts constraints on the receiver linearity). The ADC, however, needs a constant-power signal at its input for an optimal performance (quantization and clipping noise minimized). Therefore, at the output of the analog part of the receiver there is a need for an "instantaneous power stabilizer" - a device that will provide a constant-power output with a varying-power input, together with providing additional power amplification.

It is obvious that this device needs to have a varying gain; the gain of the device would change dynamically according to the input power. The device in question is usually referred to as the variable gain amplifier (VGA) and the algorithm adjusting its gain is the automatic gain control (AGC). AGC is usually implemented by determining the signal power at the output of the ADC and then feeding this value back to adjust the gain of the VGA.

The VGA needs to have a gain which will change linearly following a linear change in signal power. It is obvious that both of these changes have to be *linear in dB (logarithmic) domain* in order to achieve a constant signal power at its output [1].

VGAs can be sorted into two broad groups, depending on the nature of the gain control signal, namely *digitally controlled* and *analog controlled* VGAs [41]. Digitally controlled VGAs exploit a switched-resistor or a switched-capacitor network to adjust the amplifier gain in discrete steps. (This line of VGAs is sometimes referred to as *programmable gain amplifiers*, PGA). In the case of a discrete-step VGA, the ADC needs to support an additional dynamic range equal to the VGA step; this means additional effective bits of precision and increased power consumption. The finer the steps of the VGA, the smaller the additional dynamic range of the ADC; on the other hand, there is an increase in the number of control bits and complexity of the control mechanism.

The drawbacks of digitally controlled VGAs make the analog controlled VGAs a more suitable choice. These VGAs usually perform gain adaptation by adjusting the transconductance or resistance stage of the amplifier in a continuous manner [41]. A somewhat more detailed analysis of different types of analog VGA control is given in [42]. The main challenge with these approaches is that the control signal (current or voltage) needs to be transformed by an exponential function in order to yield a linear-in-dB variable gain. Another approach is to obtain the gain in the form of the ratio of transconductances, which will in effect give an approximation of the exponential function of the control signal in the form of a rational function, like $1+x/1-x$. The problem with these methods is that the approximation of the exponential function is valid only for a limited range of control signal values, meaning that the useful range of the gain variation is limited (*e.g.* 12 dB). To obtain a wide range of variable gain, several such VGA stages have to be cascaded; this will yield a useful gain range of 60 - 80 dB needed for most applications, but will also increase power consumption. In [41], a very successful approach to approximating the exponential function of the control signal is offered; here, more than 60 dB of gain range *per stage* are obtained; with two cascaded gain stages and taking the influence of shortcomings of the amplifier topology in concern, a gain range of 95 dB is achieved.

3.6.1 Tunability and its impact on the overall system performance

It should be noted first that the varying gain of the VGA leads to (non)linearity and noise figure being variable as well. This might be taken into concern in the system design, but the simplest thing to do is just to take the worst-case value of (non)linearity and noise figure into concern. Another important point to measure the impact of the VGA on performance is at the output of the ADC. As it is described in the chapter on ADCs, in multicarrier systems, the performance of the ADC can be measured as a function of input backoff (IBO). The error vector magnitude (EVM) for a particular ADC resolution has its minimum (perfect equilibrium between quantization noise and clipping distortion) for a certain value of IBO. If we assume an ideal AGC algorithm design, and an analog controlled VGA with an infinite variable gain range, then the EVM at the ADC output will always be optimal. However, if the variable gain range is reduced, the EVM is increased either due to quantization or clipping. So this is how the variable gain range can affect the overall system performance.

The variable gain range is also directly proportional to the power consumption. If we consider a multi-stage VGA consisting of n stages and if P_{stage} is the power consumption of one stage, then the total power consumption is $P_{VGA}=n P_{stage}$, and so the range and power consumption both scale linearly with the number of stages. The simplest way of tuning the VGA in a power-optimized adaptive receiver would be to adaptively change the number of stages, trading performance for power consumption.

The impact on the performance can be determined from received signal statistics; the overall increase in EVM is equal to the tails of the received signal power distribution, determined by the range of input signal power not covered by the variable gain. A general formula for the power consumption of the VGA is found by determining P_{stage} through measurements.

4 Direct Conversion Receiver - Analog to Digital Conversion and Digital Baseband

4.1 Analog to Digital Conversion

4.1.1 Introduction

A digital signal, as opposed to its analog counterpart, is defined over a discrete time set and its amplitude attains values from a discrete set. This "doubly discrete" nature of digital signals enables their storage and convenient digital processing using fast digital electronic devices. The device that will perform the "double discretization" of an analog signal is the *analog-digital converter* (ADC).

The most basic type of analog to digital conversion is the pulse-code modulation (PCM). An ADC based on PCM works in two stages:

1. Discretization over time, performed by a *sample-and-hold* (S-H) circuit. This circuit detects the level of the input signal and keeps it constant over a period T (*sampling period*).
2. Discretization of the amplitude, or *quantization*: the value of the signal that is being "held" by the S-H circuit is approximated by the closest *quantization level*. This quantization level can be represented as an *n*-bit binary number, and there are exactly 2^n quantization levels.

4.1.2 A brief general overview of different types of ADCs

ADCs can be coarsely divided into ones that sample the signal at Nyquist frequency (or near it), and the ones that sample the signal at a frequency much higher than Nyquist.

Among the Nyquist ADCs, the most important ones are [43]:

- Direct-conversion (flash) ADCs
- Successive approximation ADCs
- Pipelined ADCs

The ADC based on the concept of sigma-delta modulator is representative of the oversampling ADCs (working with sampling frequencies that are higher than the Nyquist frequency).

4.1.3 Sigma-delta modulator ADC

The SD ADC performs very efficient analog-to-digital conversion by relying on the mechanisms of *oversampling*, feedback and filtering of the quantization error and digital filtering of the produced digital signal. The effects of these mechanisms are now analyzed in more detail., using information from a comprehensive tutorial on sigma-delta modulator ADCs [44].

4.1.3.1 Oversampling and noise shaping

If we sample the signal at a rate higher than the Nyquist rate of $2f_B$ and then quantize it, the total quantization noise power will remain the same, but it will be spread over a larger frequency range.

Although the quantization noise power is spread over a larger freqency range, when further processing the sampled and quantized signal we are still interested in the range $[-f_B, f_B]$. With oversampling, the quantization noise power (*in-band* quantization noise power) is smaller in this range:

$$P_N = \frac{\sigma_e^2}{OSR} \quad . \tag{4.1}$$

Therefore, the power of the quantization noise is pushed outside the band by oversampling, which will increase the signal to quantization noise ratio compared to the case when we sample at Nyquist frequency.

SNR can be further improved by noise shaping. To achieve this, a filter is put in front of the quantizer, and the output of the quantizer is fed back and subtracted from the input. The resulting structure is refered to as the s*igma-delta modulator* (SDM). If we represent the quantizer as a noise source, represent the signals in the discrete *z* domain, and additionaly use a simple integrator as the loop filter, the system diagram looks like the one represented in Figure 42:

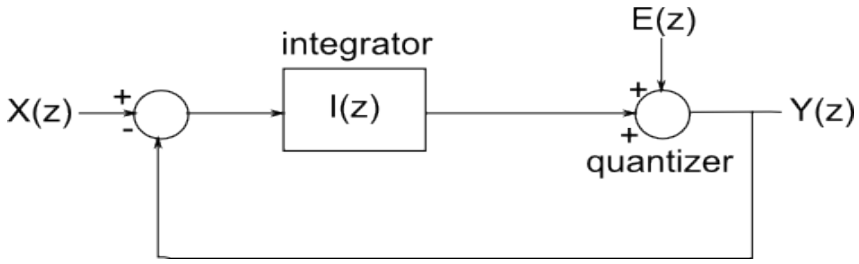

Figure 42: Discrete-time model of a simple sigma-delta modulator using an integrator as the loop filter

The transfer function of the system can be expressed as

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \quad . \tag{4.2}$$

We can see that the transfer function of the system is separated in two parts: the one corresponding to the signal (signal transfer function, STF), and the one corresponding to noise (noise transfer function, NTF). These are:

$$\begin{aligned} STF(z) &= z^{-1} \quad , \\ NTF(z) &= 1 - z^{-1} \quad . \end{aligned} \tag{4.3}$$

It can be observed that the NTF is actually a discrete-time differrentiator, so in effect the quantization noise is differentiated by the delta-sigma structure.

Using trigonometric identities, we can determine the noise spectral density envelope

$$|NTF(f)|^2=(1-e^{-j2\pi f/f_s})(1-e^{j2\pi f/f_s})=4\sin^2(\pi f/f_s) \quad .(4.4)$$

With $S_e(f)=\sigma_e^2/f_s$ being the power spectral density of the unshaped quantization noise, the overall quantization noise spectral density is then given by

$$S_e(f)|NTF(f)|^2=4\frac{\sigma_e^2}{f_s}\sin^2(\pi f/f_s) \qquad (4.5)$$

The envelope of the noise spectral density is plotted in Figure 43.

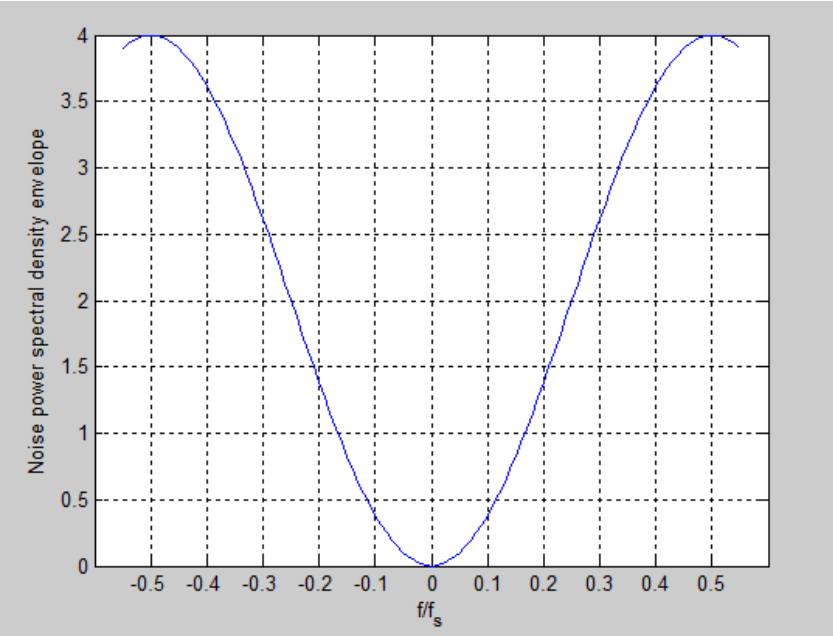

Figure 43: Envelope of the quantization noise PSD-noise shaping effect

We see that the filtering (differentiation) of the quantization noise has the effect of shaping the noise power and "pushing" it to higher frequencies. The total quantization noise power actually gets doubled by the differentiation, so if we combine sigma-delta processing with Nyquist-rate sampling, we will actually make the signal to quantization noise ratio worse. The trick is to increase the sampling rate, so $f_B \ll f_s$ and then cut the unwanted noise spectrum with a low-pass digital filter. This way the power of the in-band quantization noise is significantly reduced. The SNR can be improved even further by using higher order SD modulators in which an order-*K* noise shaping filter is used. The total in-band quantization noise power for an order-K SD modulator is [44]

$$P_N \approx \frac{\sigma_e^2\pi^{2K}}{(2K+1)OSR^{2K+1}} \quad . \qquad (4.6)$$

The dynamic range (DR) of an ideal SD ADC is given by [44]

$$DR_{dB}=10\log\left[\frac{3(2^n-1)^2(2K+1)OSR^{2K+1}}{2\pi^{2K}}\right] \qquad (4.7)$$

(An "ideal" ADC is the one with no thermal noise or distortions. The only factor impairing the performance is the quantization noise).

4.1.3.2 SD ADC Types

Given the circuit structure of the loop filter of the SDM, the SD ADCs can be classified into two groups:

- discrete-time (DT) SD ADCs
- continuous-time (CT) SD ADCs.

DT SD ADCs have a loop filter implemented in discrete-time, usually using switched-capacitor (SC) circuits. Also, it is worth noting that the SH circuit comes before the feedback is subtracted from the input signal.

As the demand for higher and higher sampling rates increases with system bandwidth, the research and practical implementations are switching over to the CT SD ADCs. These ADCs have an analog loop filter that is usually based on active-RC or Gm-C circuits. The sampling here takes place inside the loop, right before the coarse in-loop ADC. CT SD ADCs are capable of working with larger sampling frequencies compared to the DT ones; they also in general consume less power. One additional benefit of CT SD ADCs is the inherent antialiasing filtering, which can additionaly relax the demands on (or even render obsolete) the analog antialiasing filter preceding the ADC [45].

4.1.4 Tunability and its impact on the overall system performance

An accurate analytical expression that would describe the power consumption of a particular ADC is very difficult, if not impossible to find. Therefore, an accurate power consumption of a certain ADC design can only be determined by measurements. On the other hand, there have been attempts to determine trends, lower bounds, approximations and generalizations for the ADC power consumption; the numbers obtained cannot be used reliably as a substitute for measured values, but they can be used to desribe trends and dependencies.

The most basic estimate of trends in the power consumption of ADCs is the ADC figure of merit (FOM). Figures of merit relate all the important parameters of ADCs visible at system level (dynamic range/SNR/SNDR, bandwidth and power consumption) and thus serve to compare the quality of ADCs with possibly totally different design and functional context. There are several definitions of the figure of merit, but the most popular one is defined as [46]

$$FOM_1 = \frac{P}{f_s 2^{ENOB}} \quad , \tag{4.8}$$

where f_s is the Nyquist sampling rate, $f_s = 2 f_B$ and $ENOB$ is defined as (taken from the chapter on RF impairments for convenience)

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02} \quad . \tag{4.9}$$

This FOM is sometimes reffered to as "Walden FOM" and is generally used for ADCs in which quantization noise dominates over other noise sources. As it can be observed from the definition, for a constant bandwidth, a 3 dB increase in power consumption will yield an additional bit of precision (or equivalently a 6 dB increase in SNDR). Another figure of merit is the so-called "Shreier FOM" and can be defined as [47]

$$FOM_2 = DR + 10\log\left(\frac{f_B}{P}\right) \quad . \tag{4.10}$$

It is important to observe that a smaller FOM_1 and a larger FOM_2 mean a "better" ADC. FOM_2 ignores distortion and concerns only the dynamic range. However, if we substitute DR with SNDR, we can conclude that FOM_2 is, up to a constant, equivalent with the reciprocal value of $P/(f_s 2^{2ENOB})$, which helps in the comparison of the two FOMs. FOM_2 is usually used to characterize ADC which are dominated by internal thermal noise. For a constant bandwidth, a 6 dB increase in power consumption is needed for an additional bit of precision, or an additional 6 dB increase in SNDR.

A comprehensive analysis of trends in ADC designs over the years is presented in [47], where Figure 44 is borrowed from. Various ADC designs presented over the years are compared by means of power consumption, or rather, energy per sample taken (y axis is actually P/f_s which can be reffered to as *energy efficiency*).

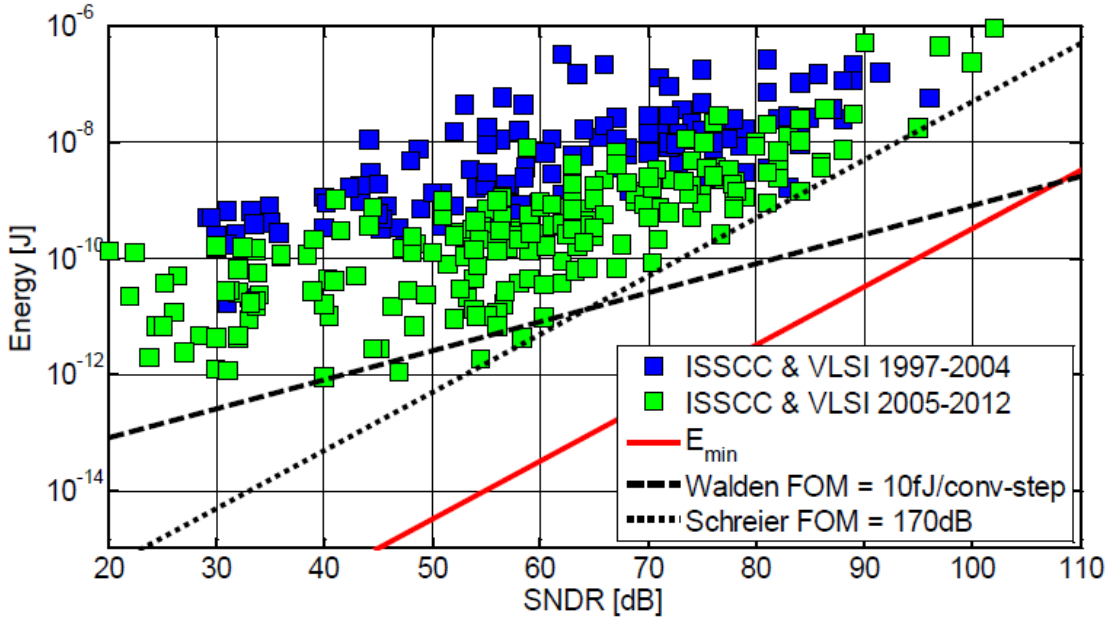

Figure 44: Energy as a function of SNDR for various ADC designs, given with lower bounds on FOM [47]

As it can be seen, the most recent ADC designs (regardless of type or use) have lower bounds on FOM given by $FOM_1 = 10\,fJ/conversion\,step$ and $FOM_2 = 170\,dB$. It can also be seen that the ADC designs with nominal SNDR larger than approximately 60 dB are dominated by thermal noise (and therefore characterized by FOM_2).

It has been observed that the input signal distortion/noise, the input-referred noise of the first stage of the ADC and DAC distortion/noise add to the input signal; assuming an ideal STF, these three go all the way through the ADC unaffected. Other noise/distortion sources coming from subsequent stages are shaped by the NTF and their influence to the overall ADC performance drops as they are placed deeper in the chain. We can therefore conclude that *the integrator in the first stage and the DAC are the dominant sources of noise and distortion in the ADC*. With this in mind, the demand on their *linearity* is high (and high linearity is directly connected to a high power consumption).

The operation of CT SD ADCs can also be impaired by the existence of strong **out-of-band blocking signals** (OOB), where OOBs mix with the quantization noise which has been pushed out-of-band due to noise shaping. This transfers the noise back in the band, in a process identical with reciprocal mixing of phase noise. In SD ADC parlance, this phenomenon is called “noise folding”. Strong OOBs can also saturate the input of ADCs, thus reducing their dynamic range (this can be ameliorated by extending the linearity of the front integrator, which has to be paid by increased power consumption).

As it can be seen, analog filters (the ADC loop filter - that is, its STF part - and the channel select filter) are successfully used in supressing the OBBs. The higher the order of the filters, the sharper the roloff and better the OBB suppression. However, with both filters being analog, a higher order costs more in terms of power consumption.

In order to analyze possible power/performance tradeoffs in the SD ADC, we can assume some simplistic scenarios. For the first scenario, we assume that the dynamic range of the ADC is dominated by quantization noise; thermal noise is below the quantization noise and nonlinear distortion effects can be disregarded. SNDR is then given by (4.7); we can conclude that increasing the OSR and loop filter order K (individually, or simultaneously) increases the SNDR. If we further assume that the ADC is designed in such a way that major reconfigurations do not affect the FOM, *i.e.* FOM is kept constant, we can conclude from (4.8) and (4.9) that an expansion of the SNDR means an increase in power consumption. On the other hand, from formula (2.55), we see that the EVM is proportional to the quantization noise (or inverse proportional to the SNDR). We can thus conclude that an *increase in OSR and K* will mean lower EVM (better performance) but also higher power consumption.

For the second scenario, we assume a presence of a powerful out-of-band blocker. This blocker desensetizes the front integrator of the loop filter and causes noise folding. This will reduce the SNDR and increase the EVM, *i.e.* the result is a performance impairment. Locally in the ADC, the desensitization can be remedied by *improving the linearity of the front integrator*; this is, however, paid by increased power consumption. On the system level, both the desensitization and noise folding can be remedied by using a channel select filter with a larger order; this, however means a higher power consumption in the channel select filter.

It is unlikely that the SNDR is affected by quantization and nonlinearities separately; in real-life systems it is most likely affected by both, and therefore real-life scenarios are a combination of the two scenarios just described. In total, we can conclude that power and performance in a SD ADC can be traded by tuning the OSR, loop filter order and the linearity of the front integrator in the loop filter; additional tuning is accomplished by changing the order of the channel select filter.

4.2 Digital baseband

4.2.1 Introduction

Implementation of very fast digital circuits was brought on by advances in integrated electronic circuit design in recent decades. Digital circuits that work on clocks on the order of GHz now serve as building blocks of various devices such as personal computers and mobile phones.

The basic building block of digital circuits is the CMOS inverter (NOT gate), shown in Figure 45 [1]

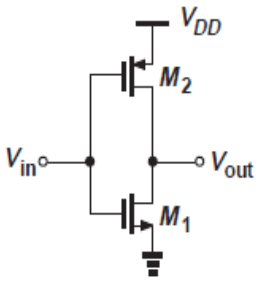

Figure 45: CMOS inverter[1]

For a "high" input, this circuit produces a "low" output, and vice versa. The CMOS inverter is used to build NAND and NOR gates which can then be used to build more complex digital circuits.

4.2.2 Structure of the baseband part of a MIMO/OFDM receiver

A general structure of a direct conversion MIMO/OFDM receiver (like the ones used for LTE/LTE-A handsets) is shown in Figure 46. The blocks shown correspond to one antenna branch.

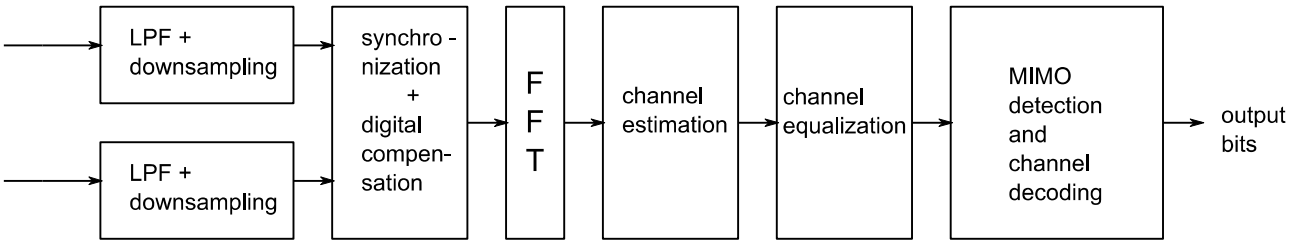

Figure 46: General MIMO/OFDM digital baseband

- Two low-pass filters with downsampling come right after the delta-sigma ADCs in I and Q branches of the receiver. Their task is to filter the quantization noise that has been pushed out of band and to downsample the signal to a correct rate;

- The subsequent block performs symbol synchronization based on pilot symbols present in the received block. It also performs an array of different digital signal processing schemes which aim to compensate for various impairments introduced by the channel and analog front end, like frequency offset and DC offset compensation, I/Q imbalance correction, etc.;
- The FFT block performs the FFT on the received symbols to complete the OFDM transmitter/receiver structure. It is preceded by cyclic prefix removal (not shown);
- After FFT comes channel estimation, again making use of known pilot symbols that are strategically spread on the time-frequency grid of the received block. The result is the estimated channel matrix $\tilde{\boldsymbol{H}}$;
- Using the channel matrix estimate, channel equalization is performed, aiming at removing the signal constellation rotation and compression introduced by the channel. The side effect is the removal of some RF-impairment-induced effects, like the rotation due to phase noise and compression due to receiver nonlinearities;
- MIMO detection and channel decoding block does the final job of producing (estimated) data bits (it has *M* inputs from *M* receive antennas; only one is shown in Figure 46 for simplicity). It can either employ linear detection schemes (like ZF, MMSE or successive interference cancellation - SIC) or schemes that approximate maximum-likelihood detection (like sphere decoding-SD). The choice between the two groups of detection schemes offers a tradeoff between performance and complexity/power consumption (this will be described later). This block also performs a QR decomposition of the channel matrix, because both SIC and SD shemes make use of the decomposed matrix; the QR decomposition is usually performed using some sophisticated numerical algorithm, like Householder transform or Givens rotations.

4.2.3 Tunability and its impact on the overall system performance

Two basic parameters that describe the operation of the CMOS inverter are *propagation delay* and *power consumption.* Propagation delay, which determines the maximum switching frequency, is directly proportional to the capacitance C_L which is attached as a load to V_{out} , and inversely proportional to V_{DD} (as shown in [1]).

For a CMOS inverter, the dynamic power (power dissipated during switching) is given by ([48])

$$P_{dynamic} = \alpha f_{clk} C_L V_{DD}^2 \quad , \tag{4.11}$$

where α is the activity factor, *i.e.* the fraction of the circuit that is actually performing switching and f_{clk} is the frequency of the switching. This indicates that, if we are able to switch off some parts of the circuit under certain conditions (disconnect them from the clock), then we will be able to save some power. We can conclude that there is a tradeoff between propagation delay/maximum operating frequency and power consumption, where the two are traded by tuning the V_{DD} . This fact can be made useful in circuits where performance depends on the time resolution of the inverter.

The CMOS circuit also experiences certain *leakage power consumption*, governed by subthreshold leakage currents. This power is given by ([48])

$$P_{leakage} = N(1-\alpha) I_0 e^{-\frac{V_T}{n V_{TH}}} V_{DD} \quad , \tag{4.12}$$

where N is the total number of gates in the circuit, α is the activity factor from before, I_0 the leakage current and V_T, n and V_{TH} are physical parameters inherent to the technology. It is clear that tuning the supply voltage will affect the leakage power as well.

Finally, there is the question of circuit delay τ which determines the switching frequency for the CMOS circuit [48]:

$$\tau = \sum_{n=1}^{A} \frac{C_n V_{DD}}{K_n (V_{DD} - V_T)^{\delta}} \quad , \tag{4.13}$$

with *n* being the gate index, *K* the "drivability factor", δ a technology dependent factor and *A* the number of gates forming the delay path of the circuit. *A* increases with increased wordlength.

Before an analysis of power/performance tunability for the baseband is given, a very important performance indicator needs to be defined. First of all, we define the *nominal information transmission rate R* as maximum transmission rate for a given modulation and coding scheme (MCS) and MIMO configuration, as per 3GPP specifications [49]. Then, the throughput TH is defined as $TH = R \cdot (1 - FER)$, where FER is the frame error rate. Since throughput does not take hardware limitations into concern, we finally define *goodput* as the minimum of maximum hardware detection rate multiplied by the code rate, and throughput:

$$goodput = min\{HW\_detection\_rate \cdot code\_rate, TH\} \tag{4.14}$$

Goodput is a figure of merit that takes both channel and hardware limitations into concern, and is thus very suitable as a performance indicator for baseband hardware.

One way of trading performance for power consumption in digital baseband circuits is to *vary the wordlength* - number of bits in the representation of a fixed-point number. The wordlength is varied by masking the least significant bits with zeros; it is obvious that this introduces an error equivalent to quantization noise in the system. Power savings with wordlength reduction have two main causes [50]:

- There is a reduction in the number of logical value changes (from 0 to 1 and vice versa) in arithmetic circuits (adders and multipliers). This signifies less switching, and consequently the dynamic power is reduced;
- The number of gates in shift registers can be reduced. In order to harvest any power savings, these redundant gates need to be disconnected from the clock by using gated-clock control technology. This feature is the principal reason for power savings in the variable wordlength scheme.

The variable wordlength scheme is described in [50], where it is applied to the LPF, FFT and channel equalizer blocks from Figure 46. The reported power savings are 30% for the AWGN channel and 20% for the multipath channel.

By observing (4.11), we conclude that power savings can be harvested by reducing the supply voltage, which will in turn increase the propagation delay in the circuit (and reduce the maximum detection rate supported by the hardware). This scheme is known as Dynamic Voltage Frequency Scaling (DVFS). The drawback of the DVFS is the described effect on the maximum hardware detection rate (and consequently goodput), which is not desirable behaviour. By observing (4.11), (4.12) and (4.13) it can be concluded that power savings can be achieved by reducing the supply voltage, but to keep the propagation delay (for the whole circuit) constant, the wordlength needs to be adjusted as well; *e.g.* reduced voltage will yield increased delay which can be compensated by decreased wordlength. The scheme that tunes supply voltage and wordlength simultaneously is known as Dynamic Voltage Wordlength Scaling (DVWS) and is described in [48]. In this paper, the scheme is applied to a 4x4 MIMO MMSE detector for IEEE 802.11n; wordlength

is dynamically changed according to SNR and multipath characteristics of the channel. Power savings of 68% (from the worst-case power consumption value of 717 mW) are achieved for the shortest wordlength (corresponding to the "weakest" MCS).

Another way of adjusting power consumption to performance is to switch between different MIMO detection algorithms according to current channel conditions. It has been observed [51] that SIC detection scheme performs better in MIMO channels with less spatial correlation, whereas SD is more suitable for channels with high spatial correlation. Since SIC costs less in terms of complexity/power consumption, an optimum power consumption would be achieved if SIC was used in low correlation conditions and SD in high correlation conditions; channel correlation can be conveniently measured by calculating the condition number of the channel matrix. The drawback to this method would be doubling of chip area to accomodate two detection algorithm implementations on one ASIC chip; an additional drawback would be the leakage power in the inactive algorithm implementation.

5 A Summary of Power Consumption/Performance Tradeoffs in the Receiver Chain

This chapter gives a summary of the most important tradeoffs between power consumption and performance in a radio receiver chain (including analog, mixed-signal and digital parts). The tradeoffs presented here are divided in two groups:

- Local (block-level) tradeoffs, where changes in a certain circuit parameter induce a tradeoff between power consumption and performance that are observed on an isolated block (the effect of the parameter changes on other blocks is disregarded),
- Global (system-level) tradeoffs, which take into concern the interaction between blocks.

For a neat and clear representation, a convenient shorthand notation for the changes in circuit and block parameters is introduced:

- **"+"** indicates that the value of the parameter is increasing,
- "-" indicates that the value of the parameter is decreasing,
- "c" - the value of the parameter is kept constant.

The analysis will cover circuit parameters (like feedback factors and bias currents) and block parameters (like gain and linearity). The measure of the performance is the EVM (larger EVM indicates poorer performance). Power consumption is denoted as P_c .

5.1 Local tradeoffs

5.1.1 LNA

The LNA design chosen for the analysis is the one described in Section 3.2. Tuning circuit parameters are feedback coefficients F_1 and F_2 . Two characteristic local power consumption/performance tradeoffs for the LNA are:

1. Jointly trading noise and linearity for power. Feedback coefficient F_2 is kept constant, thus keeping the gain constant, whereas F_1 is tuned, affecting the NF and linearity:

$$(\ cF_2\ ,\ -F_1\ ) \rightarrow \text{c gain} \rightarrow \text{+ NF} \rightarrow \text{- IIP3} \rightarrow \text{+ EVM} \rightarrow\ -P_c$$

2. Jointly trading gain and noise for power. Feedback coefficient F_1 is kept constant, which keeps the linearity constant, and F_2 is tuned, affecting the gain and NF:

$$(\; cF_1 \; , \; -F_2 \;) \rightarrow \text{ - gain} \rightarrow \text{ + NF} \rightarrow \text{ c IIP3} \rightarrow \text{ + EVM} \rightarrow \; -P_c$$

5.1.2 Frequency synthesizer

The analysis is based on the ADPLL. Tuning parameters are the tail current of the DCO, I_{SS} and time resolution of the TDC.

1. Tuning the tail current of the DCO will affect the phase noise PSD outside of the PLL loop bandwidth:

$$-I_{SS} \rightarrow \text{ + out-of-band phase noise} \rightarrow \text{ + EVM} \rightarrow \; -P_c$$

2. Tuning the resolution of the TDC results in current savings in the time-to-digital converter. At the same time, the phase noise (due to quantization) inside the PLL loop bandwidth is affected:

$$\text{- TDC resolution} \rightarrow \text{ + in-band phase noise} \rightarrow \text{ + EVM} \rightarrow \; -P_c$$

5.1.3 Downconversion mixer

Power-performance tradeoffs can only be observed in an active mixer design. The tuning is performed via the tail current I_{SS} of the mixer cell.

1. Tuning the tail current of the Gilbert cell affects the gain and IIP3 jointly. Additional "bleeding current" has to be injected and taken into concern when calculating the change in current consumption.

$$-I_{SS} \rightarrow \text{ (- conversion gain , - IIP3)} \rightarrow \text{ + EVM} \rightarrow \; -P_c$$

5.1.4 Channel select filter

In some particular cases, the tuning knob of the channel select filter is the tail current I_{SS} of an opamp, representing one stage of the filter. In a general tradeoff analysis based on FOMs, there is no clearly defined tuning knob.

1. Tuning the tail current of one stage of the filter affects the linearity of that stage:

$$-I_{SS} \rightarrow \text{- IIP3 (of one filter stage)} \rightarrow \text{+ EVM} \rightarrow -P_c$$

2. General linearity-power tradeoff based on the assumption of constant FOM:

$$(\text{c FOM, - IIP3}) \rightarrow \text{+ EVM} \rightarrow -P_c$$

3. General noise-power tradeoff (assuming a constant FOM):

$$(\text{c FOM, + Noise voltage density}) \rightarrow \text{+ EVM} \rightarrow -P_c$$

5.1.5 Variable gain amplifier

VGAs can be conveniently implemented using the same design as the LNA; in that case, all the local tradeoffs are the same as in the LNA.

5.1.6 ADC

Local tradeoffs for the ADC are given in a general form, assuming a constant FOM. OSR and K denote the oversampling ratio and order of the sigma-delta ADC, respectively.

1. Tuning the OSR:

$$(\text{c FOM, - OSR}) \rightarrow \text{- Dynamic range} \rightarrow \text{+ EVM} \rightarrow -P_c$$

2. Tuning the order of the ADC:

$$(\text{c FOM, - K}) \rightarrow \text{- Dynamic range} \rightarrow \text{+ EVM} \rightarrow -P_c$$

3. Reacting to a strong input blocker at the ADC input, the linearity of the front opamp is increased for an increase in dynamic range. This reduces the EVM but also asks for an increase in power consumption:

$$(\text{strong input blocker, + linearity of the front op-amp}) \rightarrow \text{+ Dynamic range} \rightarrow \text{- EVM} \rightarrow +P_c$$

5.1.7 Digital baseband

Only the most fundamental power/performance tradeoffs for digital circuits are given: a more thorough analysis is out of the scope of the thesis. An additional performance measure here can be the throughput.

1. Decrasing the wordlength saves power but introduces quantization noise:

$$\text{- wordlength} \rightarrow \text{- switching activity} \rightarrow \text{+ EVM} \rightarrow \quad -P_c$$

2. Decreasing supply voltage saves power, but also affects the throughput:

$$\text{- supply voltage} \rightarrow \text{- propagation delay} \rightarrow \text{- throughput} \rightarrow \quad -P_c$$

3. Jointly reducing supply voltage and wordlength keeps the throughput constant, but increases the EVM (and saves power):

$$\text{(- supply voltage, - wordlength)} \rightarrow \text{(- switching activity, - propagation delay)} \rightarrow \text{(+ EVM, c throughput)} \rightarrow \quad -P_c \quad .$$

5.2 Global tradeoffs

Global tradeoffs will be described in a generalized fashion, without noting the tuning knobs. Also, the tradeoffs listed will only be the most important ones.

1. The fundamental global tradeoff of noise, linearity and power consumption: while increasing the gain of one block reduces the effect of noise of subsequent blocks, it also increases the distortion due to nonlinearity in these blocks. The increase of gain also costs in terms of power consumption:

$$\text{+ block gain} \rightarrow \text{ - effect of thermal noise from subsequent blocks} \rightarrow \quad -EVM_{total,noise} \rightarrow +P_c$$

$$\text{+ block gain} \rightarrow \text{ + effect of nonlinearity distortion from subsequent blocks} \rightarrow +EVM_{total,nonlinearity} \rightarrow \quad +P_c \quad .$$

As it can be seen, increasing the gain to control the overall noise may cause nonlinearity distortion. As long as the decrease in $EVM_{total,noise}$ is larger than the increase in $EVM_{total,nonlinearity}$, it pays off to spend extra power to control the noise.

2. Tradeoff between baseband filter order *N* and ADC linearity:

$$+\,\mathrm{N} \rightarrow\ +\,\text{out-of-band blocker supression} \rightarrow\ -\,\text{nonlinearity distortion} \rightarrow\ -\,\mathrm{EVM} \rightarrow\ +P_{c,\,filter}$$

This tradeoff can be expanded by a decrease in ADC linearity, which is a reverse of tradeoff No. 3 for the ADC. In total this is then not a tradeoff but it is worth noting for completeness' sake:

$$(+\,\mathrm{N},\ -\,\text{linearity of ADC}) \rightarrow\ +\,\text{blocker supression} \rightarrow\ \mathrm{c}\ \text{nonlinearity distortion} \rightarrow\ \mathrm{c}\ \mathrm{EVM} \rightarrow (\ +P_{c,\,filter}\ ,\ -P_{c,\,ADC}\ ).$$

If the decrease in $P_{c,\,ADC}$ is larger than the increase of $P_{c,\,filter}$, then it is possible to maintain the EVM with an overall *decrease* in power consumption.

3. Tradeoff between the gain of the chain, quantization noise, thermal noise and nonlinearity:

$$-\,\text{front end gain} \rightarrow\ +\,\text{ADC input backoff} \rightarrow\ +\,\text{quantization noise} \rightarrow (\ +EVM_{quantization}\ ,\ -EVM_{nonlinearity}\ ,\ +EVM_{noise}\ ) \rightarrow\ -P_c\ .$$

The savings in power are justified only if the decrease in $EVM_{nonlinearity}$ is larger than the increase in EVM_{noise} and $EVM_{quantization}$.

4. Compensating the nonlinearity increase from a blocker (not a global tradeoff per se, rather a tradeoff that is applicable to any of the blocks in the chain):

$$(\text{a strong blocker},\ +\,\mathrm{IIP3}) \rightarrow\ \mathrm{c}\ \mathrm{EVM} \rightarrow\ +P_c$$

5. An addition to tradeoffs 1. and 3. for the digital baseband, including an additional decrease in power consumption by reducing the resolution of the ADC:

$$(-\,\text{wordlength},\ -\,\text{ADC resolution (ENOB/dynamic range)}) \rightarrow -\,\text{switching activity} \rightarrow\ +\,\mathrm{EVM} \rightarrow (\ -P_{c,\,ADC}\ ,\ -P_{c,\,digital\ baseband}\ )$$

6. A general tradeoff regarding "clean RF" and "dirty RF" digital compensation techniques:

$$+\,\text{"clean RF" compensation quality} \rightarrow\ -\,\text{"dirty RF" compensation quality} \rightarrow\ \mathrm{c}\ \mathrm{EVM} \rightarrow (\ +P_{c,\,clean\,RF}\ ,\ -P_{c,\,clean\,RF}\ )$$

The qualities can be traded with the ultimate goal of achieving overall savings in power consumption.

7. A generel tradeoff regarding digital compensation and RF impairment sources:

$$+\text{ digital compensation quality} \rightarrow +\text{ RF distortion} \rightarrow \text{ c EVM} \rightarrow \left(\begin{matrix} +P_{c,compensation} \\ -P_{c,block} \end{matrix} \right),$$

Digital compensation makes sense as long as $-P_{c,block} > +P_{c,compensation}$.

6 Comparison of fixed and channel-adaptive approaches in radio receiver design

6.1 Introduction

This chapter will present two simple designs of the analog and mixed-signal part of a radio receiver that could be used in LTE devices. The goal of this simplistic analysis is not to propose actual receiver designs, but merely to show the difference between the two design approaches.

As the focus of this analysis is not on the actual receiver design that will be conformant with LTE specifications, several assumptions regarding the design and analysis have been made for both fixed and adaptive designs:

- The environment is interference-free (no wideband interference or blockers);
- The channel fading is slow and flat;
- Channel quality estimation and signal strength measurements are perfect;
- In the adaptive design, the switching between different values of circuit parameters is perfect.
- Only one receive antenna (and correspondingly, one receiver chain) are considered.

With all of these assumptions, the main sources of performance degradation are noise and compression caused by the received signal power, which is time-variant, and nonlinearities. Additionally, the designs use blocks described in various research papers: only the measured parameters of the blocks are used, and possible interfacing issues between the blocks are not taken into concern.

Both designs are based on a fixed channel bandwidth of 3 MHz (one of the standard LTE channel bandwidths).

Although not conformant with the entire set of LTE specifications, the receiver designs presented here should support the performance (channel quality) frame needed for proper functioning of LTE, taking into account the assumptions listed above. This frame will serve as the basis of comparison of fixed and adaptive designs.

The operation of LTE is based on switching between modulation and coding schemes (MCS) that support a range of throughputs; the switching is based on the current channel quality. If channel quality for a flat fading environment is measured by SNDR (where the effects of the receiver distortion are included in the channel model), then a higher SNDR means that an MCS with a larger throughput can be transmitted. LTE uses a set of 15 MCS, corresponding to 15 different channel quality indicators (CQI) [55]. The SNDR ranges corresponding to different MCSs can be determined from link-level baseband simulations of the LTE system.

A set of these link–level simulations was performed, using the link-level simulator developed at TU Vienna [56]. An AWGN (flat) channel was assumed, the channel bandwidth was set to 3 MHz and the maximum number of Hybrid Automatic Repeat Requests (HARQ) was set to 3. The set of obtained SNDR limit values (the value of SNDR that gives the 90% throughput value for the current MCS) is given in Table 4.

CQI No.	90% throughput SNDR [dB]
1	-7.2
2	-5.4
3	-3.2
4	-1.4
5	0.6
6	2.6
7	4.6
8	6.4
9	8.4
10	10.6
11	12.4
12	14.2
13	16
14	18
15	23.4

Table 4: The SNDR limit values for 15 CQIs for an LTE system with 3 MHz bandwidth, AWGN channel and maximum 3 HARQ

These SNDR limit values, coupled with the input power level, give the complete set of performance constraints needed for receiver design.

6.2 Fixed design

The fixed design follows the basic receiver chain outline presented in 2.2.4:

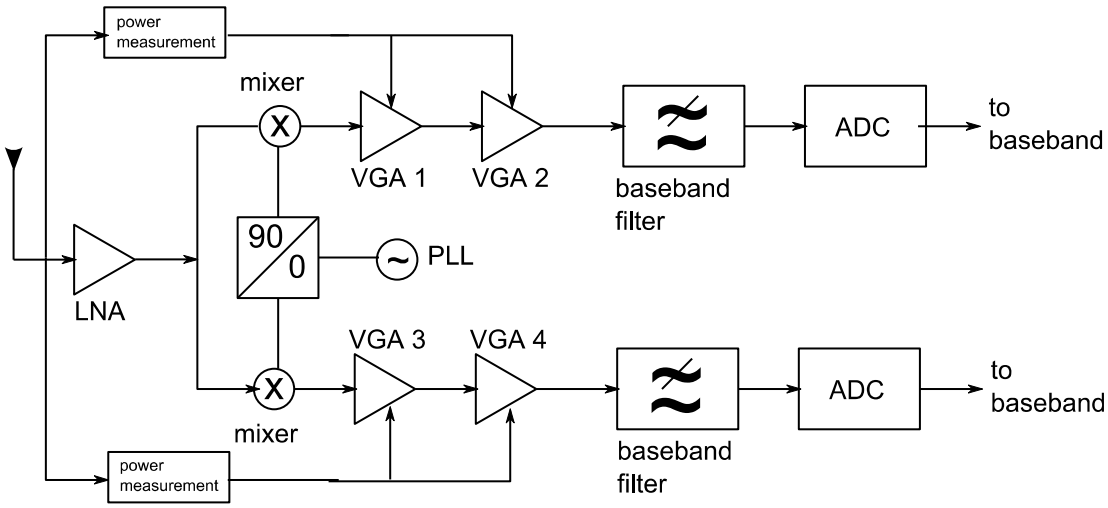

Figure 47: Block diagram of the receiver chain

We start the description of the design by introducing the block designs used.

6.2.1 Receiver block designs

6.2.1.1 LNA

The LNA design is based on the general feedback design from [22] that has already been analyzed in Chapter 3. The analytical expressions that model the LNA will be restated here for convenience. In the fixed design, it is decided that the LNA has a fixed gain and fixed NF for input powers smaller than -70 dBm; at -70 dBm, the LNA shuts down in order not to compress the subsequent stages of the chain, with NF now being 3 dB as LNA is substituted by a resistor. The complete effect of this switching will be described later in more detail.

The design of the LNA is a 4-step process, which begins with choosing the value of input resistance R_S (the natural choice is $50\,\Omega$) and nominal LNA gain and NF (G = 36 dB and NF = 1.2 dB).

- **Step 1 - determining the R_P.** By careful analysis of the LNA circuit, it is observed that the maximum gain that can be physically supported is twice the gain of a CG LNA with no feedback:

$$G_{max}=2\cdot\frac{R_P}{2R_S}=\frac{R_P}{R_S}\quad .$$

With $R_S=50\,\Omega$ and $G_{max}=10^{(36/20)}=63.1$, the needed $R_P=3154.8\,\Omega$.

- **Step 2 - determining the corresponding F_2.** Taking into account the physical limitations of the LNA circuit, we read from the formula for the voltage gain

$$G=\frac{R_P}{2R_S(1-F_2R_P)}$$

that $1-F_{2\max}R_P=0.5$. From this, $F_2=F_{2\max}=1.585\cdot10^{-4}$.

(The physical limitations of the circuit also imply that the second condition given by (3.2) needs to be restated as $R_P F_2 < 0.5$).

- **Step 3 - determining F_1 from the NF condition.** With NF being calculated as

$$NF = 1 + \gamma\left(1 - \frac{R_P F_1}{R_S} - F_2 R_P\right) + \frac{R_S}{R_P}\left(2 - \frac{R_P F_1}{R_S} - F_2 R_P\right)^2 ,$$

The feedback coefficient F_1 can be found by solving a quadratic equation and seeing that one of the solutions of the equation satisfies the first condition in (3.2):

$$\frac{R_P}{R_S} F_1 + R_P F_2 < 1 \Rightarrow \frac{R_P}{R_S} F_1 < 0.5 \Rightarrow F_1 < \frac{R_S}{R_P} \cdot 0.5 ,$$

where we took into account that $R_P F_2 = R_P F_{2\max} = 0.5$. By following the described procedure, it is found that $F_1 = 0.001$.

- **Step 4 - calculating other important parameters of the LNA block.** With known R_S , R_P , F_1 and F_2 , the corresponding IIP3 is found from

$$IIP3_{F_1} = \frac{16 V_{OV}^2 (2 + \theta V_{OV})^2}{3 R_S}\left|1 + \frac{F_1 g_m R_P}{1 + R_S g_m}\right|^3 , \quad g_m = \frac{1}{R_S - (F_1 + F_2 R_S) R_P}$$

and is found to be IIP3 = 6.59 dBm, with $\theta = 0.9 V^{-1}$ and $V_{OV} = 93 mV$ (needed for the value of IIP3 for a CG LNA without feedback, the "native CG LNA", to be equal to 6 dBm) . Current consumption is calculated as

$$I_D = \frac{g_m V_{OV}}{2} = 2.13 mA .$$

Table 4 gives the summary of LNA circuit and block parameters:

Parameter	Value
Gain	36 dB
NF	1.2 dB
R_S	50 Ω
R_P	3154.8 Ω
F_1	0.001
F_2	$1.585 \cdot 10^{-4}$
IIP3	6.59 dBm
Current consumption (I_D)	2.13 mA

Table 5: LNA parameters

6.2.1.2 Frequency synthesizer

The PLL parameters are taken from the ADPLL design presented in [57].

Parameter	Value
Current consumption	30 mA
EVM	1.02 %

Table 6: PLL parameters

6.2.1.3 Mixer

The parameters of the passive mixer were determined by analytical expressions and simulation results from [52]. A 25% duty cycle was chosen.

- Conversion gain can be analytically determined as [52]

$$G = \frac{2}{\pi} \sin\left(\frac{\pi \cdot \Delta T}{T}\right) \cdot \frac{T}{\Delta T} \quad , \tag{6.1}$$

  where $\Delta T / T$ is the duty cycle. It is found to be 5.1 dB.

- NF is found as [52]

$$NF = 1 + \sum_{n=2}^{4} \left[\frac{\sin\left(\frac{n \Delta T}{T} \pi\right)}{n \sin\left(\frac{\Delta T}{T} \pi\right)} \right]^2 + \frac{\pi^2 \Delta T}{4 T 0.05 \left[\sin\left(\frac{\Delta T}{T} \pi\right) \right]^2} \tag{6.2}$$

  and is equal to 14.2 dB.

There was no analytical expression for the IIP3 but a measured value of 5 dBm was taken as a possible value.

Parameter	Value
Gain	5.1 dB
NF	14.2 dB
IIP3	5 dBm
Current consumption	0 mA (passive mixer doesn't have a DC power consumption)

Table 7: Passive mixer parameters

6.2.1.4 VGA

The VGA design uses the same feedback design as the LNA, but with a significant difference that it allows for the gain to be tunable (easily implemented by tuning F_2). It has been observed that the presented theoretical framework doesn't give credible results for gains exceeding

40 dB. Therefore, for a full support of the wide dynamic range of input signal power, it is decided to use a cascade of two VGAs with maximum gain of 36 dB. The minimum supported gain is 5.2 dB. The value of feedback factor F_1 was chosen to be equal to -0.02. The 4-step procedure of LNA design was followed again, with the additional substep of finding a minimal F_2 corresponding to the minimal gain. As the gain changes, so does current consumption and NF. The summary of LNA parameters is given in Table 7, and the values of parameters are additionaly plotted in Figure 48.

Parameter	Value(s)
Gain (minimum, maximum)	(5.2 dB, 36 dB)
NF (corresponding to minimum gain, corresponding to maximum gain)	(12.9 dB, 3.6 dB)
R_S	50 Ω
R_P	3154.8 Ω
F_1	-0.02
F_2 (corresponding to minimum gain, corresponding to maximum gain)	(-0.0052, $1.585 \cdot 10^{-4}$)
IIP3 (corresponding to minimum gain, corresponding to maximum gain)	(5 dBm, -1.93 dBm)
Current consumption (corresponding to minimum gain, corresponding to maximum gain)	(0.05 mA, 0.53 mA)

Table 8: VGA parameters

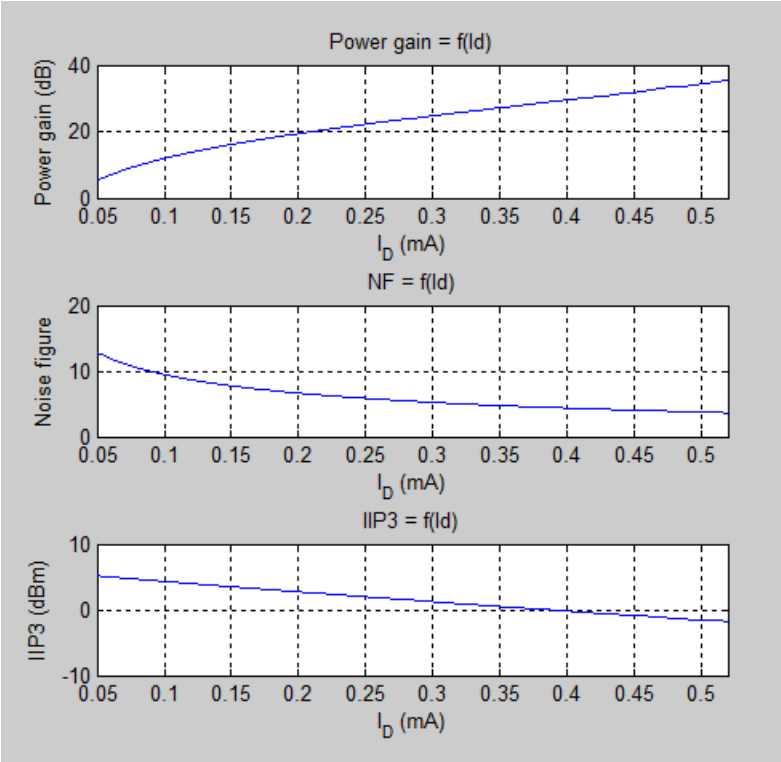

Figure 48: VGA parameters as functions of current consumption

6.2.1.5 Channel select filter

The parameters of the baseband filter are chosen from [53].

Parameter	Value
Gain (in-band)	6 dB
NF (measured on a 50Ω resistor)	32.59 dB
IIP3	21.5 dBm
Current consumption	2.83 mA

Table 9: Baseband filter parameters

6.2.1.6 ADC

The continuous-time SD ADC parameters are taken from the design given in [54].

Parameter	Value
DR	84.6 dB
ENOB (from DR)	13.76
Optimal IBO (from ENOB)	14.8 dB
Current consumption (for the 2.5 MHz setting)	1.58 mA
EVM (optimal)	0.02%

Table 10: ADC parameters

6.2.2 Receiver gain and noise/distortion budgets

The gain budget of the receiver is a function of time since the input signal power is time-variant. The total gain of the receiver changes so as to achieve that the power at the input of the ADC is 0 dBm (value selected according to a rule-of-thumb stated in [1]). Therefore, the gain budget can be represented by (all gain values are in dB, and power values in dBm)

$$P_{\text{in}}+G_{LNA}+G_{mix}+G_{VGA1}+G_{VGA2}+G_{filt}=0\,dBm \quad . \tag{6.3}$$

Since only the gain of the VGAs is tunable, their joint gain is determined as

$$G_{VGA1}+G_{VGA2}=-P_{\text{in}}-\left(G_{LNA}+G_{mix}+G_{filt}\right)=-P_{\text{in}}-46.1\left(dB\right) \tag{6.4}$$

In the fixed design, the splitting of gain between VGAs is done simply by assigning each VGA one half of the needed gain.

In order to determine the noise budget, we start with the thermal noise floor. As per LTE recommendations, ([55]), the noise floor for the 3 MHz bandwidth is determined as

$$noise\ floor=10\log\left(k\cdot T\cdot 12\cdot 180\,kHz\right)=-110.48\,dBm \quad . \tag{6.5}$$

The sensitivity level (lowest possible input power) is determined in an iterative process: first, the total noise figure for the proposed chain, with $G_{VGA1}=G_{VGA2}=36\,dB$ is determined, and

found to be equal to 1.22 dB. The sensitivity level is then found as

$$P_{sens} = noise\ floor + NF_{total} + SNDR_{min} \quad , \tag{6.6}$$

with $SNDR_{min}$ being the SNDR value needed to support a 95% throughput for the modulation and coding scheme (MCS) with the lowest throughput. From link level calculations, it is determined that $SNDR_{min} = -7.2\,dB$ and the corresponding $P_{sens} = -116.4\,dBm$. Going back to the sum of VGA gains in (6.4), it is found that for this input power we need $G_{VGA1} = G_{VGA2} = 35.15\,dB$. This is close enough to our initial guess of VGA gain value, so we keep the calculated sensitivity value of -116.4 dBm as final. The whole receiver chain thus needs to cover the input power values ranging from -116.4 dBm to -30 dBm, which is considered a rule-of-thumb upper bound of input power in receiver design [1].

The plot of SNDR as a function of input power is shown in Figure 49.

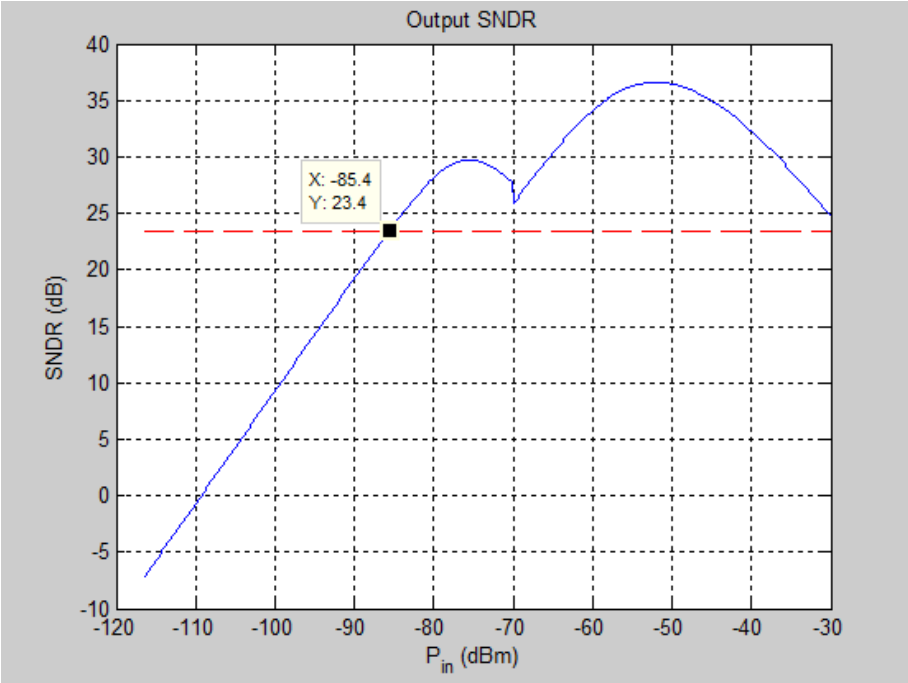

Figure 49: SNDR at the output of the receiver chain for the fixed design

As it can be seen, the increase of SNDR due to the increase of input power level is linear in dB until approximately $P_{in} = -80\,dBm$. In this first range of input power levels, the thermal noise predominantly determines the SNDR and the distortion due to nonlinearities is not pronounced. From -80 dBm to -70 dBm input power, the nonlinearity starts affecting the SNDR; at this point, the receiver is already working at the highest-throughput MCS 15 (the SNDR threshold of this MCS being 23.4 dB and shown on the plot with the horizontal dashed line). At -70 dBm, the LNA shuts down, preventing further nonlinearity distortion in the back of the receiver (which would eventually drive the receiver below the threshold of MCS 15 to lower MCSs). As the nonlinearity conditions are now relaxed, the SNDR again increases linearly in dBm with the increase in P_{in} from -70 dBm to approximately -60 dBm. Then the nonlinearity distortion again starts affecting the SNDR, and it drops, finishing at 25 dB at the maximum input power of -30 dBm. It is therefore shown that this setup guarantees that the receiver will work using the most demanding MCS in spite of the pronounced effects of nonlinearity.

For a full description of noise and distortion behaviour of the receiver, the plots of NF and

EVM (joint effect of nonlinearity, phase noise, quantization and clipping) are shown in Figure 50 and Figure 51.

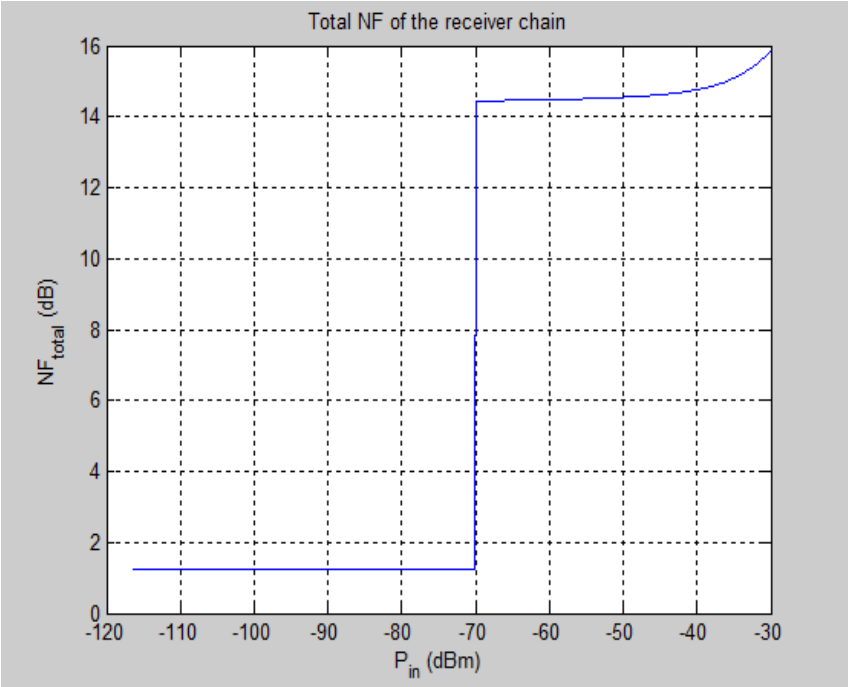

Figure 50: NF of the receiver chain for the fixed design

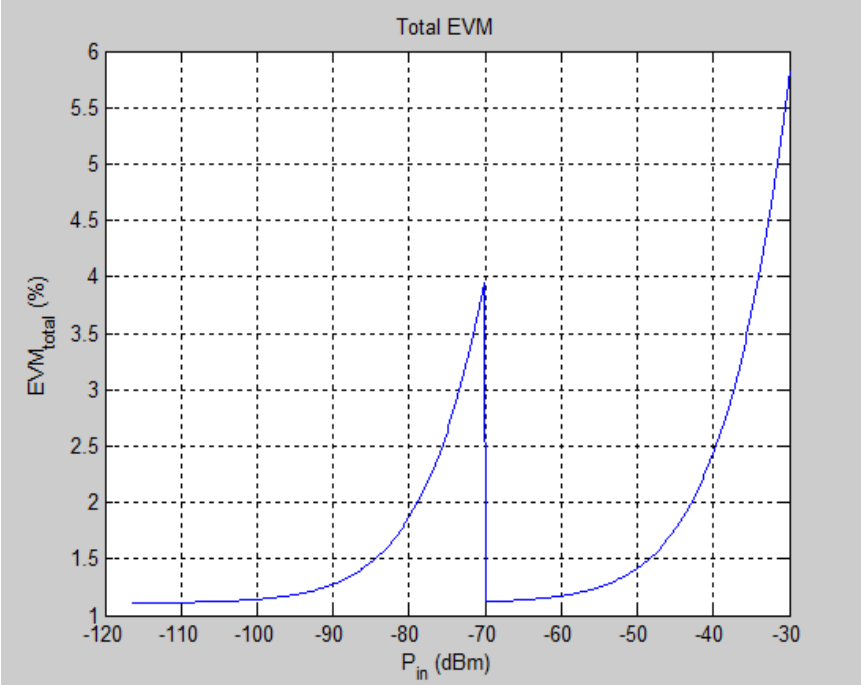

Figure 51: EVM of the receiver chain for the fixed design

Finally, the current consumption of the receiver chain is given in Figure 52.

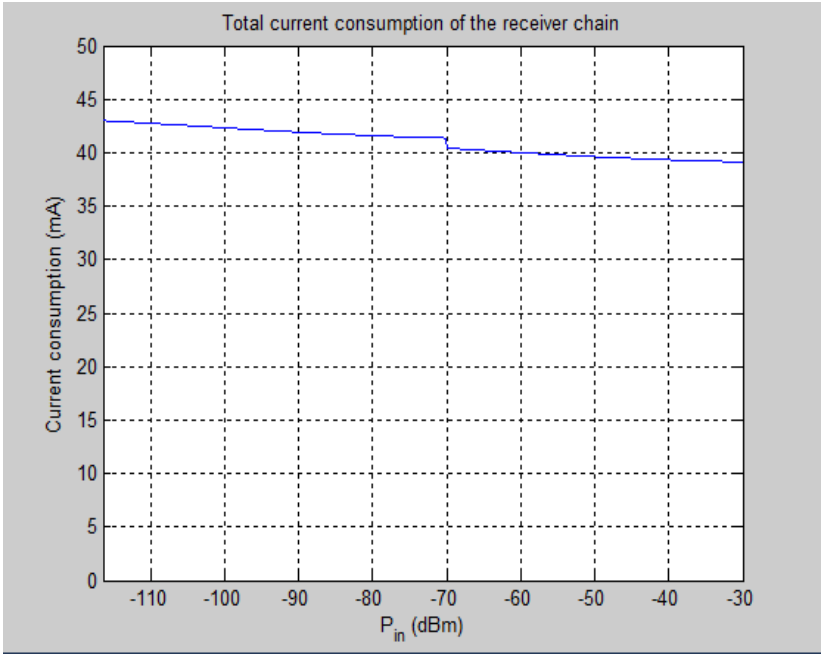

Figure 52: Current consumption of the receiver chain for the fixed design

It is useful to remind that a large part of this current consumption (30 mA) goes to the PLL. It can be observed that the current consumption in the fixed design decreases with an increase in input power because the gain of the two VGAs decreases.

6.3 Channel-adaptive design

The main motivation for the channel-adaptive design is reducing the performance margins with the goal of reducing power consumption. If, at certain channel conditions, further degradation of channel conditions does not reduce the performance quality (or rather it reduces it, but to a level that is still acceptable), then this degradation can be induced *intentionally* if it will result in power savings.

This concept is illustrated in Figure 53.

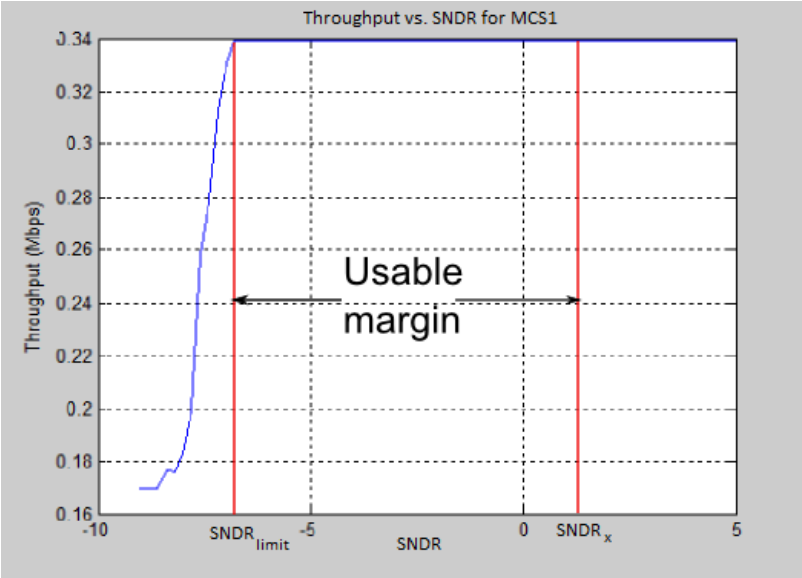

Figure 53: The concept of performance margin

The simulated throughput comes from link-level simulations of the LTE system for the modulation and coding scheme (MCS) 1 in AWGN, with maximum 3 HARQs and with a channel bandwidth of 3 MHz. It can be seen that the throughput "flattens out" at its maximum value after a certain $SNDR_{limit}$. If the SNDR at the output of the receiver (input of the baseband decoder) is at a certain $SNDR_x$, the SNDR can be reduced down to $SNDR_{limit}$ without affecting the throughput. As seen in previous chapters, a reduction in quality (increase of thermal noise, phase noise, clipping distortion, etc.) always yields power savings. Therefore, certain savings in power consumption are to be expected when using the described concept.

The concept can be extended to a system that uses several MCSs and switches between them according to present channel quality (with the goal of maximizing throughput) or following user demands. We will focus only on the maximum throughput approach here.

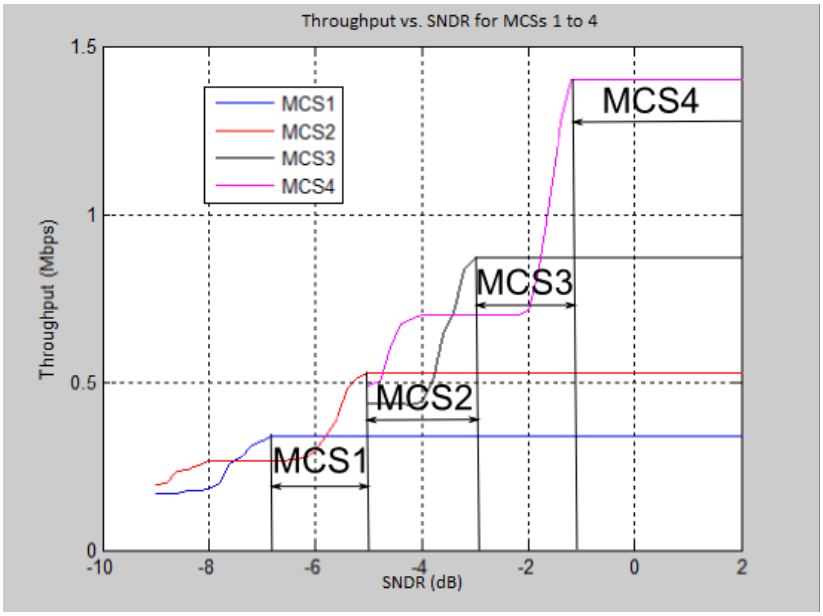

Figure 54: Performance margins in a system that uses multiple MCSs

We ilustrate the concept on just a subset of four MCSs, for clarity. Every MCS is mapped to a certain SNDR range, bounded from below by the $SNDR_{limit}$ for the current MCS and from above by the $SNDR_{limit}$ for the next MCS (that provides a larger throughput). For a given $SNDR_x$, we can always allow a certain SNDR degradation so SNDR degrades down to $SNDR_{limit}$ for the current MCS. This principle can be applied to all MCSs. This results in a "staircase" curve for the output SNDR, as it can be seen in Figure 55, comparing the SNDR curves for fixed and adaptive designs.

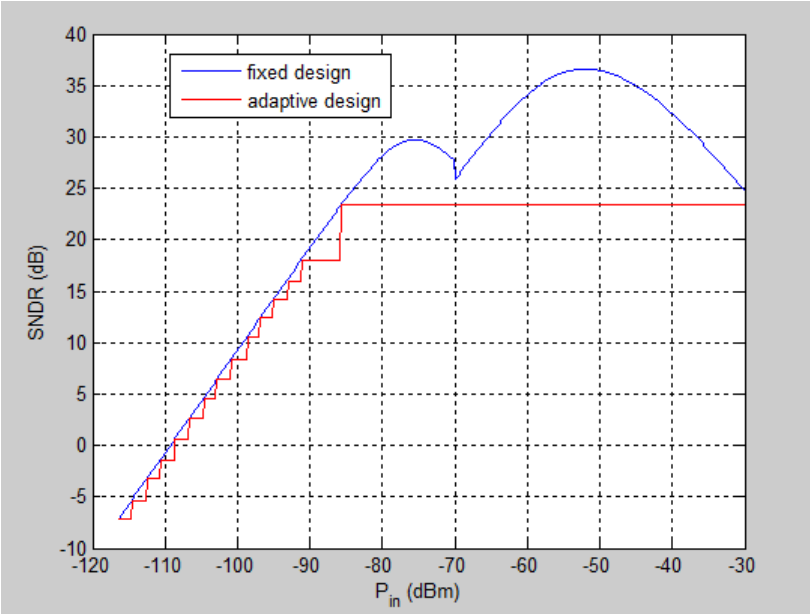

Figure 55: Comparison of output SNDR in fixed and adaptive designs

We can now formulate the adaptation strategy (applied to a flat, slowly faded channel):

1. The information about received signal power is collected. It can come from a power meter needed for adjusting the VGAs;
2. With knowledge of the received signal power, previously determined minimum SNDR for each input power point (the staircase curve in Figure 55) and precise knowledge of block parameters (*i.e.* how each parameter affects the overall SNDR), a combination of block parameter values is determined that satisfies the needed gain budget, provides SNDR larger or equal to the minimum SNDR and yields minimum power consumption (this is conveniently done offline);
3. The optimal combination of block parameters is applied to the tunable blocks; there is no throughput loss and the the overall power consumption is minimized.

If implemented in an actual LTE receiver, this simple strategy doesn't require any additional overhead in terms of power consumption, area, etc.: it uses the power measurement from a block that is present in the "fixed" design also (and that is actually required for proper operation of the fixed design).

If we establish the time index *i* to denote different (discrete) values of input power, then the optimal combination of block parameters $\left(\alpha_{1,opt}^{(i)}, \alpha_{2,opt}^{(i)}, \ldots \alpha_{K,opt}^{(i)}\right)$ can be determined as a solution of the optimization problem

$$\begin{aligned} &\text{minimize} && I^{(i)}(\alpha_1^{(i)}, \alpha_2^{(i)}, \ldots \alpha_K^{(i)}) \\ &\text{subject to} && SNDR^{(i)}(\alpha_1^{(i)}, \alpha_2^{(i)}, \ldots \alpha_K^{(i)}, P_{\text{in}}^{(i)}) \geq SNDR_{limit}^{(i)} \end{aligned} \qquad (6.7)$$

where $I^{(i)}$ is the current consumption at input power index *i*. Optimization problem (6.7) is a special case of the general problem (1.2). Problem (6.7) is solved for every *i* and the optimal combination of block parameters is saved in a lookup table; adaptation algorithm then simply consists of taking the measured power and applying the corresponding combination of block parameteres from the table.

The block diagram of the channel-adaptive receiver is shown in Figure 56 (only one branch shown for clarity).

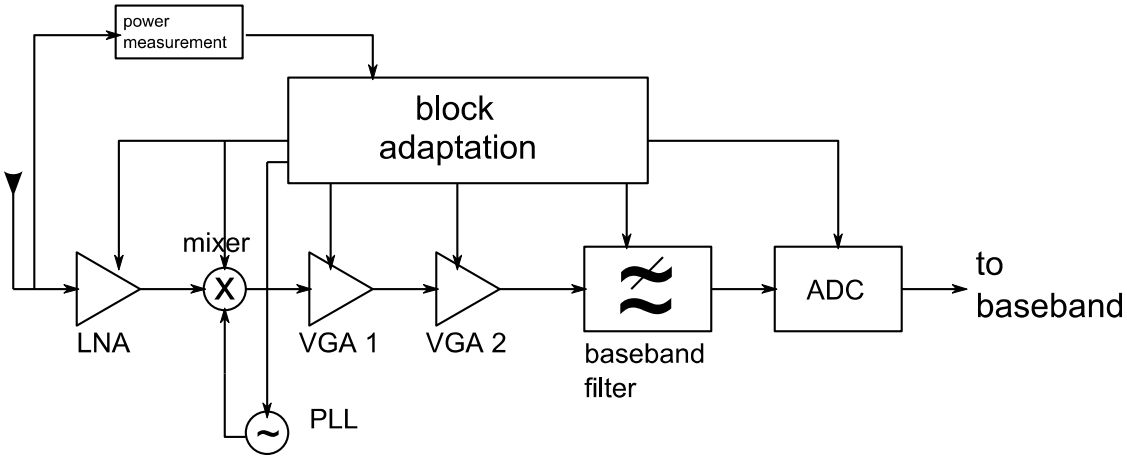

Figure 56: The channel-adaptive receiver design

6.3.1 Receiver block designs

The designs of the PLL, mixer, filter and ADC are retained in the adaptive design. What is changed are the properties of the LNA and VGAs: generally, both gain and NF for LNA and VGAs can be tuned according to channel conditions. The overall gain, however, still needs to compensate for the input power so as to keep a constant input power to the ADC. This puts a constraint on values of G_{LNA}, G_{VGA1} and G_{VGA2}:

$$G_{LNA} + G_{VGA1} + G_{VGA2} = -P_{\text{in}} - (G_{mix} + G_{filt}) = -P_{\text{in}} - 11.1(dB) \quad . \qquad (6.8)$$

6.3.1.1 LNA

The parameters F_1 and F_2 of the LNA are independently tunable, but the range of F_1 is determined by the value of F_2 (gain) because the minimum NF has to be supported for every gain. Current consumption is constant for a particular value of the NF, regardless of the gain; the smallest current consumption corresponds to the highest NF. Ranges of LNA parameter values are given in Table 10.

Parameter	Value range
Gain	(5.2 dB, 36 dB)
NF	(1.2 dB, 13.9 dB)
Current consumption (highest NF, lowest NF)	(41 μA , 2.15 mA)
IIP3	(G = 36 dB, NF = 13.9 dB): -29.83 dBm (G = 36 dB, NF = 1.2): 6.64 dBm (G = 5.2dB, NF = 13.9 dB): 2.8 dBm (G = 5.2 dB, NF = 1.2 dB): 38.68 dBm

Table 11: LNA parameters for the adaptive design

6.3.1.2 VGA

The design of the VGA is closely related to the LNA, but with a larger minimum NF and thus a smaller range of current consumption values.

Parameter	Value range
Gain	(5.2dB, 36 dB)
NF	(2 dB, 14.8 dB)
Current consumption (highest NF, lowest NF)	(35.7 μA , 1.18 mA)
IIP3	(G = 36 dB, NF = 14.8 dB): -31.64 dBm (G = 36 dB, NF = 2): 3.76dBm (G = 5.2 dB, NF = 14.8 dB): 1 dBm (G = 5.2dB, NF = 2 dB): 35.93 dBm

Table 12: VGA parameters for the adaptive design

6.3.2 Calculation and analysis of optimal block parameters

Using the blocks described above, optimal values of LNA and VGA gains and NFs/IIP3s, represented by feedback coefficients F_1 and F_2 are determined for input power levels from -116.4 to -30 dBm, using 0.2 dB steps, by solving the optimization problem (6.7). SNDR is found from (2.78), and the total EVM needed for determining the SNDR is found by using (2.79). Limiting SNDR values for each $P_{\text{in}}^{(i)}$ are determined by observing the SNDR values for $P_{\text{in}}^{(i)}$ that correspond to the "switching" points from Table 4 and keeping these SNDR values throughout the P_{in} range supporting one MCS. This is how the staircase curve from Figure 55 is obtained, and this curve represents $SNDR_{limit}$ values for all $P_{\text{in}}^{(i)}$.

The optimization problem is 6 – dimensional, and it was solved by a sequential search over all dimensions (and using some observed functional properties of the SNDR to make the search less computationally intensive). In this way, an optimized power consumption characteristic was obtained, and it is shown in Figure 57.

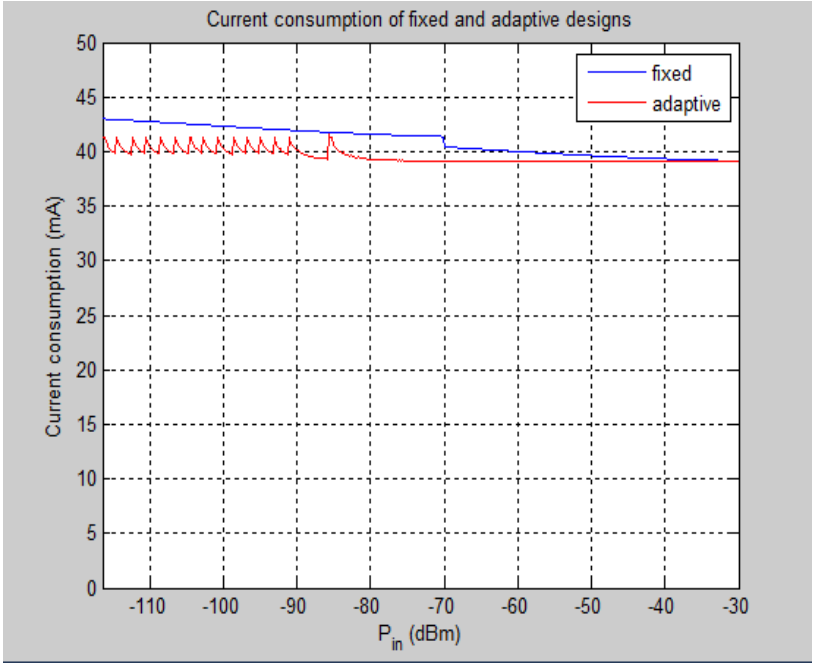

Figure 57: Comparison of current consumptions of fixed and channel-adaptive designs

The adaptive receiver introduces a slight improvement of the current consumption. The improvement in percents for each input power point is given in Figure 58.

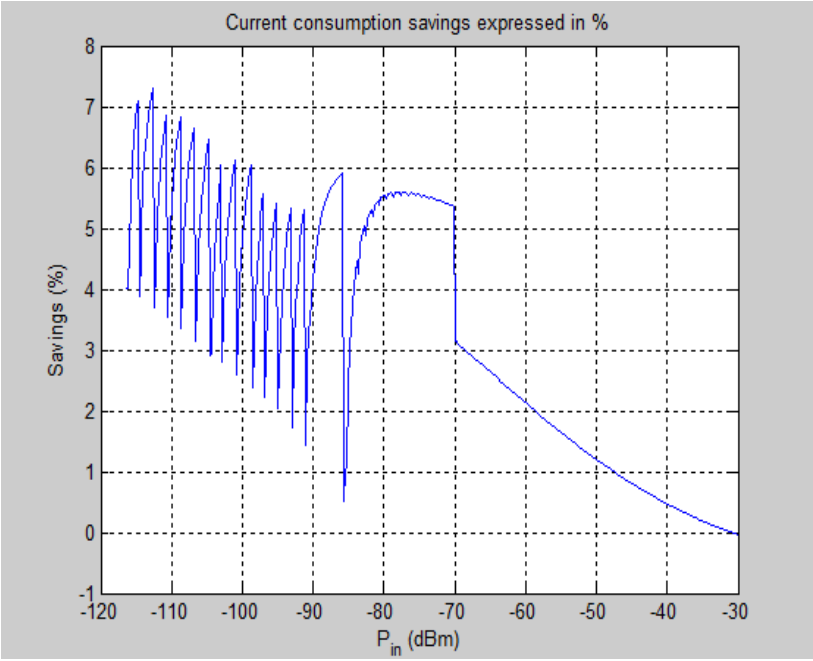

Figure 58: Savings introduced by using a channel-adaptive receiver, expressed in percents

It can be clearly observed how the margin between the worst-case and "sufficient" SNDRs is used to reduce power consumption; an increase of this margin is followed by the increase in current consumption savings.

Although the power consumption savings obtained here might not seem impressive, one has to be reminded that the observed design considers only one antenna with its corresponding receiver

chain, where the current consumption is dominated by the PLL. In multiantenna systems, the receiver is made up out of several receiver chains, and then the current consumption of the PLL takes up a smaller part of the overall consumption; as a consequence, an increase in percentage savings between fixed and adaptive designs is to be expected. Testing this hypothesis might be a subject of further research.

In addition to the current consumption, it is interesting to observe how other block and system parameters follow the changes in input power. First, we analyze the SNDR values obtained with solutions of (6.7).

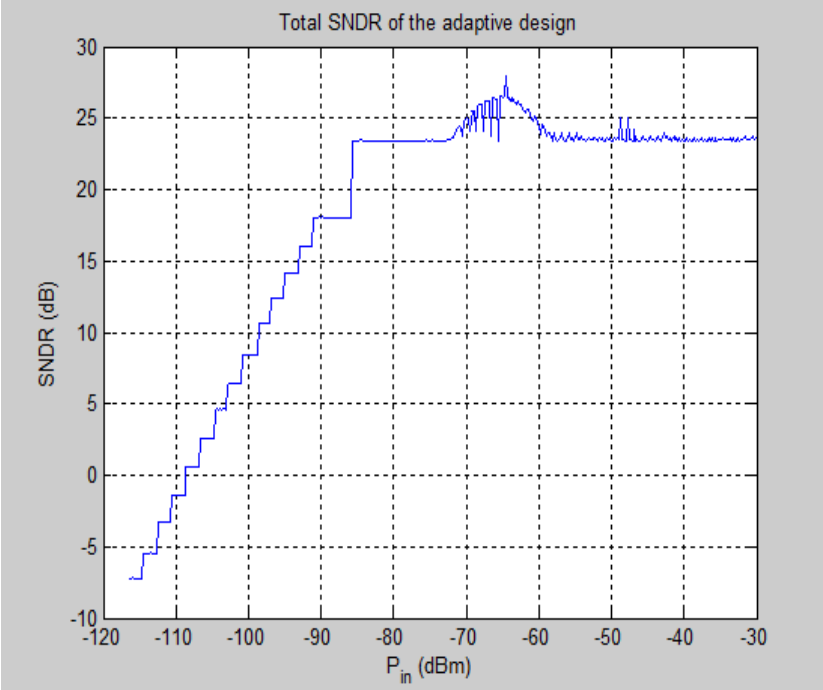

Figure 59: SNDR values corresponding to optimum block parameters

It is observed that these values are almost always equal to the limiting value (although they need not be). This confirms the intuitive assumption that the solution with the minimum SNDR (minimum allowed quality) is always the most power-efficient one.

The next thing that is analyzed is the total EVM and individual EVM contributions from all the blocks. It is observed that the total EVM is dominated by the EVM stemming from the nonlinearity distortion created at the second VGA. This is shown in Figure 60 (curves overlap completely until the -100 dBm point is reached).

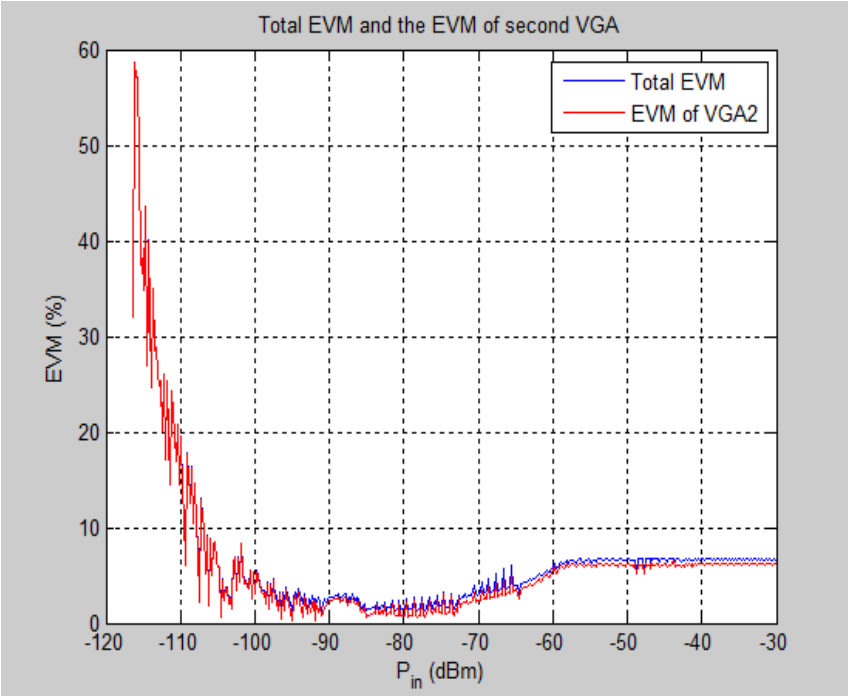

Figure 60: Total EVM and the EVM of nonlinearity for the second VGA in the adaptive receiver design

Another important thing to observe is the behaviour of the noise figure value for the LNA and VGAs, which is tunable in the adaptive design.

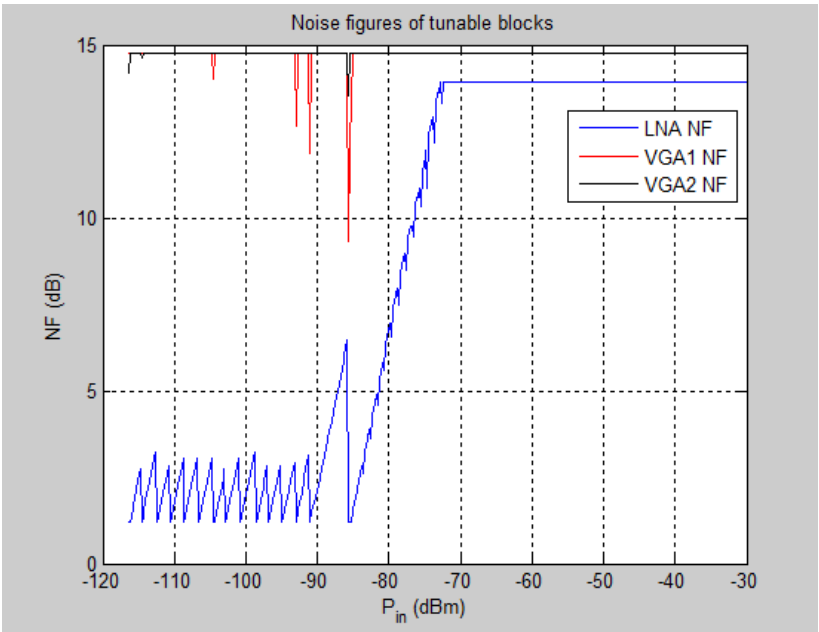

Figure 61: Noise figures of LNA and the two VGAs

Interestingly, the value of NF in the two VGAs remains at its largest value (the least power-consuming) for almost all points. At the same time, the NF of the LNA "breathes" simultaneously with the changes in the SNDR margin. It can then be concluded that the optimal receiver design allows the blocks in the back of the chain to be noisy, as this doesn't change the quality significantly. This is due to the properties of the overall noise calculated by (2.3); the gain of front blocks supresses the noise coming from the back of the chain.

Finally, the behaviour of gain and IIP3 of tunable blocks can be analyzed side by side.

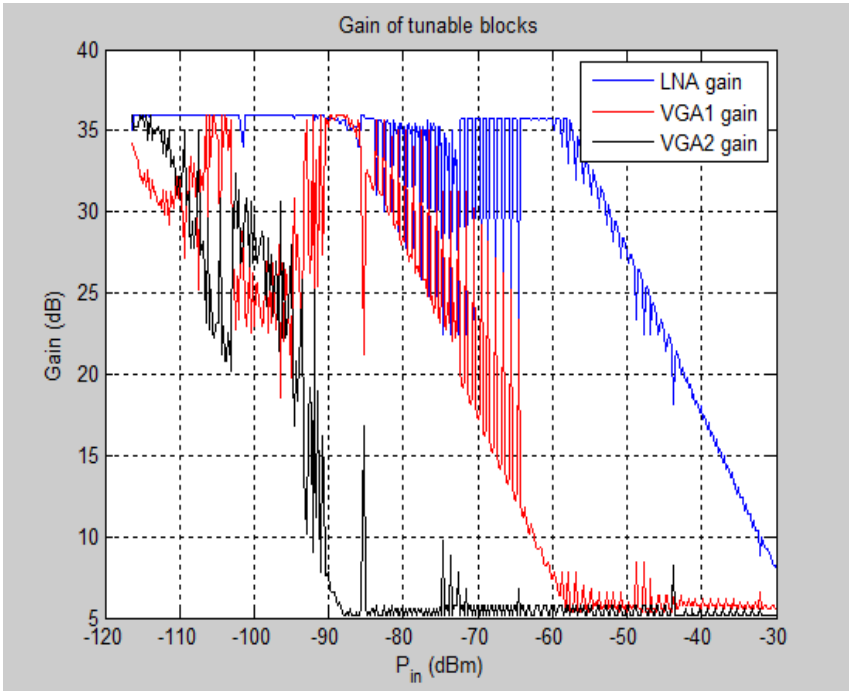

Figure 62: Gains of LNA and the two VGAs

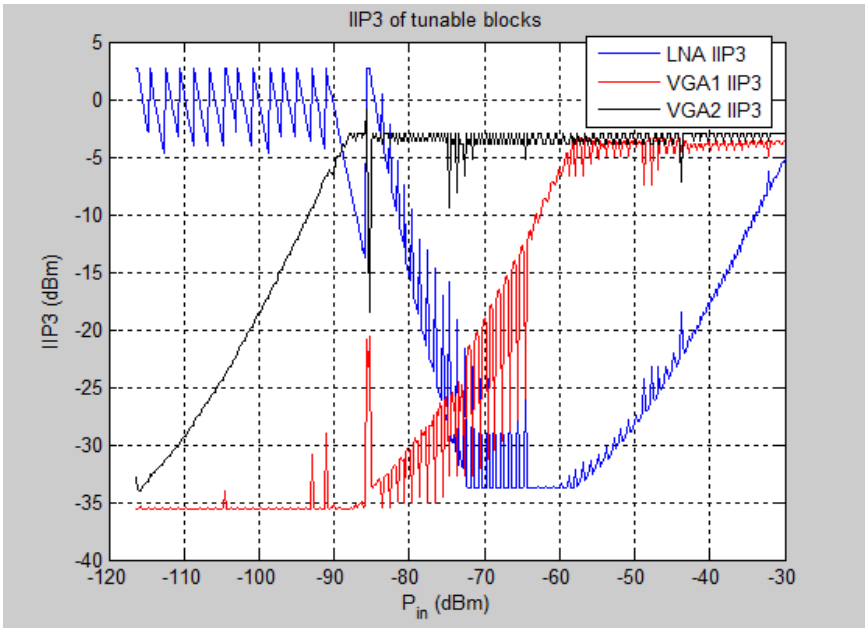

Figure 63: IIP3s of LNA and the two VGAs

It is observed that the decrease in gain, while NF is constant, always results in an increase of IIP3. If we focus the analysis just on VGA2, we can see how the decrease in gain of this block (implying a larger input power to it, since the gain of the filter is fixed) is closely followed by a steady increase in IIP3, inherent to the block. This tradeoff of the block gain and IIP3 helps to control the value of the EVM contribution coming from the block, without additional increase in power consumption. It can be concluded that, if this particular amplifier design is used to

implement the VGAs, the optimum setting is to keep the noise of the amplifier high and constant (resulting in a very low power consumption) and control the gain; the necessary increase in IIP3 will come as a by-product of the gain increase. This implies that the feedback CG amplifier model, initially used for LNAs, can be conveniently used to implement very low-power VGAs.

7 Conclusions and future work

Continuous development of mobile systems asks for a continuous improvement of mobile devices. The receivers should support increasing throughputs, while at the same time their power consumption should not increase drastically, due to battery limitations; in other words, the goal is to design highly power – efficient receivers.

One way of increasing power efficiency is to design a receiver that will save on power whenever this is possible, that is, whenever channel conditions and/or user demand for throughput permit it. If, for instance, wireless channel conditions are such that intentionally introducing degradation into the channel would not decrease the throughput, then the receiver can be designed to introduce intentional degradation. Due to inherent properties of electronic circuits, an immediate consequence would be the decrease of power consumption of the receiver.

In order to be able to determine the right values of receiver block parameters that will introduce the right amount of deliberate distortion and, at the same time, yield savings in power, it is important to know two things: first, how the power consumption of the block changes with these changing parameters, and second, how does the changing of the parameters affect the overall performance. In this work, this "double characterization" of blocks is done by jointly analyzing the power – performance tradeoffs due to the tuning of the block parameters, and a summarized list of characteristic tradeoffs is given.

To be able to quantitatively assess the impact of tuning a block parameter on the overall receiver performance, a proper model that incorporates all the diverse RF impairments is needed. It is shown that the Error vector magnitude (EVM) can be used to model the influence of block parameters and environment variables (such as input power) on the overall performance; using certain assumptions, the EVM can provide a relatively simple (and still sufficiently precise) analytical model of signal distortion for the entire receiver chain. The information about thermal noise and distortion due to other RF impairments can then be combined into a joint indicator of the channel quality – the SNDR.

The EVM/SNDR – based framework is then put into practical use in the design of a radio receiver. By analyzing the LTE system using 15 modulation and coding schemes (MCSs), it was observed that for each MCS, a certain degradation of the SNDR can be allowed; this degradation doesn't affect the throughput and brings certain power savings. The information about the current input power, the SNDR achieved by the fixed receiver design and the allowed degradation of the SNDR are combined to provide a minimal SNDR value that has to be fulfilled, and it is always smaller or equal to the SNDR provided by the fixed design. Then, for each input power value, the right combination of parameters of an adaptive receiver is determined that satisfies the SNDR constraint while consuming least power. It is observed that, by adapting the system parameters in this way so that the output channel quality is not better than it is necessary, certain power consumption savings can be achieved; in a single-antenna system, assuming an interference-free environment and flat fading, these savings reach 7% and are expected to be larger in multiple antenna systems.

A large set of assumptions that simplified the modeling of the system was used in the described calculations: a flat, slow fading was assumed; the effect of narrowband blockers and wideband interference was disregarded; a very general, analytical model of feedback amplifiers was used; etc. Further work conducted on the subject must expand the modeling of power consumption and performance of the system by:

- Considering the effect of narrowband blockers and wideband interference;
- Accounting for the time and frequency selectivity of the wireless channel;
- Extending the analysis to cover multiple antenna systems;
- Considering models of nonlinearity other than the third-order polynomial one;
- Working with frequency selective nonlinearities;
- Taking into account imperfect channel estimation and equalization;
- Considering more realistic ways of input signal power measuring in real - time;
- Taking into concern system delays and finite time needed for circuit parameters to switch from one value to another;
- Including the digital part of the receiver (digital compensation, detection) in the overall power/performance model of the receiver;
- Working with actual block designs and their models.

The expanded model can finally be used in the design of an actual, implementable receiver.

Reference list

[1] Razavi, B: "RF Microelectronics", Prentice Hall, 2nd ed., 2012.

[2] Horlin, F.; Bourdoux, A.; "Digital Compensation for Analog Front-Ends: A New Approach to Wireless Transceiver Design", John Wiley and Sons, Chichester, 2008.

[3] Brajal, A.; Chouly, A.;"Compensation of Nonlinear Distortions for Orthogonal Multicarrier Schemes Using Predistortion", *Global Telecommunications Conference, 1994. GLOBECOM '94. Communications: The Global Bridge., IEEE* , vol.3, no., pp.1909-1914 vol.3, 28 Nov- 2 Dec 1994

[4] Santella, G.; Mazzenga, F.; "A hybrid analytical-simulation procedure for performance evaluation in M-QAM-OFDM schemes in presence of nonlinear distortions," *Vehicular Technology, IEEE Transactions on* , vol.47, no.1, pp.142-151, Feb 1998

[5] Dardari, D.; Tralli, V.; Vaccari, A.; "A theoretical characterization of nonlinear distortion effects in OFDM systems," *Communications, IEEE Transactions on* , vol.48, no.10, pp.1755-1764, Oct 2000

[6] Ding, L.; Zhou, G. T.; "Effects of even-order nonlinear terms on power amplifier modeling and predistortion linearization," *Vehicular Technology, IEEE Transactions on* , vol.53, no.1, pp.156-162, Jan. 2004

[7] Syrjala, V.; Valkama, M.; Tchamov, N. N.; Rinne, J.; "Phase noise modelling and mitigation techniques in ofdm communications systems," *Wireless Telecommunications Symposium, 2009. WTS 2009* , vol., no., pp.1-7, 22-24 April 2009

[8] Petrovic, D.; Rave, W.; Fettweis, G.; "Effects of Phase Noise on OFDM Systems With and Without PLL: Characterization and Compensation," *Communications, IEEE Transactions on* , vol.55, no.8, pp.1607-1616, Aug. 2007

[9] Armada, A. G.; Calvo, M.; "Phase noise and sub-carrier spacing effects on the performance of an OFDM communication system," *Communications Letters, IEEE* , vol.2, no.1, pp.11-13, Jan. 1998

[10] Armada, A. G.; "Understanding the effects of phase noise in orthogonal frequency division multiplexing (OFDM)," *Broadcasting, IEEE Transactions on* , vol.47, no.2, pp.153-159, Jun 2001

[11] 3GPP 36. 101 version 10. 2. 1 Release 10, LTE Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception

[12] Shafik, R. A.; Rahman, S.; Islam, R.; Ashraf, N. S.; "On the error vector magnitude as a performance metric and comparative analysis," *Emerging Technologies, 2006. ICET '06. International Conference on* , vol., no., pp.27-31, 13-14 Nov. 2006

[13] Mohammadi, A.; Ghannouchi, F. M.; "RF Transceiver Design for MIMO Wireless Communications", Springer-Verlag, 2012.

[14] Tubbax, J.; Come, B.; Van Der Perre, L.; Deneire, L.; Donnay, S.; Engels, M.; "Compensation of IQ imbalance in OFDM systems," *Communications, 2003. ICC '03. IEEE International Conference on* , vol.5, no., pp.3403-3407 vol.5, 11-15 May 2003

[15] Tubbax, J.; Come, B.; Van Der Perre, L.; Donnay, S.; Engels, M.; De Man, H.; Moonen, M.; "Compensation of IQ imbalance and phase noise in OFDM systems," *Wireless Communications, IEEE Transactions on* , vol.4, no.3, pp.872-877, May 2005

[16] Moose, P. H.; "A technique for orthogonal frequency division multiplexing frequency offset correction," *Communications, IEEE Transactions on* , vol.42, no.10, pp.2908-2914, Oct 1994

[17] Heung-Gyoon, R.; Ying-Shan, L.; "Phase noise analysis of the OFDM communication system by the standard frequency deviation," *Consumer Electronics, IEEE Transactions on* , vol.49, no.1, pp.41-47, Feb. 2003

[18] Bohara, V.A.; See Ho, T.; "Theoretical analysis of OFDM signals in nonlinear polynomial models," *Information, Communications & Signal Processing, 2007 6th International Conference on* , vol., no., pp.1-5, 10-13 Dec. 2007

[19] Zhao, C.; Baxley, R.J.; "Error Vector Magnitude Analysis for OFDM Systems," *Signals, Systems and Computers, 2006. ACSSC '06. Fortieth Asilomar Conference on* , vol., no., pp.1830-1834, Oct. 29 2006-Nov. 1 2006

[20] Bernhard, M.; et al.: "Analytical and Numerical Studies of Quantization Effects in Coherent Optical OFDM Transmission with 100 Gbit/s and Beyond", *ITG-Fachtagung Photonische Netze,* Leipzig, Germany, 7./8. May 2012, pp. 34-40.

[21] Razavi, B., "Design considerations for direct-conversion receivers," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on* , vol.44, no.6, pp.428-435, Jun 1997

[22] Liscidini, A.; Martini, G.; Mastantuono, D.; Castello, R., "Analysis and Design of Configurable LNAs in Feedback Common-Gate Topologies," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.55, no.8, pp.733-737, Aug. 2008

[23] Sen, S.; Banerjee, D.; Verhelst, M.; Chatterjee, A., "A Power-Scalable Channel-Adaptive Wireless Receiver Based on Built-In Orthogonally Tunable LNA," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.59, no.5, pp.946-957, May 2012

[24] Staszewski, R. B.; "Digital Deep-Submicron CMOS Frequency Synthesis for RF Wireless Applications", PhD thesis, University of Texas, Dallas, 2002

[25] Staszewski, R.B.; Leipold, D.; Chih-Ming Hung; Balsara, P.T., "TDC-based frequency synthesizer for wireless applications," *Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE*, vol., no., pp.215-218, 6-8 June 2004

[26] Staszewski, R.B.; Chih-Ming Hung; Maggio, K.; Wallberg, J.; Leipold, D.; Balsara, P.T., "All-digital phase-domain TX frequency synthesizer for Bluetooth radios in 0.13µm CMOS," *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International* , vol., no., pp.272-527 Vol.1, 15-19 Feb. 2004

[27] Staszewski, R.B.; Vemulapalli, S.; Vallur, P.; Wallberg, J.; Balsara, P.T., "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.53, no.3, pp.220-224, March 2006

[28] Ping Lu; Liscidini, A.; Andreani, P., "A 3.6 mW, 90 nm CMOS Gated-Vernier Time-to-Digital Converter With an Equivalent Resolution of 3.2 ps," *Solid-State Circuits, IEEE Journal of* , vol.47, no.7, pp.1626-1635, July 2012

[29] Vercesi, L.; Fanori, L.; De Bernardinis, F.; Liscidini, A.; Castello, R., "A Dither-Less All Digital PLL for Cellular Transmitters," *Solid-State Circuits, IEEE Journal of* , vol.47, no.8, pp.1908-1920, Aug. 2012

[30] Fanori, L.; Andreani, P., "Highly Efficient Class-C CMOS VCOs, Including a Comparison With Class-B VCOs," *Solid-State Circuits, IEEE Journal of* , vol.48, no.7, pp.1730-1740, July 2013

[31] Liscidini, A.; Fanori, L.; Andreani, P.; Castello, R., "A 36mW/9mW power-scalable DCO in 55nm CMOS for GSM/WCDMA frequency synthesizers," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International* , vol., no., pp.348-350, 19-23 Feb. 2012

[32] Voltti, M.; Koivi, T.; Tiiliharju, E., "Comparison of active and passive mixers," *Circuit Theory*

and Design, 2007. ECCTD 2007. 18th European Conference on , vol., no., pp.890-893, 27-30 Aug. 2007

[33] NacEachern, L.A.; Manku, T., "A charge-injection method for Gilbert cell biasing," *Electrical and Computer Engineering, 1998. IEEE Canadian Conference on* , vol.1, no., pp.365-368 vol.1, 24-28 May 1998

[34] Steininger, J.M., "Understanding wide-band MOS transistors," *Circuits and Devices Magazine, IEEE* , vol.6, no.3, pp.26-31, May 1990

[35] Shaeffer, D. K.; "The Design and Implementation of Low-Power CMOS Radio Receivers", PhD thesis, Stanford University, Stanford, 1998

[36] Geiger, R.L.; Sanchez-Sinencio, E., "Active filter design using operational transconductance amplifiers: A tutorial," *Circuits and Devices Magazine, IEEE* , vol.1, no.2, pp.20-32, March 1985

[37] Amir-Aslanzadeh, H.; Pankratz, E.J.; Sanchez-Sinencio, E., "A 1-V +31 dBm IIP3, Reconfigurable, Continuously Tunable, Power-Adjustable Active-RC LPF," *Solid-State Circuits, IEEE Journal of* , vol.44, no.2, pp.495-508, Feb. 2009

[38] Yoshizawa, A.; Tsividis, Y., "A Channel-Select Filter With Agile Blocker Detection and Adaptive Power Dissipation," *Solid-State Circuits, IEEE Journal of* , vol.42, no.5, pp.1090-1099, May 2007

[39] Giannini, V.; Craninckx, J.; D'Amico, S.; Baschirotto, A., "Flexible Baseband Analog Circuits for Software-Defined Radio Front-Ends," *Solid-State Circuits, IEEE Journal of* , vol.42, no.7, pp.1501-1512, July 2007

[40] Yoshizawa, A.; Tsividis, Y., "Anti-blocker design techniques for MOSFET-C filters for direct conversion receivers," *Solid-State Circuits, IEEE Journal of* , vol.37, no.3, pp.357-364, Mar 2002

[41] Quoc-Hoang Duong; Quan Le; Chang-Wan Kim; Sang-Gug Lee, "A 95-dB linear low-power variable gain amplifier," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.53, no.8, pp.1648-1657, Aug. 2006

[42] Elwan, H.; Tekin, A.; Pedrotti, K., "A Differential-Ramp Based 65 dB-Linear VGA Technique in 65 nm CMOS," *Solid-State Circuits, IEEE Journal of* , vol.44, no.9, pp.2503-2514, Sept. 2009

[43] Andreani, P.: “Nyquist-rate A/D Converters”, Lecture slides for Integrated A/D and D/A Converters course, Lund University

[44] De la Rosa, J. M.: “Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey”, *IEEE Transactions on Circuits and Systems - I: Regular Papers*, vol. 58, No. 1, January 2011.

[45] Shoaei, O.: “Continuous-Time Delta-Sigma A/D Converters for High Speed Applications”, PhD Thesis, Carleton University, 1995.

[46] Murmann, B.: “A/D Converter Trends: Power Dissipation, Scaling and Digitally Assisted Architectures”, *Proc. of IEEE Custom Integrated Circ. Conf. (CICC),* San Jose, California, USA, pp. 105–112, Sept., 2008.

[47] Murmann, B.: “Energy limits in Current A/D Converter Architectures”, Lecture slides for an IEEE SSCS Distinguished Lecture, Austin, Texas, USA, August 2012.

[48] Jaeseong Kim; Yoshizawa, S.; Miyanaga, Y., "A low-power MMSE MIMO detector using dynamic voltage wordlength scaling for 4×4 MIMO-OFDM systems," *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on* , vol., no., pp.2793-2796, 20-23 May 2012

[49] 3GPP TS 36.213 Version 8.3.0 Release 8, Physical Layer Procedures

[50] Yoshizawa, S.; Miyanaga, Y., "Use of a Variable Wordlength Technique in an OFDM Receiver to Reduce Energy Dissipation," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.55, no.9, pp.2848-2859, Oct. 2008

[51] Ketonen, J.; Juntti, M.; Cavallaro, J.R., "Performance—Complexity Comparison of Receivers for a LTE MIMO–OFDM System," *Signal Processing, IEEE Transactions on* , vol.58, no.6, pp.3360-3372, June 2010

[52] Sining Zhou; Chang, M.-C.F., "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *Solid-State Circuits, IEEE Journal of* , vol.40, no.5, pp.1084-1093, May 2005

[53] Abdulaziz, M.; Nejdel, A.; Tormanen, M.; Sjoland, H., "A 3.4mW 65nm CMOS 5th order programmable active-RC channel select filter for LTE receivers," *Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE* , vol., no., pp.217-220, 2-4 June 2013

[54] Yang Xu; Baoyong Chi; Zhihua Wang, "Power-scalable multi-mode reconfigurable continuous-time lowpass/quadrature bandpass sigma-delta modulator for zero/low-IF receivers," *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on* , vol., no., pp.293-296, 20-23 May 2012

[55] Holma, H.; Toskala, A. (editors); "LTE for UMTS: OFDMA and SC-FDMA Based Radio Access", John Wiley and Sons, 2009.

[56] Mehlführer, C.; Wrulich, M.; Colom Ikuno, J.; Bosanska, D.; Rupp, M., " Simulating the Long Term Evolution Physical Layer", *Proc. of the 17th European Signal Processing Conference (EUSIPCO 2009)*, August, 2009.

[57] Ping Lu; Sjoland, H., "A 5GHz 90-nm CMOS all digital phase-locked loop," *Solid-State Circuits Conference, 2009. A-SSCC 2009. IEEE Asian* , vol., no., pp.65-68, 16-18 Nov. 2009