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DEPARTMENT OF ELECTRICAL AND INFORMATION TECHNOLOGY

MASTER OF SCIENCE THESIS

Equalizer for an Integrated Optical Receiver in 65nm CMOS

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Abstract

This thesis describes the design of an analog equalizer for a fully integrated optical receiver in 65nm CMOS process. An equalizer is designed which compensates for the limited bandwidth of n-well/p-sub photodiode with a roll-down of about 5dB/decade. A transimpedance amplifier is also designed which has transimpedance gain of 70dBΩ and 3dB bandwidth of 1.3GHz. Equalization extends the bandwidth of the optical receiver to 1GHz from 6MHz. The design is simulated with Cadence Spectre® simulator. Corner simulations are performed to ensure robust operation under process variations. Total power consumption is 7mW.

Acknowledgments

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Pramod Ghimire
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List of Acronyms

BW Bandwidth

CS Common Source

FF Fast NMOS Fast PMOS

FS Fast NMOS Slow PMOS

GaInAs Indium Gallium Arsenide

HPF High Pass Filter

LED Light Emitting Diode

LPF Low Pass Filter

SD Source Degeneration

SF Slow NMOS Fast PMOS

SS Slow NMOS Slow PMOS

TIA Transimpedance Amplifier

TT Typical NMOS Typical PMOS

VCSEL Vertical Cavity Surface Emitting Laser

CHAPTER 1

Introduction

1.1 Fundamentals of Optical Communication

The speed of microprocessors have increased a lot during the last decade. The computing power of microprocessor alone does not define the overall speed of the system. The speed of the system is restricted by the speed of the channels by which data is distributed inside the system. To accommodate a very high speed of data transmission and reception, optical fiber has been used to keep up with the increased data rate. Data is represented as light signal inside an optical cable. It has to be converted back to an electrical signal at the target system where that data has to be used. Optical receiver is used to convert the light signal into electrical signal to be used in the target system. A residential internet connection usually uses an optical fiber connection from an ISP provider. Fig. 1.1 shows a general optical communication system. The electrical signal at ISP is converted to an optical signal before it passes through the optical cable. The light signal reaches the destination. At the destination, optical signal is converted to an electrical signal by an optical receiver. It will be soon clear how the operation of the optical receiver limits the overall bandwidth of a system.

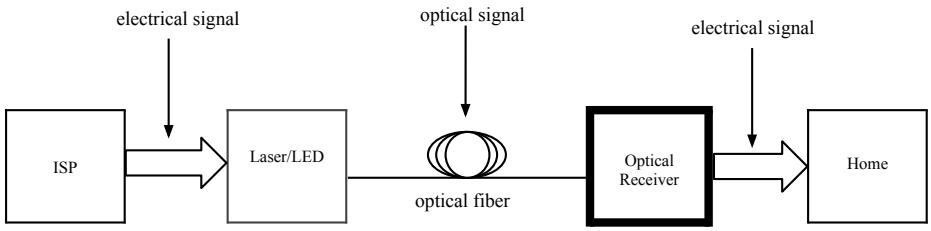

Fig. 1.1: An optical communication system

1.2 Components of Optical Fiber Communication System

The building block of an optical fiber communication system consists of a light source at its transmitter, an optical fiber cable to carry the light signal and an optical receiver at the receiver side to detect the signal in optical form and convert it into an electrical form. Fig. 1.1 shows components of the optical communication system. The light source can be a laser or a LED. LED is cheaper than a laser. However, laser source produce coherent light which can travel longer distance than light from a LED.

1.2.1 Lasers

Lasers produce coherent light which can be focussed in a narrow point. They have applications ranging from laser printing to laser surgery. Lasers are constructed from semiconductor diodes. The light can be emitted from the surface of the diode or edge of the diode. Accordingly lasers are of two types. Surface emitters and edge emitters. Surface emitters are better source of laser as light emitting characteristics can be controlled during the manufacturing process. A vertical cavity surface emitting laser(VCSEL) is a commonly used laser. A vertical cavity surface emitting laser (VCSEL), formed in a single epitaxial growth, is realized by sandwiching a light-emitting semiconductor diode between multi-layer crystalline mirrors. The technologies used for VCSEL fabrication are typically InGaAs or AlGaAs [1].

1.2.2 Light Emitting Diodes(LEDs)

The working principle of the LED is based on emission of photons due to recombination of holes and electrons in a semiconductor device. The

number of carriers present in the active LED region is proportional to the forward current through the LED. In most LEDs the light is not completely monochromatic i.e, show relatively broad spectra.

1.2.3 Optical Fiber

An optical fiber is a dielectric waveguide that operates at optical frequencies. This fiber waveguide is normally cylindrical in form. It confines electromagnetic energy in the form of light to within its surfaces and guides the light in a direction parallel to its axis. The structure of an optical fiber consists of a core and cladding. Variations in the material composition of the core give rise to the two commonly used fiber types [2].

Single-mode fiber

A single-mode filber has a core diameter of approximately 8-10μm. Single-mode fibers have lower signal loss and higher information capacity than multimode fibers. They are capable of transferring higher amounts of data due to low fiber dispersion.

Multimode fiber

A multimode fiber has a core diameter of 50-100μm. Multimode fibers propagate more than one modes. Multimode fibers have high loss compared to single-mode fiber. Multimode fibers can be used for short-haul communication.

1.2.4 Optical Receiver

Optical receivers are used to detect light coming out of fiber at the destination of the optical communication system. The main four components of an optical receiver is depicted in Fig. 1.2. Photodiode converts optical signal to an electrical current signal. Transimpedance amplifier that follows the photodiode amplifies current signal and convert it into a voltage signal. Post amplifier further amplifies the signal. Post amplifier is followed by a clock and data recovery circuit(CDR). CDR extracts the carrier and data signal from the received signal at the output of the optical receiver.

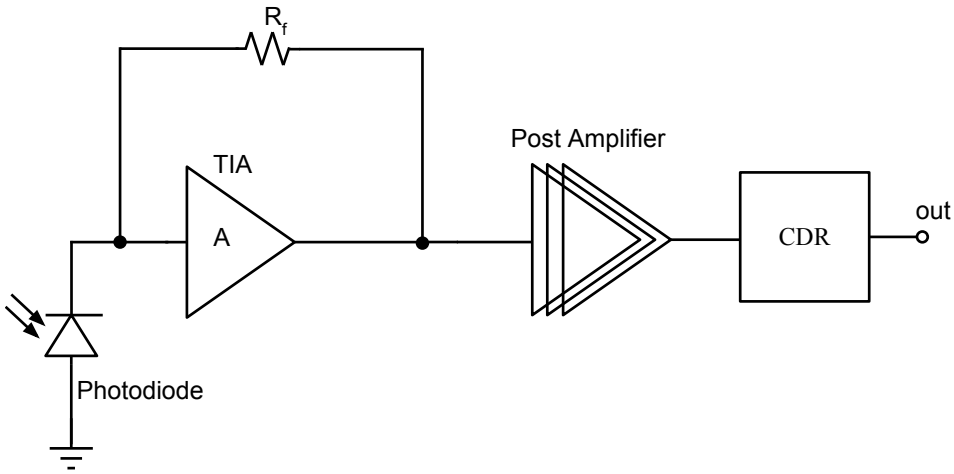

Fig. 1.2: Architecture of a typical optical receiver

1.3 Fully Integrated Vs Discrete Optical Receiver

The advantages offered by the use of optical fiber in long-haul communication is fundamentally different than the advantages when used for short-haul communication. Optical fiber connection has superior performance in long-haul communication. In short-haul communication, copper interconnect can provide satisfactory signal integrity upto few Gbps data rates. The installation cost of fiber optic system has reduced lately. The optical fiber used in long-haul communication has found its way to short-haul communication due to advances made in optics and photonics. The popularity of multi-mode fiber and 850-nm VCSELs for optical communication for short-haul communication has demonstrated that optical communication technologies even with reduced performance with respect to long-haul design is suited to shorter distances. The use of a CMOS photodetector on the same die as the receiver circuitry permits a high level of integration, improving the economics of short-reach parallel optical communication. Integration of all the components in an optical receiver offers the potential for a compact and low cost receiver solution, avoiding the signal integrity challenges and yield losses associated with hybrid implementation of the photodetector and transimpedance amplifier (TIA) [3].

1.4 Challenges in Fully Integrated Optical Receiver

The high speed response of a CMOS integrated photodiode is worse than that of optimized discrete-component photodiode, both in terms of its intrinsic and electrical bandwidth. Deep sub-micron CMOS process, with low supply voltage, leads to smaller reverse voltage. It can affect the carrier speed in the depletion region of a photodiode in the receiver. As the CMOS process is scaled down, high doping concentration used leads to smaller depletion region where light is absorbed. Deep-submicron processes using upto 7 metal layers can reflect the incident light without being getting absorbed in the photodiode. In addition to this, silicon has low absorption coefficient which means light is able to penetrate down to the substrate level where it gets mainly absorbed. As a result, not much light is absorbed in the depletion region. This adversely affects the responsivity of the photodetector. It looks like a not so good situation. CMOS is a widespread cheap process. The photodetecters built in CMOS process also offers lesser bandwidth than the one where discrete components are used. It is a challenging task to use CMOS process to build an integrated optical photdetectors and yet be able to get the enough performance with respect to hybrid implementation.

1.5 Why Photodiodes are Bottleneck?

The bandwidth of an electrical signal generated from a photodiode is in MHz range($<$10MHz) [1] for a n-well/p-sub photodiode. The bandwidth of a channel in an optical fiber is in GHz range. It means the electrical bandwidth of a photodiode restricts how fast the data can be accessed. Increasing this bandwidth thus guarantees the higher data speed and bandwidth. Photodiode implemented in CMOS process is thus a critical element in restricting the data access.

1.6 How to Overcome these Limitations?

The limited bandwidth offered to an electrical signal by a photodiode in an optical receiver has to be extended if one wishes to make use of the benefit of scaled down CMOS technology.

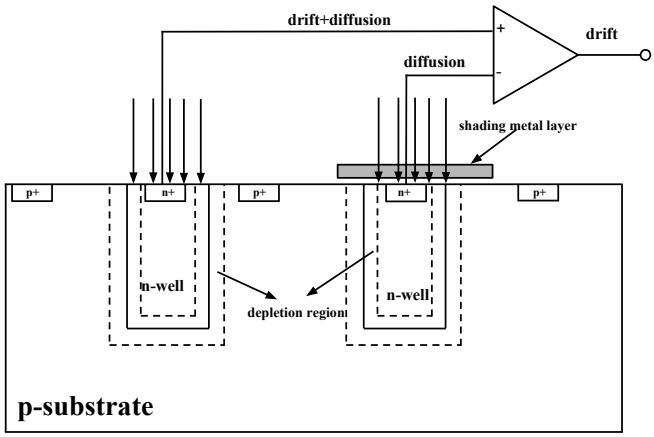

Fig. 1.3: Differential photodiode

Differential Photodiode

A differential photodiode is also called a spatially modulated photodiode. In a differential photodiode, alternating fingers are covered with a metal layer. This shading metal layer blocks the incoming light signal. As a result, the current components present under illuminated finger will consists of a diffusion and a drift current. Whereas the current present under the non-illuminated finger consists of only diffusion component. When these current components pass through transimpedance amplifier(TIA), diffusion current cancels out and only the drift component is left. The transimpedance amplifier should have high common mode rejection ratio(CMRR) while using a differential photodiode. This is diagrametically depticted in Fig. 1.3. The bandwidth is improved as a byproduct of being able to remove the slow diffusion current component by the preceding TIA. The disadvantage of using a differential diode is that only half the light signal can fall onto the diode structure. Half the signal is simply not used. This causes reduction of the responsivity of the photodiode. Responsivity will be explained in chapter 2 when the geometry of n-well/p-sub diode is explained in details. The bandwidth of a differential photodiode can be as high as 1GHz [4].

Avalanche Photodiode

Avalanche photodiodes internally multiply the primary signal photocurrent before it enters the input circuitry of the following amplifier. This increases

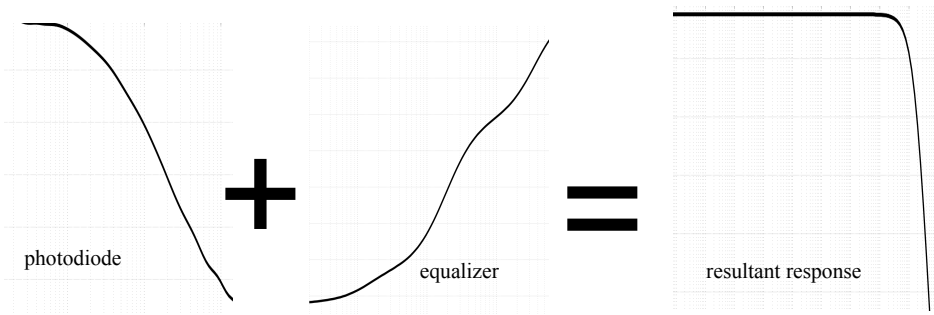

Fig. 1.4: Equalization approach

receiver sensitivity, since the photocurrent is multiplied before encountering the thermal noise associated with the receiver circuit [2]. Avalanche photodiodes offer high bandwidth and responsivity at the same time. Use of high reverse biased supply voltage is the only concern of using an avalanche photodiode(-10V). This high reverse bias voltage also concerns about the stability of the diode structure.

Equalization

A circuit which response is exactly inverse to that of a photodiode can be used to increase the bandwidth of a CMOS photodiode. This circuit is called an equalizer. It will be described in more details in chapter 3 and 4. Fig. 1.4 shows this approach in diagrammatic form. When the responses of the photodiode and equalizer circuits are multiplied in time domain, the resultant signal can have a high bandwidth as depicted in the diagram. Multiplication in time domain corresponds to addition in frequency domain.

Equalization is used in this work. An equalizer circuit is designed to extend the bandwidth limited by the use of a CMOS integrated photodiode in an optical receiver. This thesis work uses an experimental data obtained from a n-well/p-sub photodiode measured in [5]. It will be shown in chapter 4, how equalization is achieved in circuit level.

1.7 About this Thesis Work

This project is carried out at the Department of Information & Electrical Technology(EIT) at Lund University. The main goal of this project is to investigate an architecture of an optical receiver and find a way to increase the bandwidth of a photodiode with the use of an analog equalizer circuit.

1.8 Thesis Organization

In the second chapter the basics of an optical receiver are described. This chapter details the factors that affect the photoresponse of a typical photodiode. A short theory of TIA and equalizer circuit is given. The third chapter explains the system design in Verilog-A. It explains how the coefficients needed for schematic level simulations are derived. The transistor level circuit is designed for TIA and equalizer in chapter four. Chapter five describes the system simulation results. Conclusions and future works are discussed in chapter six.

CHAPTER 2

Theory

The working principle of a photodiode is described first with the help of an energy diagram.

Next, the topologies of a transimpedance amplifiers are explained. At the end of this chapter, equalizer principle is described.

2.1 Photodiode

In equilibrium state, in a semiconductor, the rate of generation of new electrons and holes equals the recombination rate.

$$n \cdot p \quad = \quad {n_i}^2 \tag{2.1}$$

n_i is the intrinsic concentration of a semiconductor material whereas n and p represent the concentration of electrons and holes in the material respectively.

Any deviation from 2.1 causes an increased net generation or recombination. Electromagnetic radiation can generate electron-hole pairs in a semiconductor. An electron-hole pair is created in the semiconductor crystal when an

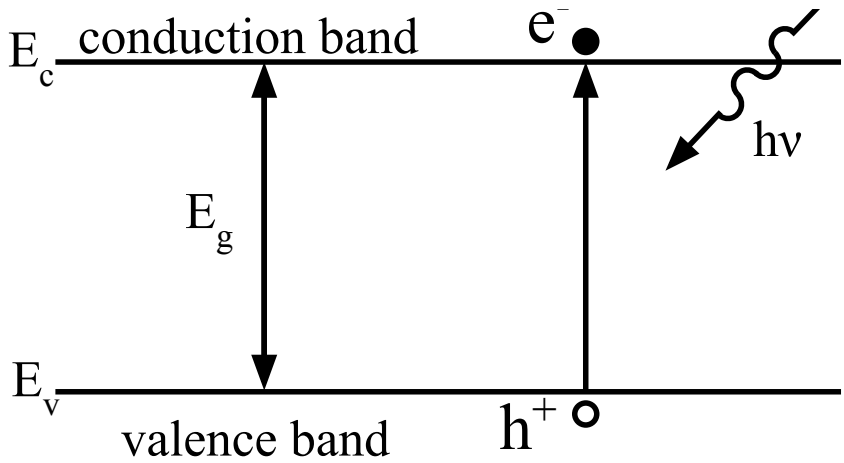

Fig. 2.1: Energy diagram

electron is moved from the valence band into the conduction band. In addition to this electron, a hole is created in the valence band. To generate an electron-hole pair, the energy level of the electron needs to rise by an amount larger than or equal to the band gap energy E_g. This condition can be expressed in a mathematical form as

$$h\nu \quad \geq \quad E_g = E_c - E_v \tag{2.2}$$

where h is Planck's constant, ν is the frequency of the electromagnetic wave, E_c, E_v represent the lower level of conduction energy band and the highest level of the valence energy band.

Equation (2.2) shows that the a photon with energy at least band gap energy can create an electron-hole pair. It can be put in another way if (2.2) is rewritten as

$$\nu \quad = \quad \frac{E_g}{h} \tag{2.3}$$

The excess energy on a photon is dissipated as heat energy. To maximize the number of electron-hole pairs created by impinging electromagnetic wave with a certain power, the frequency of wave should be chosen as predicted by (2.3). The band gap energy of silicon is 1.2eV. This suggests that the frequency of the wave should be at least 271THz in order to create an electron-

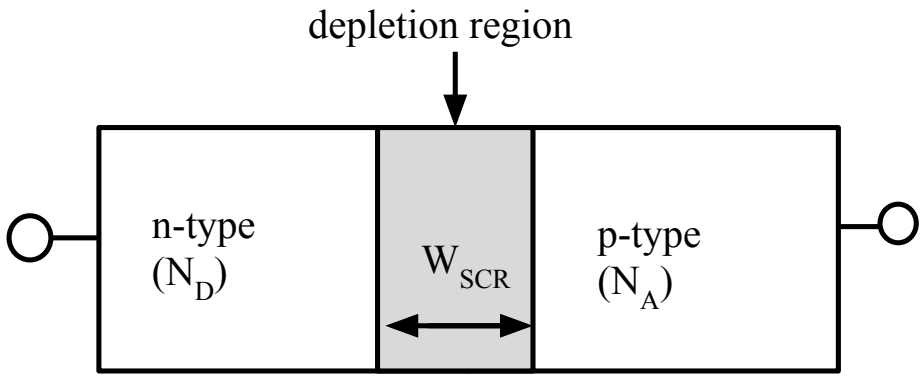

Fig. 2.2: PN junction

hole pair.

$$c = \lambda \cdot \nu \tag{2.4}$$

where c represents the speed of light in free space and λ represents the wavelength of the photon. 271THz frequency corresponds to 1.1μm in terms of wavelength. It means any electromagnetic wave with wavelength smaller than 1.1μm is able to create a photoelectric effect i.e generate an electron-hole pair. The lasers and LED sources operating at 850nm, which is typical wavelength used for short distance communication, are economically attractive, since they are less expensive than lasers operating at 1300nm and 1550nm [1]. Optical sources and photodetectors operating at 850nm are readily available. The response of the photodiode characterized in 850nm wavelength is investigated in this work when the equalization is considered since wavelength more than 1.1μm can not be used with silicon photodiodes.

Photodiodes in CMOS

A diode is a semiconductor that is n-type doped on one side and p-type doped on the other side. The n-type side is called cathode and it has a lot of free electrons. The p-type side is called anode and it has a lot of holes in it. In equilibrium state, space charge region region is formed in the junction. There are no carriers in this region. It is also called depletion region. Fig. 2.2 shows a pn junction.

The width of space charge region is denoted by W_{SCR} in Fig. 2.2. The doping concentration in n-type and p-type region is denoted by N_D and N_A.

The depletion region width is related to the doping concentration of the n-type and p-type region.

$$W_{SCR} = \sqrt{\frac{2\epsilon}{q} \cdot \frac{N_A + N_D}{N_A N_D} \cdot V_{bi}} \tag{2.5}$$

where ϵ is the permittivity of the semiconductor material used, V_{bi} is the built-in potential at the junction. The higher doping concentration corresponds to a smaller depletion region as per (2.5).

If photons with sufficient energy impinge on a semiconductor diode, electron-hole pairs are created in the n-type region, in the p-type region, and in the depletion region. The electric field within the depletion region separates the electron from the holes. In this manner, a photocurrent is generated that flows between the anode and the cathode of the diode which is then called a photodiode.

In a standard CMOS process four types of pn junctions can be used for light detection;

- n-well/p-sub
- n-well/p-well
- n-well/p+
- p-well/n+

A simplified cross-section geometry of a n-well/p-sub junction is shown in Fig. 2.3. It is due to less dopant concentration in n-well, depletion region is more when n-well is used to form a diode. The depletion region of n-well/p-sub junction is wider than that of other junction types due to the same reason. The incident light absorbed at depletion region produces an electron-hole pair which travel in opposite direction and a current of value I_{out} flows from the junction. Not all of the incident light gets absorbed at the depletion region. Some part is absorbed in neutral region of the junction in n-well and most of the light manage to penetrate down to the p-substrate

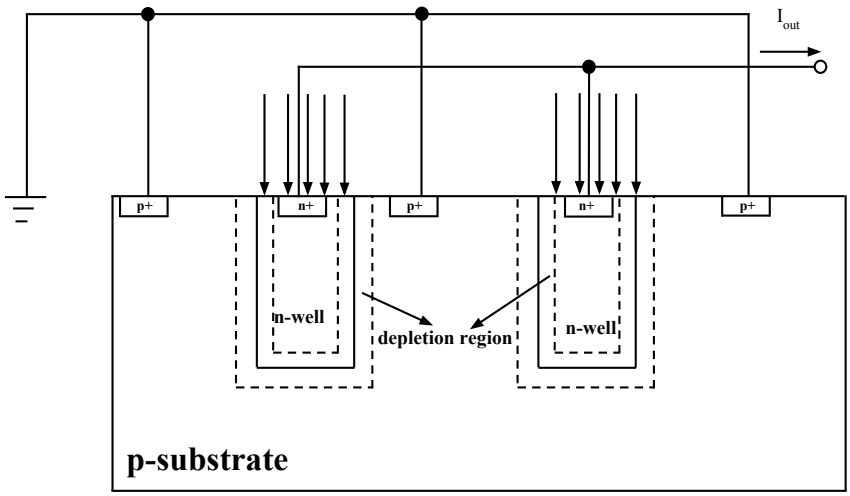

Fig. 2.3: Cross section of a typical n-well/p-sub junction diode

giving rise to n-well diffusion current and p-substrate diffusion current. The total current flowing through a diode can be expressed as

$$I_{tot} = I_{well} + I_{p-sub} + I_{drift} \tag{2.6}$$

where I_{tot}, I_{nwell}, I_{p-sub}, and I_{drift} represent total current, n-well diffusion current, p-sub diffusion current and depletion region generated drift current component, respectively.

The bandwidth of the current generated within depletion region is greater than 10GHz. The bandwidth of the diffusion current generated in n-well region is about 1.5GHz, and the bandwidth of the current component generated in the p-sub region is hardly more than 2.5MHz. When these three current components are summed, the bandwidth of the resultant signal is limited by the smallest bandwidth i.e the bandwidth due to p-sub current component [1]. The frequency response of a n-well/p-sub photodiode in a 65nm CMOS process is shown in Fig. 2.4. The magnitude of the response in this plot is normalized with respect to the value at low frequency. BW is about 6.25MHz.

For completeness of the photodiode, parameters used to measure figure of merit are presented here. Quantum efficiency is used as a measure for a photodiode response. It is defined as the number of carriers produced per

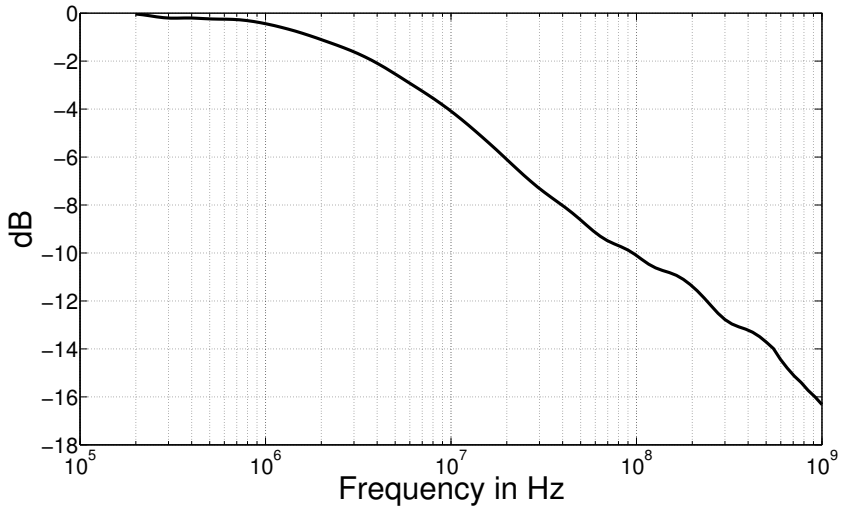

Fig. 2.4: Normalized frequency response of a n-well/p-sub photodiode

photon, or

$$\eta = \frac{I_{ph}}{q\phi}$$

$$= \frac{I_{ph}}{q} \cdot \frac{h\nu}{P_{opt}} \tag{2.7}$$

where I_{ph}, ϕ, P_{opt} represent the photocurrent, the photon flux and the incident optical power respectively. The ideal quantum efficiency is unity. Another similar metric is the responsivity [6] defined as

$$\Re = \frac{I_{ph}}{P_{opt}}$$

$$= \frac{\eta q}{h\nu} \quad \frac{A}{W} \tag{2.8}$$

where q represents charge in an electron, h represents planck's constant, ν represents frequency of light signal.

2.2 Transimpedance Amplifier(TIA)

The main objective of a TIA is to convert the small photocurrent into a voltage signal. The output signal of a TIA is therefore a voltage signal, while the input signal is a current signal. The relationship between these two quantities is given by the transimpedance Z_{TIA};

$$Z_{TIA} = \frac{v_{out}}{i_{in}} \tag{2.9}$$

where v_{out}, and i_{in} represent the output voltage signal and input current signal respectively. Because the current signal is converted into a voltage signal, Z_{TIA} has the units of Ω or dBΩ

2.2.1 Comparison of TIA Topologies

Different topologies of TIA are described briefly under this section.

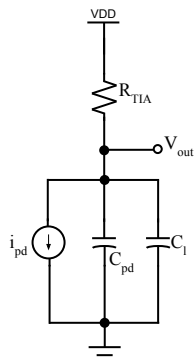

Fig. 2.5: Single resistor TIA

Single Resistor TIA

The basic objective of a TIA is to convert a current into a voltage signal. A resistor is able to do this. Consequently, the simplest TIA topology one can imagine consists of a single resistor. This is depicted in Fig. 2.5, where the resistor is connected between the supply voltage and the output node, while the anode of the photodiode with parasitic capacitance C_{pd} is connected to the ground. C_l represents the capacitive load offered by TIA. The BW of

TIA is expressed as;

$$BW_{TIA} = \frac{1}{2\pi R_{TIA}(C_{pd} + C_l)} \tag{2.10}$$

$$|Z_{TIA}| = R_{TIA} \tag{2.11}$$

The transimpedance bandwidth product is given by:

$$ZBW = \frac{1}{2\pi(C_{pd} + C_l)} \tag{2.12}$$

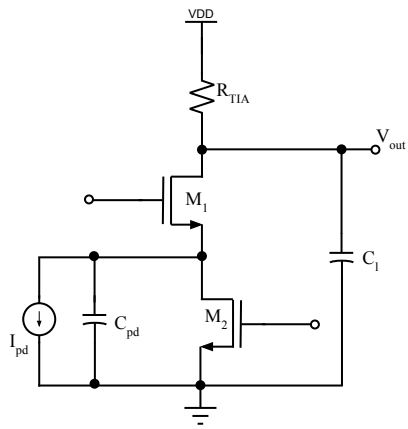

Fig. 2.6: Common gate TIA

Common Gate TIA

The problem with the single-resistor TIA is the limited transimpdeance-bandwidth product which is governed only by the capacitance of the photodiode. As a result, the BW of a single resistor TIA is less. The common-gate TIA improves this fundamental trade-off between transimpedance gain and bandwidth. The circuit diagram of a common-gate TIA connected to a photodiode with a parasitic capacitance C_{pd} is shown in Fig. 2.6.

$$BW_{TIA} = \frac{g_{m,M1}}{2\pi C_{in}} \tag{2.13}$$

$$|Z_{TIA}| = R_{TIA} \tag{2.14}$$

The transimpedance bandwidth product is given by:

$$ZBW = \frac{g_{m,M1}R_{TIA}}{2\pi C_{in}} \tag{2.15}$$

where $C_{in} = C_{pd} + C_{gs,M1}$. Transimpedance and bandwidth are decoupled from each other.

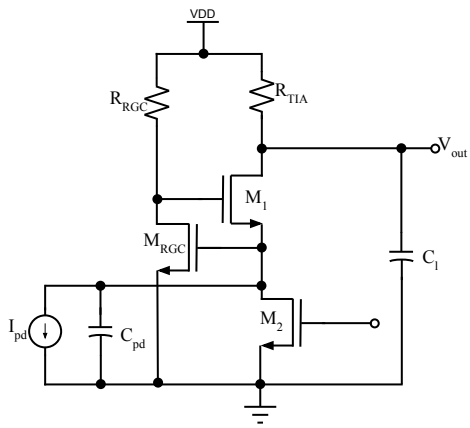

Fig. 2.7: Regulated-cascode TIA

Regulated-Cascade TIA

Feedback can be applied to the common-gate TIA to increase its performance. This leads to the regulated-cascode TIA. This is shown in Fig. 2.7. By contrast with the common-gate TIA, the gate voltage of transistor M_1 is not fixed as in the regulated-cascode TIA topology. The effective transconductance of M_1 can be regulated by amplifying the voltage at the source of this transistor with an inverting voltage gain.

$$BW_{TIA} = \frac{g_{m,M1}(1 + |A_{RGC}|)}{2\pi C_{in}} \tag{2.16}$$

$$|ARGC| = g_{m,M1} \cdot R_{RGC} \tag{2.17}$$

$$|Z_{TIA}| = R_{TIA} \tag{2.18}$$

The transimpedance bandwidth product is given by:

$$ZBW = \frac{g_{m,M1}(1 + |A_{RGC}|)R_{TIA}}{2\pi C_{in}} \tag{2.19}$$

If we look at (2.16), the BW is increased by the factor of $(1+|A_{RGC}|)R_{TIA}$.

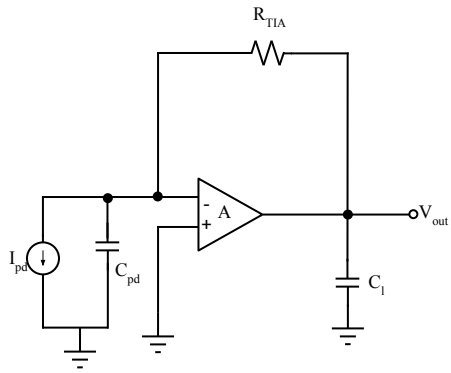

Fig. 2.8: Shunt-shunt feedback TIA

Shunt-Shunt Feedback TIA

Yet another possibility to convert a current into a voltage is shown in Fig. 2.8. A negative feedback network senses the voltage at the output and returns a proportional current to the input. This configuration is known as shunt-shunt feedback TIA configuration. The bandwidth, and transimpedance gain are given by following expressions;

$$BW_{TIA} = \frac{A}{2\pi R_{TIA} C_{in}} \tag{2.20}$$

$$|Z_{TIA}| = R_{TIA} \tag{2.21}$$

The transimpedance bandwidth product is given by:

$$ZBW = \frac{A}{2\pi C_{in}} \tag{2.22}$$

where A represents the voltage gain of the negative feedback amplifier.

The TIA topology that is used in this work is the shunt-shunt feedback TIA. Advantage of using this architecture include lowering of input and output impedances. This helps to shift the pole location at input and output terminal farther away. In addition to this, it results in the increase of the closed

loop bandwidth by factor of the loop gain.

The voltage gain, A needs to be realized by more than one amplifier stages in a shunt-shunt TIA. The bandwidth of the amplifier decreases when more than two amplifiers are cascaded to increase the gain. Different approach should be used to increase the bandwidth decreased by cascading of multiple stages. Miller transistors are used in between the stages in [7] for this purpose of BW extension. In [7], two stage core amplifiers are used as a voltage amplifier. 90fF capacitors are used between the two core amplifiers. These capacitances are further implemented by two NMOS in cutoff mode [8] as an enhancement to the circuit in [7]. An NMOS in cut-off mode can act like a capacitor in cut-off mode with value of C_{gd} equal to C_{ov} [9]. The value of C_{gd} is used to implement the capacitance. C_{gd} represents the capacitance between gate and drain terminal. C_{ov} represents the overlap capacitance.

Inductive peaking [10] can be used to extend the bandwidth. The effect of node capacitances at the drain of the input transistors are cancelled using drain inductances. This approach is costly in terms of area occupied by drain inductors. However, the bandwidth can be increased to a great extent when bandwidth is criteria and not area.

Capacitive peaking is used in [11]. By putting a capacitance in series, it is possible to increase the bandwidth by decreasing the capacitance value in the node concerned. This approach uses less area than the one using inductive peaking.

All these approaches can be put aside if the use of very low gain and very high bandwidth amplifiers formed by cascading of differential CS amplifiers are used as the core voltage amplifier to provide voltage gain mentioned above. [4].

The noise at TIA dominates the overall noise performances of the photoreceiver. Equivalent input-referred noise is usually presented for noise performance of a receiver. It is defined as the current source that, together with the ideal noiseless TIA, reproduces the output noise of the actual noisy TIA [12]. The RMS noise voltage is calculated as:

$$v_{n,out,RMS} = \sqrt{\int_0^\infty \overline{dv_{n,out}^2}} \tag{2.23}$$

where $v_{n,out,RMS}$ represents the output RMS noise voltage, and $dv_{n,out}^2$ represents the differential noise voltage in a small frequency range. The input-referred noise is defined as

$$i_{n,in,RMS} = \frac{v_{n,out,RMS}}{|Z_{TIA}|} \tag{2.24}$$

where $i_{n,in,RMS}$ represents the input referred noise, and Z_{TIA} represents the total transimpedance gain of the amplifier. Higher the transimpedance gain is, lower the input referred noise is.

The feedback impedance in the transimpedance amplifier can lead to the system stability issues. It must be ensured that the loop gain phase drops down to 0dB only after the loop gain magnitude drops to 0dB reference line in the bode plot. Bode plot represents the magnitude response together with the phase response at the same plot. It is easier to check the stability of a system by inspection in a bode plot. This ensures the system stability [13]. For a system to be stable, phase margin of more than 45 ° is needed [14].

2.3 Equalizer

Equalizer section is the main important section of an integrated optical receiver. To compensate the characteristics roll down of a photodiode, a slow roll up circuit is required. High pass filter is a right candidate for this purpose. Unfortunately, these filters have high roll up of approximately 20dB/decade. However, an integrated photodiode have a characteristics curve which falls slowly at around 4dB/decade-10dB/decade. Hence it is clear that, a simple high pass filter is not sufficient to equalize the slow roll down of the photodiode characteristics. An approach used in [1], [4] is used in this work. Few high pass filters(HPF) are combined in parallel to get the required characteristics slow roll up as is done in [4], [15]. Equalizer has the following transfer function.

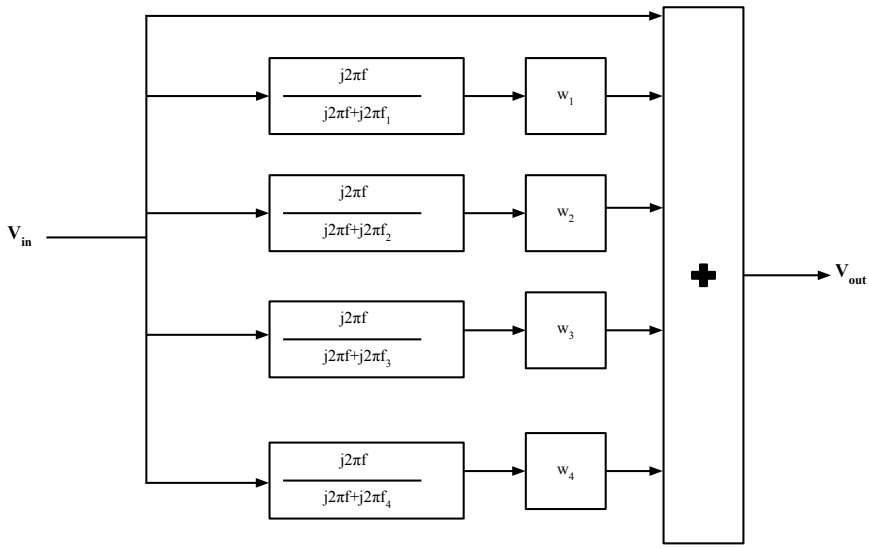

Fig. 2.9: Diagrammatic representation

$$E(f) \quad = \quad 1 + \frac{w_1 \cdot j2\pi f}{j2\pi f + 2\pi f_1} + \frac{w_2 \cdot j2\pi f}{j2\pi f + 2\pi f_2} + \cdots + \frac{w_n \cdot j2\pi f}{j2\pi f + 2\pi f_n} \quad (2.25)$$

where $w_1, w_2, w_n, f_1, f_2, f_n$ represent the weights and cutoff frequencies of the corresponding high pass filters. The expression in (2.25) can be represented in diagrammatic form as in Fig. 2.9. The block diagram implements four filter sections alongwith a direct path above the first section. The output of the filter sections are multiplied by corresponding weights and then summed to get the resultant voltage signal. Fig. 2.10 represents the frequency response of each sections used in the equalizer circuit as well as the resultant frequency response of the total block diagram. In short, it can be said that if one can design these filter blocks separately and then amplifies by a constant gain using an amplifier and sums them up with an adder circuit, the equalizer circuit can be realized.

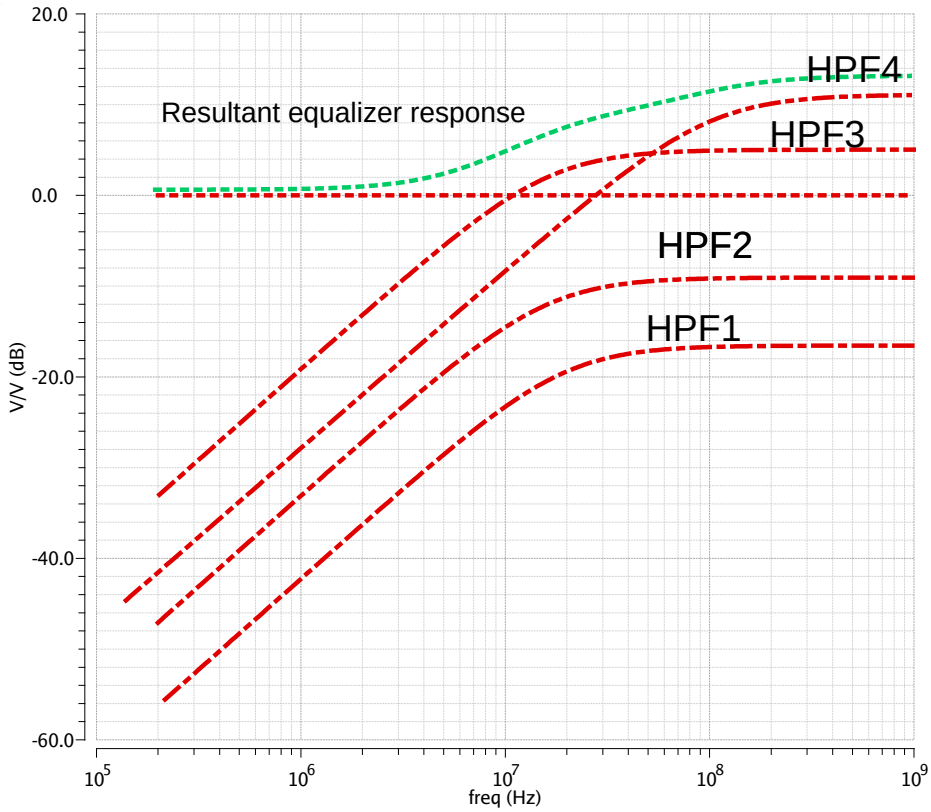

Fig. 2.10: High pass filter responses

CHAPTER 3

System Design

This chapter discusses the system design approach. It describes the methodology used in this project work. The verilog-A modeling of the system is explained with the help of the characteristics response obtained from the verilog-A simulation of TIA and equalizer section.

3.1 Methodology

The response of the photodiode is first derived from the experimental data [16]. The transimpedance amplifier circuit is then simulated in verilog-A. Afterwards, it is simulated alongwith an equalizer model where HPF sections are implemented. In the simulation, parametric sweep is done to the weights and corner frequencies variables until the required response similar to that of an inverse photodiode response is observed. The weights and corner frequencies required to compensate the diode response curve are determined. These weights and corner frequencies were defined in chapter 2. These values are then used in schematic level simulation in Cadence Virtuoso Analog Design Environment to get the response of the equalizer in chapter 4. The obtained plot is compared with the standard inverse photodiode response characteristics. By comparing with the inverse characteristics, it is easier

to find the required coefficients. The methodology used is depicted in a diagrammatic form in Fig. 3.1.

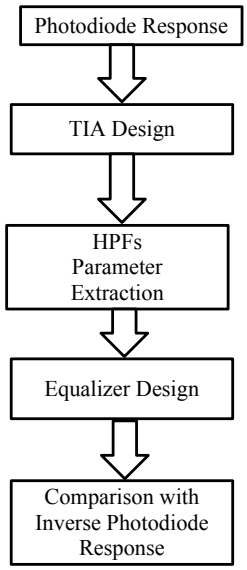

Fig. 3.1: Methodology of this project work

3.2 Test Bench

The test bench used for simulation is shown in Fig. 3.2. The TIA and equalizer sections are connected in series. I_{diode} represents the current source. C_{diode} represents the photodiode capacitance. A current source in parallel with a capacitance is equivalent to a photodiode. The photodiode response that is equalized in this project work is a n-well/p-sub photodiode [5]. The geometry and characteristics of the n-well/p-sub photodiode were described in chapter 2. The capacitance attached at the negative terminal of the voltage amplifier is a dummy capacitance, C_{dummy} used to balance the capacitive effect due to a photodiode at the input of the TIA in a differential structure. The value of these capacitors used in this test bench are 1.5pF each. The feedback resistances R_f are placed around the core voltage amplifier. The value of these feedback resistors are 3.05KΩ each. The output of the TIA is connected to the equalizer input. The output is taken from the output terminals at the equalizer.

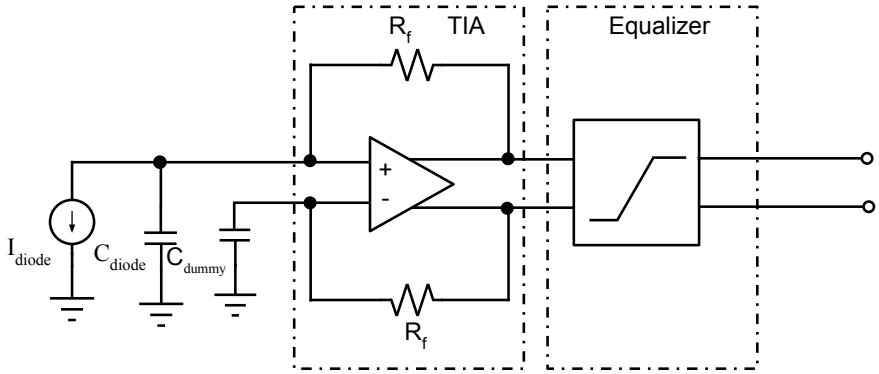

Fig. 3.2: Test bench setup in verilog-A simulation

3.3 TIA

The required bandwidth of the system is 1GHz. The transimpedance gain of 70dB and 3-dB BW of 1.5GHz for the TIA is targeted. If we recall (2.20), it gives the relationship between the voltage gain, feedback resistance, and total capacitance at the input node, $C_{in} \approx C_d$.

$$\begin{aligned} C_d &= 1.5pF \\ R_f &= 3.05K\Omega \\ BW_{TIA} &= \frac{A}{2\pi R_f C_d} \\ BW_{TIA} &= 1.5GHz \\ \Rightarrow A &= 43 \approx 33dB \end{aligned}$$

The voltage gain provided by the voltage amplifier at the core should be 33dB. Also the bandwidth of the voltage amplifier should be greater than that of TIA. The voltage amplifier is targeted to have approximately 30dB gain and BW of 2GHz. Fig. 3.3 shows the frequency response of the TIA obtained from verilog-A simulation. The transimpedance gain is set by the feedback resistor. The magnitude response shows 70dBΩ which corresponds to 3.05KΩ. The 3-dB bandwidth observed is 1.5GHz as expected.

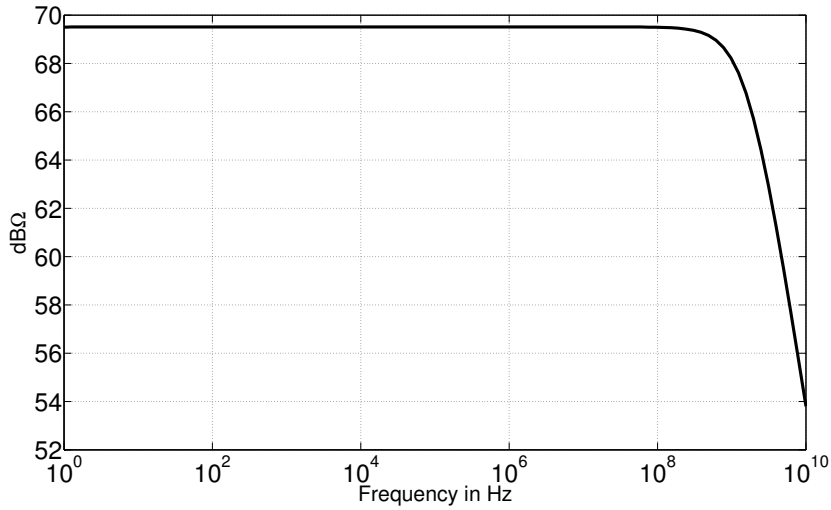

Fig. 3.3: Frequency response in verilog-A

3.4 Equalizer

It is worthwhile to have a short glimpse of photodiode response before discussing about the equalizer frequency response. Fig. 3.4 shows the inverted form of the n-well/p-sub response characteristics described in chapter 2. It is again a normalized plot. The photodiode response was plotted from experimental data obtained from [5]. The inverted characteristics plot in Fig. 3.4 is easy to match the required equalizer characteristics. As explained in chapter 2, the equalizer designed should provide exactly the same curve if total compensation is desired. Since it is not possible to compensate all the response, point by point, feasible requirements were set for the project. The ripple voltage signal should not fluctuate with respect to a flat reference line, i.e 0dB line by 0.5dB. Fig. 3.5 shows the equalizer frequency response. It can be observed that the difference between the gain at low frequency and at 1GHz is approximately 15dB. This difference is suitable for exact equalization of the photodiode characteristics observed in Fig. 3.4 in inverted form. This curve is obtained by sweeping the weights and corner frequencies. The cutoff frequencies are set at 1MHz, 10MHz, 100MHz, and 1GHz tentatively. The values of weights are sweeped to calculate them so as to exactly get the response to that shown in Fig. 3.4. The equalization can be better observed

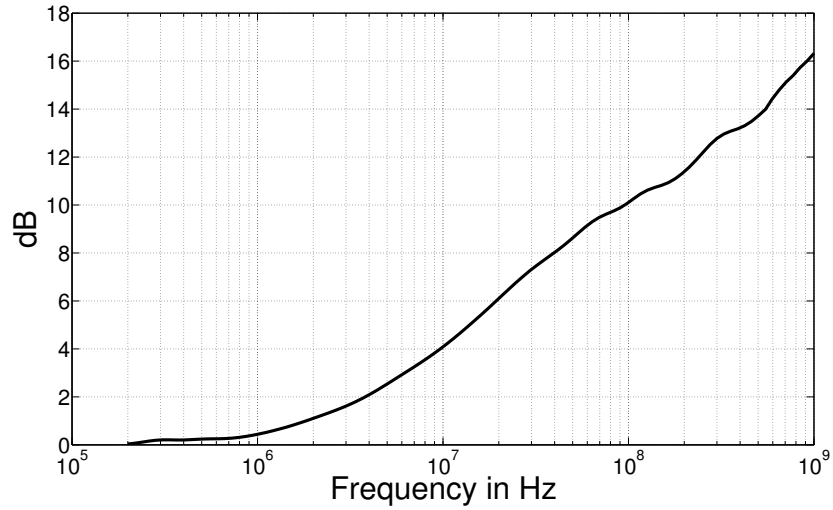

Fig. 3.4: Inverse diode characteristics plot

if these two plots in Fig. 3.4 and Fig. 3.5 are plotted at the same graph. This is depicted in Fig. 3.6. The red plot corresponds to the equalizer response. The black plot represents the inverse photodiode response. Both the responses are normalized responses. It can be observed that the match is not perfect. However, the error difference is less than ±0.5dB until 1GHz. How well the red curve fits the black curve depends on how well the coefficients for weights and corner frequencies are selected. This is explained in the next section.

Table 3.1: Extracted parameters

weights	values	corner-frequencies	values
w_1	0.02	f_1	1MHz
w_2	0.22	f_2	10MHz
w_3	1.87	f_3	188MHz
w_4	4.0	f_4	4.1GHz

3.4.1 Parameter Extraction

Eight parameters have to be extracted from the verilog-A simulation which needs to be used in schematic simulations. These include the corner fre-

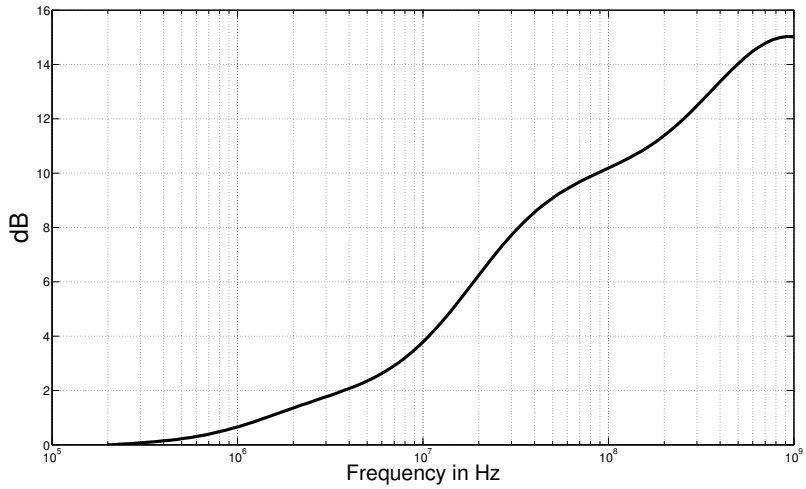

Fig. 3.5: Frequency response of equalizer in verilog-A

quencies and corresponding weights for each filters. These are represented by $f_1, f_2, f_3, f_4, w_1, w_2, w_3$, and w_4 as mentioned in 2.3. These values are found by using genetic algorithm in [4]. However in this work, these values are found out by sweeping the corresponding variables inside the equalizer section parametrically. By sweeping these values parametrically, the values found are presented in Table 3.1. These values will be used in schematic design described in chapter 4.

In Fig. 3.7 is shown the phase response of the equalizer that corresponds to the magnitude response of it shown in Fig. 3.5. The phase response shows that the phase increases upto 29 °and starts to drop down due to the location of the pole at the output terminal. This phase corresponds to the summation of the phases of four sections of HPF used in equalizer section. It can be seen two peak in the plot. It helps to make the phase plot look similar to the inverse phase response of the photodiode calculated theoretically in [1]. [1] shows that the phase of a photodiode stays at 26 °after 100 MHz. To obtain such equalized phase response, it is desirable to have as many peaks as possible. However it is difficult to exactly match this phase stabilization calculated from theoretical derivation. The best way to estimate this is to expect a response with two peaks such that phase remains between

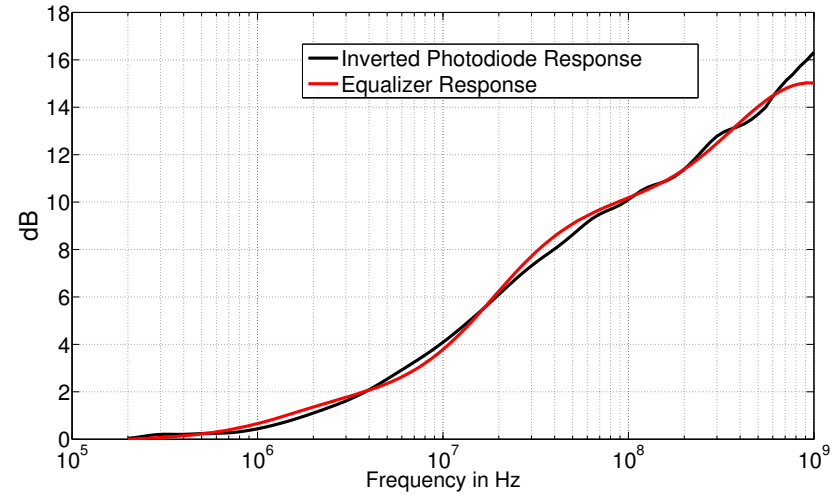

Fig. 3.6: Equalizer and inverse photodiode response

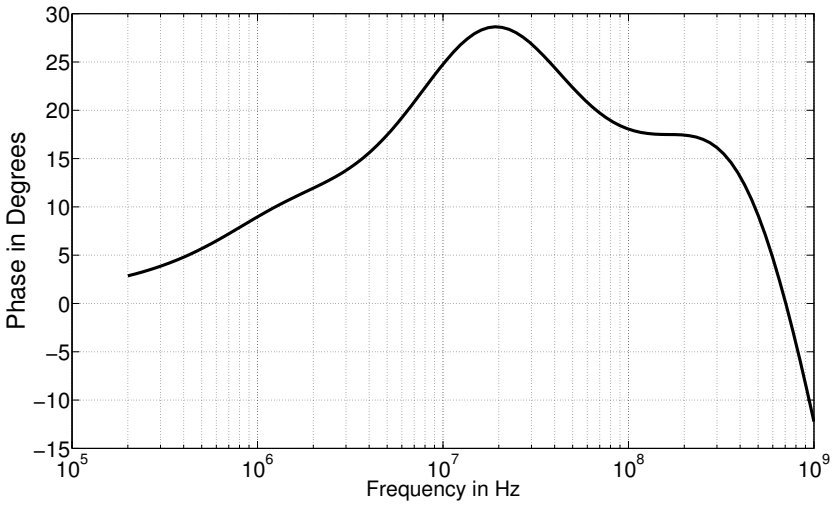

Fig. 3.7: Phase response of equalizer in verilog-A

20 °to 30 °and at the same time get the magnitude equalization. The plot in Fig. 3.7 shows one way to equalize phase. It is however difficult to equalize the magnitude and the phase at the same time. It is concluded from the sim-

ulation of equalizer circuit in Verilog-A that the equalization for magnitude response of the photodiode which gives best solution for magnitude equalization does not give optimum equalization for the phase response. Fig. 3.7 gives the optimum phase equalization which corresponds to the best fitted magnitude equalization. This can be a good topic for the future work.

3.5 System Simulation

The total equalization when photodiode response is added with the equalizer response is demonstrated in Fig. 3.8. TIA response is also shown. It can be observed that the TIA bandwidth is greater than the equalizer response. The green curve represents the total equalized response. The 3-dB BW of this signal is 1GHz and the voltage fluctuations is within ±0.5dB around the 0dB line. Red curve represents the equalizer response. The black curve represents the photodiode response. The blue curve represents the TIA response. All the plots are normalized with respect to 0dB line. For example, the TIA transimpedance gain is 70dBΩ(blue curve). When this is plotted, it is plotted as 0dB in this plot. The same reason applies to the other plots in the diagram.

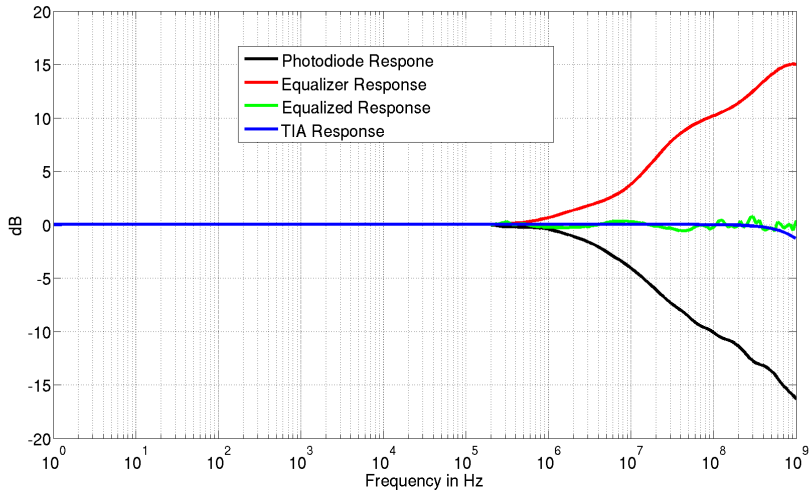

Fig. 3.8: System simulation result

CHAPTER 4

Schematic Design and Simulations

This chapter describes the schematic level circuit of a TIA and an equalizer used in an optical receiver mentioned in previous chapters. First, TIA is explained in details with the help of a three stage core voltage amplifier. Equalizer is described afterwards.

4.1 Transimpedance Amplifier(TIA)

The shunt-shunt feedback topology is used to design a transimpedance amplifier as described in chapter 2. The gain and the bandwidth of the core amplifiers are designed according to the system design specifications.

The schematic level representation of a TIA is shown in Fig. 4.1. Three differential amplifiers in cascade are used as the voltage amplifier. The overall voltage gain of the core amplifier is the product of three individual amplifiers.

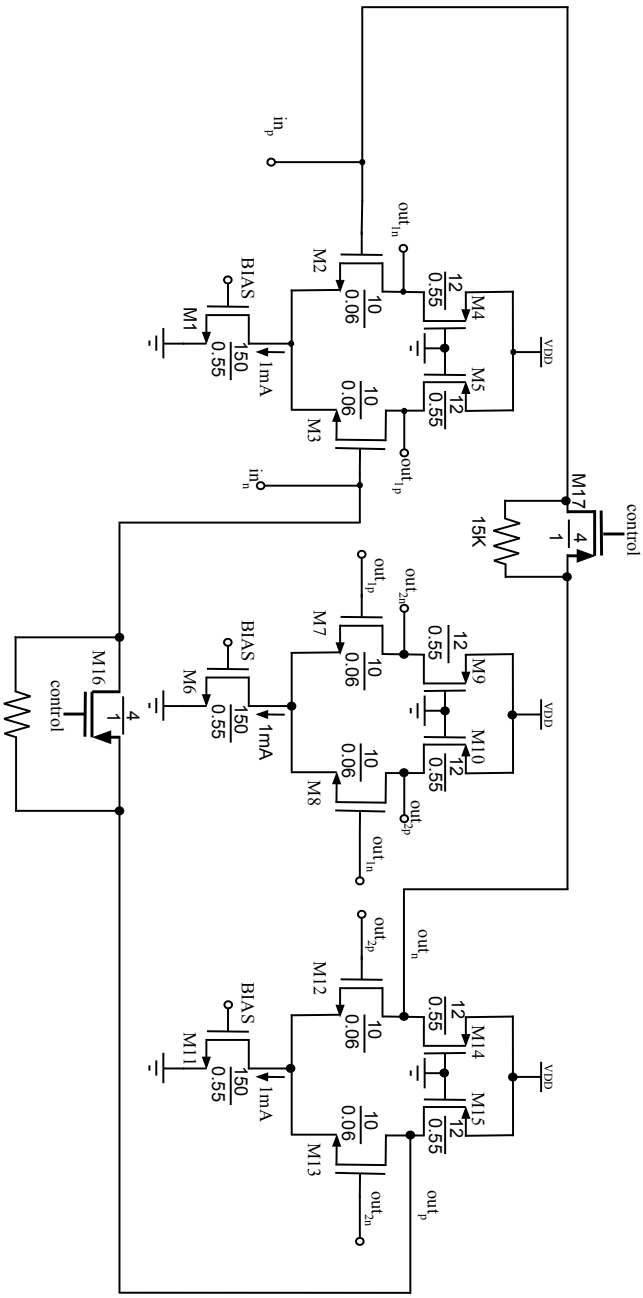

Fig. 4.1: Schematic of transimpedance amplifier

The total voltage gain of the core amplifier is 30dB and BW is $1.75GHz$. The dimensions and bias current are depicted explicitly in the diagram. The output from third stage is feedback to the first stage via PMOS transistors M_{16} and M_{17} to convert the core voltage amplifier to a TIA. M_{16} and M_{17} are biased to operate in a linear region. The "control" signal is used to vary the linear resistance of the feedback transistor. A resistance of $15K\Omega$ is in parallel with PMOS M_{16} and M_{17}. At $0V$ gate volts to PMOS M_{16} and M_{17}, the equivalent impedance is approximately $3K\Omega$. This corresponds to the transimpedance gain of 70dBΩ.

Frequency Response

The frequency response of the core voltage amplifier is depicted in Fig. 4.2. It is observed that, the voltage gain is slightly more than 30dB. The BW is approximately 1.75GHz.

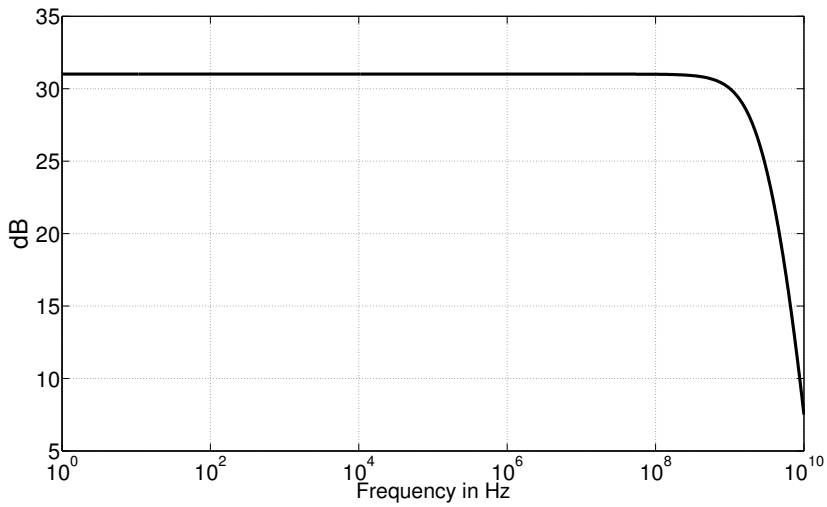

Fig. 4.2: Frequency response of core voltage amplifier

The frequency response of the TIA is shown in Fig. 4.3. The minimum transimpedance gain that can be achieved is more than 70dBΩ. To be precise, it is 72.14dBΩ. The BW observed is 1.3GHz, and phase margin is approximately $50\,^\circ$. The maximum transimpedance gain that can be obtained by contolling the gate voltage of PMOS transistors is 83.27dBΩ. The BW is

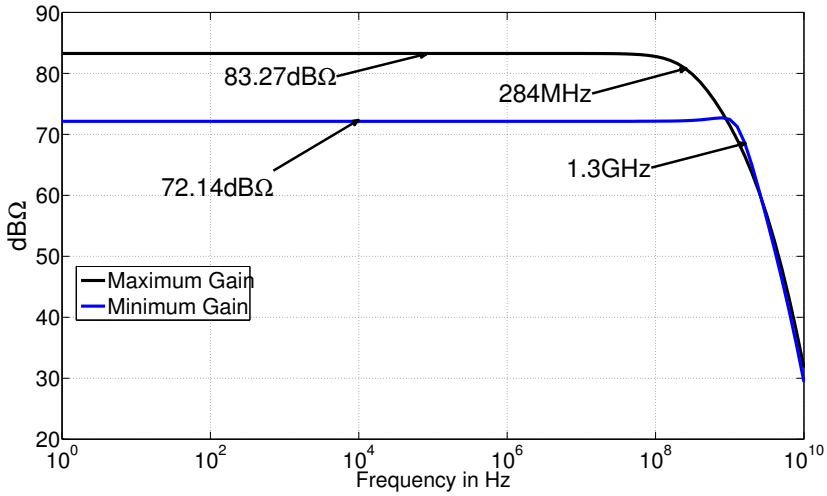

Fig. 4.3: Frequency response of TIA

decreased to 284MHz. Phase margin increases to 52 °. All these values are explicitly shown in Fig. 4.3. Blue response corresponds to minimum gain and the black curve corresponds to maximum gain.

Stability Analysis

The output of the third stage amplifier is passed through "cmdm" probe before connecting them to input gate terminal of input stage via feedback PMOS resistor to check stability conditions. The loop gain magnitude and loop gain phase are plotted in Fig. 4.4. The phase margin is 49.9 degrees when the gain is minimum. The plot in Fig. 4.4 only shows the phase margin for minimum gain case. The phase margin for maximum gain case is 81 degrees. It is not shown in this plot however.

Noise Analysis

The current noise density is plotted in Fig. 4.5. The value of current density in useful range of 100MHz to 1GHz is between $5.78\frac{pA}{\sqrt{Hz}}$ to $28\frac{pA}{\sqrt{Hz}}$. In the plot, where noise is minimum for considerable range of frequency, noise desnsity value is less than $6\frac{pA}{\sqrt{Hz}}$. The total integrated noise from 1Hz to 1GHz is $0.529\mu A_{RMS}$. The noise summary shows that most of noise originates from input common-source differential pair(M_2 and M_3, 33%) and

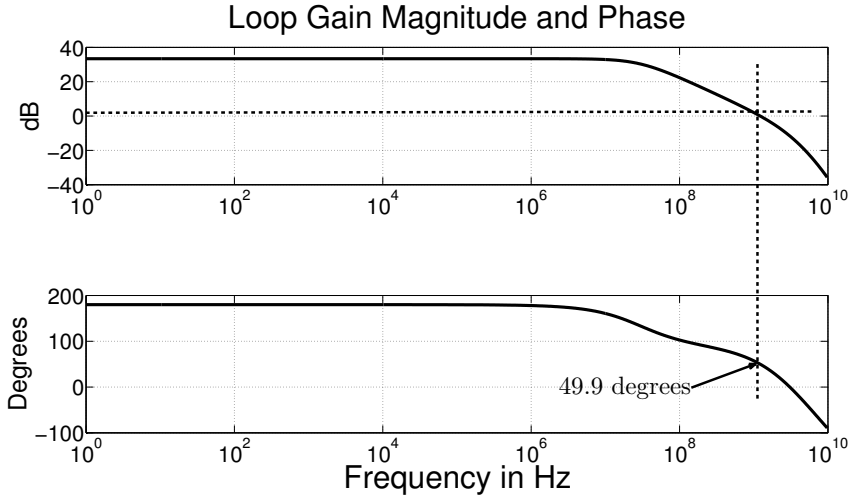

Fig. 4.4: Loop gain magnitude and phase

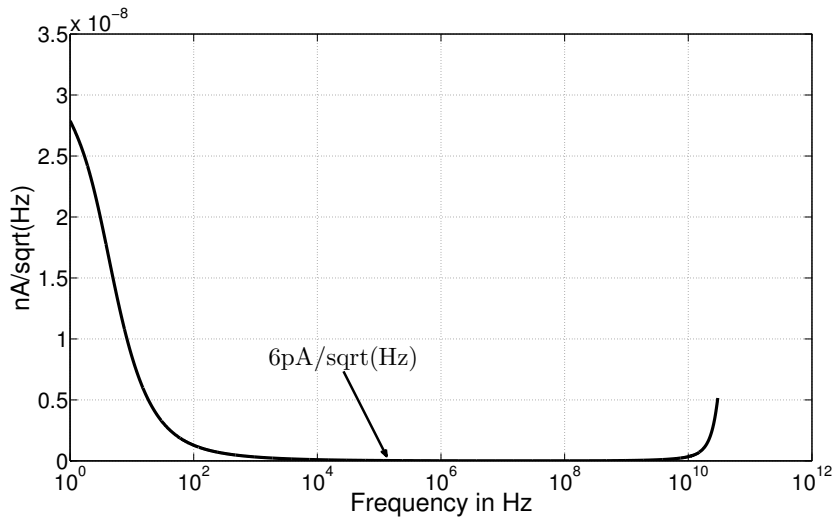

Fig. 4.5: Noise current density

PMOS transistors(M_4 and $M_5, 11\%$). M_7 and M_8 contribute only 3% of total integrated noise. Noise from second stage hardly matters. Improving noise contribution in first stage helps to improve the total noise contribution. One approach of doing it is mentioned in [17]. Here the authors are able to reduce total integrated noise from 302nA to 256nA by making use of a

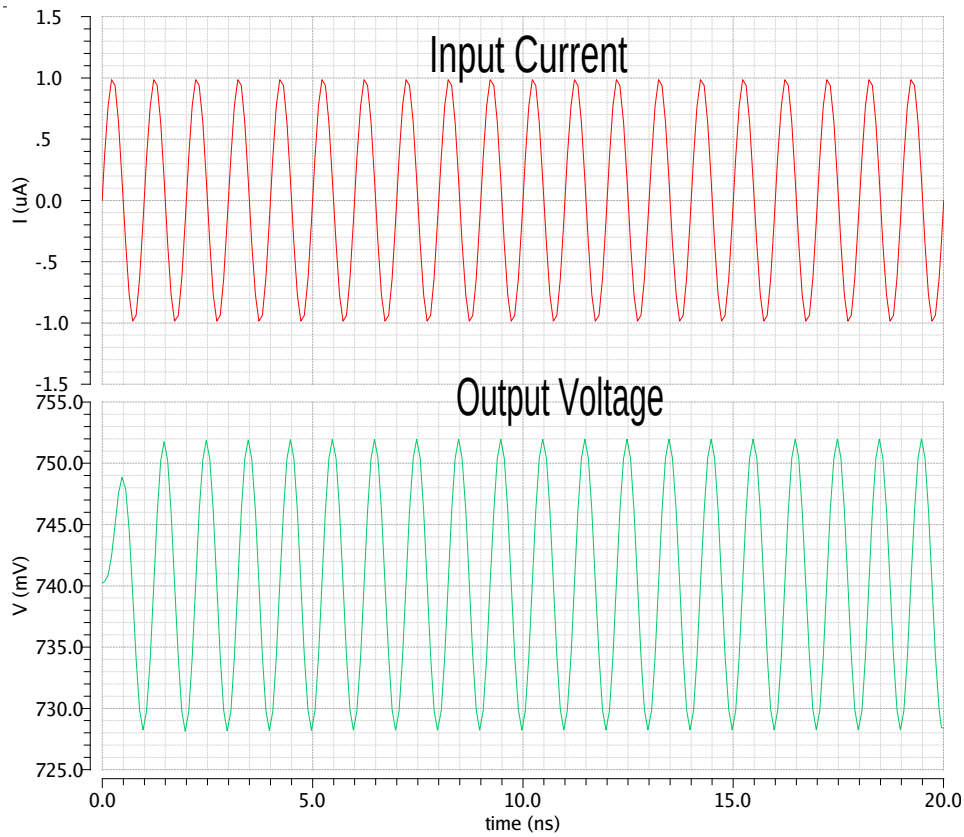

Fig. 4.6: Transient analysis

virtual ground mentioned in [18]. The paper however does not mention the frequency range that was considered in their design. It is assumed that [17] have considered the lowest point in the plot to provide those small values of total integrated current noise. To make use of simple architecture, those approaches are not considered here. The plot in Fig. 4.5 indicates dominant flicker noise at lower frequencies which does not have effect as it can be tuned out with the use of a high pass filter having a low cutoff frequency.

Transient Analysis

Transient simulation result of the TIA circuit is shown in Fig. 4.6. Green plot corresponds to the output signal. The red plot corresponds to the input current signal. The common mode signal at the output is at 740mV. The

input signal is 1μA in magnitude and the transient simulation is run for 20ns.

Table. 4.1 shows the summary of the simulations performed on the TIA circuit.

Table 4.1: Summary of the simulation results of the TIA

Specifications	Value
Minimum Gain	72.14dBΩ
Maximum Gain	83.27dBΩ
Minimum Bandwidth	284MHz
Maximum Bandwidth	1.94GHz
Phase Margin	49.9 °
Input referred Current Noise	$0.529\mu A_{rms}$

4.2 Corner simulations of TIA

The details of all the corner simulations for TIA is provided in Table 4.2. Control voltage is the voltage bias given at the gate terminal of the feedback PMOS transistor. The frequency region of interest is 1Hz to 1GHz while calculating the equivalent input-referred noise. The maximum transimpedance gain that can be achieved is 83dBΩ which corresponds to the control voltage of 1.2V. PMOS are in cutoff region in this case and only the feedback path available is from $15K\Omega$ resistor. It is observed that the best possible bandwidth is achieved for FF corner at 1.94GHz. The worst case bandwidth is observed for SF corner at 1.06GHz. Phase margin is best observed for SF corner while the worst case is observed for FS corner. FF corner consumes the highest power while SS corner consumes the lowest power.

4.3 Equalizer

A source degenerated(SD) amplifier is used to realize the equalizer function. SD is described shortly before delving into the design of the equalizer.

A Source-Degenerated Amplifier

A resistor is placed in series with the source terminal of the common source amplifier in a source-degenerated amplifier as shown in Fig. 4.7. The equiv-

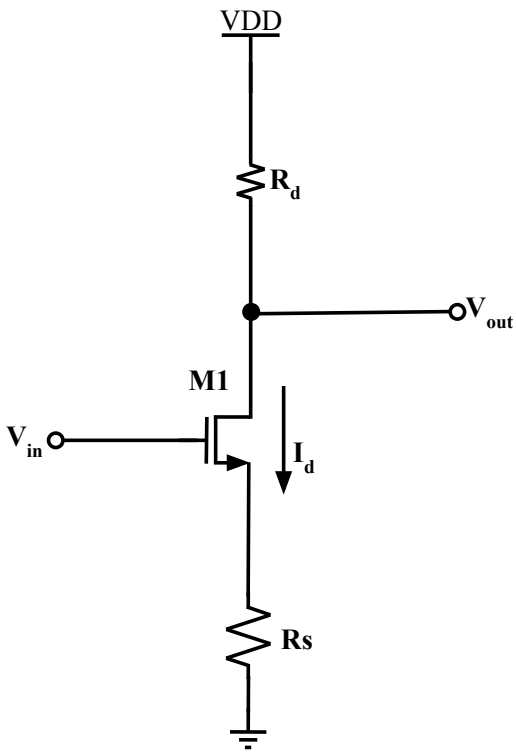

Fig. 4.7: Source degeneration

alent transconducatance of the circuit is derived in [19]

$$G_m = \frac{g_{M1}}{1 + g_{M1} \cdot R_S} \tag{4.1}$$

$$\tag{4.2}$$

And small-signal voltage gain is given by the following expression

$$\begin{aligned} A_v &= -G_{M1} \cdot R_d \\ &= \frac{-g_{M1} R_d}{1 + g_{M1} R_S} \end{aligned}$$

This equation can also be re-written as

$$A_v = -G_m R_d \,||\, R_{out} \tag{4.3}$$

where R_{out} is the output resistance of the input transistor M_1. Since the gain of common source with degeneration is equivalent to

$$A_v = -G_m R_d \parallel (resistance\ seen\ at\ input\ source\ terminal) \quad (4.4)$$

The gain reduces as the total impedance observed at the source terminal of the input transistor happen to decrease. If the source degenerated amplifier is used to form an equalizer circuit, an amplifier is required as a second stage to the equalizer to compensate this decrease in the gain.

Equalizer First Stage

The design of equalizer is centered around finding the number of coefficients described in chapter 3 (section 3.4.1) and implementing the circuit to get the desired characteristics response to compensate the photodiode characteristics response. The transfer function in (2.25) shows that an equalizer should consist of one direct path from input to output and parallel branches of high pass filters with corresponding term in a transfer function. The block diagram used to construct (2.25) as depicted in Fig. 2.9 is designed in transistor level in this section. To design the circuit, the transfer function in 2.25 has to be realized first. The transfer equation mentioned in (2.25) can also be written in the following form [1].

$$\frac{V_{out}}{V_{in}} = E_5$$

$$= \left(1 + \frac{sR_dC_1}{1+sR_1C_1} + \frac{sR_dC_2}{1+sR_2C_2} + \frac{sR_dC_3}{1+sR_3C_3} + \frac{sR_dC_4}{1+sR_4C_4}\right) \quad (4.5)$$

E_5 can be designed using few parallel HPFs according to (4.5). The circuit used in this work is the differential version of the one used in [1]. A source degenerated amplifier with corresponding filter sections indicated in chapter 2 can be used to implement the equalizer. The circuit implemented for an equalizer is presented in Fig. 4.8. The transfer function of this circuit is given by

$$E_5 = \left(\frac{-g_{M1}R_d}{1 + g_{M1}\frac{R_0Z_1Z_2Z_3Z_4}{Z_1Z_2Z_3Z_4+R_0Z_2Z_3Z_4+R_0Z_1Z_3Z_4+R_0Z_1Z_2Z_4+R_0Z_1Z_2Z_3}}\right. \quad (4.6)$$

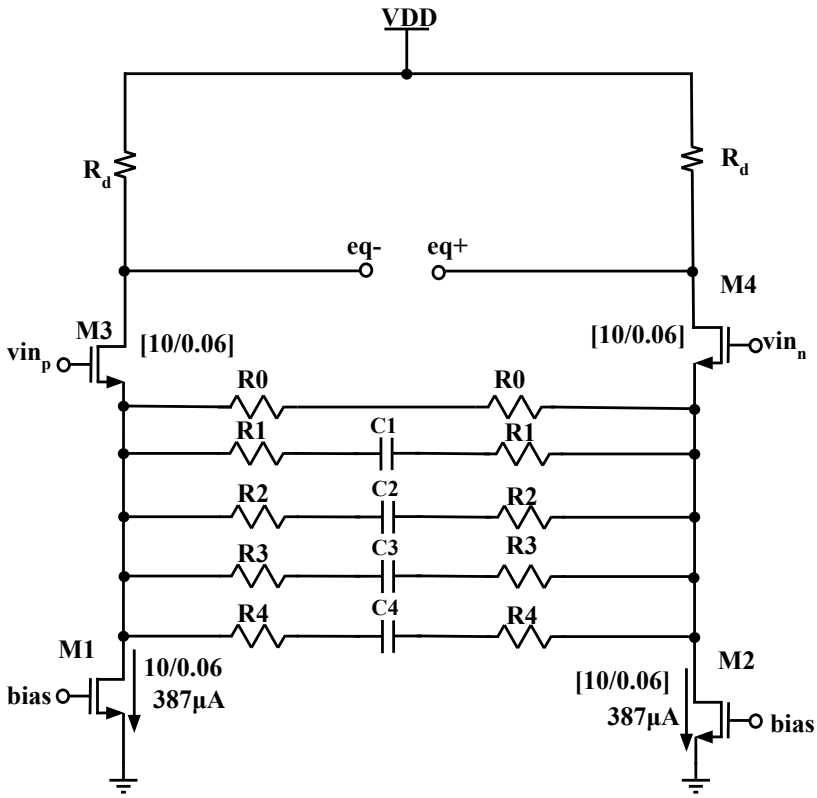

Fig. 4.8: Equalizer first stage

where $Z_i, i = 1, 2, 3, 4$ represent the impedance provided by each section of the filter. E_5 represents the transfer function of an equalizer with five sections in it. To be able to compensate the diode characteristics upto desired frequency range, the pole generated by equalizer output capacitance C_{out} and load resistance R_d should be farther away from the equalization frequency range. The lower is the value of the load resistance, R_d, higher is the bandwidth of this equalizer source degenerated stage. However, this will necessitate R_0, R_1, R_2, R_3, R_4 to be small as well which in turn leads to a higher values of the capacitance values required for each stage of the passive filter. The ratio of R_d/R_4 has to be around 4.0 to be able to compensate the diode response curve [1]. This value matches with the one derived for this

work from verilog-A simulation model. The lower value of R_4 leads to lower impedance value at the source terminal of M_3. All the values for passive components used in the first section of the equalizer sections are tabulated in Table. 4.3. An example is given below to show how the passive components are calculated.

$$\begin{aligned} R_d &= 0.02R1 \\ R_d &= 0.22R2 \\ R_d &= 1.85R3 \\ R_d &= 4.0R4 \\ \frac{R1}{50} = \frac{R2}{4.54} &= \frac{R3}{0.54} = \frac{R4}{0.25} \\ R_d = 500\Omega \Rightarrow C_1 = \frac{1}{2\pi f_1 R_1} &= 3.18pF \end{aligned}$$

The theoretical values derived as in this example are slightly modified to get the desired response curve. The tabulated passive components values are thus slightly different than that can be calculated in this manner with $R_d = 500\Omega$.

SD equalizer tend to reduce some of the gain. An amplifier is required after the first section of the equalizer to compensate this degradation.

Equalizer Second Stage

Fig. 4.9 shows the second stage of the equalizer which is a differential common source amplifier stage. First stage has a loss of 10dB which will be compensated by the second stage. An amplifier with gain of 10dB serves the purpose. This amplifier is similar to the one of the stages of the three stage amplifier designed in TIA circuit. This analysis tallies with the concept of second stage use in [20]. However, the work in [20] is related to designing an equalizer for a USB and not a standard characteristics plot of photodiode as in this work has to be compared with the equalized response. This work requires maximum boosting of signal by 15dB. In [20], the boost is only around 5dB which is not sufficient to compensate the 15dB roll down of photodiode response. The first section of the equalizer in this work thus have more sections than in [20]. Also the second stage gain is more than in that work.

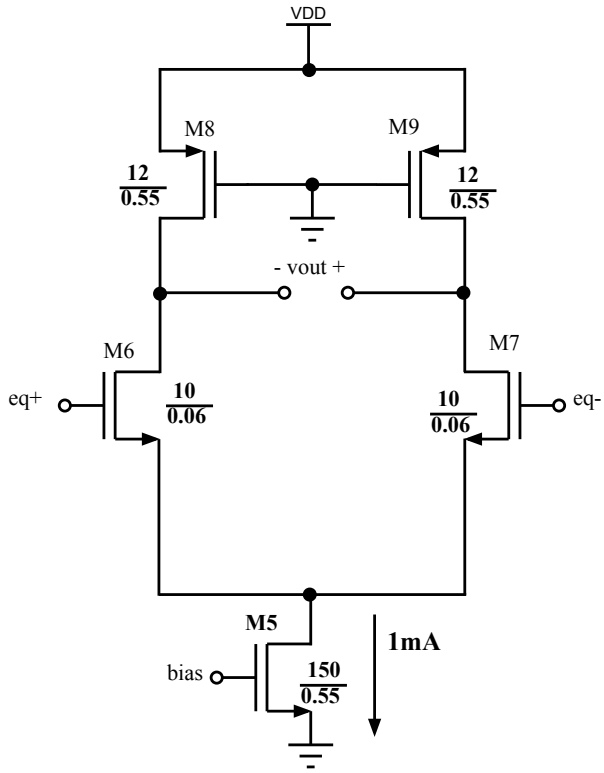

Fig. 4.9: Equalizer second stage

Frequency Response

Frequency response of the equalizer is depicted in Fig. 4.10. The gain is normalized with respect to 0dB. This response corresponds to the typical corner of the transistors and nominal values of the resistive components. As can be observed, the total boost is approximately 15dB from 1MHz to 1GHz. This is what needed to fully compensate the slow roll down introduced by the photodiode characteristics response.

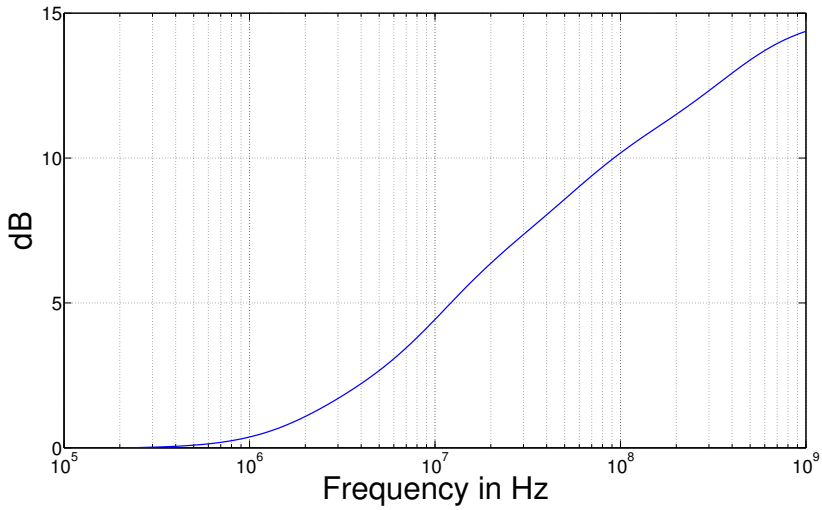

Fig. 4.10: Frequency response of first stage of equalizer

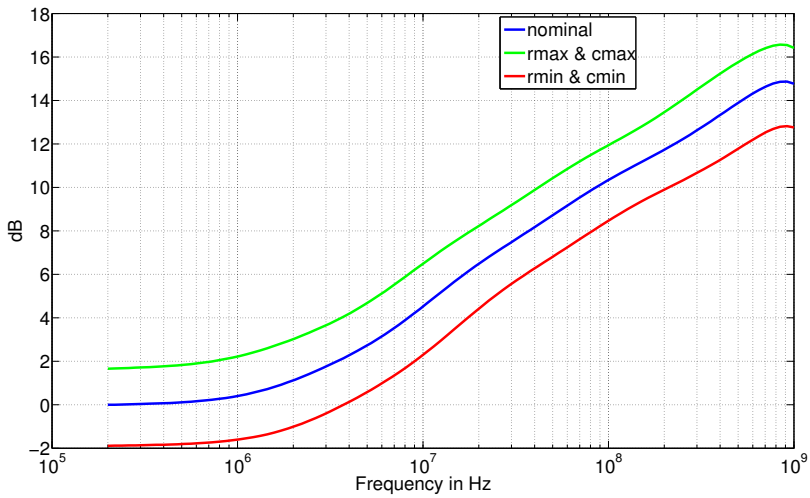

Fig. 4.11: Frequency response of the equalizer in TT process corner

4.4 Corner simulations of equalizer

Due to process variations, the value of resistances can change ±20%. The effect of this variation is discussed here. The main variation comes from the resistor R_d as it changes the gain associated with the input transistor

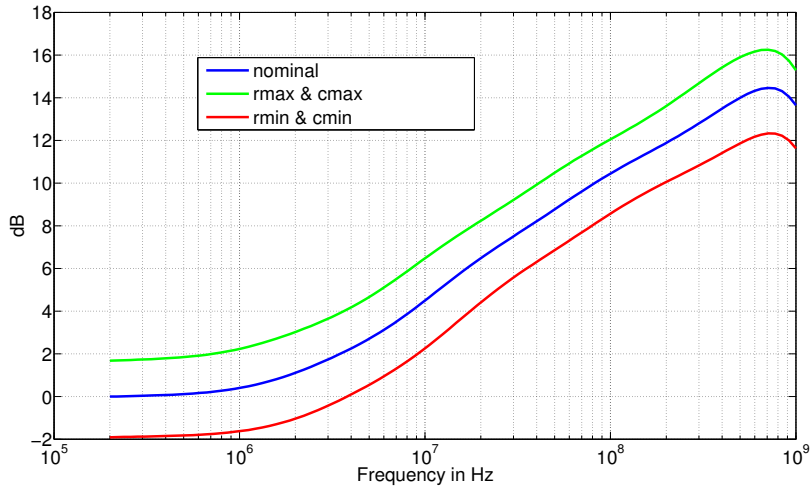

Fig. 4.12: Frequency response of the equalizer in SS process corner

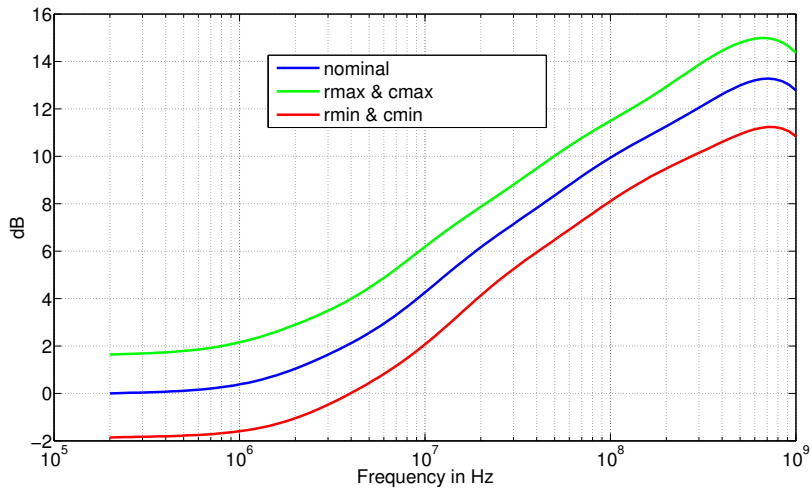

Fig. 4.13: Frequency response of the equalizer in FF process corner

of the equalizer. The resistances and capacitances in the source terminal of the transistor in first section of equalizer have effect in changing the slope of the equalizer response. First TT process corner is discussed. The value of resistances and capacitances are set maximum and the simulation is done. Again, the values of the resistances and capacitances are set at

minimum and the simulation is done. These simulation result alongwith the nominal values of capacitances and resistances are shown in Fig. 4.11. It is observed that the variations in the resistive components usually affects the gain of the equalizer. Fig. 4.12 and Fig. 4.13 shows the same simulation performed for the SS and FF corner of the transistors. It is observed that, the gain changes while the slope remains almost constant in all the cases. The magnitude plots are normalized in Fig. 4.11, Fig. 4.12, and Fig. 4.13.

Area Estimation

The equalizer in this project is simulated in verilog-A and transistor schematic level. The layout of the equalizer circuit is not done. However, to tentatively approximate the area that can be occupied, a very rough sketch level layout approximation is also performed. The analysis showed , the area occupied can be as high as $0.2mm^2$. The equalizer make use of ten resistors and five capacitors. This leads to slightly more area consumption.

Table 4.2: Corner simulations

parameters	[3]	[6]	TT	FF	FS	SF	SS
current(mA)	31.5	7.74	3.77	4.2	3.47	3.64	2.98
VDD(V)	1.8	1.2	1.2	1.2	1.2	1.2	1.2
power(mW)	56.7	9.3	4.52	5.04	4.16	4.36	3.57
transimpedance gain($dB\Omega$)	73.9	49.37	72.14	71.87	73.48	69.85	71.3
input referred noise RMS(A_{rms})	659n	2.8u	0.529u	0.516u	0.515u	0.55u	0.564u
BW(GHz)	2.71	2.9	1.43	1.94	1.7	1.06	1.17
phase margin($^\circ$)	69	69	53	61	48	65	56
control(mV)	$\cdots$	$\cdots$	420	400	370	450	420

Table 4.3: Component values

Resistances	Values(Ω)	Capacitances	Values(pF)
R_0	10K	C_1	6.5
R_1	4K	C_2	4.6
R_2	960	C_3	1.7
R_3	423	C_4	1.5
R_4	0	–	–
R_d	500	–	–

CHAPTER 5

Results

5.1 System Simulation Result

The system simulation result obtained from the schematic level design is discussed in this chapter. Fig. 5.1 shows the total system simulation result in a single plot. The red curve in Fig. 5.1 represents the photodiode response. The green curve represents the equalizer response. The blue curve represents the response from the TIA. The black curve represents the total equalized response. The bandwidth of the photodiode response is 6.25MHz as discussed in chapter 2. The frequecncy response plot(blue curve) of TIA obtained from schematic level shows that the 3-dB bandwidth obtained is higher than 1GHz. The 3-dB bandwidth of the system is observed to be greater than 1GHz(black curve). All these responses are normalized plot.

Fig. 5.2 shows the equalization response with FF process corner while Fig. 5.3 shows the simulation result for SS process corner. FF stands for fast NMOS and fast PMOS process corner while SS stands for slow corner for NMOS and slow corner for PMOS. The photodiode response is also shown (red curve) in these plot. The black curve represents the equalizer response while the green curve represents the equalized system response. The performance of

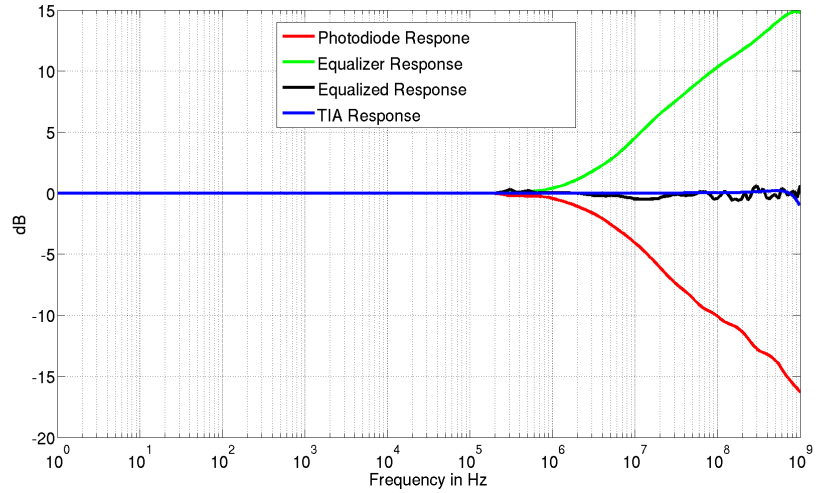

Fig. 5.1: System simulations result

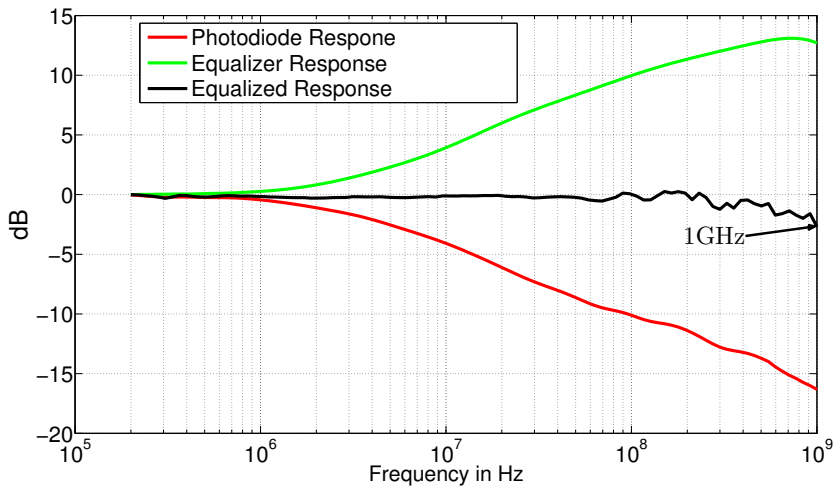

Fig. 5.2: System response with FF corner(minimum capacitance,minimum resistance)

the design is tabulated in Table. 5.1. BW_{worst} and BW_{best} denote the worst and the best equalized bandwidth respectively that can be achieved. The worst BW is observed for SF process corner(nominal resistance and nominal capacitance).

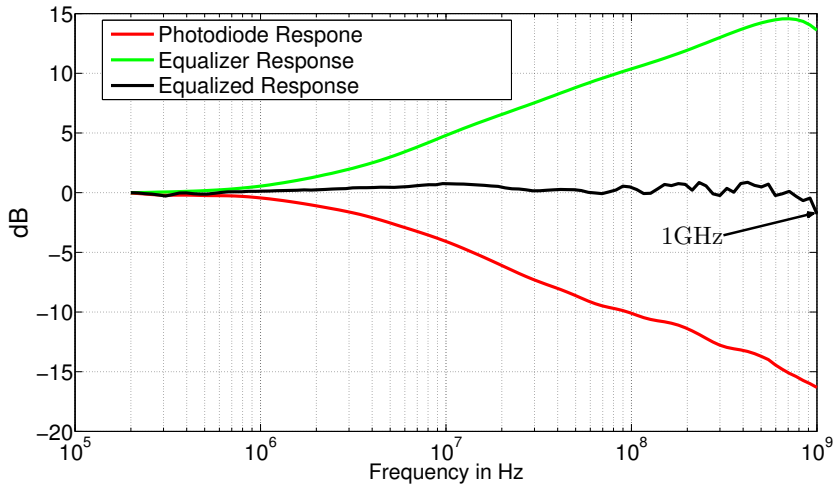

Fig. 5.3: System response with SS corner(maximum capacitance,maximum resistance)

Table 5.1: Performance summary

Parameters	Values
Technology	65nm CMOS
VDD	1.2V
BW_{best}	1GHz
BW_{worst}	841MHz
Power Consumption	7mW
Area occupied	$0.2mm^2$

CHAPTER 6

Conclusions

6.1 Conclusions

The study of an equalizer for an integrated optical receiver is carried out in this thesis work. A receiver chain consisting of a photodiode, TIA and an equalizer is implemented in verilog-A and schematic level. Three stages of differential common-source amplifier are used to implement TIA. The transimpedance gain of TIA is 70dBΩ and 3dB bandwidth is 1.3GHz. A source-degenerated differential common source equalizer section is implemented. The total magnitude response of the design is able to realize compensation until 1GHz from 6.25MHz. Corner simulations are performed to ensure the robust operation. The worst bandwidth is observed for SF process corner with 841MHz. The circuit consumes 7mW from a 1.2V voltage supply.

6.2 Future Works

The future work can include the layout design for the current work. The design can make use of noise cancelling techniques in transimpedance amplifier design which is in itself a huge topic. It can also include all the components of an optical receiver in the receiver chain in which case the project can be a

large one. Layout design to this big design can be a rewarding task. In this project, the total power consumption is significantly less than recent work compared in this report. The future work can further look into low power design with power consumption less than 1mW.

APPENDIX A

Verilog-A code

A.1 Verilog-A code for TIA Section

```
`include "constants.vams"
`include "disciplines.vams"
module tia(in1,in2,out1,out2);
input in1,in2;
output out1,out2;
electrical in1,in2,out1,out2;
parameter real vgain=46.77;
real outputvoltage;
parameter real R1=3e3;
parameter real R2=3e3;
analog begin
outputvoltage=vgain*V(in1,in2);
V(out2,out1)<+outputvoltage;
end
endmodule
```

A.2 Verilog-A code for Equalizer Section

```
`include "constants.vams"
`include "disciplines.vams"
module equalizer(in1,in2,out1,out2);
inout in1,in2,out1,out2;
electrical in1,in2,out1,out2;
electrical n1,n2,n3;
electrical n4,n5;
parameter real w1=0.02;
parameter real w2=0.220;
parameter real w3=1.87;
parameter real w4=4.6;
parameter real f1=1e6;
parameter real f2=10e6;
parameter real f3=188e6;
parameter real f4=4.1e9;
analog begin
V(n1,out2)<+laplace_nd(V(in1,in2),{1.0},{1.0});
V(n2,out2)<+laplace_nd(V(in1,in2),{1.0,1.0},{f1,1.0});
V(n3,out2)<+laplace_nd(V(in1,in2),{1.0,1.0},{f2,1.0});
V(n4,out2)<+laplace_nd(V(in1,in2),{1.0,1.0},{f3,1.0});
V(n5,out2)<+laplace_nd(V(in1,in2),{1.0,1.0},{f4,1.0});
V(out1,out2)<+V(n1,out2)+w1*V(n2,out2)+w2*V(n3,out2)
             +w3*V(n4,out2)+w4*V(n5,out2);
end
endmodule
```

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