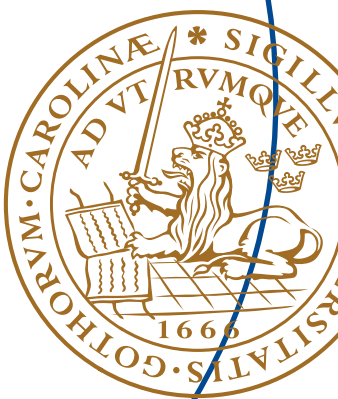
Master's Thesis

Optimization of Standard Cell Architecture for Advanced Technology Node

Bhavana Ballal



Department of Electrical and Information Technology,
Faculty of Engineering, LTH, Lund University, August 2014.

Master's Thesis

Optimization of Standard Cell Architecture for Advanced Technology Node

By

Bhavana Ballal

Department of Electrical and Information Technology,
Faculty of Engineering, LTH
Lund University
SE-221 00 Lund, Sweden

Abstract

As the transistor size reduces in the traditional manufacturing process, the short channel effects become prominent. There is a shift in industry from tradition CMOS to FinFET for better scalability and performance. FinFET has a number of design challenges due to its 3D structure, which has to be addressed to reduce its drawbacks and make it more suitable for replacements of traditional CMOS. This thesis explores the FinFET Technologies, its manufacturing Processes and discusses the design and optimization of standard cell architectures designs for Advanced Technology nodes using IMEC's Design Rules. Comparison and Analysis is done for different architecture designs and the Power Consumption is analyzed for design variants introduced in the same architectures of Standard Cells.

Acknowledgments

I would like to thank Mr. Diederik Verkest, Director of Logic Insite Group and Mr. Julien Ryckaert, Manager of Logic Insite Group for giving me an opportunity to work at IMEC, Belgium and Dr. Arindam Mallik and for mentoring me throughout my thesis work.

I would also like to thank Asst. Prof. Markus Tormanen and Dr. Carl Bryant from the Department of Electrical and Information Technology, Lund University for their supervision and support in completion of the thesis.

A Special thanks to all my friends and family, who have been with me throughout the completion of my project.

Bhavana Ballal

Contents

Abstract	ii
Acknowledgements	iii
Contents	4
Chapter 1 – Introduction	12
1.1 CMOS to Non Classical CMOS	12
1.1a Scaling theory	12
1.1b Drivers of scaling	14
1.1c Challenges in Scaling	15
1.1d Roadmaps	16
Chapter 2 - FinFET – the next big nano FET	18
2.1a Insight into a FinFET	18
2.1b FinFET Working Principle	19
Chapter 3 - Development of FinFET standard cell architecture	21
3.1 Lithography Processes used to develop beyond 22nm	21
3.2 Development of SADP standard cell architecture	26
3.2a Layers used in Standard cell architecture	26
3.2b Steps in standard cell architecture	36
Chapter 4 - Optimization of the Library	40
4.1 Challenges in optimization	41
4.2 Types of Architecture	43
Chapter 5 - Result and Analysis	56
5.1 Circuit Setup	56
5.2 Delay of Different Types Of Layout Designs	63
5.3 Power Consumption of Different Types Of Layout Designs	72
5.4 Improvised Design Layouts	87
5.5 Power Delay Product	94
Chapter 6 - Conclusion	99
Bibliography	101

List of Figures

1	Principles of constant-electric field scaling for MOS Transistors and integrated circuits	13
2	Technology vs. Gate length, Oxide thickness and Vdd	16
3	ITRS FinFET Technology Roadmap	17
4	Traditional 2-D planar transistor form a conducting channel in the silicon region under the gate electrode when in the “on” state	18
5	3-D Tri-Gate transistor form conducting channel on three sides of a vertical fin structure, providing “fully depleted” operation	18
6	Manufacturing Process of LELE Process	22
7	Manufacturing Process of LFLE PROCESS	23
8	Manufacturing Process of SADP PROCESS (IMEC Process)	24
9	SOI FinFET and Bulk FinFET	25
10	Poly Layers used in cell architecture	26
11	IMEC Fin Patterning Process	27
12	Fincore, Finnocut and Fin layers	27
13	Fincore, Finnocut and Fin in cadence software	28
14	Interconnect Layer IM1	28
15	Interconnect Layers IM2, namely IM2A and IM2B	29
16	Metal1 (M1) Core layers	30
17	Metal1 (M1) Core and Metal1 noblock layers	30
18	Metal1 (M1) layers: M1A and M1B Layers	31
19	Via0	32
20	Gate Open Layer	33
21	Cross-section view of different layers and their connections possible	34

22	Power rails Vdd and ground and the track height	35
23	Poly and polynocut layers	35
24	Placement of fins	36
25	Placement of Interconnect Layers IM1	37
26	Placement of Interconnect Layers IM2A and IM2B	37
27	Placement of Vias	38
28	Placement of Nwell, Pwell layers	38
29	Standard cell with 10 track height with 2 fins	40
30	Standard cell with 6 track height with 1 fin	41
31	Standard cell with only 1 dummy fin core	41
32	Proposed design architecture, but need for optimization	42
33	Architecture with IM2 layers crossing over the active poly	43
34	12track-2 fins inverter architecture	44
35	12track-2 fins NAND architecture	44
36	2track-2 fins NOR architecture	45
37	12track-2 fins AOI-21 architecture	45
38	12track-2 fins AOI-22 architecture	46
39	12track-3 fins Inverter architecture	46
40	12track3 fins Nand architecture	47
41	12track-3 fins NOR architecture	47
42	12track-3 fins A0I-21 architecture	48
43	12track-3 fins A0I-22 architecture	48
44	12track-4 fins Inverter architecture	49
45	12track-2 fins Nand architecture	49
46	12track-2 fins NOR architecture	50
47	12track-2 fins AOI-21 architecture	50
48	9track-2 fins Inverter architecture	51
49	9track-2 fins Nand architecture	51
50	9track-2 fins NOR architecture	52
51	9track-3 fins Inverter architecture	52
52	9track-3 fins Nand architecture	53

53	9track-3 fins NOR architecture	53
54	9track-3 fins AOI-21architecture	54
55	9track-3 fins AOI-22architecture	54
56	12 Track -2 fins Ring –Oscillator	55
57	12 Track -3 fins Ring –Oscillator	55
58	12 Track -4 fins Ring –Oscillator	55
59	Test Bench of Inverter	57
60	Test Bench of Nand Gate	58
61	Test Bench of Nor Gate	60
62	Test Bench of AOI-21 Gate	61
63	Test Bench of AOI-22 Gate	63

List of Tables

1	General rules for scaling proposed by Baccarani	13
2	Inputs for an Inverter	56
3	Setup Conditions for Inverter	56
4	Inputs for Nand Gate	57
5	Set Up Conditions for a Nand Gate	58
6	Inputs for Nor Gate	59
7	Set up conditions for Nor gate	59
8	Inputs for AOI-21 Gate	60
9	Set-up conditions for AOI-21 Gate	61
10	Inputs for AOI-22 Gate	62
11	Set up conditions for AOI-22 Gate	63

List of Graphs

1	Delay of Inverter with different capacitor Loads for a Baseline Layout	64
2	Delay of Nand Gate with different capacitor Loads for a Baseline Layout	64
3	Delay of Nor Gate with different capacitor Loads for a Baseline Layout	65
4	Delay of AOI-21 Gate with different capacitor Loads for a Baseline Layout	65
5	Delay of AOI-22 Gate with different capacitor Loads for a Baseline Layout	66
6	Delay of Inverter with different capacitor Loads for a Optimized Layout	67
7	Delay of Nand Gate with different capacitor Loads for a Optimized Layout	67
8	Delay of Nor Gate with different capacitor Loads for a Optimized Layout	68
9	Delay of AOI-21 Gate with different capacitor Loads for a Optimized Layout	68
10	Delay of AOI-22 Gate with different capacitor Loads for a Optimized Layout	69
11	Delay of Inverter Gate with different capacitor Loads for a 3 - Fins Layout	70
12	Delay of Nand Gate with different capacitor Loads for a 3 - Fins Layout	70
13	Delay of Nor Gate with different capacitor Loads for a 3 - Fins Layout	71
14	Delay of AOI-21 with different capacitor Loads for a 3 - Fins Layout	71
15	Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=1ns	72
16	Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=2ns	73
17	Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=4ns	73
18	Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=8ns	74
19	Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=16ns	74
20	Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=1ns	75
21	Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=2ns	76
22	Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=4ns	76

23	Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=8ns	77
24	Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=16ns	77
25	Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=1ns	78
26	Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=2ns	79
27	Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=4ns	79
28	Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=8ns	80
29	Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=16ns	80
30	Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=1ns	81
31	Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=2ns	82
32	Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=4ns	82
33	Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=8ns	83
34	Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=16ns	83
35	Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=1ns	84
36	Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=2ns	85
37	Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=4ns	85
38	Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=8ns	86
39	Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=16ns	86

40	Comparison of Delay of a Inverter with 5 different Layout Designs	88
41	Comparison of Delay of a Nand Gate with 5 different Layout Designs	88
42	Comparison of Delay of a Nor Gate with 5 different Layout Designs	89
43	Comparison of Delay of a AOI-21 Gate with 5 different Layout Designs	89
44	Comparison of Delay of a AOI-22 Gate with 4 different Layout Designs	90
45	Comparison of Power Consumption of a Inverter with 5 different Layout Designs	91
46	Comparison of Power Consumption of a Nand Gate with 5 different Layout Designs	91
47	Comparison of Power Consumption of a Nor Gate with 5 different Layout Designs	92
48	Comparison of Power Consumption of a AOI-21 Gate with 5 different Layout Designs	93
49	Comparison of Power Consumption of a AOI-22 Gate with 4 different Layout Designs	94
50	Power- Delay Product for inverter with different combinations of track height and fins	95
51	Power- Delay Product for Nand Gate with different combinations of track height and fins	95
52	Power- Delay Product for Nor Gate with different combinations of track height and fins	96
53	Power- Delay Product for AOI-21 Gate with different combinations of track height and fins	96
54	Power- Delay Product for AOI-22 Gate with different combinations of track height and fins	97
55	Power- Delay Product for Ring- Oscillator with different combinations of fins and capacitor load of 1fF	97
56	Power- Delay Product for Ring- Oscillator with different combinations of fins and capacitor load of 5Ff	98
57	Power- Delay Product for Ring- Oscillator with different combinations of fins and capacitor load of 10fF	98

Chapter 1

INTRODUCTION

Motivation

The motivation behind this project is to focus on studying the FinFET device manufacturing process in a foundry. Further study is done on designing and optimizing the standard cell Layout design and evaluating one of the main drivers of technology scaling i.e. Power consumption using these layout design variants and deciding the optimum Layout architectures. Power consumption plays one of the prominent roles and is the motivation for the semiconductor industry to scale down to next technology node.
Hence for the current version of a developing PDK (Process Design Kit), one of the Figure of merit for a standard cell performance namely power delay product is calculated for the basic standard cells .The Power delay product is analyzed and compared to different variant of finfets namely number of fins and height of the cell for the current version of IMEC's Design rules. Hence based on the conclusion of the performances of different types of fins and layout architectures, the data is given to the IMEC foundry which helps in optimizing the developing PDK ((Process Design Kit).

1.1 CMOS to Non Classical CMOS - Small is Big

"The number of transistors on a chip will double approximately every two years "as stated by Gordon Moore, has been one of the most crucial and revolutionary law steering the Semiconductor Industry.

Scaling: The demand for better performance, low power and cost, faster and compact devices have been the driving forces for the semiconductor industry to move from micrometer to nanometer regime during the last two decades. Transistors today are extremely small (about 10nm) as compared to its predecessors and are further scaled down, much lesser than a Human blood cell.By comparison a human red blood cell is 7,500 nm and a strand of DNA is 2.5 nm

1.1a Scaling principle: Robert Dennard and Baccarani proposed the two main scaling Theories [1].

Robert Dennard during 1970's gave a insight into future of scaling. According to him reducing the dimensions of the MOS transistors and the wires connecting them is the simple basic idea of Scaling.

He defined Constant electric field scaling Theory, where the same electric field are achieved during scaling of transistors by reducing the applied voltage, thickness of insulating oxide between the silicon substrate and gate. The field is further maintained constant by increasing the impurity doping concentration.

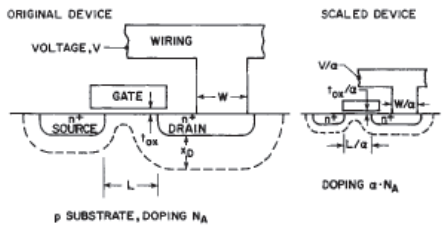


Figure 1. Principles of constant-electric field scaling for MOS Transistors and integrated circuits[1]

One of the important conclusion from the Constant Electric field scaling is the power dissipation factor is reduced by $1/\alpha^2$, as the voltage and current is reduced in each device. Hence its possible to keep the same power, but increase the chip density. But the disadvantage of this theory is that reducing the threshold voltage of the device, increases the leakage current of the device, which limits the scaling of threshold voltage at a point.

In the year 1984, Baccarani, proposed a generalized set of scaling rules. According to Baccarani, the basic idea is to relax the pace of scaling of voltage, and improve the channel impurity concentration by a factor αk, where k is a scaling factor and α is a additional scaling factor >1

Table 1. General rules for scaling proposed by Baccarani [2]:

Scaled Parameters	Constant Field Scaling	Generalized Scaling	
Dimensions *(L, W, t_{ox} X_j)*	$1/k$	$1/k$	
Voltage *(V)*	$1/k$	α / k	
Doping concentration *(N_a N_d)*	k	αk	
Electric Field *(E)*	1	α	
Depletion-Layer width *(W_d)*	$1/k$	$1/k$	
Capacitance *($C = \varepsilon A/t_{ox}$)*	$1/k$	$1/k$	
Inversion Charge Density *(Q_{inv})*	1	α	
Carrier Velocity *(v)*	1	α (Long ch.)	1(Vel. Sat.)
Current, drift *(I)*	$1/k$	α^2/k	α / k
Delay time/circuit *($r \sim CV/I$)*	$1/k$	$1/\alpha k$	$1/k$
Power dissipation/circuit *($P \sim VI$)*	$1/k^2$	α^3/k^3	α^2/k^2

Power-delay product/circuit (P_T)	$1/k^3$	α^2/k^2
Circuit density (α 1/A)	k^2	k^2
Power density (P/A)	1	α^3 α^2

Baccarani's theory introduces increase in Voltage and current in short channel devices and thereby comparing with the Dennard's principle of constant field-power scaling, the power dissipation increases [2]. This affects the further shrinking of devices.

Hence miniaturization of semiconductor devices is a complex process. Scaling down considering all the factors is not possible beyond 90nm In order to keep up with the Moore's Law, devices have been smartly modified like the Finfets.

1.1b Drivers of Scaling:

The main elements, which drive the technology scaling, are Power, Performance, Area and Cost. The basic rule followed by the designers in the semiconductor industry is

a) Power for every next technology is expected to reduce ideally by 30%.

b) Performance is expected to improve by 30%

c) As the scaling enters the nanometer regime, chips are more compact, hence the area has to be reduced by 50%

d) One of the key factors in technology scaling is the Cost and it is expected to reduce by 50%.

Power plays a key role in scaling technology. With every next emerging technology, lesser power and better performance are expected. As seen in the previous technology nodes, it's tricky to deal with power and performance, as lowering energy may result with poor performance circuits. Vdd scaling is the key to reduce Power crisis. It is known that, low Vdd is near the end of roadmap (~0.5 V) and sets new challenges for future scaling. Another major factor affecting the scaling and contributing for high power and low performance as the transistor shrinks is the tunneling current through the gate oxide.[3] (ITRS 2012)

Most of the semiconductor companies do not prefer to move to the next technology node, if the cost is not substantially reduced by 50%. Hence the Processing technology plays a key rule, as the Mask set and the tools for printing the devices on to the chip play a major role in deciding the effective cost for manufacturing devices.

1.1c) Scaling Challenges: As the size of the transistor is scaled with the advancement of every technology node, the design challenges increases by a greater amount, especially when the device transformation is from CMOS to non CMOS devices.[5]

The key design challenges are

Patterning

Optical Lithography is the most frequently used technique for patterning. With the advancement of technology nodes, Optical Lithography has also been used for sub wavelength imaging. In the past 180nm technology, krypton Flouride laser light was introduced with a wavelength of 248nm. And for 130nm, argon Fluoride (ArF) having a wavelength of 193nm was used.[4]

With the progression of smaller transistors, several Resolution enhancement techniques had to be introduced along with the Optical Lithography tool. For such sub wavelength lithography, one of the popular enhancement techniques know as Optical Proximity Correction and Phase shifting Masks has been used.

Hence for such sub wavelength imaging, the design rules for designing a transistors would be more complex.

Power and Performance: One of the biggest and a tricky challenge is to maintain a good tradeoff between Power and Performance and improve the yield of production of chips. This basically splits priority in chip designing into two different application requirements.

They are

a) High Performance Applications: The need for high performance is mainly needed for microprocessor chips. Hence the main aim during high performance applications would be speeding up the transistors, but this in turn would result in high leakage current.

b) Low Power Applications: Low power is the one of the drivers of scaling transistors. Low power would mostly be needed in communication devices. This can be achieved by reducing the leakage currents, but the speed of the circuits is affected.

The image below shows the downscaling of Vdd and Oxide thickness. In order to further decrease oxide thickness and reduce excessive gate leakage, high k dielectrics was introduced.

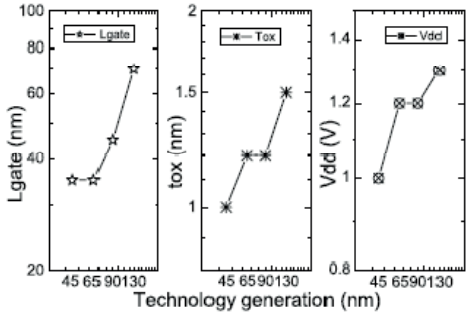


Fig 2. Technology vs Gate length, Oxide thickness and Vdd[5]

1.1d) Futuristic Roadmaps

ITRS had defined that a the half pitch of Dynamic Random Access Memory (DRAM) or the half pitch of metal 1 (M1) interconnects of Microprocessor unit (MPU)/Application-specific integrated circuit (ASIC) depending on the relevant Technology driver, defines technology generation. [6]

Below the image shows the Finfet Technology Roadmap as designed by ITRS. It shows a transition from planar to non planar from 22nm.

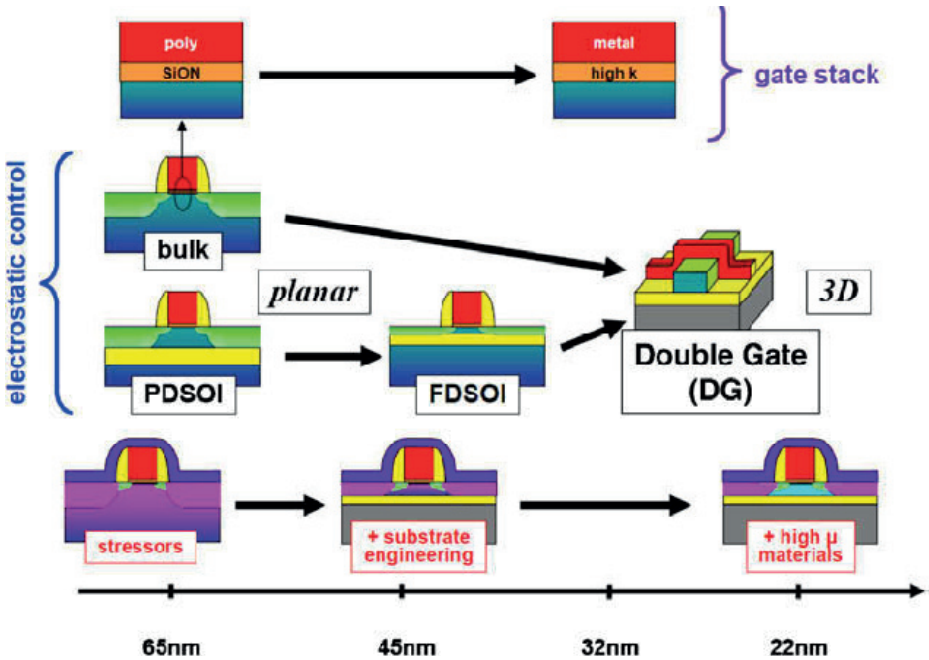


Fig 3: ITRS FinFET Technology Roadmap

Chapter 2

2.1 FINFET – the next big nano FET

2.1a) Insight into a FinFET:

FinFET is a three dimensional revolutionary device, which has helped to push scaling further down to nanometer scale. The exotic extended gate structure of FinFET has increased thrice the surface area for electrons to travel and also helped tremendously to overcome the scaling issues posed by MosFET. Due to the vertical structure of the gate, the stress profile of the device is different as compared to MosFET.[6]

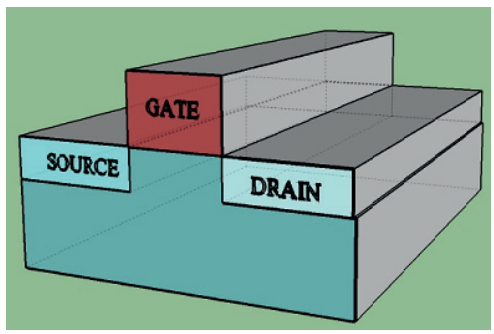


Figure 4: Traditional 2-D planar transistor form a conducting channel in the silicon region under the gate electrode when in the "on" state

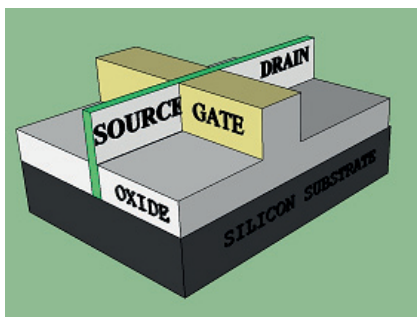


Figure 5: 3-D Tri-Gate transistor form conducting channel on three sides of a vertical fin structure, providing "fully depleted" operation

2.1 b) FinFET Working Principle:

Working of a FinFET is similar to a conventional MosFET. In FinFET, channel of the transistor, extends out from the wafer, and allows the gate to wrap around and cover both sides of the FinFET channel. In FinFET, gate has better control of current flowing, and hence helps to reduce the short channel effects.

In the ON state there is greater flow of electrons because of the increased surface area, hence increases the electron mobility. In the OFF state, the gate has a better control over the channel and hence the transistor leakage is low. [6]

In finfet the gate wraps around the channel and hence provides better electrostatic control of the device. In Finfet the width of the gate of the fin is measured as the sum of Fin with and twice the fin height. The gate length is the measured in parallel to the length of the fin. Spacers are introduced across the finfets. The main advantage of spacers is reduction in subthresold slope and DIBL [8]
. At constant leakage current ON current increases, as the width of the spacer increases , due to the reduction in sub threshold slope. But ON current starts to decline as the Access Resistance appears. Access Resistance varies with the width of the spacer.

Challenges:
The main challenge in FinFET based circuits design is since it is a 3 dimensional structure; it introduces additional parasitic capacitances, which need to be as minimum as possible in order to optimize the performance of the FinFET devices. Additionally the increased Fin Height would introduce more transistor density.
Manufacturing a FinFET with critical dimensions with small scale features pose a process challenge for the Finfets.

FinFET Applications:

1. Low power design in digital circuit, such as RAM, because of its low off-state current.
2. Power amplifier or other application in analog area, which requires good linearity.

Advantages:

1. Superior Scalability. The extended gate achieves intrinsic gain for smaller transistors compared to the conventional MosFET.
2. Lower off-state current compared to bulk MosFET. Promising matching behavior.
3. Reduced leakage current, threshold voltage and Power
4. Multi Fin design can be used for faster Performance.
5. FinFETs are up to 35% faster, using lesser than half the dynamic power and reduces static leakage current by as much as 90%. [6]
6. Devices run faster with the same power compared to MosFET.

Disadvantages:

1. The Overlap capacitance is high
2. High Parasitic Resistance. This is the major design challenge as it lowers speed and increases noise
3. The production cost is marginally higher than the conventional technology

CHAPTER 3

Development of FinFET standard cell architecture

3.1) Lithography Processes used to develop beyond 22nm

The manufacturing processes get more complex with the shrinking of the devices. The conventional lithography processes are not suitable for Finfets. Hence single patterning Lithography techniques are now converted to Double patterning techniques for finfet devices. As the manufacturing processes continue to get more complex, the cost of the processes increases. With the shrinking technology , more layers are also introduced to reduce the layout densities and to make the layout more uniform to ease the manufacturing process.

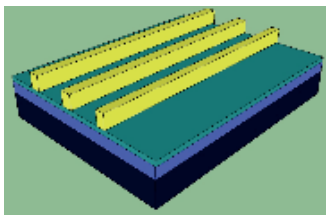
There are three main Lithography techniques. The Three main Lithography Techniques for Double patterning [11] used in the foundries are

- Litho Etch Litho Etch (LELE)
- Litho Freeze Litho Etch (LFLE)
- Self Alignment Double patterning (SADP)

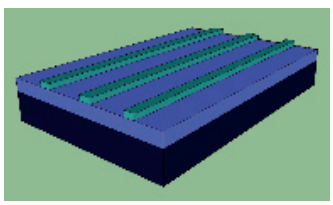
1) Litho Etch Litho Etch (LELE)

LELE is a double line process. Which involves two lithography steps? The first step will involve the deposition of the resist and exposure of the pattern. In the second step the pattern is etched on the hard mask. This followed by another deposition of resist and transferring of the pattern. Here Overlay alignment is very critical for the process. This is followed by the etching of the second pattern. The pattern pitch density is thus doubles. The final step will be the rinsing of masks.

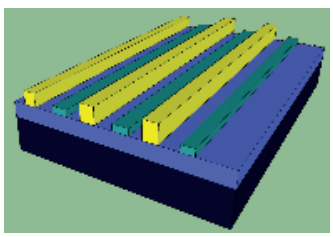
1) Litho 1. First Pattern exposure on hard mask



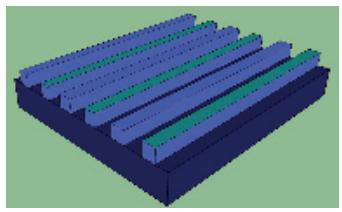
2) Etch 2. Pattern etched on hard mask



3) Litho 2. Second Pattern etched on Silicon



4) Etch 2. Second Pattern etched on Silicon



5) Rinse. The mask is rinsed away

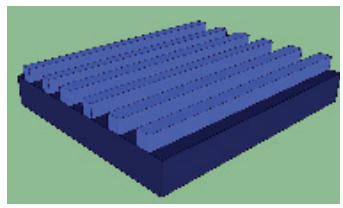


Figure 6: Manufacturing Process of LELE PROCESS

Advantage of LELE

- Higher Resolution with existing processes

Disadvantages

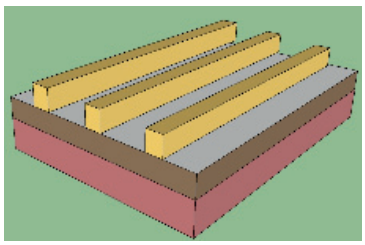
- Higher Process steps
- Expensive due to 2 litho steps

- Overlay pattern sensitivity is high

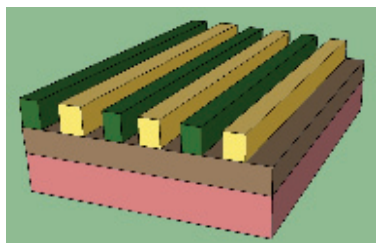
2) Litho Freeze Litho Etch (LFLE)

LFLE also involves two lithography steps. The first step will involve the deposition of the resist and exposure of the pattern. Unlike in the LELE, in LFLE the developed layer is frozen. Which is followed by coating of a new resist layer. This process also involves a second pattern to be overlayed hence alignment is critical. After the second pattern is exposed and developed. The etching of silicon done at once and hence achieving double density.

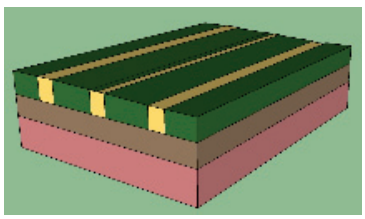
1) Litho 1. First Pattern exposure on Silicon



3) Litho 2. Second Pattern exposed



2) The developed layer is frozen, the coat new resist



4) Etch. The exposed Silicon is etched

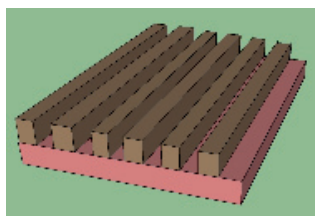


Figure 7: Manufacturing Process of LFLE PROCESS

Advantages

- Lower Process steps compared to LELE
- Higher Throughput
- Reduced Cost

Disadvantages

- Overlay pattern sensitivity is high

3) Self Aligned Double patterning (SADP)

SADP is a double patterning technique, which use spacers also called dummy pattern. At first the core pattern is defined by conventional lithography. This will be the only litho step in this process. A conformal Resist layer is deposited over this pattern and the core pattern is etched which will leave the spacer lines which serve as hard mask with double the density. Further etching will result in double density patterns. This process's limit can extended beyond the half pitch limit.

Figure 8: Manufacturing Process of SADP PROCESS (IMEC Process)

Advantages

- High Tolerance for pattern Overlay
- Only on Litho step hence more economical
- Can achieve beyond half pitch limit

Disadvantages

- Higher Process steps
- Suited for Uniform patterns

The Process in this case is SADP. The target is also to make the patterns as uniform as possible

The trigate finfets can be manufactured by 2 main substrates namely SOI or bulk.

In SOI based Finfets a better fin shape and control is achieved as etching of the fins are ended at the buried oxide

In bulk finfet substrate, the extension of the fin is from the silicon substrate to above the shallow trench isolation. Hence etching of the trenches after the fin production could vary the fin shape.[9]
In Current Project, Bulk Finfet is used.

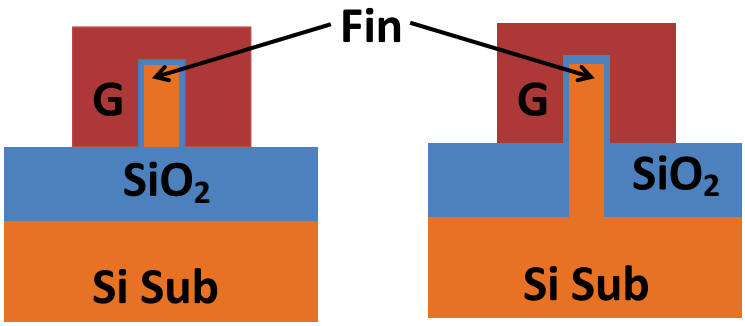


Figure 9: SOI FinFET and Bulk FinFET

Advantages of Bulk FinFET over SOI FinFET

- Low Wafer Cost
- Low Defect Density
- No Floating Body Effect
- High Transfer rate to substrate
- Good process compatibility

Differences between SOI Finfet and Bulk Finfet

In Bulk FinFET the isolation of transistors should be done during the manufacturing process, unlike the SOI transistors where the buried oxide layers itself creates isolation.SOI Transistor substrates are more expensive compared to Bulk transistors but Bulk transistors introduce more process variability during the manufacture process. Hence the matching characteristics are better in SOI FINFET devices.SOI transistors have a buried oxide layer which help in reducing capacitances, while in Bulk FinFET devices, have more 5% to 6% more capacitances due to the Junction Isolations as compared to the former one. Bulk Finfets have better electrostatic integrity as compared to SOI based finfets because the stopper doping in Bulk Finfet process reduces the field of drain entering into the channel, hence improves the DIBL and subthresold slope, where as in SOI finfet , penetration of the drain field depends on the buried oxide layer.[8]

3.2 Development of SADP standard cell architecture

3.2a. Layers Used in the standard cell architecture

This section gives a brief of the layers used in the FinFET design and eventually how a architecture is developed.
In the MOSFET devices usually Metal layer combined with via is used to make a connection to one of the terminals or the gate. But when makes similar connections in the non-planar MosFET, here we introduce several additional interconnect layers(like IM1, IM2). [12]

There are pros and cons in adding the layers. The additional layers help to reduce the Layout density and simplify the interconnections between the points. But introducing the layers also adds respective Resistance and Capacitance in the layout and thereby increasing the parasitics.
Due to miniaturization of the devices in the technology, growing a device in nanometer regime would be difficult using the single patterning or the conventional lithography process. Hence few layers used to draw a layout for the FinFET devices uses Self Aligned Double Patterning Process or Triple Litho Etch process depending the technology node.

Device Layers:

FinFET using SADP(Self Aligned Double Patterning) process:

1) Poly

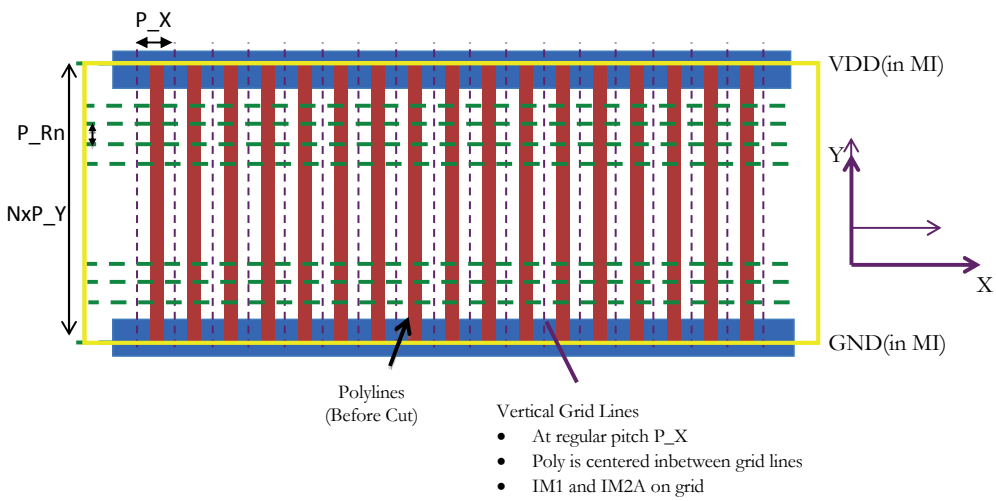


Figure 10: Poly Layers used in cell architecture

The above figure 10. shows the poly placed with a fixed Poly Pitch. Between each poly there is a dummy poly for better routing.

2) Growing a Fin involves using 2 layers:

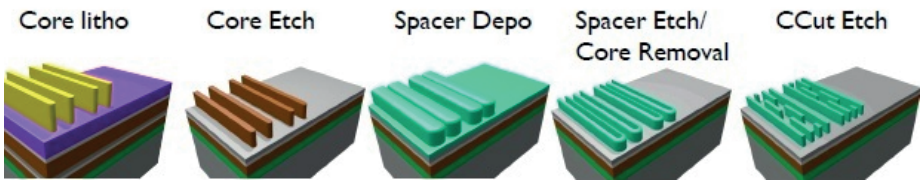


Figure 11. IMEC Fin Patterning Process

To develop a finfet, first we need to place fincore layer and then grow finnocut and finnoblock to generate a fin.

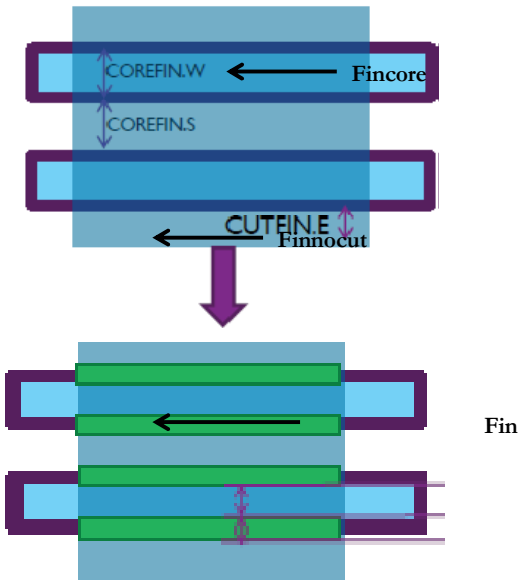


Figure 12. Fincore, Finnocut and Fin layers

Finnocut Layer is placed over the Fincore layer , and it blocks and protects the area needed to develop fins during the double patterning process

Depending on the requirement more than one fin can be grown on different Fincore as shown below:

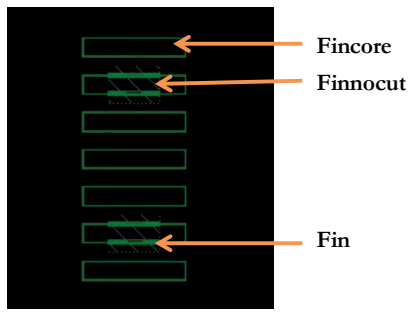


Figure 13. Fincore, Finnocut and Fin in cadence software

Interconnect layers: When a connection to a gate or one of the terminals has to be done, these layers are used to begin with. There are 3 types of Interconnect layers used here, namely:

IM1

When a connection to the Finfet has to be done, IMI layer has to be used first. This layer is used to short the fins in a single FinFET device as show in the figure below.

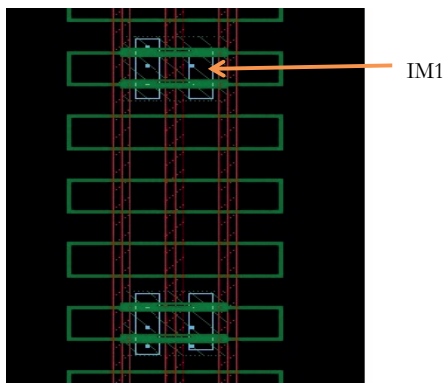


Figure 14: Interconnect Layer IM1

IM2 layer:

If a connection to a FINFET device or a gate has to be done, this layer is used.

This layer is split in to 3 different categories namely : IM2A , IM2B ,IM2C.
IM2A and IM2B : The layers are 1D routable layers i.e. IM2A can only be routed horizontally and IM2B can only be routed vertically .
These two layers are used to make a connection to the FinFET device .

Connection to the gate: When connection to the gate has to be done, and if IM2A layer is being used, it should always be used with IM2B layer and vice versa. As shown in the figure below:

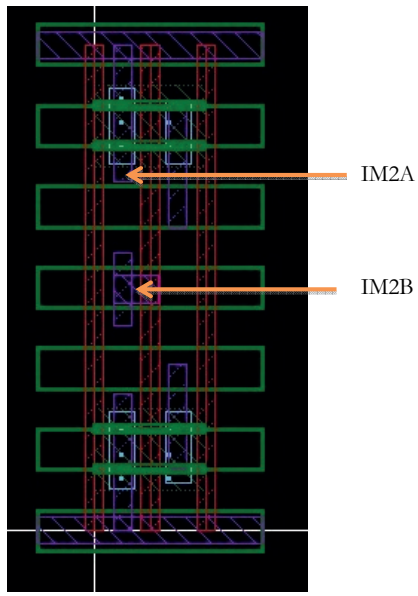


Figure 15: Interconnect Layers IM2, namely IM2A and IM2B

The figure 13 shows the overall connections using the local interconnect. On comparing the connections to the planar devices the main advantage of using the local interconnects is reducing the length of the metal for routing, which in turn reduces the parasitics.

Metals:

Metal1 and Metal2 are used for this project . Metals are grown using Self Aligned Double Pattering Process in 14nm and Triple Litho Etch in 10nm Node.

Metal1Layer: Metal1 is split into Metal1A and Metal1B in the Self Aligned Double Pattering. Metal1 runs both vertically and horizontally and hence a two dimensional Metal. Metal1 is developed using M1 core and M1 noblock, as shown in the figure below. First M1core is drawn, then M1 noblock is grown. The area with M1 Core and M1 noblock forms M1B Metal and the area with M1 core only forms M1A metal layer.

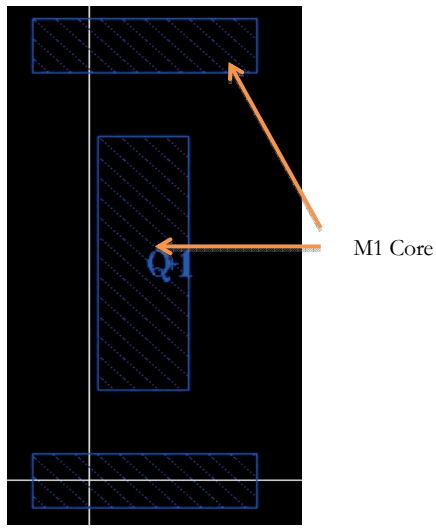


Figure 16. Metal1 (M1) Core layers

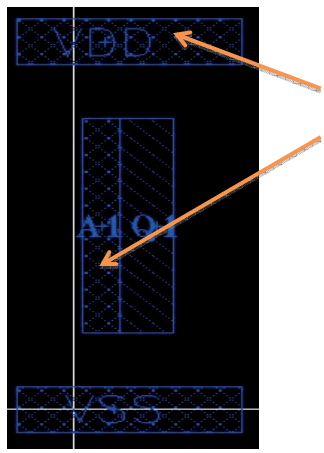
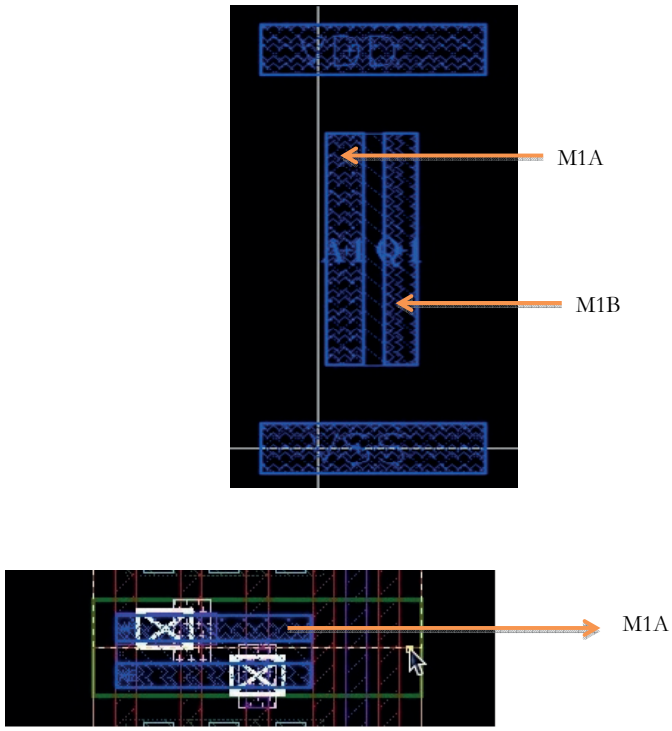


Figure 17: Metal1 (M1) Core and Metal1 noblock layers



Metal1A layers can also be place next to each other but there has to be a minimum distance as stated by the IMEC design rules. Metal1B layers can also be placed in the similar manner.

Figure 18. Metal1 (M1) layers: M1A and M1B Layers

Metal2 Layer: Metal2 layer is also split in the same manner as metal1 layers. Metal2 layer is split into Metal2A and Metal2B. Metal1runs both vertically and horizontally and hence a 2D Metal. Metal2 is developed using M2 core and M2noblock, similar to Metal 1 development. . First M2core is drawn, then M2 noblock is grown. The area with M2 Core and M2 noblock forms M2B Metal and the area with M2 core only forms M2A metal layer.

VIAs: There are two vias used. They are:
1)Via0 : It is used to make a connection from the interconnect layers to the metal1, as shown in the figure below.

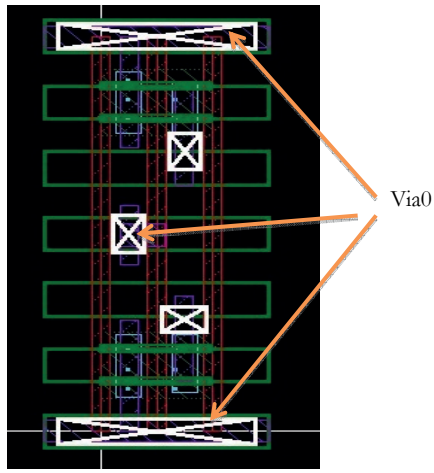
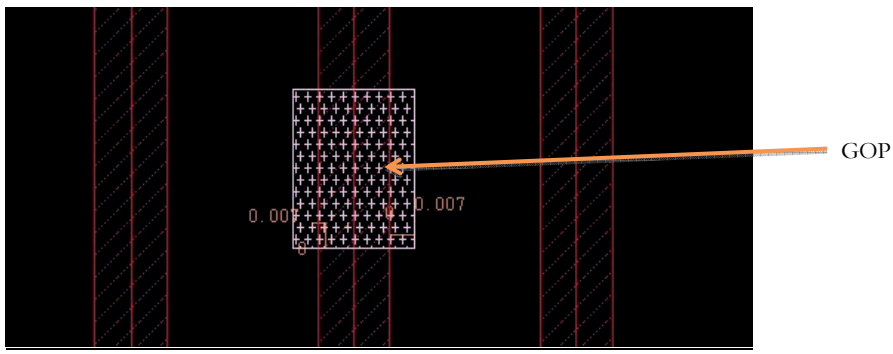


Figure 19. Via0

2) **Via1**: It is used to make a connection from the Metal1 to Metal2

GOP – Gate Open Layer:

When the connection to the gate has to be done, the GOP layer is initially used to provide the first connection from the gate and then connected to the interconnects, as shown in the figure below.



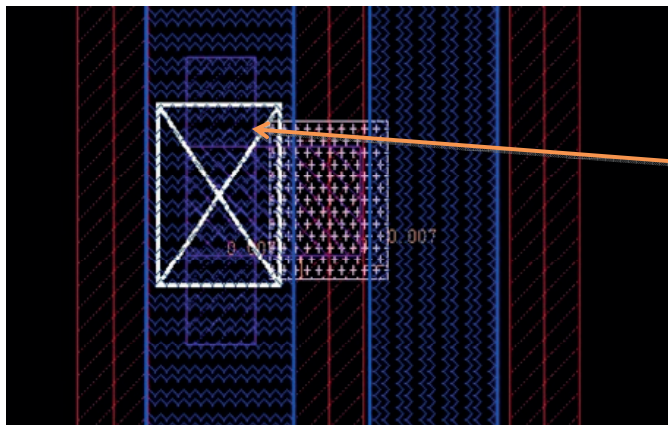
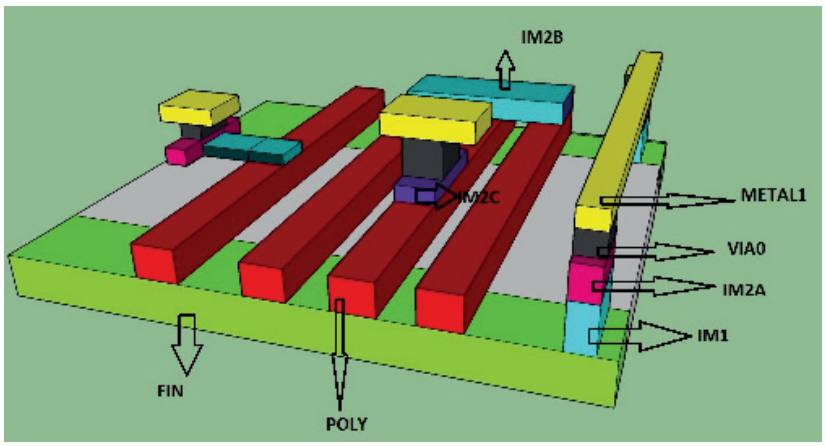


Figure 20. Gate Open Layer

The other layers NWell, Pwell, Nplus, Pplus are used similar as used in MosFET.



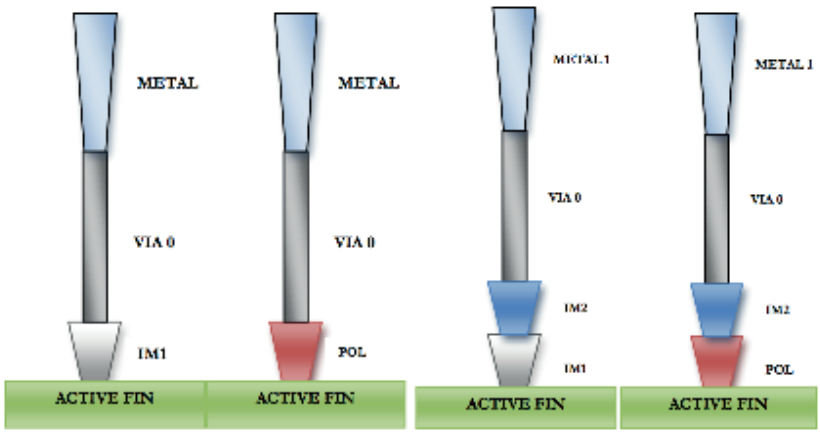


Figure 21. Cross-section view of different layers and their connections possible

3.2b) Steps in SADP Standard cell architecture:

In the following section standard cell architecture is planned using the SADP(Self Aligned Double Patterning Process.)

The main aim of any standard cell architecture is to reduce the area size, reduce cost and improve performance with advancement of every technology node.

For the current technology node, the basic standard cell template is of height 12 track. The track represents the height of the cell from the either ends of the power rail points.. Each track is equal to a width of a metal. The current design rule uses metal of width 45nm.

Initially the layout is defined with the placement of power rails. The poly layers are drawn from the middle end of either power rails as shown in the following steps below. New layers are introduced here unlike the MosFET Layouts. These layers are known as Interconnect layers. The interconnect layers make the routing and connection to different points easier and reduces the use of vias.

The following steps are explained briefly when planning standard cell architecture Layout

Power rail placement Width: First the main power source is considered for building the standard cell.

Power rail is planned to be 3 times the Critical Dimension Unit. As higher the power rail width , the lesser the IR drop.

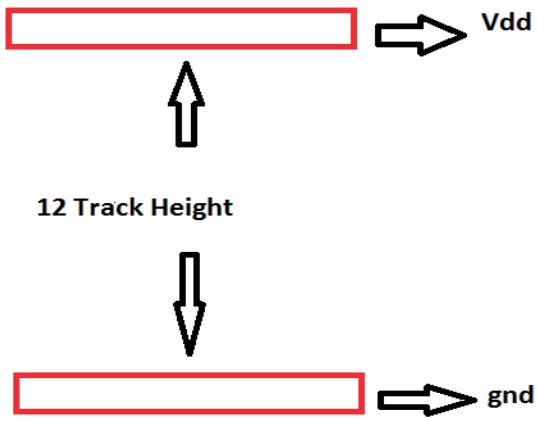


Figure 22. Power rails Vdd and ground and the track height

Placement Of poly: The poly pitches are placed at "x" distance from each poly. Each poly connects the extreme power rails. A dummy poly is use between each active poly, to provide more space for running the metals and Vias, and to avoid violating the DRC rules.

The disadvantage of a dummy poly, would be increase in the area of the cell. But it is also needed with the advancement of smaller devices, as to implement the design with complex design rules.

Polynocut layer is used, if a connection is not required at a certain point in poly.

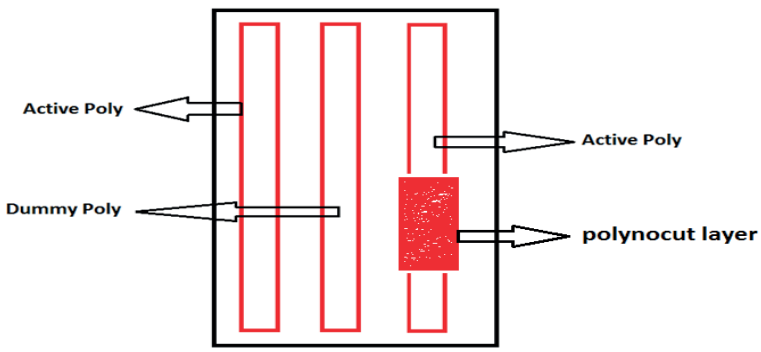


Figure 23. Poly and polynocut layers

Placement of fins: Once power rails are placed, only 2 active fin core are required for a standard cell. Hence only the fincore close to the power rails will have a additional layer finnocut layer to grow fins. The in between space will be placed with Dummy fincore, without finnocut layer, as no fins need to be developed in this area. There are dummy fins placed in between the power rails, but without Finnocut Layer, as fins are not needed there

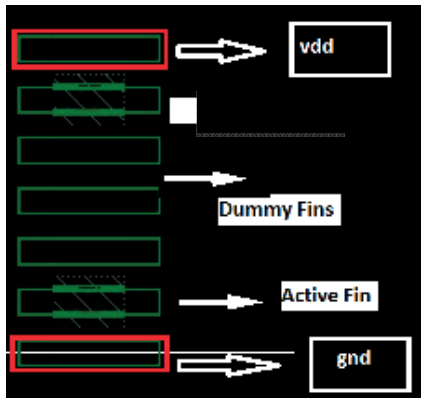


Figure 24. Placement of fins

Metal dimensions and types of metals used**:** The metals dimensions play an important role in deciding the layout density. Here Metal1 is to be drawn horizontally and Metal2 only vertically.

Placement of Interconnect Layers: The interconnect layers are used to connect between 2 points, instead of a metal.

The interconnect layers used here are:

IM1: This layer is used to short the fins of a FinFET.

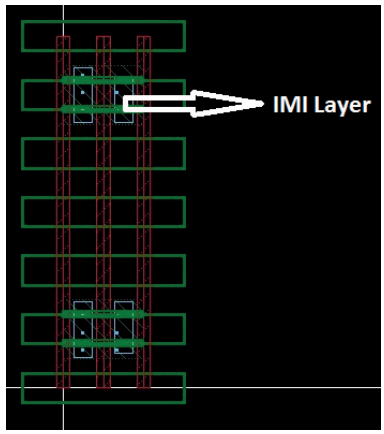


Figure 25 : Placement of Interconnect Layers IM1

IM2A: This is a unidirectional layer, which runs only horizontally between 2 metal connections
IM2B: It is a unidirectional layer which is used to connect vertically only between two layers

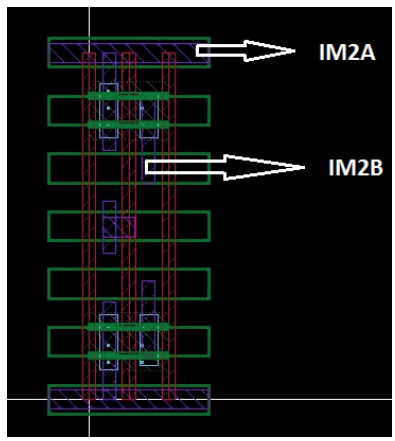


Figure 26. Placement of Interconnect Layers IM2A and IM2B

Type of placing the contacts: The contacts or Vias are the main components that help to make a connection at a point. Here a staggered Vias contact stratergy has been used to give maximum spacing and to make maximum connections as possible.

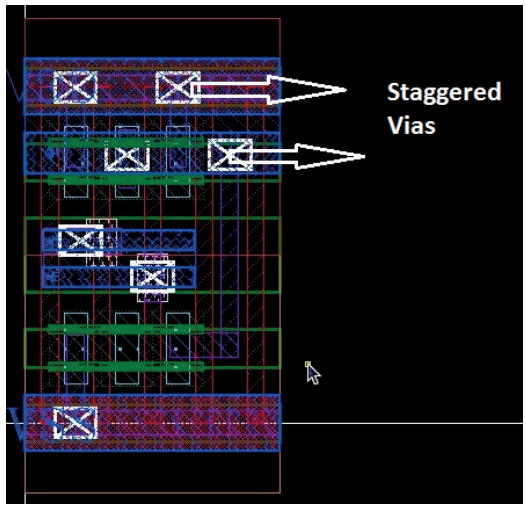


Figure 27: Placement of Vias

NWELL and PWELL layers are placed accordingly for Pfet and Nfet. They co-incide at a point as shown in the figure below. PWELL and NWELL layer are also merged and cover the entire cell.

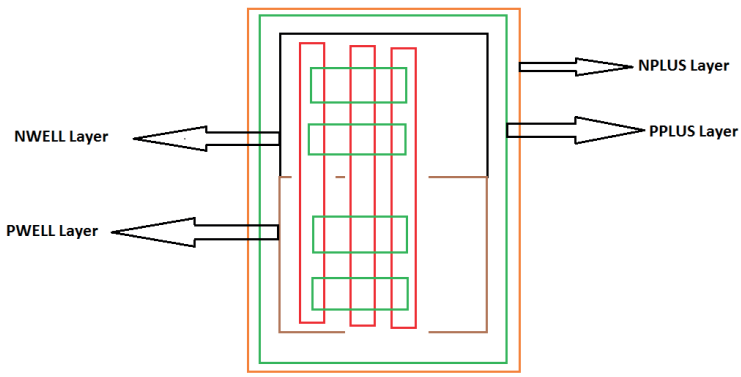


Figure 28: Placement of Nwell, Pwell layers

A basic complete 12 track standard basic cell inverter is seen in the figure below. It's a 12 track, 2 fins Inverter. The cell is divided into 2 regions. The Top half is the PFET region and the second half is the NFET region.

Need for optimization:

The standard basic cell template seen above is optimal for simple basic cells. But the main disadvantage would be, it would not have met the basic rule of 50 % reduction in area to its previous Technology Node. (IMEC, 20 nm Technology node).

Hence more design architectures are discussed in the next chapter to optimize the standard cell architecture, in order to intergrate more circuits in a compact area, and yet be low cost.

Chapter 4

Optimization of the Library

4.1: Challenges in optimization

Standard cell libraries are built and can be optimized for specific requirements. Various FinFET Libraries are built using IMEC process assumptions and rules. Exploration study is done in this chapter, focusing on optimizing Power and performance.[13]

There are three main types of constraints in the Proposed standard cell Template

1)Front end of the Line (FEOL) constraints

2)Middle end of the line(MOL) constraints

3)Back end of the Line(BEOL) constraints.

1) FEOL Constraint: This constraint is represented by the fins. The fins can be more optimized for reduction in area.

The following options were tried:

1) Reduce the track / Height of the cell, and introduction of reduced fin pitch.

In the figure below, the track height of the cell is reduced from 12 track to 10 track inverter.

The height of the cell can be calculated by 10 times the Metal pitch.

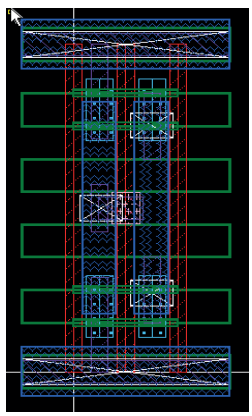


Figure 29. Standard cell with 10 track height with 2 fins

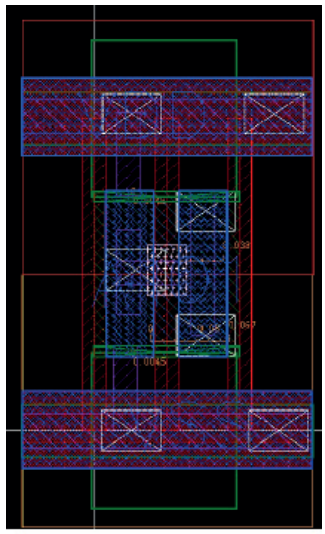


Figure 30. Standard cell with 6 track height with 1 fin

Disadvantage: Routing gets more difficult, and rules have been violated.

2) Implementing only one fin and one wide dummy in between PFETS and NFETS.

Here only one fin has been grown in the active area for both PFETS and NFETS. Many dummy fins have been replaced with a single wide dummy fin.

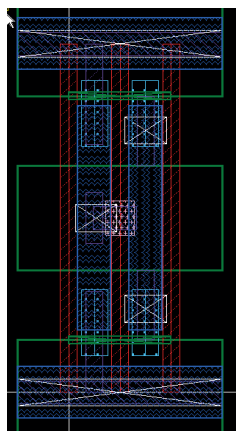


Figure 31: Standard cell with only 1 dummy fin core

Disadvantage: The dummy Fincore is unstable. The introduction of one fin in the active area, reduces the performance of the circuit.

Optimum Design for FEOL:

A cell with reduced cell height was tested. Here the track height was reduced from 10 track to 8 track. The dummy fin core was removed and only one active fin is grown.

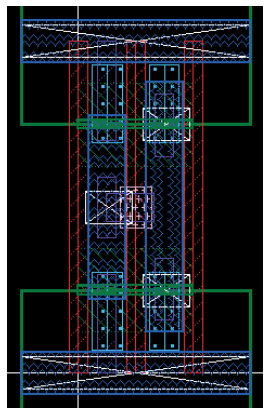


Figure 32: Proposed design architecture, but need for optimization

This design architecture is comparatively better than the previous design templates.
Advantages:

- Reduced area.
- Low leakage and dynamic power

Disadvantages:

- The design is more suitable for simple design and it gets more difficult with complex design
- The accessibility of ports like the input and output port would be difficult
- Since only one fin is grown in active area, the performance of the cell would be degraded.

2) MOL CONTRAINTS:

This constraint deals with the interconnect layers.

The IM2 layers cannot cross over the active poly. But an option was tried where the IM2 was able to cross the active poly. This reduced the interconnect density, as the use of metal connections was reduced.

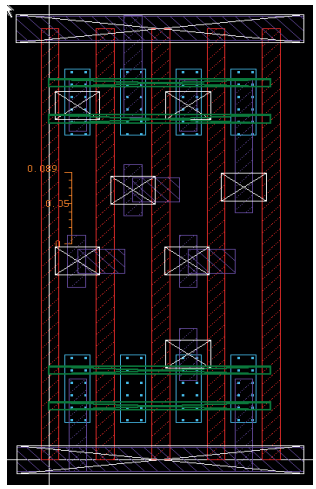


Figure 33: Architecture with IM2 layers crossing over the active poly

This method reduces the area, but the leakage power is increased.
The accessibility to the ports is better, but the performance of the device is degraded.

3) BEOL Constraint: This constraint deals mainly with the metals.
Earlier in the proposed 12 track cell. The metals Metal1 and Metal2 were both bi directional.
Here this is optimized by:
1) using a reduced track height, 10 track
2) The metals were drawn unidirectional. The Metal1 was drawn only horizontal and Metal was drawn only Vertical.

This method reduces cost for printing metals, as the metals were unidirectional. But in 12 track only metal1 was used, but here introduction of 2 metals is done. This would introduce more parasitic and degrade the performance of the cell.

Introduction of 2 types of metals would also lead to use of more Vias. Hence staggered contact strategy would be more difficult to implement. This would also lead to violating the design rules.

4.2. Types of Architecture

A study was done on 2 different types of cell architecture. The main focus was done on Optimising Area and Performance. The 2 main categories studied here are done using SADP process:

1) With different number of fins

2) With different Cell Height.

1) 12track cell with 2 fins, 3 fins, and 4 fins:

12Track 2Fins Layout: This is a baseline Layout design with 12 track height and 2 fins for PFET and NFET respectively. The various cells built here are:

a) INVERTER

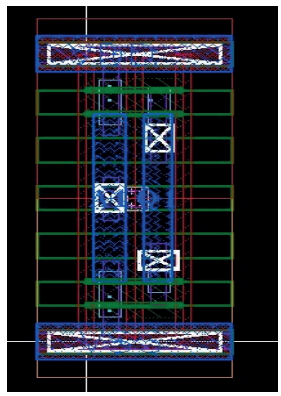


Figure 34: 12track-2 fins inverter architecture

b) NAND Gate

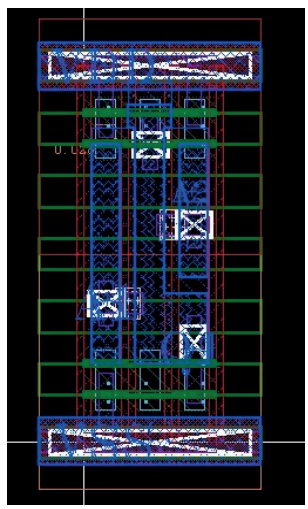


Figure 35: 12track-2 fins NAND architecture

c) NOR Gate :

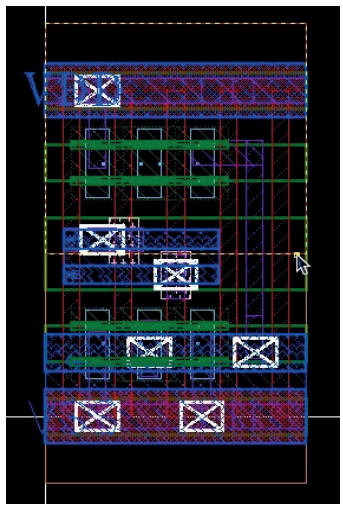


Figure 36:12track-2 fins NOR architecture

d) AOI-21

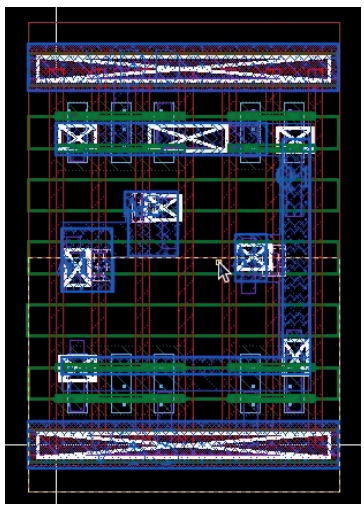


Figure 37:12track-2 fins AOI-21 architecture

e)AOI-22

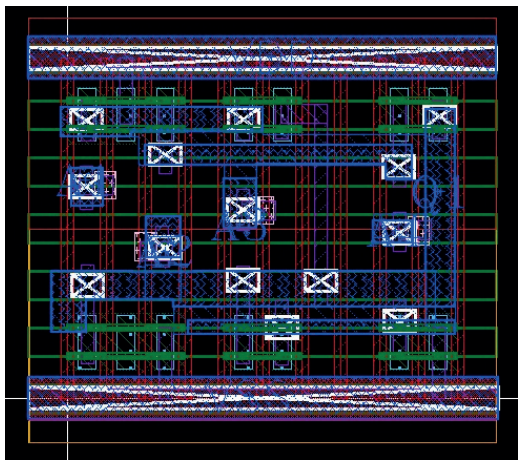


Figure 38: 12track-2 fins AOI-22 architecture

2) 12Track 3Fins : This is a Optimized Layout design with 12 track height and 3 fins for PFET and NFET respectively

a)Inverter

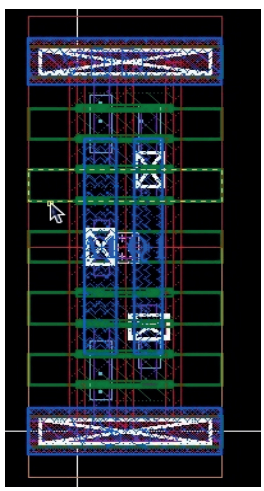


Figure 39: 12track-3 fins Inverter architecture

b) NAND Gate

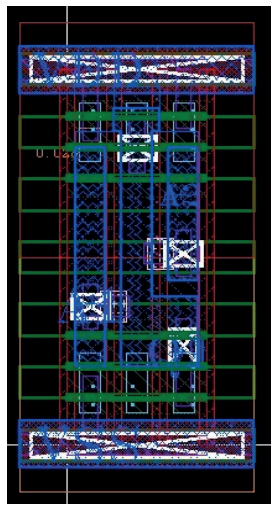


Figure 40: 12track3 fins Nand architecture

c) NOR Gate

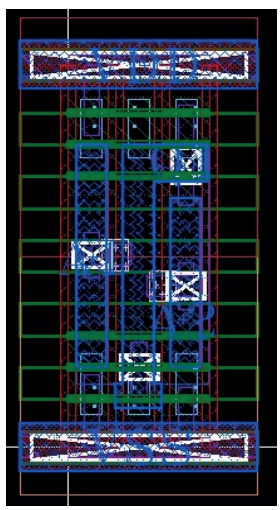


Figure 41: 12track-3 fins NOR architecture

d)AOI-21

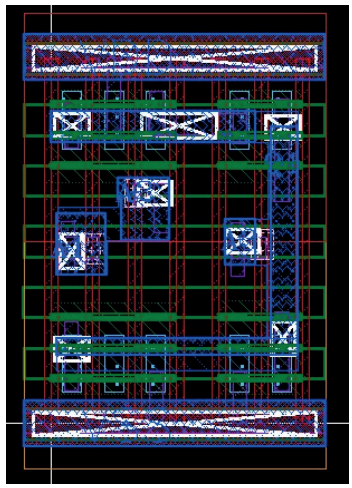


Figure 42: 12track-3 fins A0I-21 architecture

e) AOI-22

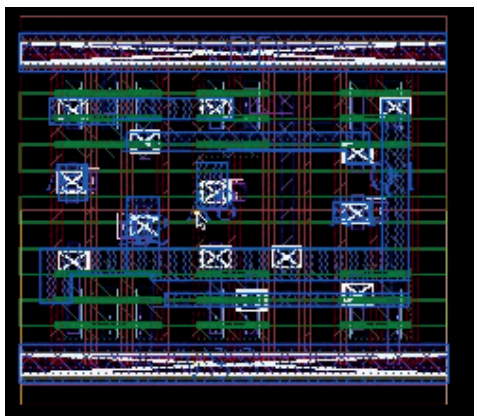


Figure 43: 12track-3 fins A0I-22 architecture

3) 12Track-4fins Layout: This is a improvised design layout of Baseline design layout , which has 4 fins each for PFET and NFET devices.

a) Inverter Gate:

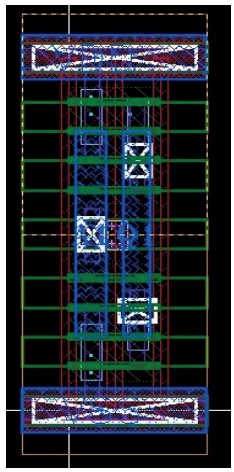


Figure 44: 12track-4 fins Inverter architecture

b) NAND Gate

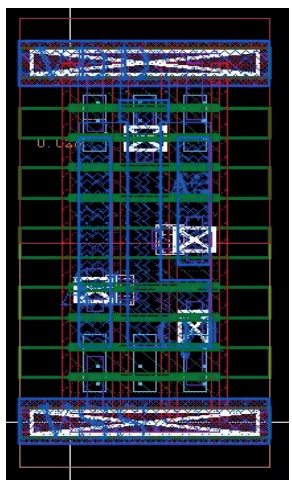


Figure 45 12track-2 fins Nand architecture

c) NOR Gate

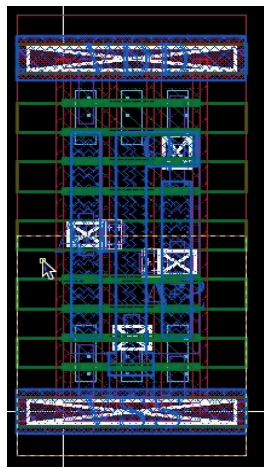


Figure 46: 12track-2 fins NOR architecture

d) AOI -21Gate

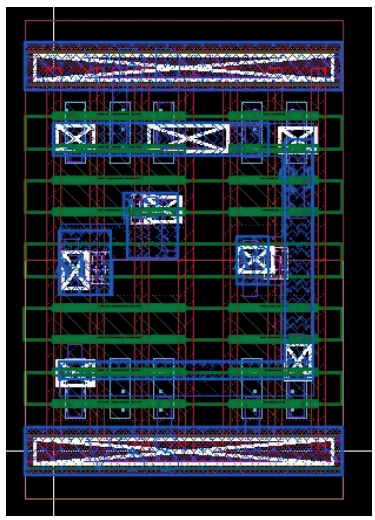


Figure 47: 12track-2 fins AOI-21 architecture

4**) 9 TRACK Layout**: This Layout has reduced cell height compared to Baseline Layout design . It is a 9 track height cell, with 45nm metal width , which makes it a 450nm cell height. It has 2 fins each for PFET and NFET device.

a) Inverter

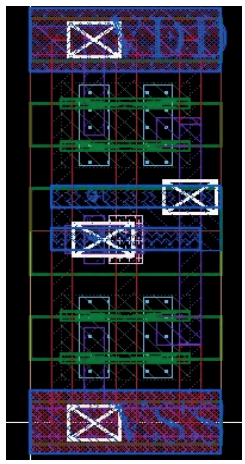


Figure 48: 9track-2 fins Inverter architecture

b)NAND Gate

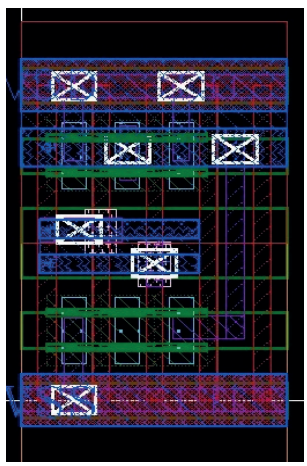


Figure 49: 9track-2 fins Nand architecture

c) NOR Gate

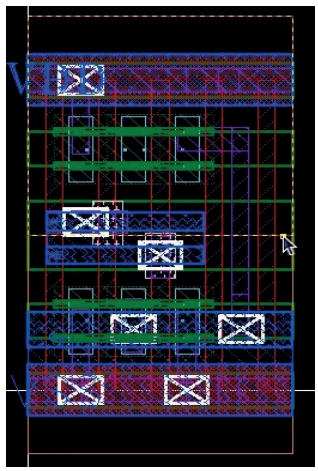


Figure 50: 9track-2 fins NOR architecture

5) 9TRACK-3FINS Layout: This layout design consists of 3 fins each for PFET and NFET. The cell height is 9 track i.e. 450nm height.

a) Inverter Gate

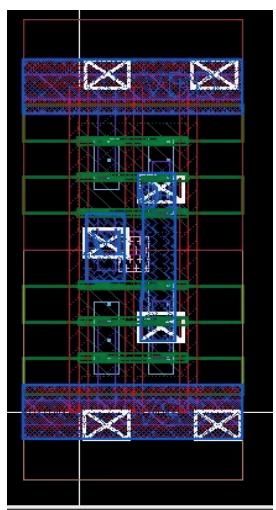


Figure 51: 9track-3 fins Inverter architecture

b)NAND Gate

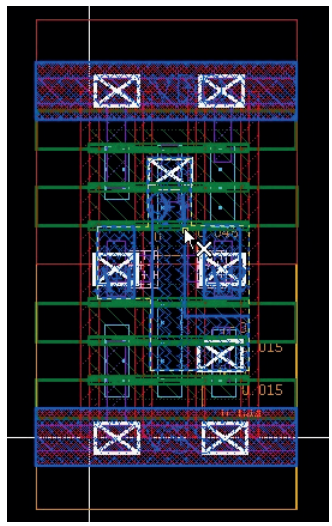


Figure 52: 9track-3 fins Nand architecture

c) NOR Gate

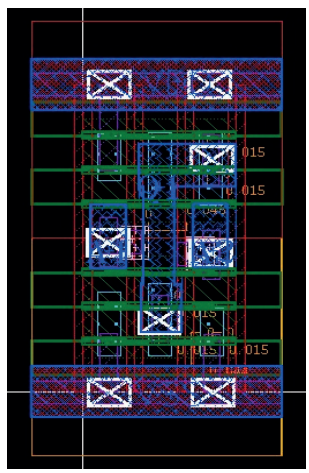


Figure 53: 9track-3 fins NOR architecture

d) AOI-21 Gate

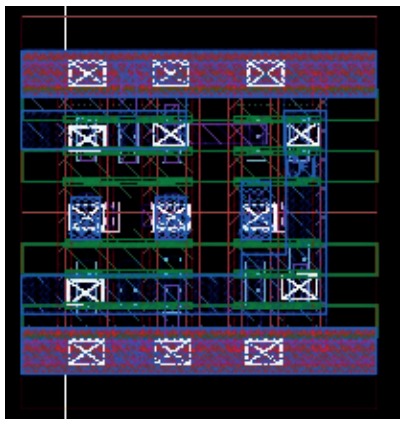


Figure 54: 9track-3 fins AOI-21architecture

f) AOI-22 Gate

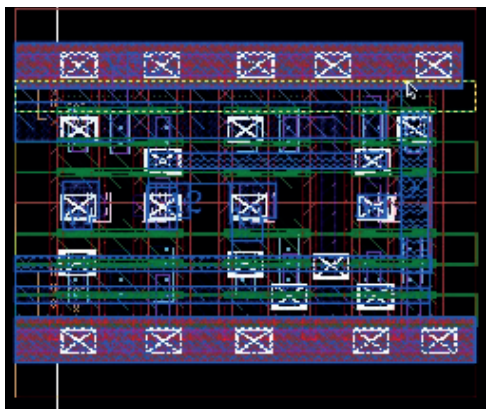


Figure 55: 9track-3 fins AOI-22architecture

Ring Oscillator

21 stage Ring Oscillator is designed using baseline design layout template. Three types of Ring Oscillator was designed using baseline Design Layout using 2 fins , 3 fins and 4 fins.

21stage RO – 12track 2fins

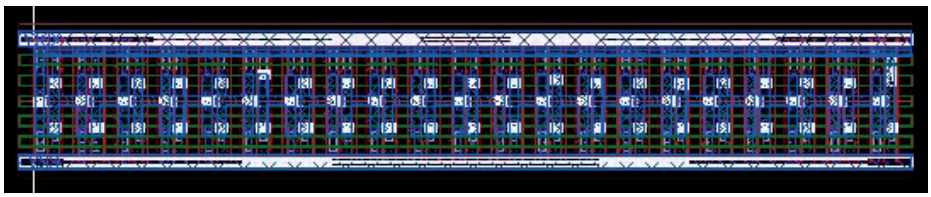


Figure 56: 12 Track -2 fins Ring –Oscillator

21stage RO – 12track 3fins

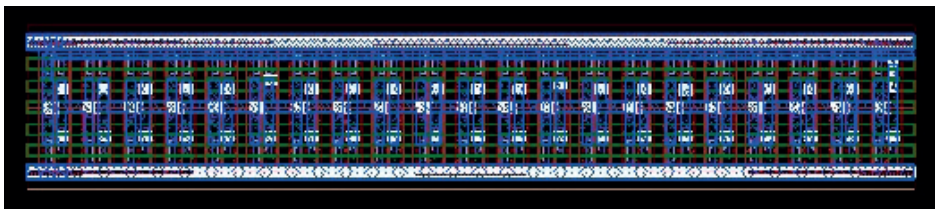


Figure 57: 12 Track -3 fins Ring –Oscillator

21stage RO – 12track 4fins

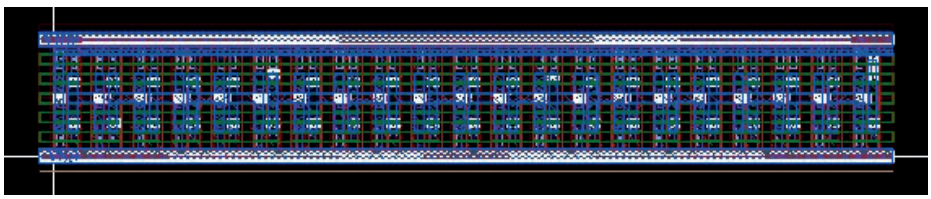


Figure 58: 12 Track -4 fins Ring –Oscillator

Chapter 5

Results and Analysis

In this chapter the power analysis of different types of layout architecture is shown. Initially the 3 basic cell layout architecture are analyzed, namely a) baseline standard cell layout b) optimized standard cell layout. c) 3 fin standard cells. These 3 design layout architectures are improvised and its Performance is compared with Improvised Design Layouts and analyzed.

5.1 CIRCUIT SETUP: The test bench and the set up conditions for the different circuits are shown below.

a) INVERTER:
Here the Voltage source or Vdd is 0.8V. Input 1 and Input 2 are varied with different combinations as shown in the truth table below. The rise time and fall time for the inputs are 100ps and different period and pulse width are shown in the table below. The capacitor loads were analyzed for 1fF, 10fF, 25fF, 50fF, 100Ff.

Input1
0
1

Table 2: Inputs for an Inverter

Period	Pulse Width
1ns	0.5ns
2ns	1ns
4ns	2ns
8ns	4ns
16ns	8ns

Table 3: Setup Conditions for Inverter

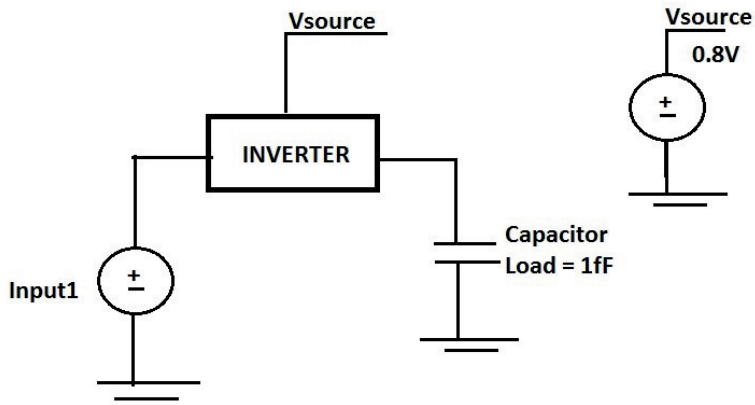


Fig 59: Test Bench of Inverter

b) NAND GATE:

Here the Voltage source or Vdd is 0.8V. Input 1 and Input 2 are varied with different combinations as shown in the truth table below. The rise time and fall time for the inputs are 100ps and different period and pulse width are shown in the table below. The capacitor loads were analyzed for 1fF, 10fF, 25fF, 50fF, 100Ff.

Input1	Input2
0	0
0	1
1	0
1	1

Table 4: Inputs for Nand Gate

Period	Pulse Width
1ns	0.5ns
2ns	1ns
4ns	2ns
8ns	4ns
16ns	8ns

Table 5: Set Up Conditions for a Nand Gate

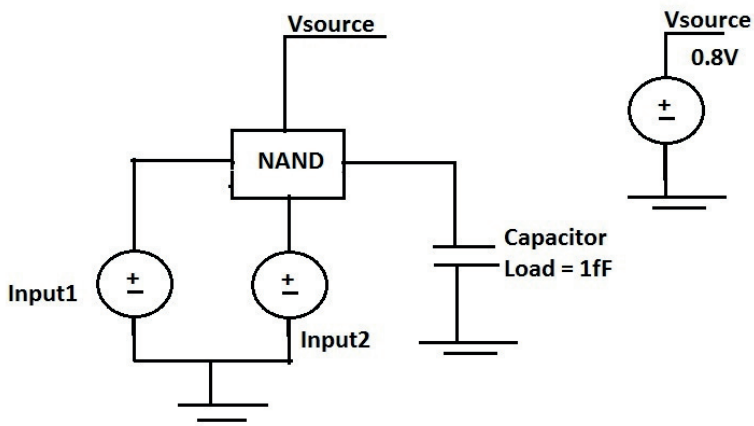


Fig 60: Test Bench of Nand Gate

c) NOR GATE:

Here the Voltage source or Vdd is 0.8V. Input 1 and Input 2 are varied with different combinations as shown in the truth table below. The rise time and fall time for the inputs are 100ps and different period and pulse width are shown in the table below. The capacitor loads were analyzed for 1fF, 10fF, 25fF, 50fF, 100Ff.

Input1	Input2
0	0
0	1
1	0
1	1

Table 6: Inputs for Nor Gate

Period	Pulse Width
1ns	0.5ns
2ns	1ns
4ns	2ns
8ns	4ns
16ns	8ns

Table 7: Set up conditions for Nor gate

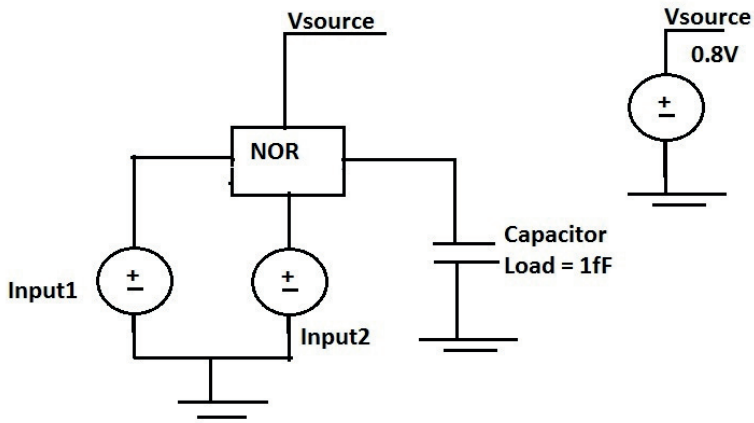


Fig 61: Test Bench of Nor Gate

d) AOI-21 GATE:

Here the Voltage source or Vdd is 0.8V. Input 1 and Input 2 are varied with different combinations as shown in the truth table below. The rise time and fall time for the inputs are 100ps and different period and pulse width are shown in the table below. The capacitor loads were analysed for 1fF, 10fF, 25fF, 50fF, 100Ff.

Input1	Input2	Input3
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Table 8 Inputs for AOI-21 Gate

Period	Pulse Width
1ns	0.5ns
2ns	1ns
4ns	2ns
8ns	4ns
16ns	8ns

Table 9: Set-up conditions for AOI-21 Gate

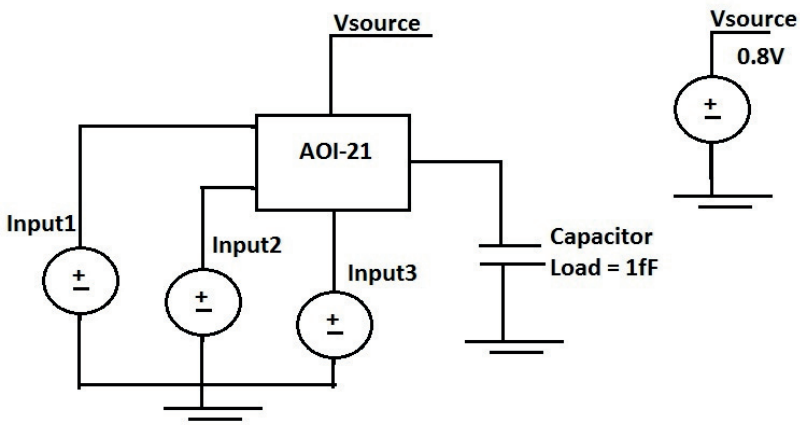


Fig 62: Test Bench of AOI-21 Gate

e) AOI-22 GATE:

Here the Voltage source or Vdd is 0.8V. Input 1 and Input 2 are varied with different combinations as shown in the truth table below. The rise time and fall time for the inputs are 100ps and different period and pulse width are shown in the table below. The capacitor loads were analyzed for 1fF, 10fF, 25fF, 50fF, 100Ff.

Input1	Input2	Input3	Input4
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Table 10: Inputs for AOI-22 Gate

Period	Pulse Width
1ns	0.5ns
2ns	1ns
4ns	2ns
8ns	4ns
16ns	8ns

Table 11: Set up conditions for AOI-22 Gate

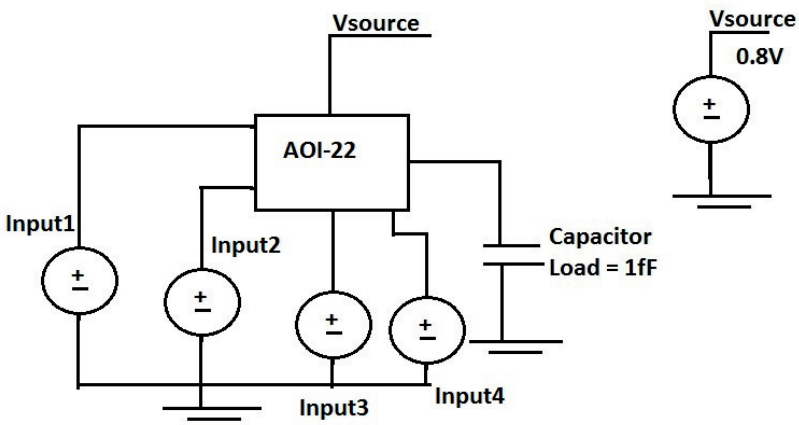


Fig 63: Test Bench of AOI-22 Gate

5.2 DELAY AND POWER FOR DIFFERENT TYPES OF LAYOUT:

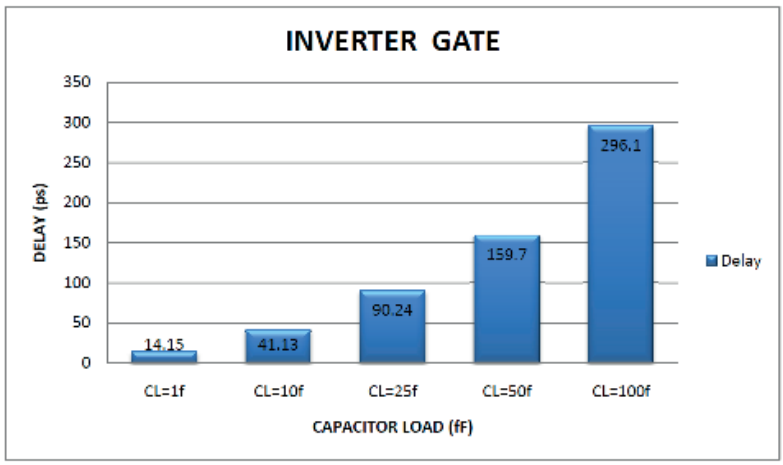
The 3 basic cell layouts are analyzed which were designed namely a) baseline standard cell layout b) optimized standard cell layout. c) 3 fin standard cells.

a) DELAY OF BASELINE STANDARD CELL LAYOUT CELLS:

The Baseline standard cell is the basic type of standard cell to design with the current rules of the foundry. The track height of the cell is 12. The track Height is a multiple of the metal width used. The metal width used here is 45nm and hence a 12 track height cell would measure up to 540nm. Every device i.e. PFET and NFET consists of 2 fins each. The following cells were designed with this type of layout. Each standard cell is analysed for Power with different capacitor load and different frequencies.

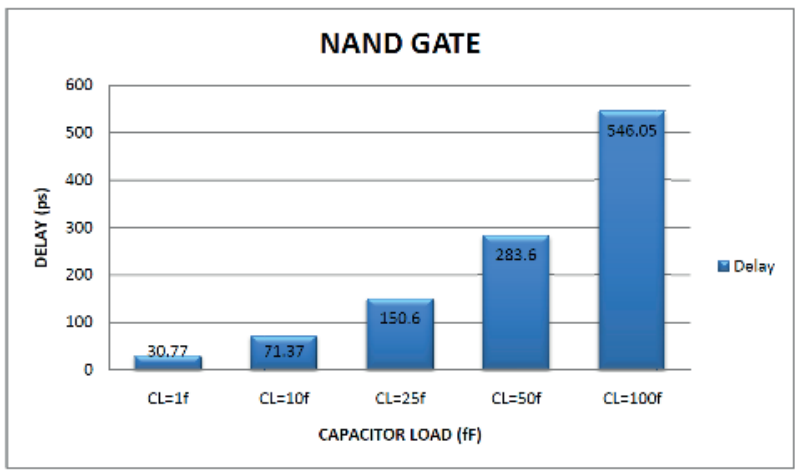
In the following below tables, Delay is plotted with different capacitor loads and speed is evaluated and compared among different layout designs.

1) INVERTER



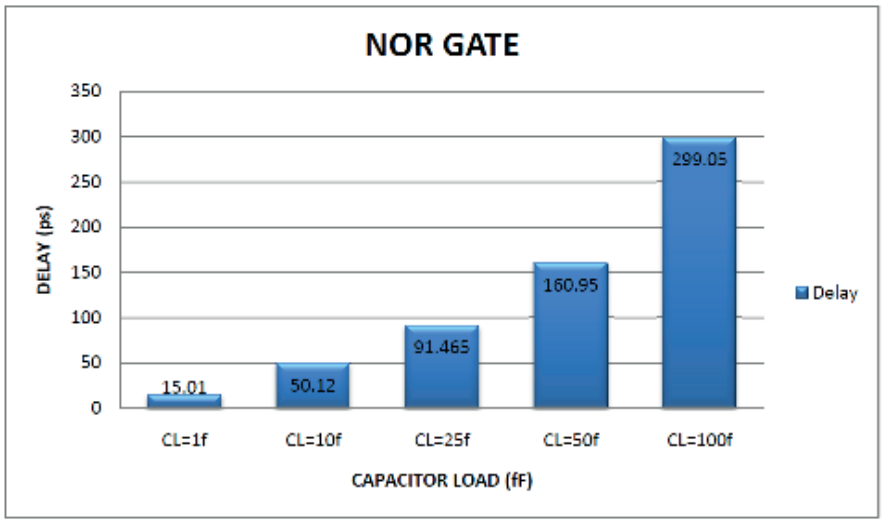
Graph 1: Delay of Inverter with different capacitor Loads for a Baseline Layout

2) NAND GATE



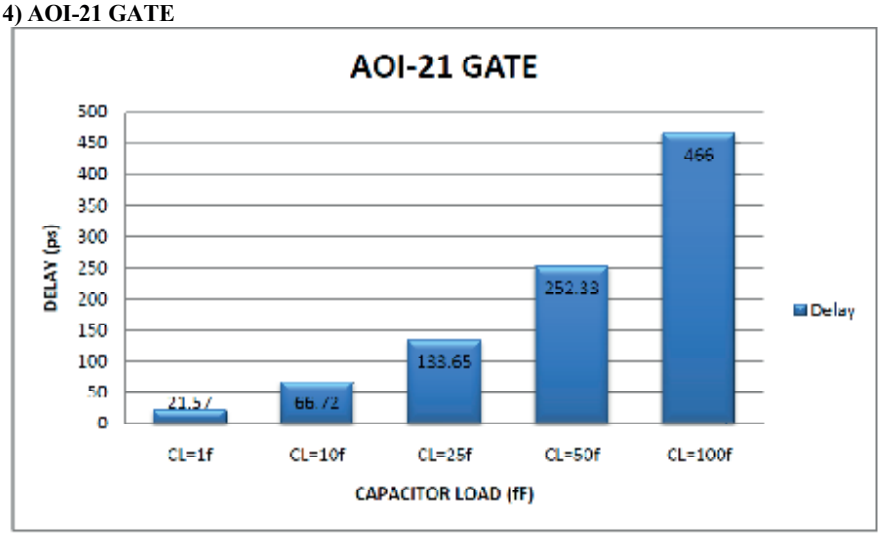
Graph 2: Delay of Nand Gate with different capacitor Loads for a Baseline Layout

3) NOR GATE



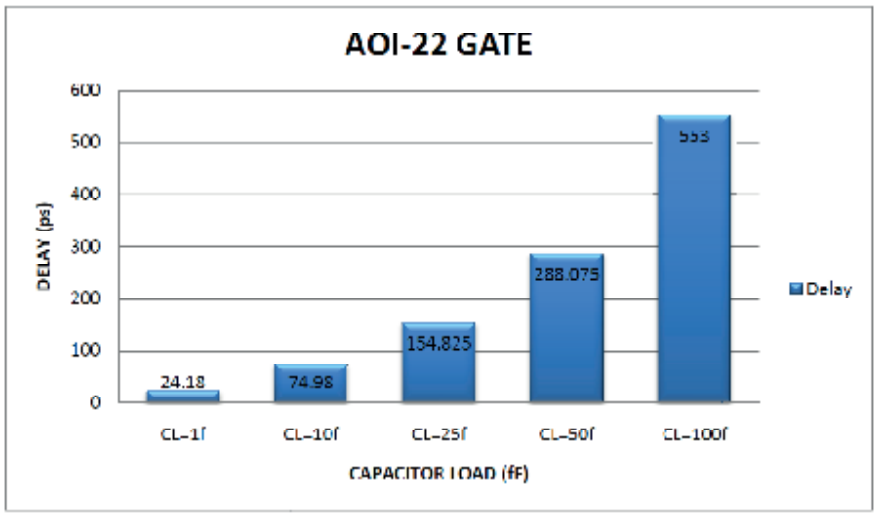
Graph 3: Delay of Nor Gate with different capacitor Loads for a Baseline Layout

4) AOI-21 GATE



Graph 4: Delay of AOI-21 Gate with different capacitor Loads for a Baseline Layout

5) AOI-22 GATE



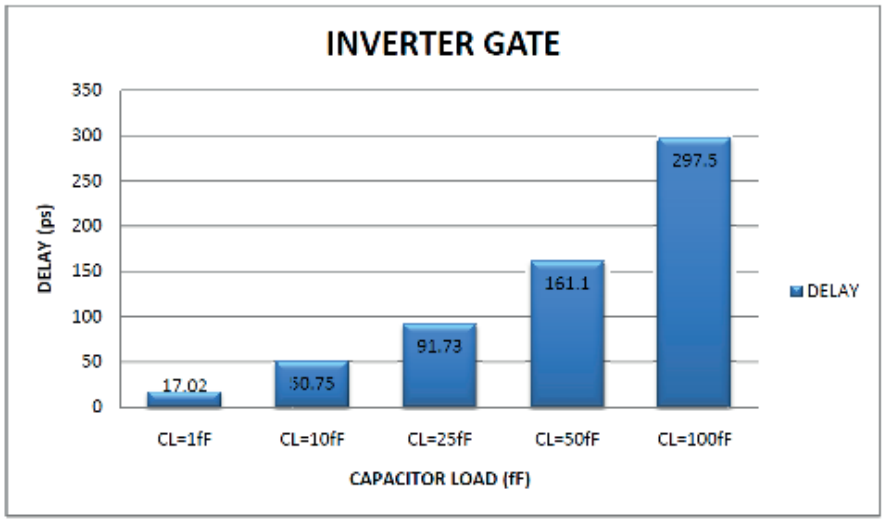
Graph 5: Delay of AOI-22 Gate with different capacitor Loads for a Baseline Layout

b) DELAY OF OPTIMISED STANDARD CELLS :

The Optimized standard cell is the improved version of the basic of standard cell. The track height of the cell is 9. The metal width used here is 45nm and hence a 9 track height cell would up to 450nm, unlike the Baseline where the track height of the cell was 12 . As the baseline design layout each PFET and NFET consists of 2 fins respectively. The following cells were designed with this type of layout. Each standard cell is analysed for Power with different capacitor load and different frequencies.

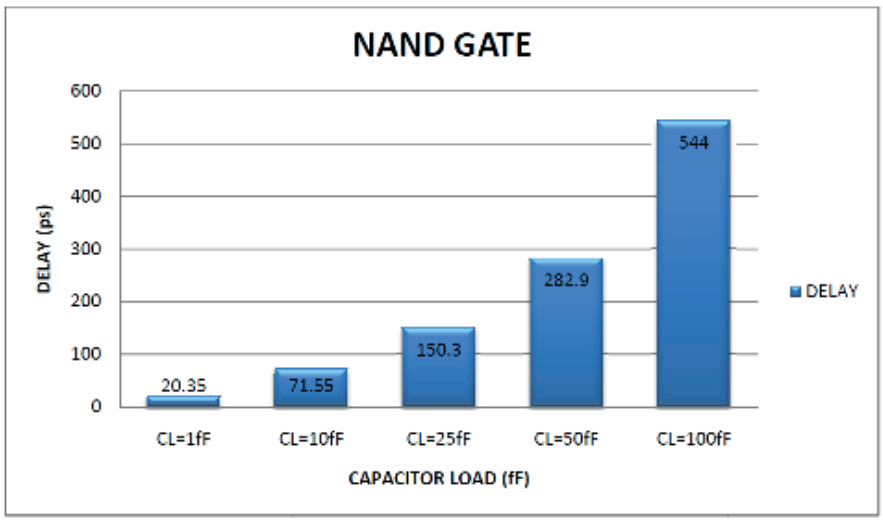
In the following below tables, Delay is plotted with different capacitor loads and speed is evaluated and compared among different layout designs.

1)INVERTER



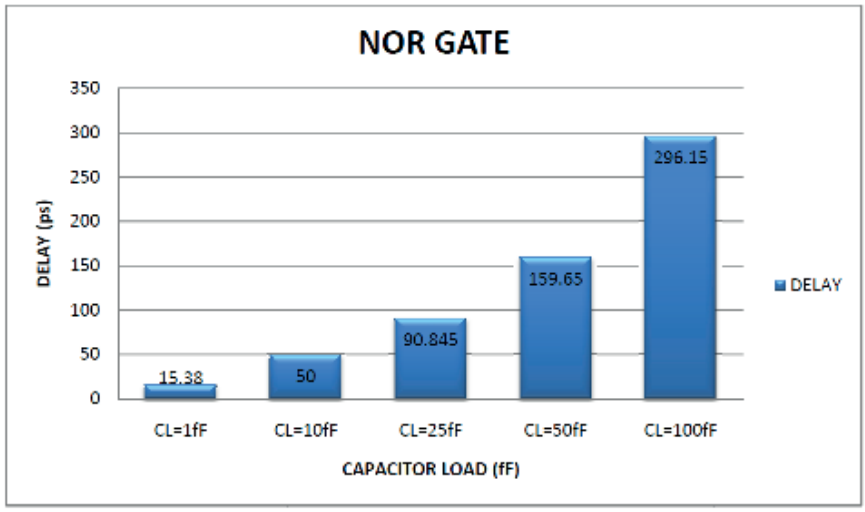
Graph 6: Delay of Inverter with different capacitor Loads for a Optimised Layout

2) NAND GATE



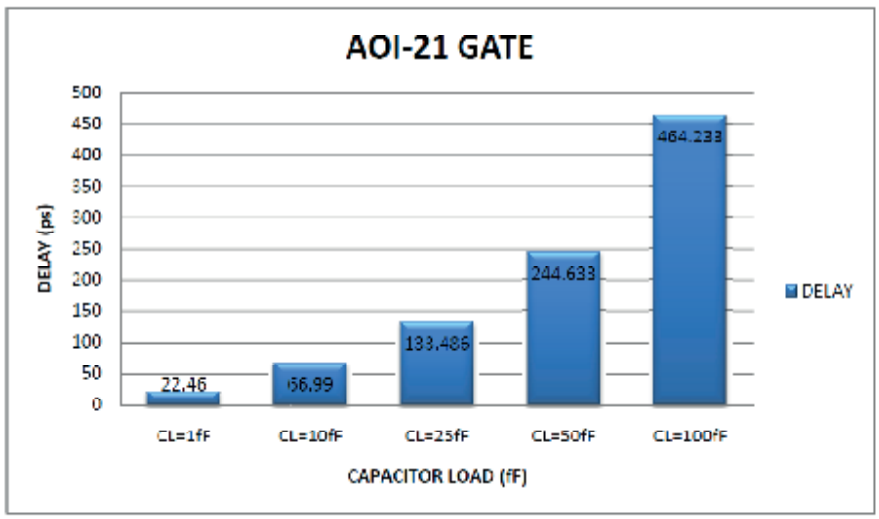
Graph 7: Delay of Nand Gate with different capacitor Loads for a Optimised Layout

3) NOR GATE



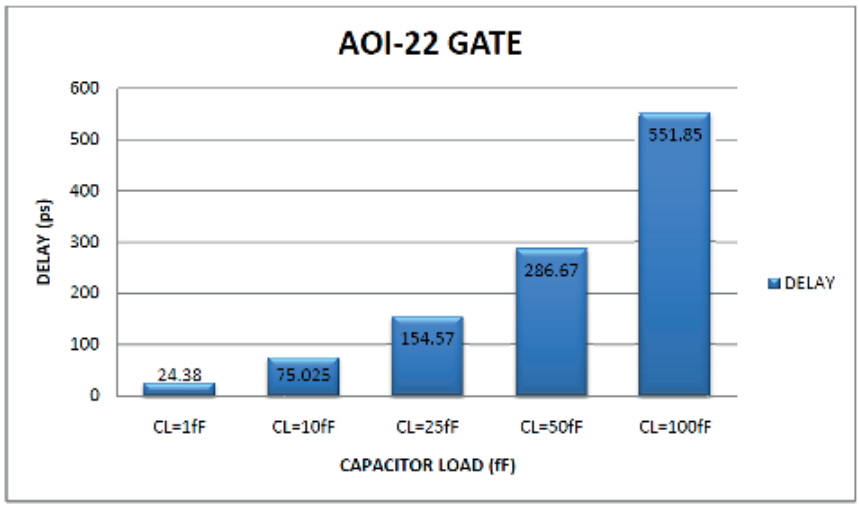
Graph 8: Delay of Nor Gate with different capacitor Loads for a Optimised Layout

4)AOI-21 GATE



Graph 9: Delay of AOI-21 Gate with different capacitor Loads for a Optimised Layout

5) AOI-22 GATE

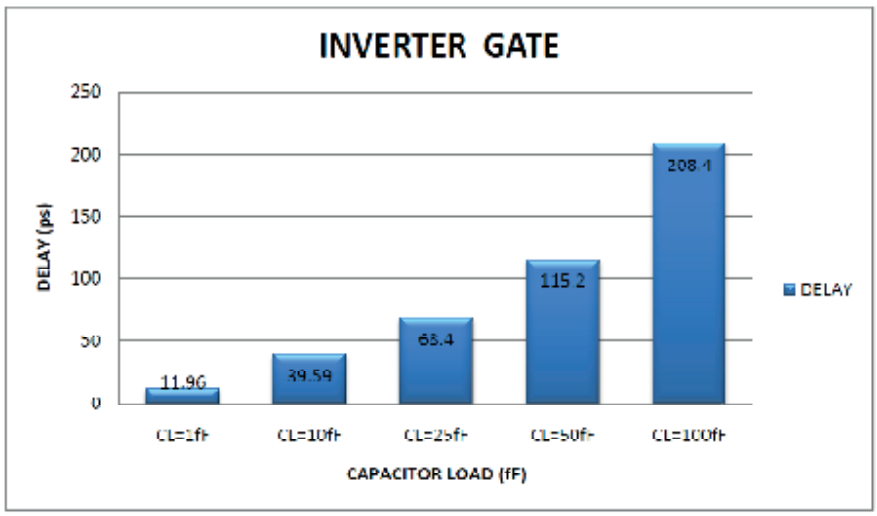


Graph 10: Delay of AOI-22 Gate with different capacitor Loads for a Optimised Layout

c) DELAY OF 3 FINS LAYOUT CELLS :

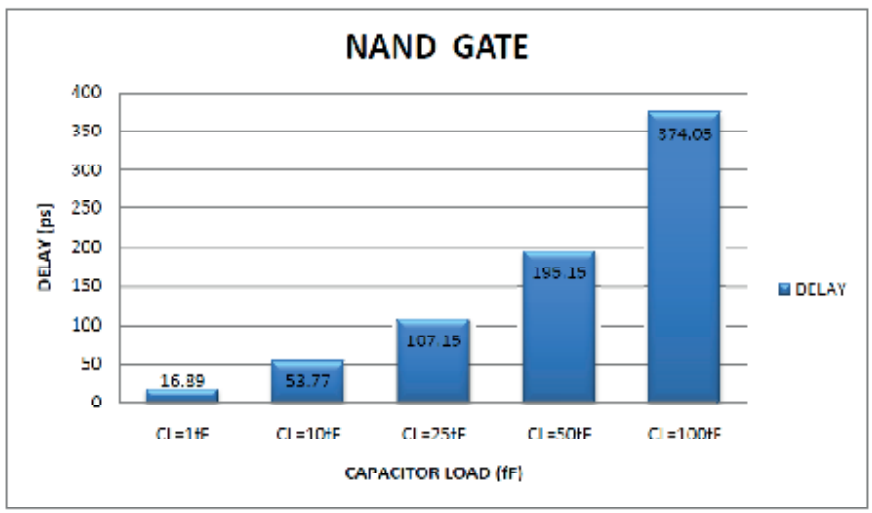
In this type of layout design, each standard cells are 9 track. The metal width used here is 45nm and hence a 9 track height cell would up to 450nm Height. Each PFET and NFET device consists of 3 fins respectively. The following cells were designed with this type of layout. Each standard cell is analyzed for speed with different capacitor load and different frequencies

1)INVERTER



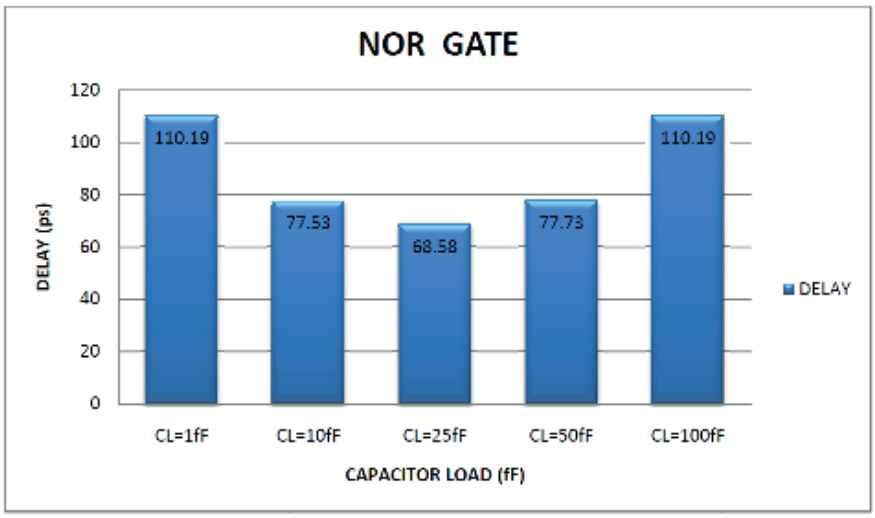
Graph 11: Delay of Inverter Gate with different capacitor Loads for a 3 - Fins Layout

2) NAND GATE



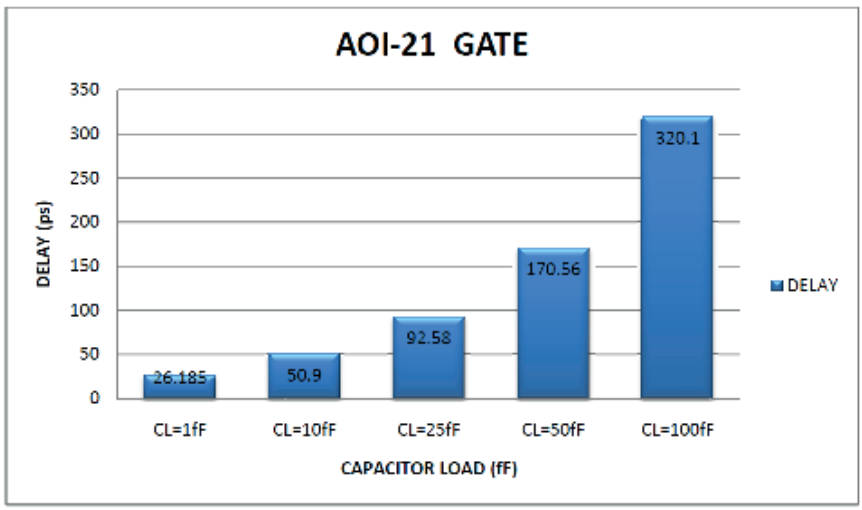
Graph 12: Delay of Nand Gate with different capacitor Loads for a 3 - Fins Layout

3) NOR GATE



Graph 13: Delay of Nor Gate with different capacitor Loads for a 3 - Fins Layout

4)AOI-21 GATE

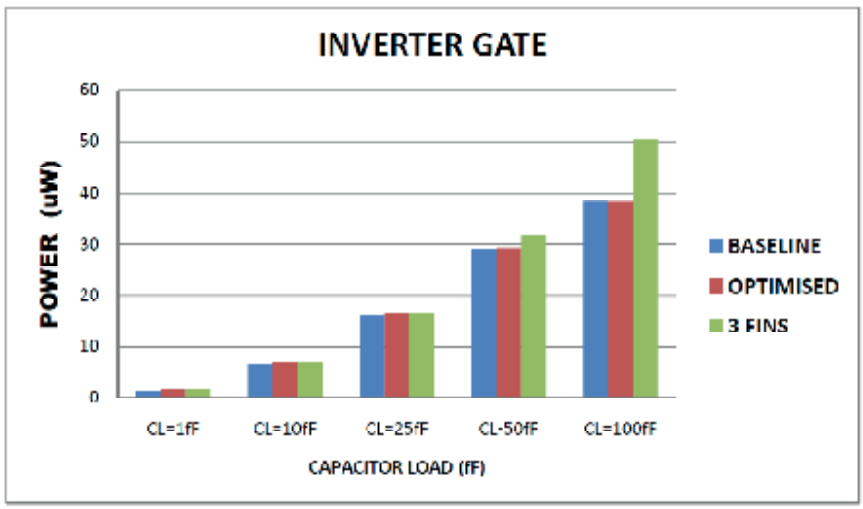


Graph 14: Delay of AOI-21 with different capacitor Loads for a 3 - Fins Layout

With Reference to the above graphs the following results can be concluded:
INVERTER GATE: On comparing with the 3 types of architecture, the fastest inverter is layout with **3 fins**.
NAND GATE: The fastest Nand gate layout is **3 fins** architecture layout.
NOR GATE: The least delay NOR gate layout is **optimised design layout.** The 3 fins have the least speed comparing to the other design layouts.
AOI-21GATE: The faster AOI-21 design layout is **3 fins** architecture.
AOI-22 GATE: The speed performance of the AOI-22 architecture is almost the same for **baseline and optimised layouts**.
Based on the current method of routing the metals in the layout, Delay numbers for the 3 fins design layout seems to be the best layout architecture. One of the main reason for 3 fins being the best layout among the others is the higher the number of fins, faster the circuit.

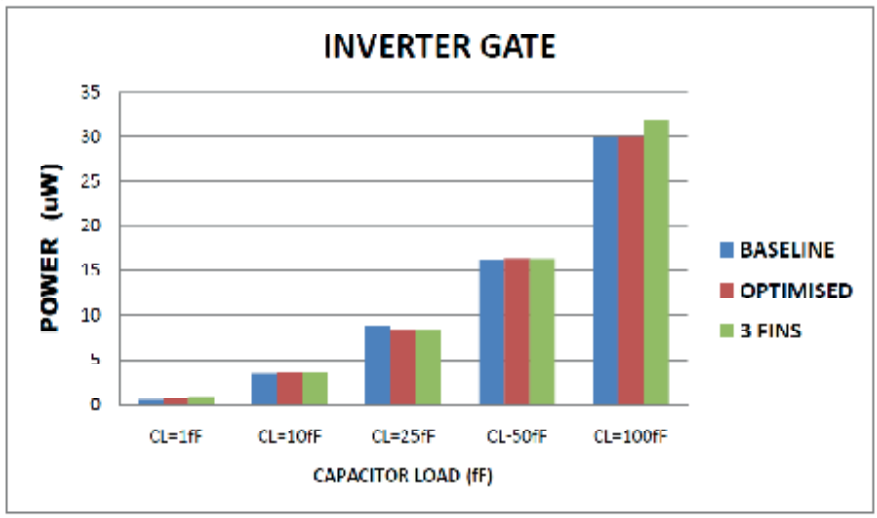
5.3 POWER CONSUMPTION FOR DIFFERENT TYPES OF LAYOUT DESIGNS:
In this section Power of the three basic design layouts are analyzed. The various gates are analyzed for capacitor loads of 1fF, 10Ff, 25fF, 50Ff and 100Ff. The period or frequency of the signal is also varied as shown in the table above. The power values are compared with different designs and the layout for lowest power usage is obtained.

a) INVERTER:
1) PERIOD = 1ns



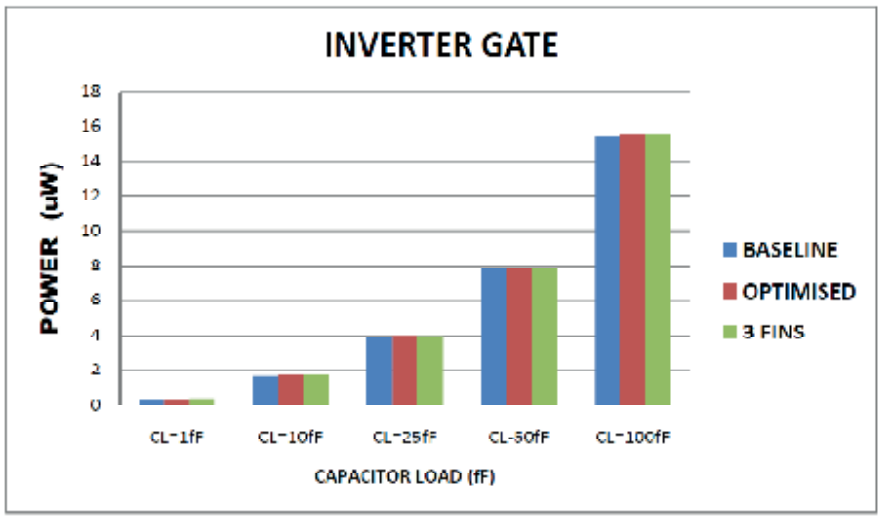
Graph 15: Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=1ns

2) PERIOD = 2ns



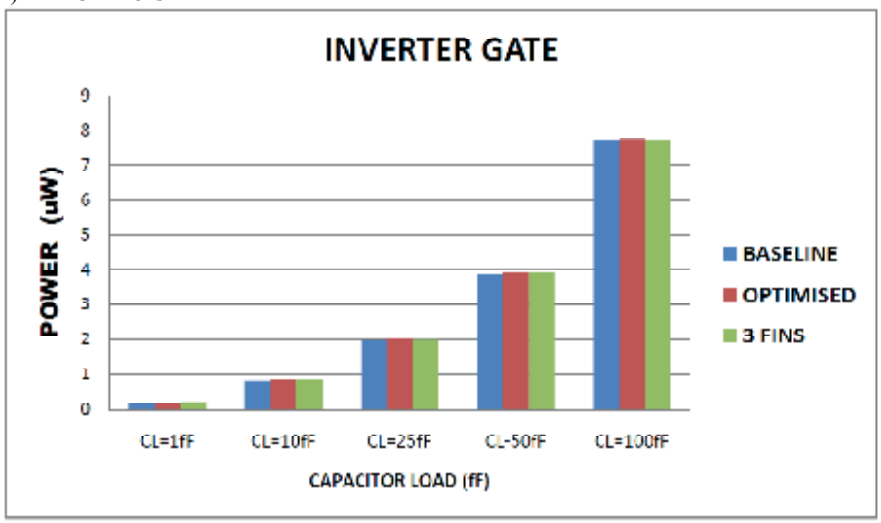
Graph 16: Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=2ns

3) PERIOD = 4ns



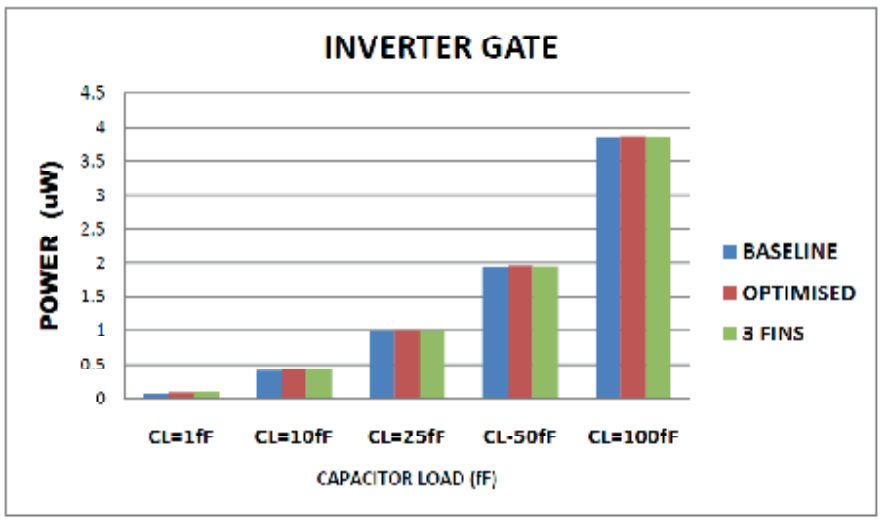
Graph 17: Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=4ns

4) PERIOD = 8ns



Graph 18: Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=8ns

5) PERIOD = 16ns

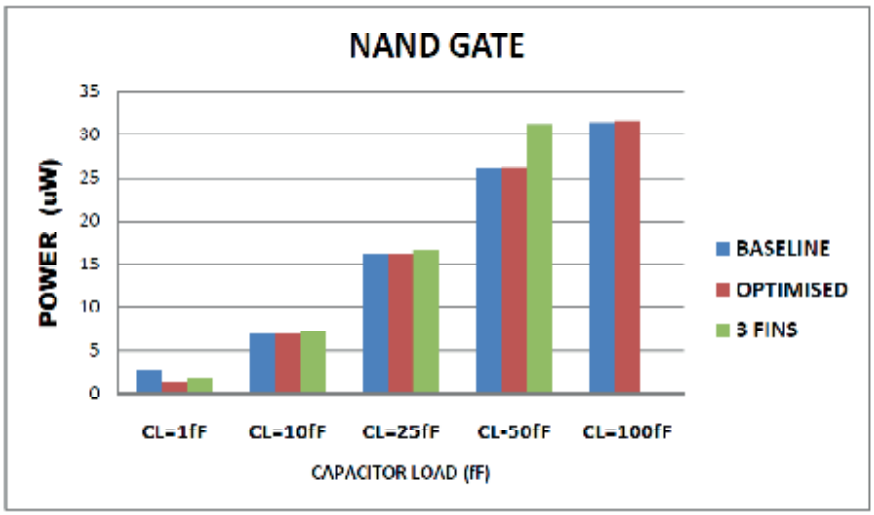


Graph 19: Comparison of Power Consumption of Inverter with 3 different Layout Designs for a period=16ns

INVERTER GATE ANALYSIS : With reference to the above power tables for 3 different types of layouts, for lower frequencies of input signals the baseline and optimised layout designs show the same performance and use low power compare to the 3 fins layout design. But as the frequency of the input signal increases, the performance of the three types of layout is almost the same.

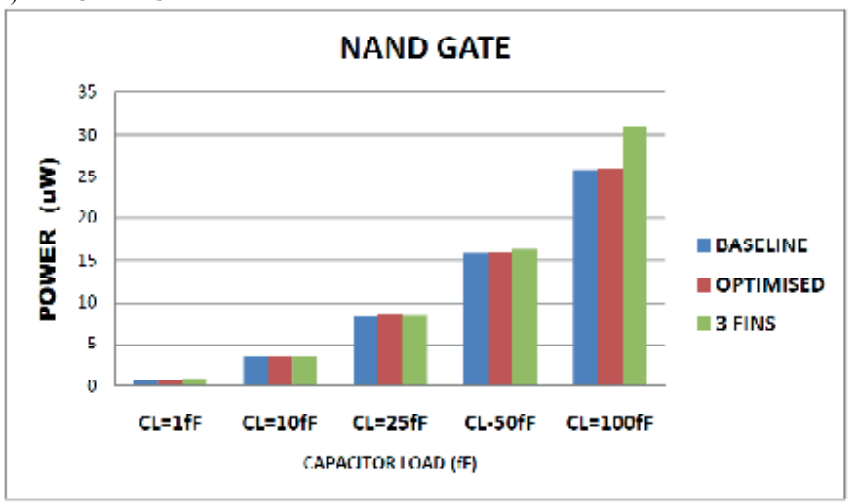
b) NAND GATE

1) PERIOD = 1ns



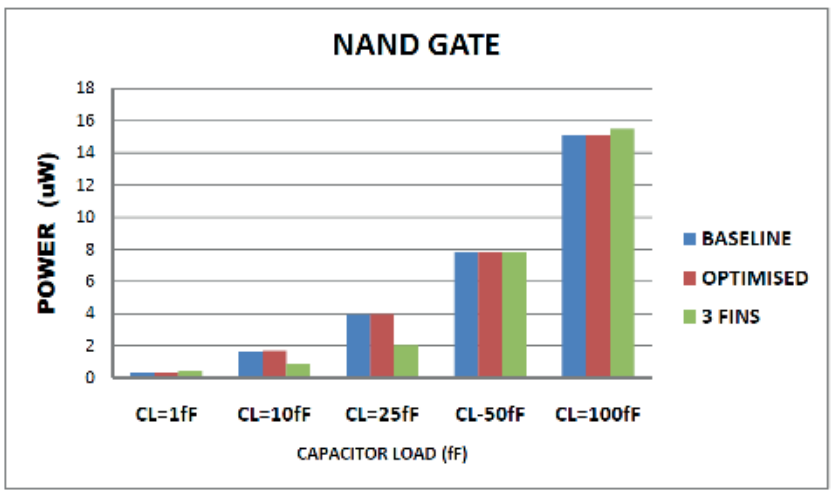
Graph 20: Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=1ns

2) PERIOD = 2ns



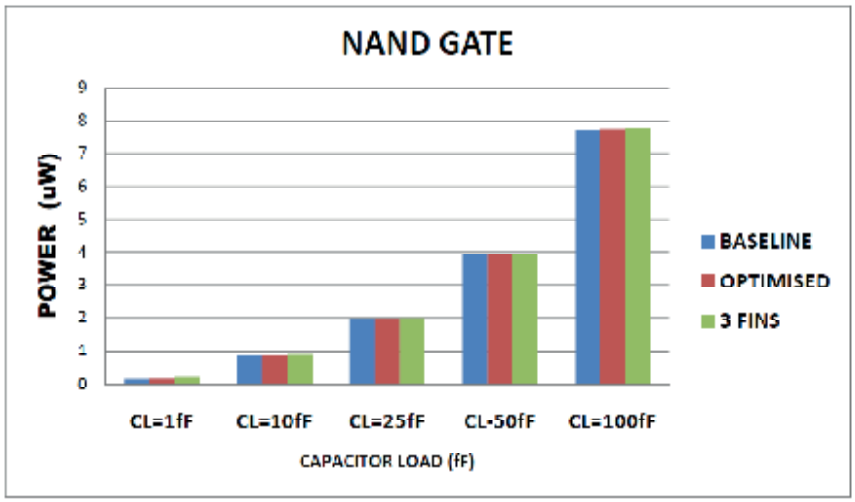
Graph 21: Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=2ns

3) PERIOD = 4ns



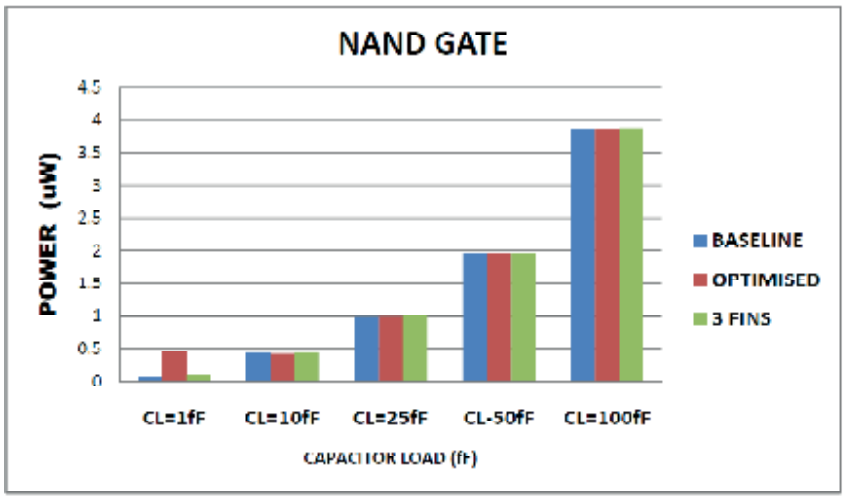
Graph 22: Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=4ns

4) PERIOD = 8ns



Graph 23: Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=8ns

5) PERIOD = 16ns



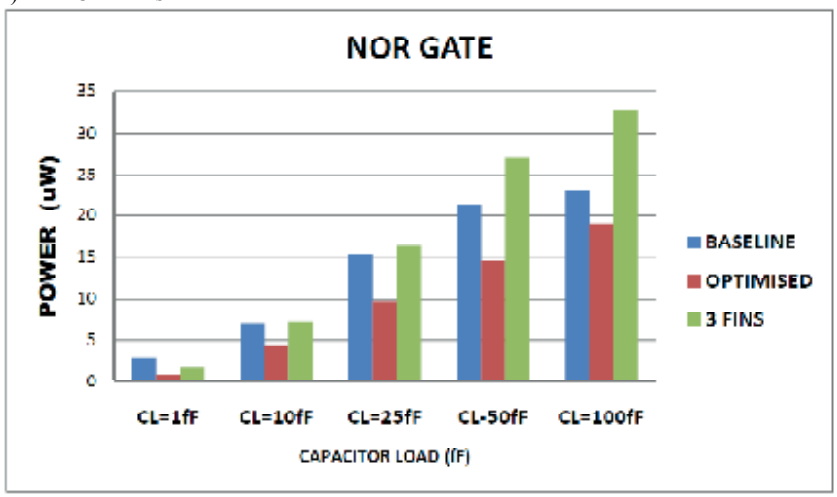
Graph 24: Comparison of Power Consumption of a Nand Gate with 3 different Layout Designs for a period=16ns

NAND GATE ANALYSIS:

On comparing the power numbers for the Nand gate, the performance is similar to that of Inverter gate. But here for the Nand gate, only during the least frequency period baseline and optimized design layout show similar performance. But with the next increased frequency , the performance of all the 3 design layouts are the same.

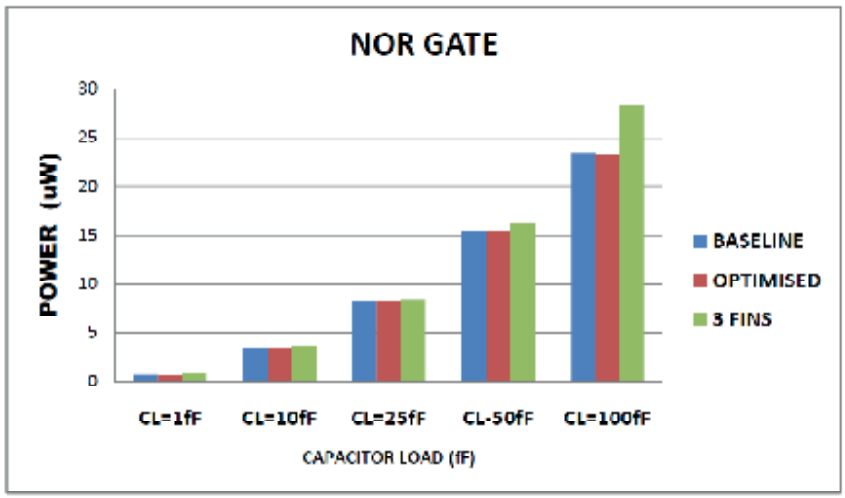
c) NOR GATE

1) PERIOD = 1ns



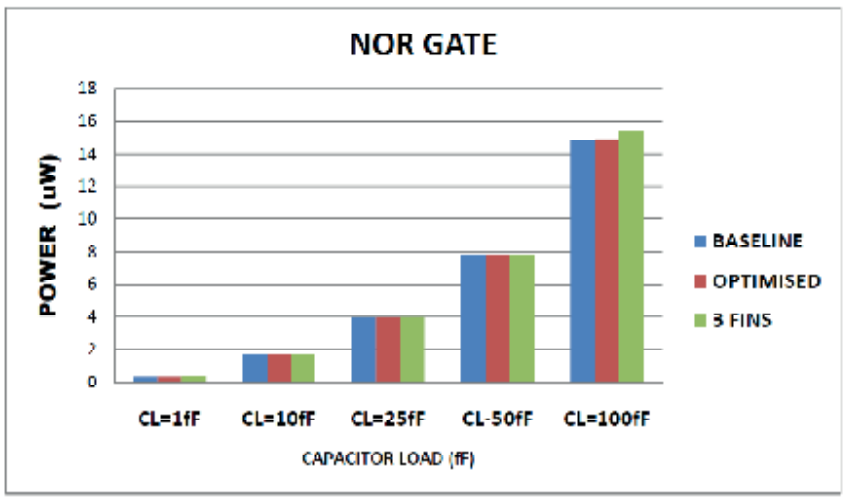
Graph 25: Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=1ns

2) PERIOD = 2ns



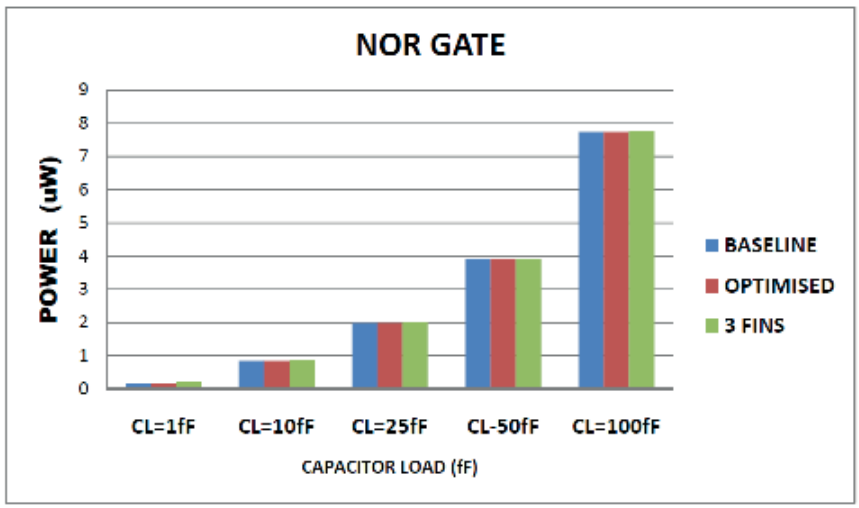
Graph 26: Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=2ns

3) PERIOD = 4ns



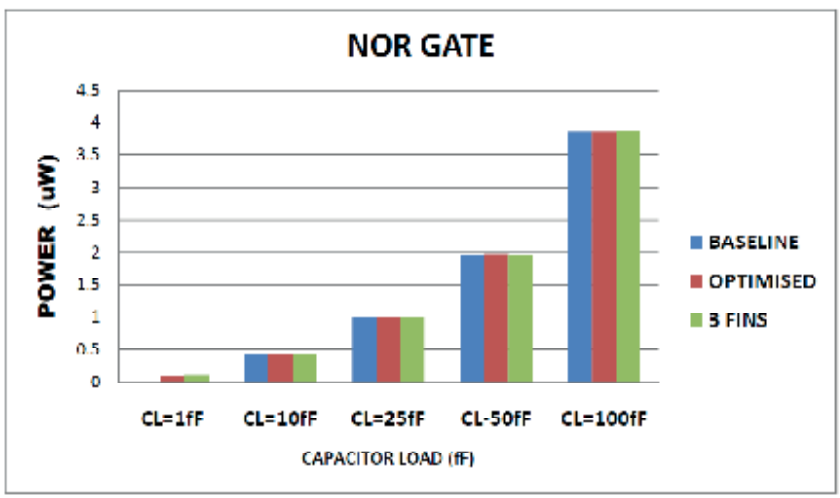
Graph 27: Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=4ns

4) PERIOD = 8ns



Graph 28: Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=8ns

5) PERIOD = 16ns



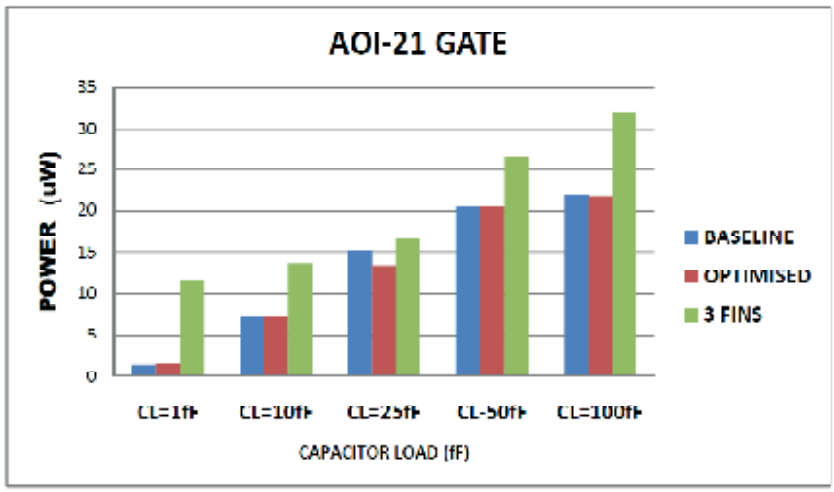
Graph 29: Comparison of Power Consumption of a Nor Gate with 3 different Layout Designs for a period=16ns

NOR GATE ANALYSIS:

From the above power tables of Nor gate, it can be seems that the power numbers fluctuate with frequencies. For the least frequency in the input signals, the optimised design layout shows least power consumption, then the trend for the power number is the same for optimized and baseline design layouts. For higher frequencies the power performance is the same for all the three design layouts.

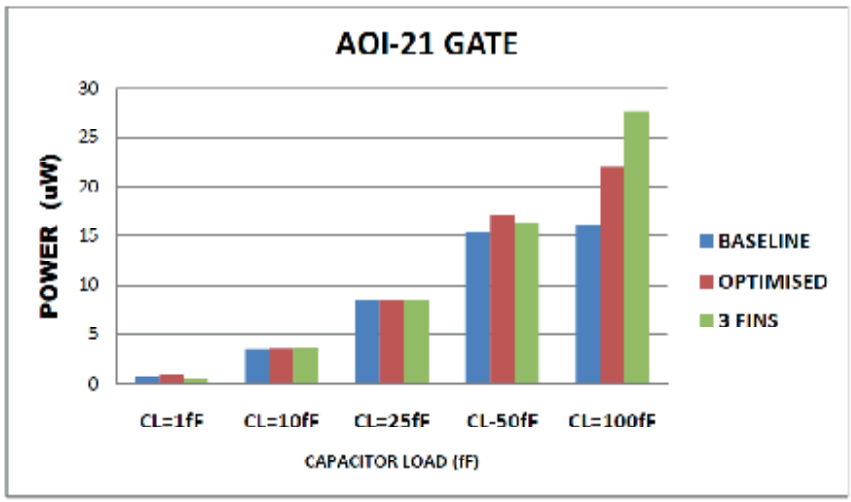
d) AOI-21 GATE

1) PERIOD = 1ns



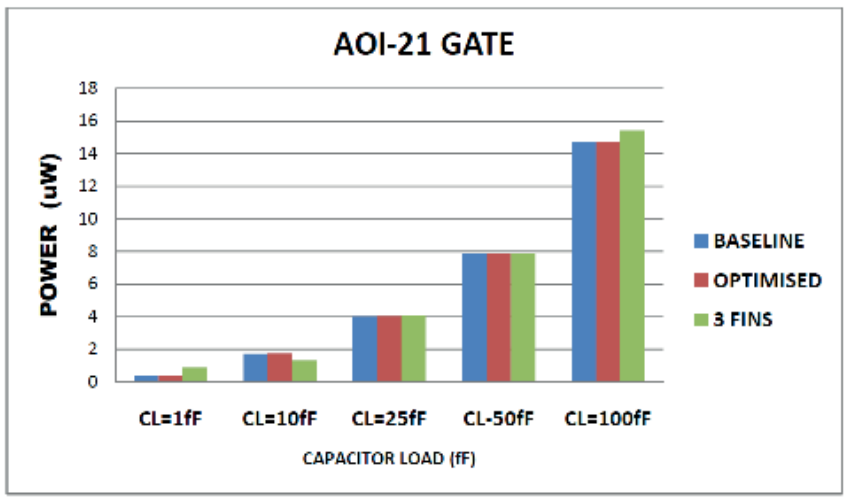
Graph 30: Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=1ns

2) PERIOD = 2ns



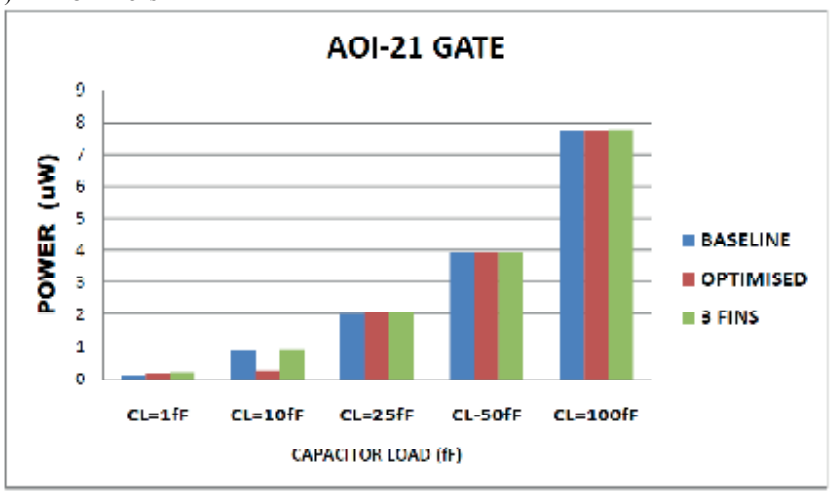
Graph 31: Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=2ns

3) PERIOD = 4ns



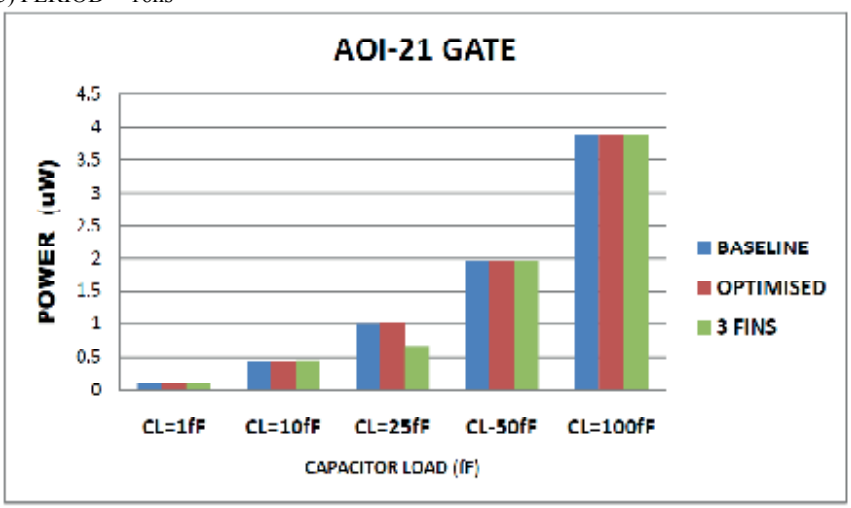
Graph 32: Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=4ns

4) PERIOD = 8ns



Graph 33: Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=8ns

5) PERIOD = 16ns



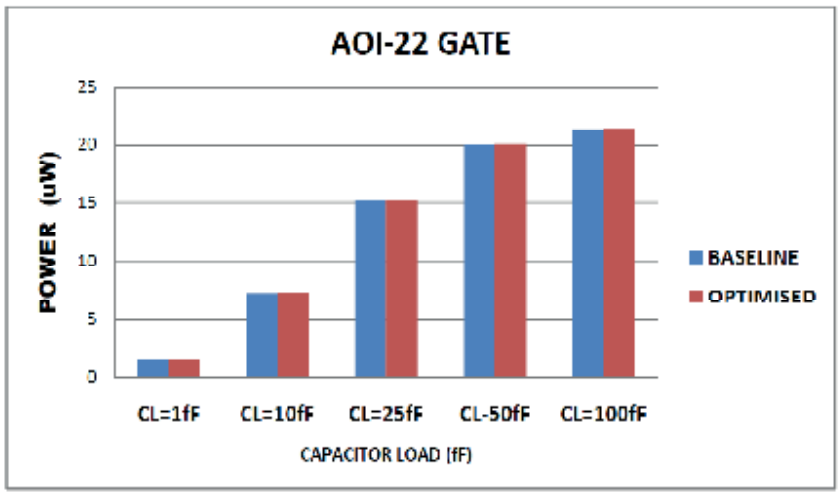
Graph 34: Comparison of Power Consumption of a AOI-21 Gate with 3 different Layout Designs for a period=16ns

AOI-21 GATE:

The power performance for the AOI-21 gate comparing with the various design layouts on an average shows the same consumption of Power.

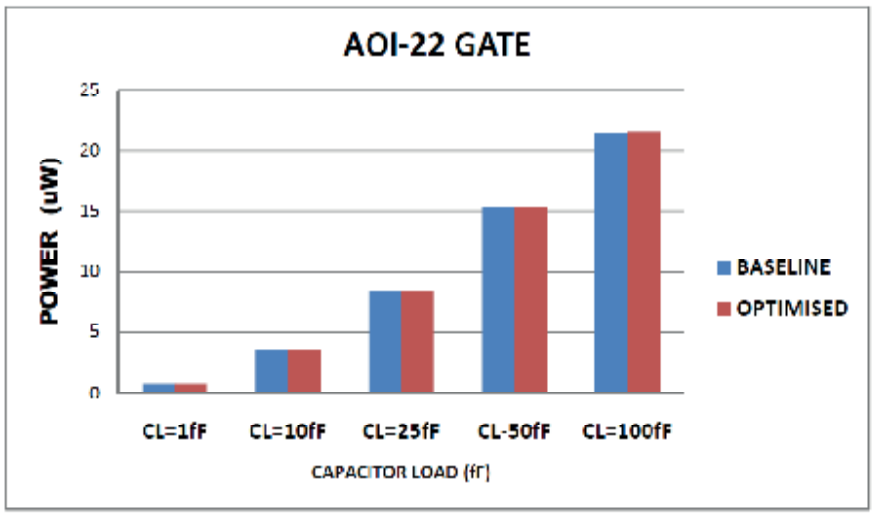
f)AOI-22 GATE

1) PERIOD = 1ns



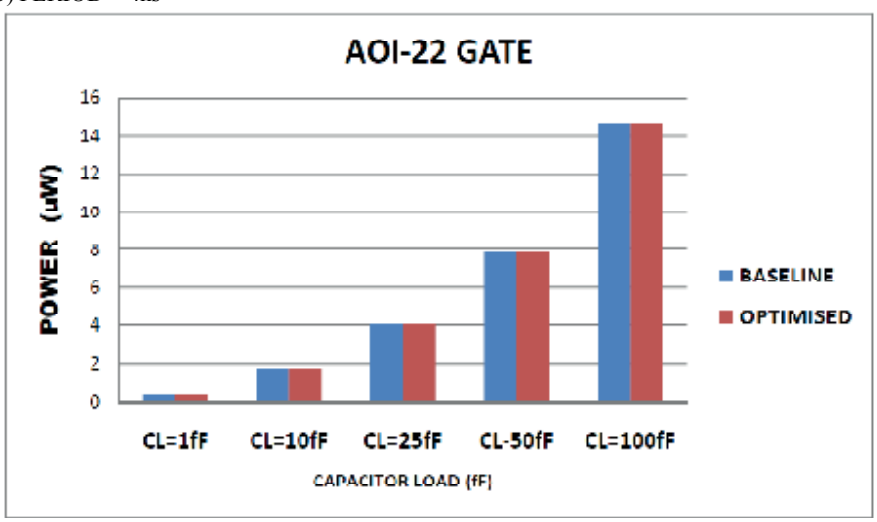
Graph 35: Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=1ns

2) PERIOD = 2ns



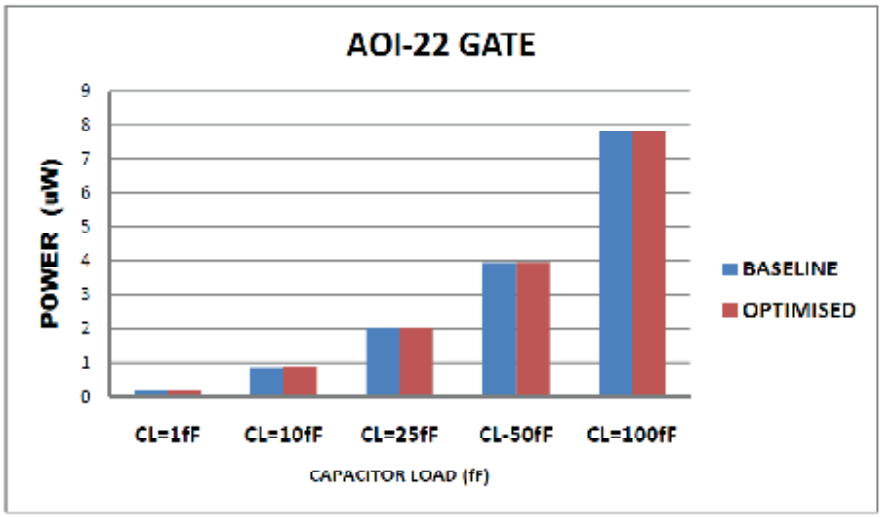
Graph 36: Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=2ns

3) PERIOD = 4ns



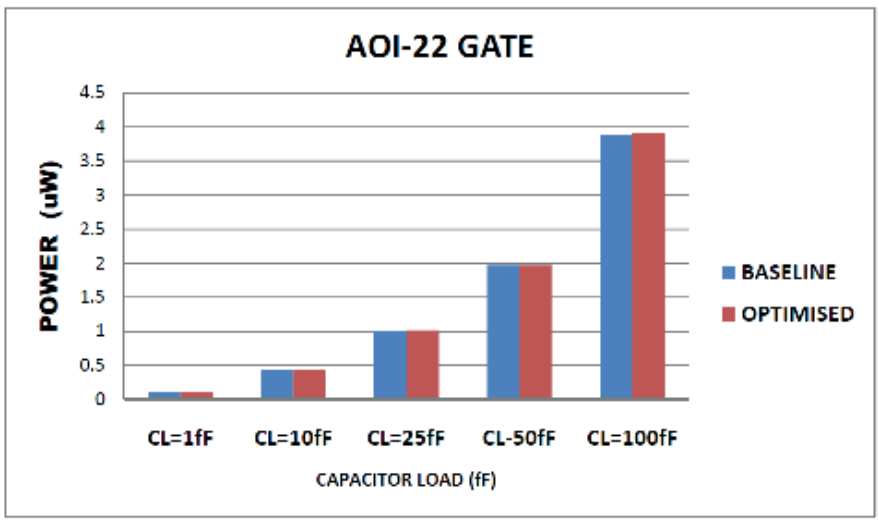
Graph 37: Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=4ns

4) PERIOD = 8ns



Graph 38: Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=8ns

5) PERIOD = 16ns



Graph 39: Comparison of Power Consumption of a AOI-22 Gate with 3 different Layout Designs for a period=16ns

AOI-22 GATE:

The AOI-22 gate has 2 design layout types. Similar to the AOI-21 performance, power performance remains similar to both the design layouts namely baseline and Optimised design layouts.

5.4 IMPROVISED DESIGN LAYOUTS:

The routing of the metal wires and placement of the vias and other components can vary the power numbers. Hence many iterations of the layout designs were power values for the improved version of layout is seen below and analyzed.

Baseline standard layouts were improvised and tested for the same with a capacitor load of 25fF. The additional standard cell layouts were

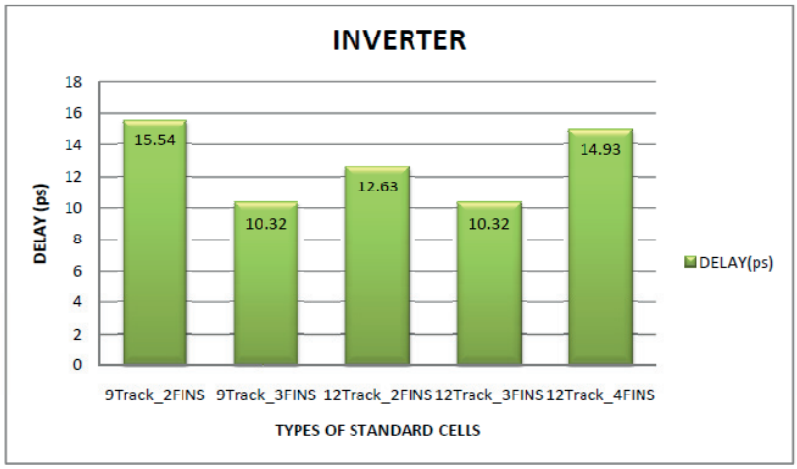
a) Baseline (12 Track) with 3 fins
b) Baseline (12 Track) with 4 fins.

The following graphs show a comparison of the power and Delay for the 5 different types of layouts used with a capacitor load of 25fF.

1)Baseline
2)Optimized
3)3 fins
4)Baseline with 3 fins
5) Baseline with 4 fins.

DELAY

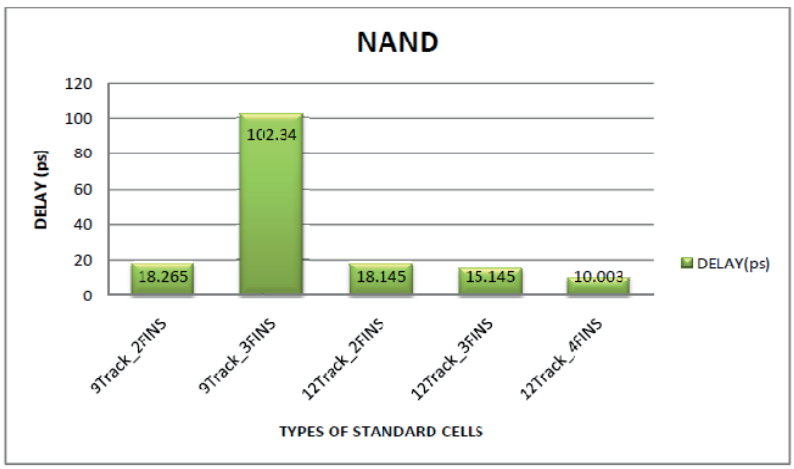
a) INVERTER



Graph 40: Comparison of Delay of a Inverter with 5 different Layout Designs

The Optimum Layout design architecture for an Inverter gate with reference to speed was achieved for **12 Track 3 fins and 9 Track 3 fins.**

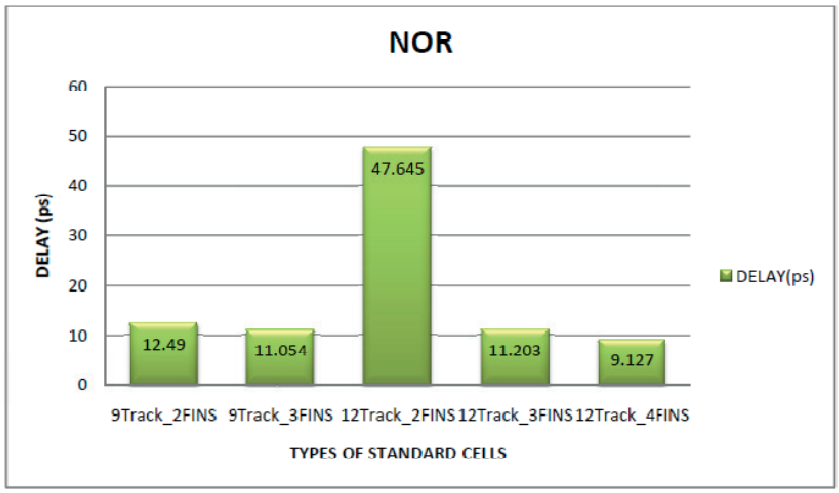
b) NAND



Graph 41: Comparison of Delay of a Nand Gate with 5 different Layout Designs

The Optimum Layout design architecture for a Nand gate for speed performance was achieved for **12 Track 4 fins.**

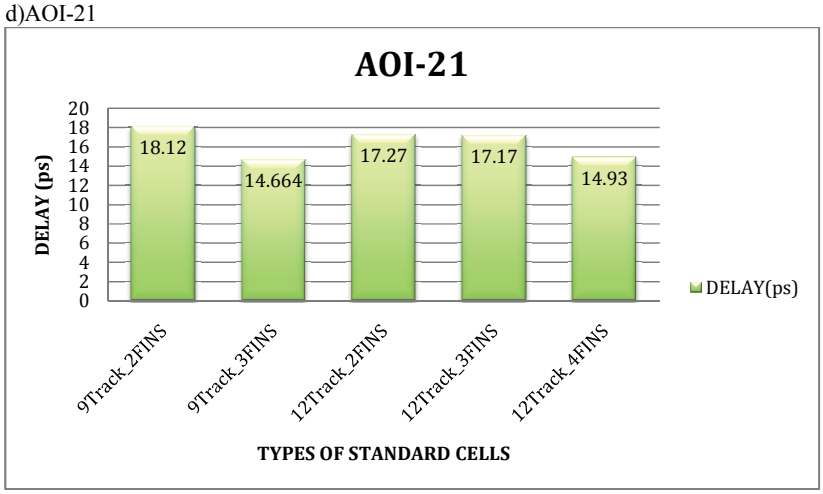
c)NOR



Graph 42: Comparison of Delay of a Nor Gate with 5 different Layout Designs

The Optimum Layout design architecture for NOR Gate was **12 Track 4 fins.**

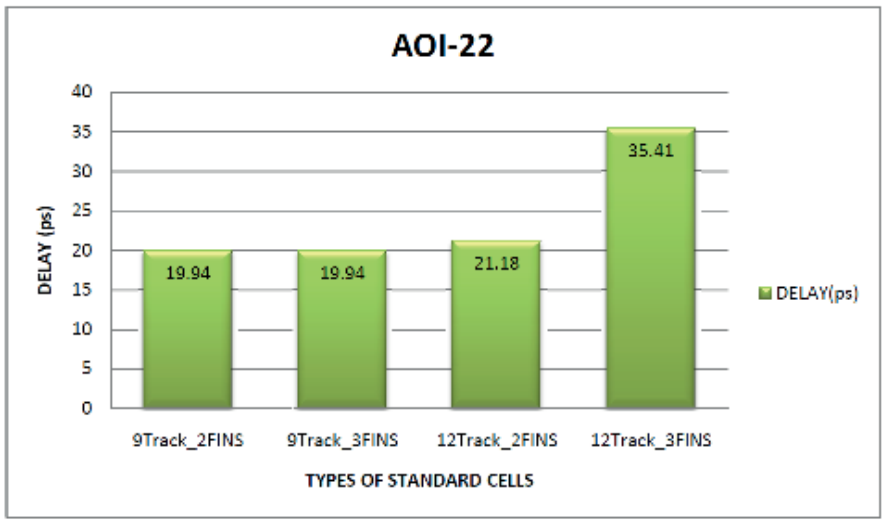
d)AOI-21



Graph 43: Comparison of Delay of a AOI-21 Gate with 5 different Layout Designs

The Optimum Layout design architecture for an Inverter gate with reference to speed was achieved for **9 Track- 3 fins Layout**

e) AOI-22

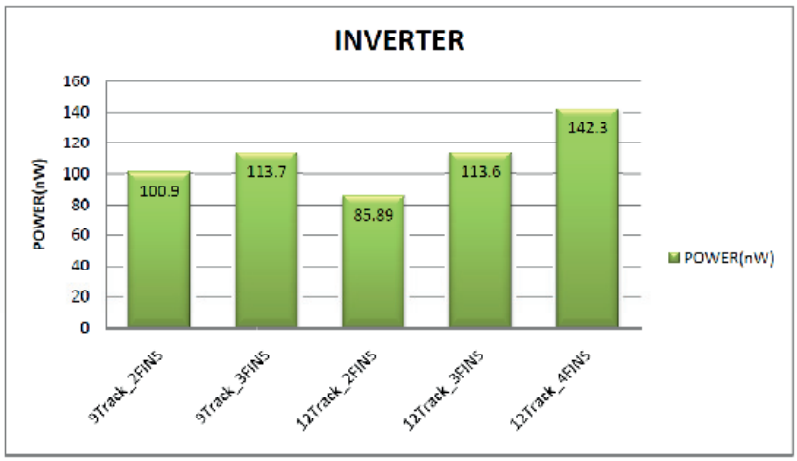


Graph 44: Comparison of Delay of a AOI-22 Gate with 4 different Layout Designs

The Optimum Layout design architecture for an AO1-22 gate with reference to speed was achieved for **9 Track 2 fins and 9 Track 3 fins.**

POWER

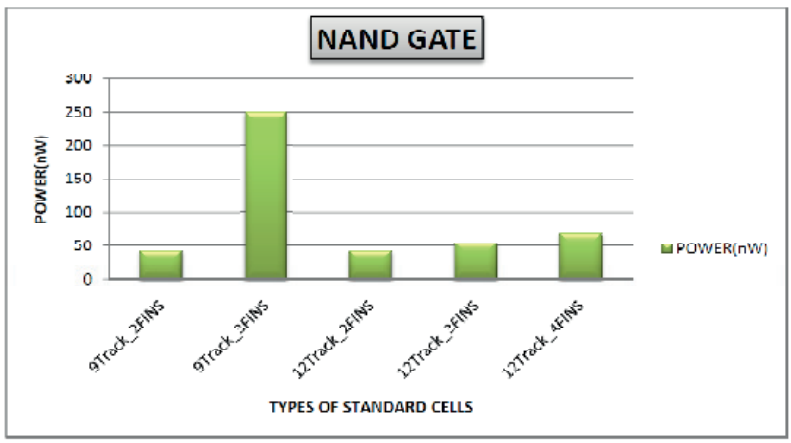
a) INVERTER



Graph 45: Comparison of Power Consumption of a Inverter with 5 different Layout Designs

The Optimum Layout design architecture for an Inverter gate based on Power consumption was achieved for **12 Track 2 fins**.

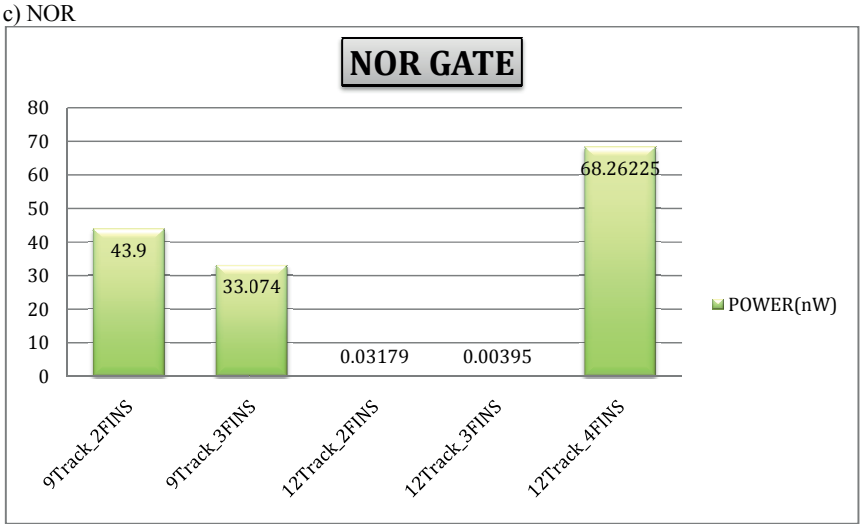
b) NAND



Graph 46: Comparison of Power Consumption of a Nand Gate with 5 different Layout Designs

The Optimum Layout design architecture for Nand gate was **12 Track 2 fins and 9 track 2 fins**.

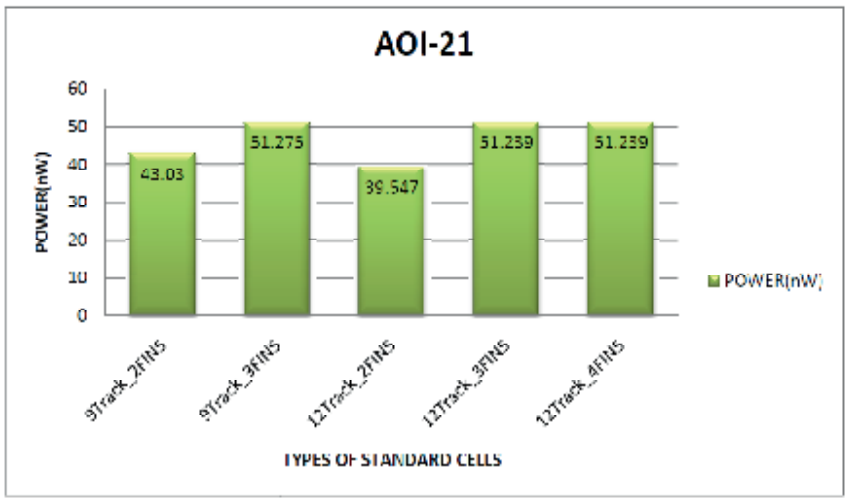
c) NOR



Graph 47: Comparison of Power Consumption of a Nor Gate with 5 different Layout Designs

The Optimum Layout design architecture for a Nor gate based on Power consumption was achieved for **12 Track 2 fins**.

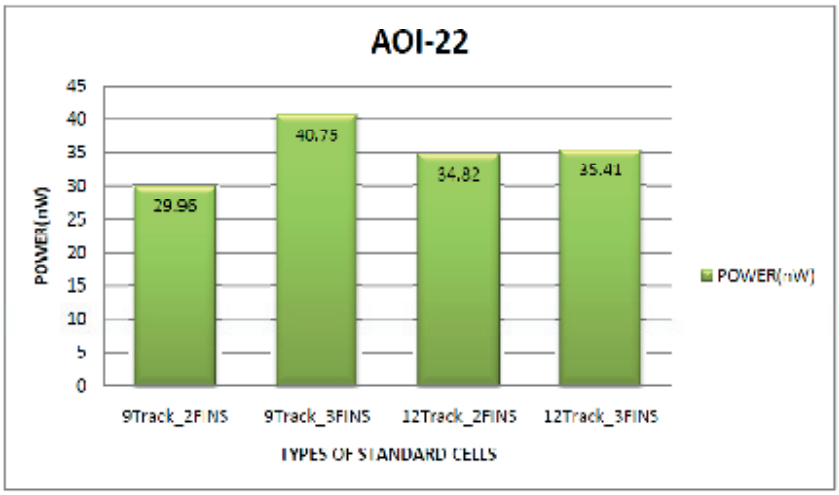
d) AOI-21



Graph 48: Comparison of Power Consumption of a AOI-21 Gate with 5 different Layout Designs

The Optimum Layout design architecture for a AOI-21 gate based on Power consumption was achieved for **12 Track 2 fins**

e) AOI-22



Graph 49: Comparison of Power Consumption of a AOI-22 Gate with 4 different Layout Designs

The Optimum Layout design architecture for a AOI-22 gate was achieved for **9Track- 2 fins**

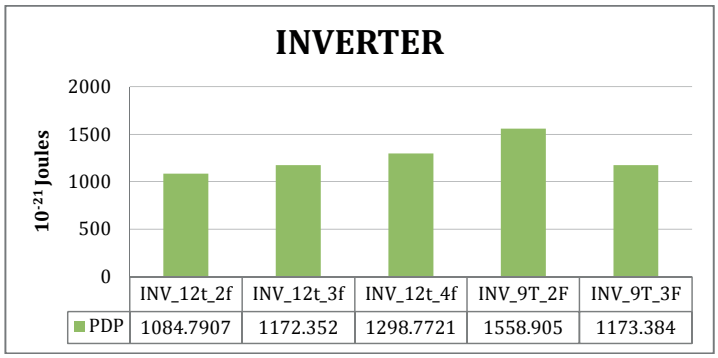
5.5 POWER DELAY PRODUCT:

The power and performance are plotted for different combinations and analysed.
The logic level transition depends on 2 factors – Capacitance at the nodes and the current, which can be supplied to charge and discharge these nodes. The larger the value of current available, the faster the nodes can be charged or discharged and hence faster the gate. However this implies the power consumption would be affected and hence an optimum metric to compare would be to use the power delay product (PDP). PDP also measures the energy consumed during a switching event of a signal.

Power Delay Product is measured as a product of delay of the switching event and power consumption during that event.
The power values shown in table and corresponding delay values of respective circuits are used and the PDP values are obtained.

With reference to the layout drawn in this thesis the following results are observed.

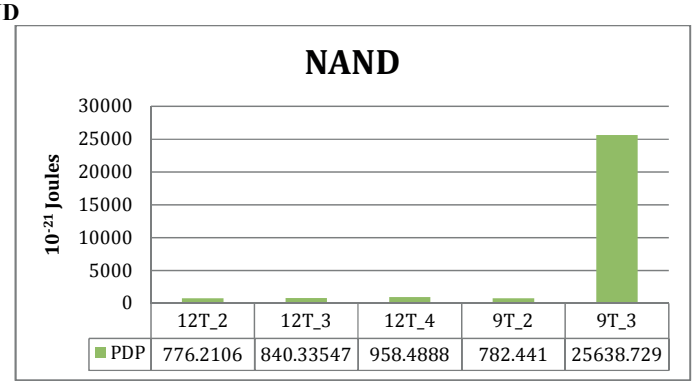
1) INVERTER



Graph 50: Power- Delay Product for inverter with different combinations of track height and fins

The Optimum Inverter design was achieved for **12 Track 2 fins**

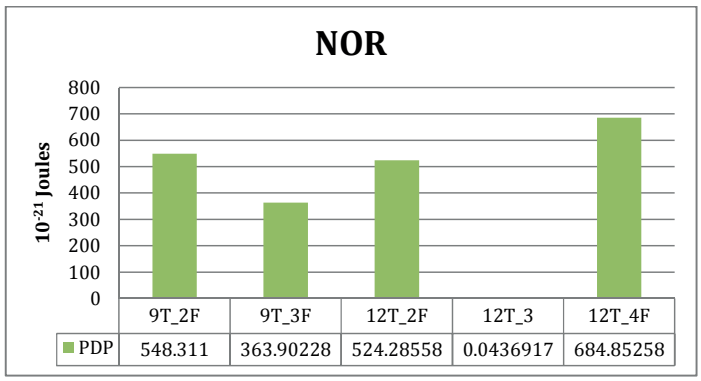
2) NAND



Graph 51: Power- Delay Product for Nand Gate with different combinations of track height and fins

Optimum Nand Gate design was achieved for **12 Track 2 fins**

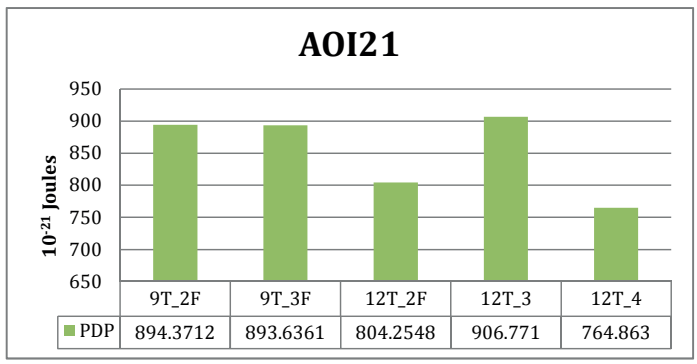
3) NOR



Graph 52: Power- Delay Product for Nor Gate with different combinations of track height and fins

Optimum NOR Gate design was achieved for **12 Track 3fins**

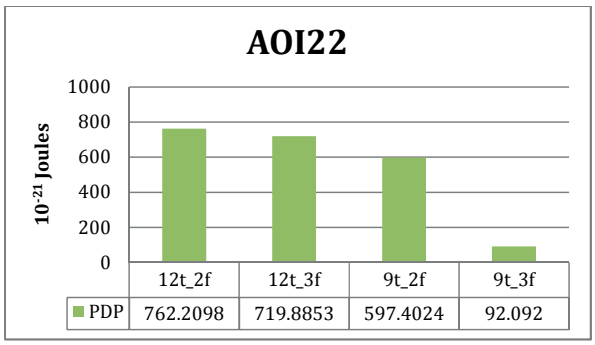
4) AOI-21



Graph 53: Power- Delay Product for AOI-21 Gate with different combinations of track height and fins

Optimum AOI-21 Gate design was achieved for **12 Track 4 fins**

5)AOI-22

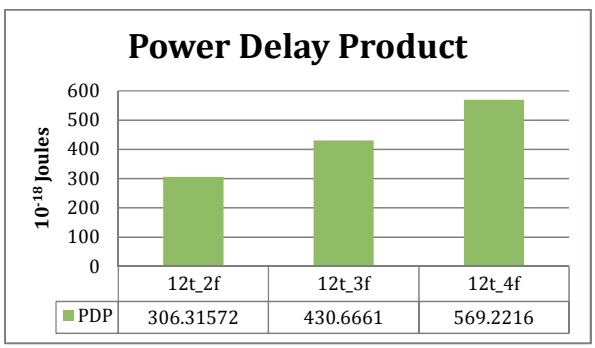


Graph 54: Power- Delay Product for AOI-22 Gate with different combinations of track height and fins

Optimum AOI-22 Gate design was achieved for **9 Track 3fins**

RING OSCILLATOR: Ring Oscillator is designed using the baseline architecture. It consists of 12 track height and metal width used is 45 . The PFET and NFET use 2 fins each respectively.
A 21 stage ring oscillator is designed using the inverter cell. Below graph shows the the power and Power delay product of the Ring oscillator for different capacitor Loads namely 1fF, 5Ff, 10Ff.

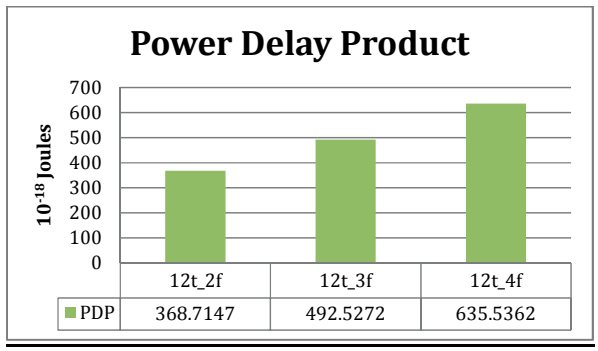
a) Baseline Design Layout :



Graph 55: Power- Delay Product for Ring- Oscillator with different combinations of fins and capacitor load of 1fF

Optimum Ring Oscillator Gate design was achieved for **12 Track 2 fins**

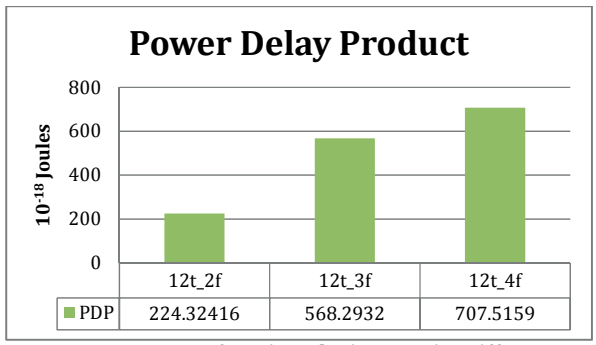
b) Baseline Design Layout :



Graph 56: Power- Delay Product for Ring- Oscillator with different combinations of fins and capacitor load of 5fF

Optimum Ring Oscillator Gate design was achieved for **12 Track 2 fins**

c) Baseline Design Layout :



Graph 57: Power- Delay Product for Ring- Oscillator with different combinations of fins and capacitor load of 10fF

Optimum Ring Oscillator Gate design was achieved for **12 Track 2 fins**

It is seen that in most cases the 12track 2 fins was the optimum one in terms of Power Delay Product. This could possibly be because of easier routing of the layers. Having more number of fins increases the power, but the performance increases. Hence with respect to the application the specific standard cell architecture is chosen.

Chapter 6

Conclusion

This thesis mainly focusing mainly on manufacturing process and deciding the best ways to optimize the architecture of standard cell layout for 10nm node using Finfet devices.
Based on the study during the thesis, it can be concluded that Self Aligned Double patterning was the best method for producing Fin devices with the current Foundry facilities available at IMEC, Belgium.

The best layout for the standard cells with reference to routing of metals for the current design rules was 12 track 2 fins. This is mainly due to the following reasons namely, layouts designed with these specifications gave more routing space especially when designing complex circuits. During scaling of devices, the design rules get more complex due to the shrinking of devices and many new layers are also introduced during this project. Another main focus subject during my thesis was to decide types of design layouts would result in low power design layouts. Theoretically as the number of fins in a circuit increases the speed increases, but power consumption also increases. With reference to the delay numbers for different cells designed using 2, 3 and 4 fins, it was expected that for all the circuits cells with 4 fins would perform fastest. But in few cases except Nand and Nor Gates, Inverter, AOI-21, AOI-22 gates showed that devices using 2 or 3 fins could also perform faster or equal to performance of 4 fins devices.

Regarding Power consumption of cells, in most of the cases the baseline design layout consisting of 12 track cell height and 2 fins devices shows low consumption of power. They were few circuits like Nand and AOI-22 gates which show 9 track cells with 2 fins also consuming low power. The reason some values were not as expected could be also be due to the current version of Layout Design Rules given by the foundry and also the ways the metals were routed.

Power Delay Product (PDP) for different sets of finfets was observed. The number of fins and height of the cell played the main variants for the comparison. With reference to the Power Delay Product results, the majority of cell types showing low power and energy consumption is 12 track 2 fins cells i.e. Baseline design layout cells. The reason for the drawn layout could be abundance routing space and hence with less use of VIAS and use of newly introduced layers during this project namely the local interconnects. However the Nor gate showed unexpected value for Power Delay Product, this could also be due to the circuit connections

Hence it is seen that SADP Manufacturing process, using the track height cells as 12 with 45 nm of metal width and hence having a cell height of 540nm gives optimum results for the current circuits used.

Future work:

The current work can be further carried out for different manufacturing process like SAQP-Self Aligned Quadruple Patterning and with different design rules. Updated version of Layout Design Rules with reference to corresponding foundry specifications, the above circuits can be routed and its performance can be compared with the obtained results. The design rules can also be applied to more complex circuits. Variants of Layout design templates with reduced or increased track heights could be tested. The other main key factors for technology scaling namely Cost and Area can also be evaluated for different Layout architectures.

Bibliography

1. David J Frank, Hon-Sum Philip Wong et al.,"Device Scaling Limits of Si MOSFETs and their application dependencies" Proceedings of the IEEE, Vol 89, No.3, March 2001

2. G. Baccarani, M.R. Wordeman, and R.H. Dennard, "Generalized scaling theory and its Application to 1/4th um MOSFET Design", IEEE Trans. Electron Devices, Vol ED-331, No.4, pp 452-462, April 1984

3. James Warnock, "Circuit Design Challenges at the 14nm Technology Node," DAC 2011, IBM 14nm Design Challenge.

4. Gordon E. Moore, "Cramming more components onto integrated circuits," Electronics, pp, 114-117, April 19, 1965.

5. Wolfgang Arden , Michel Brillouët , Patrick Cogez , Mart Graef , Bert Huizing , Reinhard Mahnkopf , "More-than-Moore" White Paper ,IRC-ITRS

6. Finfets and Other Multi-Gate Transistors by J.-P. Colinge

7. David Fried, Thomas Hoffman, Bich-Yen Nguyen and Samavedam, "Comparison Study of Finfets: SOI vs. Bulk, SOI industry consortium

8 Andrew R. Brown, Nicolas Daval, Konstantin K. Bourdelle, Bich-Yen Nguyen, and Asen Asenov "Comparative Simulation Analysis of Process-Induced Variability in Nanoscale SOI and Bulk Trigate Finfets", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 11, NOVEMBER 2013

9. Comparing SOI and Bulk Finfets: Performance, manufacturing variability, and cost, SOLID STATE TECHNOLOGY, NOVEMEBER 2009, Cover Article.

10. Xin Sun, *Member, IEEE*, Victor Moroz, Nattapol Damrongplasit, *Student Member, IEEE*,Changhwan Shin, *Student Member, IEEE*, and Tsu-Jae King Liu, *Fellow, IEEE* , "Variation Study of the Planar Ground-Plane Bulk MOSFET, SOI FinFET, and Trigate Bulk MOSFET Designs" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 10, OCTOBER 2011

11. Double Patterning process development at IMEC

12. Design Rule Manual DR01, DR02, IMEC FOUNDRY

13. Arindham Mallik, Diederik Verkest, Bhavana Ballal et al, “TEASE: A systematic analysis
Framework for early evaluation of FinFET based advanced technology nodes,” in Design Automation conference, USA 2011

14. Rani S. Ghaida, Kanak B. Agarwal_, Sani R. Nassif_, Xin Yuany, Lars W. Liebmannz, Puneet Gupta, “A Framework for Double Patterning-Enabled Design” DRE_ICCAD 2011

15. Abde Ali Kagalwalla1, Swamy Muddu2, Luigi Capodieci2, Coby Zelnik3, and Puneet Gupta “Design-of-Experiments Based Design Rule Optimization “DRE-SPIE-2012

16. Tsu-Jae King Liu, Department of Electrical Engineering and Computer Sciences University of California, “FinFET History, Fundamentals and Future”.

LUND
UNIVERSITY

Series of Master's theses
Department of Electrical and Information Technology
LU/LTH-EIT 2014-403

http://www.eit.lth.se