

LUND UNIVERSITY



Extraction of Border Trap Density in InAs Nanowire Transistors

MSc Thesis in Nanoscience

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List of Abbreviations

ALD: Atomic Layer Deposition

Al₂O₃: Aluminum Oxide

g_m: Transconductance

HfO₂: Hafnium Oxide

KMP-1B-B1: Name for an InAs Nanowire Sample

MOVPE: Metal Organic Vapor Phase Epitaxy

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

N_{bt}: Border Trap Density

Si₃N₄: Silicon Nitride

SiO₂: Silicon Oxide

S06A-E2: Name for an InAs Nanowire Sample

VLS: Vapor Liquid Solid

VLSI: Ultra Large Scale Integration

VNA: Vector Network Analyzer

1 INTRODUCTION

1.1 Background

The problem with SiO₂ as the gate dielectric for transistors is that gate current leakage occurs, resulting from carriers being able to tunnel through dielectric when this film is required to scale to ultrathin ^[1]. It is unfavorable to use SiO₂ for VLSI where the transistors are required to be smaller and smaller, therefore searching for a new insulator with a higher permittivity became a necessity. The HfO₂ has been used as a substitute by researchers in recent years, yet the trick with this high k film is there exists the near-interface traps; those border traps in oxide are responsible for frequency dispersion of capacitance in accumulation ^[2]. Solutions, i.e. annealing of ALD deposited films or using the bilayer structure of Al₂O₃ plus HfO₂, as a consequence have been made to reduce the number of those charges. Meanwhile, it is equally important to see to what extent these traps affect the transistor performance, so in this work we are interested in calculating the number of this type of defects.

The trapping ability of a border trap in the nanowire can be directly described by its location: the farther a trap is seated from the interface, the longer time it will take for the trap to be filled by the carriers from the semiconductor. Therefore, the higher frequency it goes with the semiconductor, the less the possibility it is for the carrier to be trapped. For convenience, there is a need to describe the traps in terms of their trapping ability by a similar concept as the frequency for carriers in semiconductor: the time constant.

1.2 Time constant

In a MOS, the time constant τ by its definition is the time period before which a trap site in the oxide is filled by tunneling of an electron from the semiconductor and is in an exponential relation with the trap location from semiconductor-oxide interface ^[3]:

$$\tau(x) = \tau_0 e^{2\kappa x} \quad (1)$$

where prefactor τ_0 is inversely proportional to the carrier density at the interface, x the distance of a trap from the interface, and κ is the attenuation coefficient for the wave function of an electron with energy E under an energy barrier E_C^{ox} :

$$\kappa = \sqrt{2m^*(E_C^{ox} - E)/\hbar} \quad (2)$$

where m^* is the effective mass of electron in the dielectric and E_C^{ox} is the energy of the top of the dielectric barrier.

The time constant of a trap is related to its location by equation (1): the further the trap is located from the interface, the longer the time constant of the trapping it costs. At the same time, the frequency of a trap can be related to its location as the frequency is reversely proportional to the time constant.

According to Fleetwood ^[4], it is these traps who are located within 3 nanometers from the semiconductor-insulator interface in the oxide are called the near-interface-traps or the so-called border traps.

1.3 Border traps

Due to the location characteristic of these border traps, the performance of the MOS device is deteriorated by those traps, depending on the operation frequency as the frequency of a trap is correlated to its location by equation (1).

In figure 1(a), the molecule structure for the interface is not perfect as indicating in the graph, yet there are 3 types of defects existing within 3 nm from the interface ^[4]:

- (1) Pb-like defects: which are the dangling bonds of, for instance, In^+ atoms diffusing to the oxide, they are the closest to the interface;
- (2) Anonymous positive charge centers: caused by the detrapping of electrons from the trap sites, they are less closer to the interface;
- (3) Rechargeable E' centers: who have more dangling bonds, diffuse into the deepest part of the oxide and still exchange the electrons with the semiconductor.

All of these above traps are switching oxide traps and are selective in trapping the carriers in terms of the frequency of the signal; it can be demonstrated by the dark stripe area in figure 1(b) as well, including the boundary.

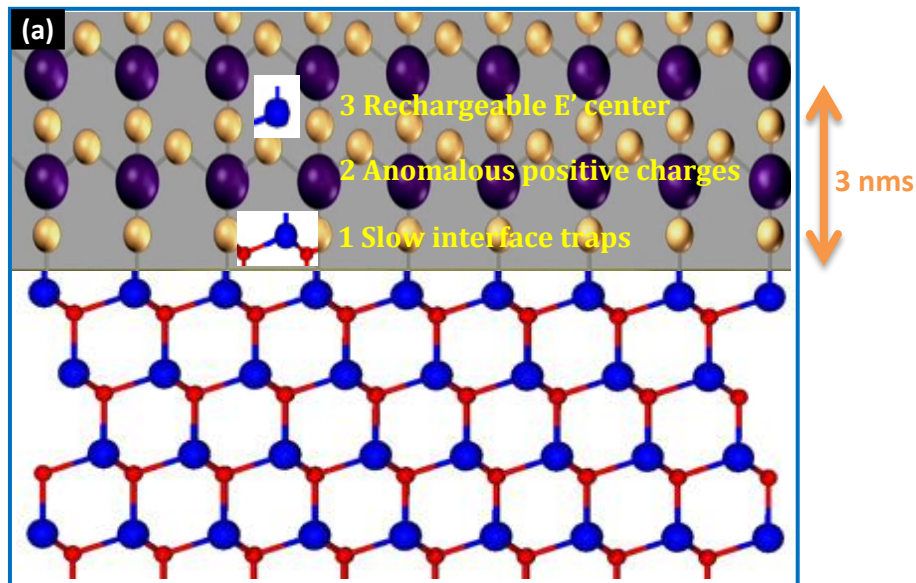


Figure 1(a) Molecular structure of InAs (lower part) and Al₂O₃ (upper part) interface. Blue and red circles denote In and As respectively for InAs, plus purple and yellow circles indicate Al and O atoms respectively for Al₂O₃ ^[5].

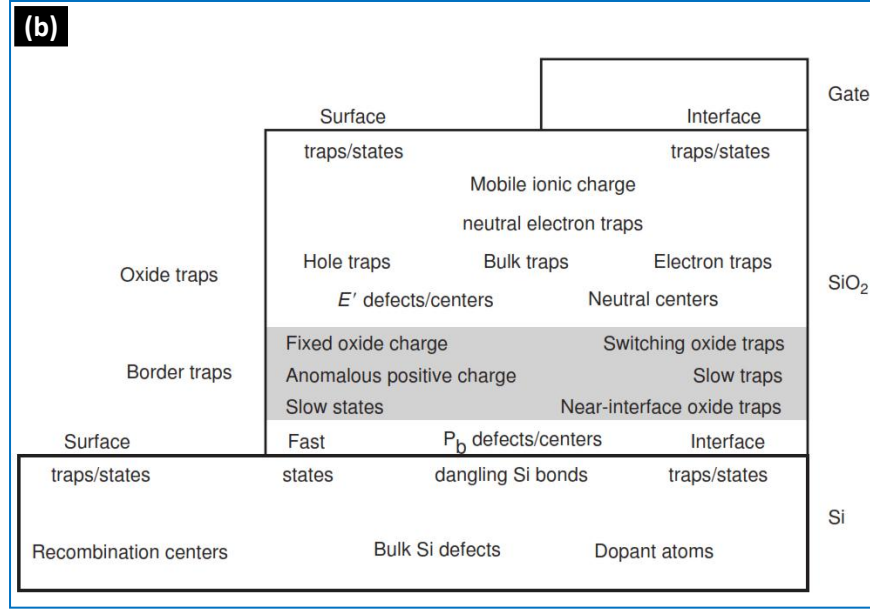


Figure 1(b) The distribution of the traps on the interface and the border traps for a MOS device, which include Pb-like defects, anonymous positive charge centers and rechargeable E' centers in the picture ^[6].

In terms of electrical response, the border traps are also defined as those charges whose time constant is comparable to the frequency of the transmission signal in the semiconductor, here in the thesis work we are concerned with the frequency from several mHz up.

1.4 Motivation

The reported frequency dispersion of capacitance in accumulation by *Kim et al. 2010* ^[2] is a good illustration of how the border traps can deteriorate the device performance, with the comparison device under forming gas annealing. Thus it is of ultimate interest to study on the transistor oxide and discover the number of those border traps, as a result of this, the trapping of border sites should be circumvented by, for instance, using bilayer structure of Al₂O₃ plus HfO₂ in the high-k dielectric.

1.5 The idea

In the thesis, one very important part of the work is that we will design an electrical circuit with a lock-in amplifier for low frequency measurement (mHz ~ 100 kHz) to characterize the InAs nanowire transistors and plot the relation of transconductance g_m against the frequency, see figure 2(b), from which we are able to extract the border traps density N_{bt} .

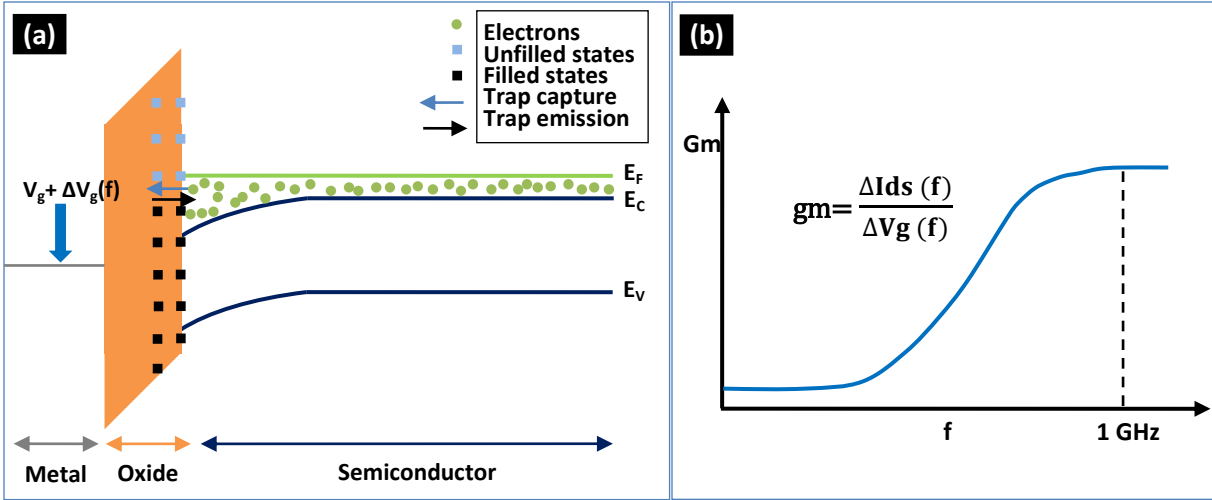


Figure 2(a) A schematic image of the band structure for a MOS transistor with positive bias, where electrons in conduction band can tunnel through the semiconductor-dielectric interface and trapped in the dielectric; (b) A schematic of how g_m of the transistor changes with the frequency of input gate signal $V_g(f)$.

There is an equilibrium of the trap capture and emission when there is a DC gate bias, see figure 2(a), in a transistor due to the difference of the carrier density around the interface and also the detrapping of the electrons. However, this equilibrium will be disturbed unidirectionally once the gate bias is perturbed by a small frequency dependent voltage.

- (1) When the frequency is low, the traps follow the signal, thus there will be electrons from the channel that are trapped in the oxide and the measured transconductance will be low;
- (2) When the frequency is increased, the charge are less able to trap the signal, thus the trapping is reduced and correspondingly the transconductance is increased;
- (3) When the frequency is very high and the carrier exchange is totally suppressed, then the transconductance is recovered to a normal and stable level.

Therefore, the higher the frequency goes, the less the equilibrium could be affected and less trapping can happen.

In principle, the intrinsic transconductance (g_m at very high frequency) indicates how well the drain current I_{ds} can follow with the changes in gate voltage V_g , but the quality of the transistor is determined by below which frequency the g_m starts to decrease. The border traps well explain the decay of transconductance at low frequency once these charges are comparably fast enough to catch the transmission signal. Therefore, we will obtain some relation as plotted in figure 2(b), where it is flat and low level at low frequency but flat and high level at high frequency after a steady increase. The increase of the transconductance thus is caused by the border traps, from the slope of the curve we will be able to calculate these trap density.

In our experiment, the time scale for electrical characterization we are interested in was mHz ~ 1GHz, as a consequence, the switched states in HfO₂ that we are able to read out must be in this scale.

2 DEVICES

The devices we used for the analysis are: (1) S06A HfO₂ gate wrapped nanowire transistor^[7], consists of n-InAs are vertically grown by the VLS technique on a silicon substrate; (2) KMP-1B with an oxide structure of bilayer Al₂O₃+HfO₂ gate wrapped nanowire transistor^[8].

2.1 S06A

The n-doped InAs nanowires, which will be acting as the carrier channel, are epitaxially grown on the silicon (111) substrate. The HfO₂ gate oxide is wrapped around the vertical standing nanowires, refer to figure 3.

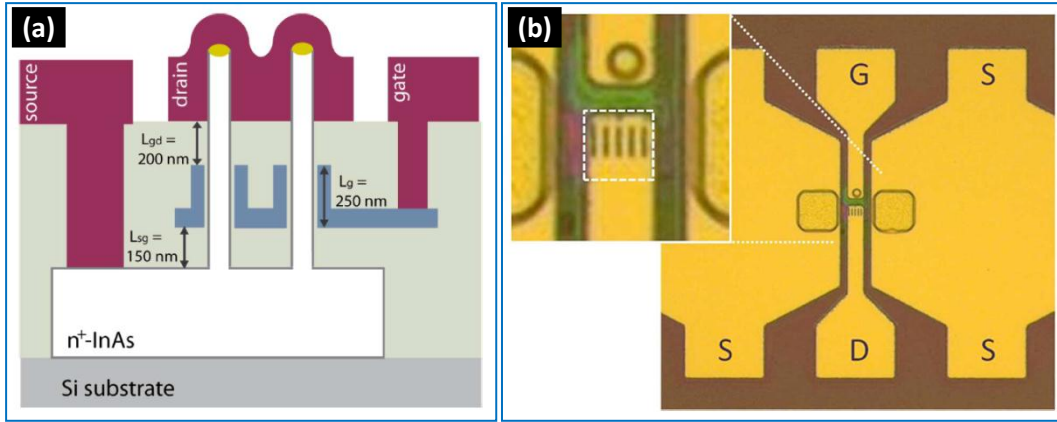


Figure 3 (a) A schematic side view of the InAs nanowire transistor with HfO₂ dielectric (ALD temperature of 250 °C) at the gate length $L_g=250\text{nm}$; (b) the top view of the metal pads from a microscopy, where the inset in the dashed rectangular gives the nanowire cell^[7].

The number of nanowires coupled for the transport as well as the diameter of each single nanowire will affect the drain current that the device can reach. For our experiment, we chose the device S06A-E2, with the best performance in terms of I_{ds} . The nominal number of nanowires coupled for the S06A-E2 is 190 and diameter of each nanowire is 40 nm, however the real number of nanowires is around 160 ~ 170.

2.2 KMP-1B

As a comparison, we consider another nanowire transistor KMP-1B, see figure 4 below, where the gate dielectric (the white line wrapped around the nanowire) consists of a bilayer of Al₂O₃ and HfO₂. Since the border traps in HfO₂ close to the interface is replaced by Al₂O₃, thus the

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trapping ability of the oxide should be reduced. Besides, the ALD temperatures for Al_2O_3 and HfO_2 are 250 °C and 100 °C respectively.

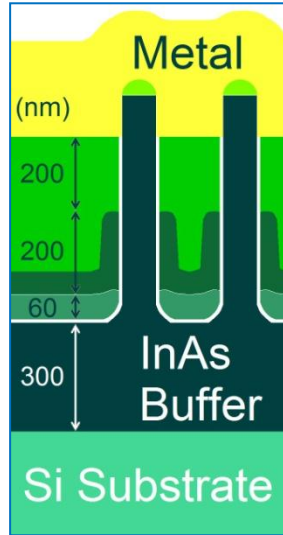


Figure 4 a schematic of side view of the InAs nanowire transistor with Al_2O_3 (0.5nm)+ HfO_2 (6.5nm) dielectric at the gate length $L_g=200\text{nm}$ [8].

NW diameter: 45 nm, NW length: 800 nm, Gate metal: W (Tungsten, sputtered 60 nm thick), Average dielectric permittivity: 15, Bottom separation layer material: Si_3N_4 (60 nm thick), Top separation layer material: Polymer (300 nm thick).

The relative permittivity of the bilayer is estimated to be 15, where there is good fitting of the result between the modeling and experimental data [8].

The design of this bilayer oxide makes it possible that the trapping sites close to interface in HfO_2 are reduced by a layer of Al_2O_3 , where seat less border traps. Therefore, this Al_2O_3 should be closer to the interface with the nanowires.

3 CIRCUIT DESIGN

The concept of the circuit is that we apply a small AC signal $\Delta V_g(f)$ to the gate pad of the transistor together with DC gate bias to see the indulging influence to the AC current $\Delta I_{ds}(f)$; by measuring the amplified $\Delta I_{ds}(f)$ flow out of the source, with the lock-in amplifier we can then obtain the g_m from the ratio:

$$G_m = \frac{\Delta I_{ds}(f)}{\Delta V_g(f)} \quad (3)$$

which is a function of the frequency. In order to sweep the frequency in range of mHz to GHz, we need a combination of tools of the lock-in amplifier for low frequency (mHz \sim 100 kHz) and VNA for high frequency measurement (from 20 kHz upwards).

3.1 Low frequency measurement (mHz \sim 100 kHz)

The current we are going to measure is very low: the AC current $\Delta I_{ds}(f)$ is around several micro amps, so a lock-in amplifier was used in order to read the current from the signal with high noise ratio. Below is the circuit design for the low frequency measurement.

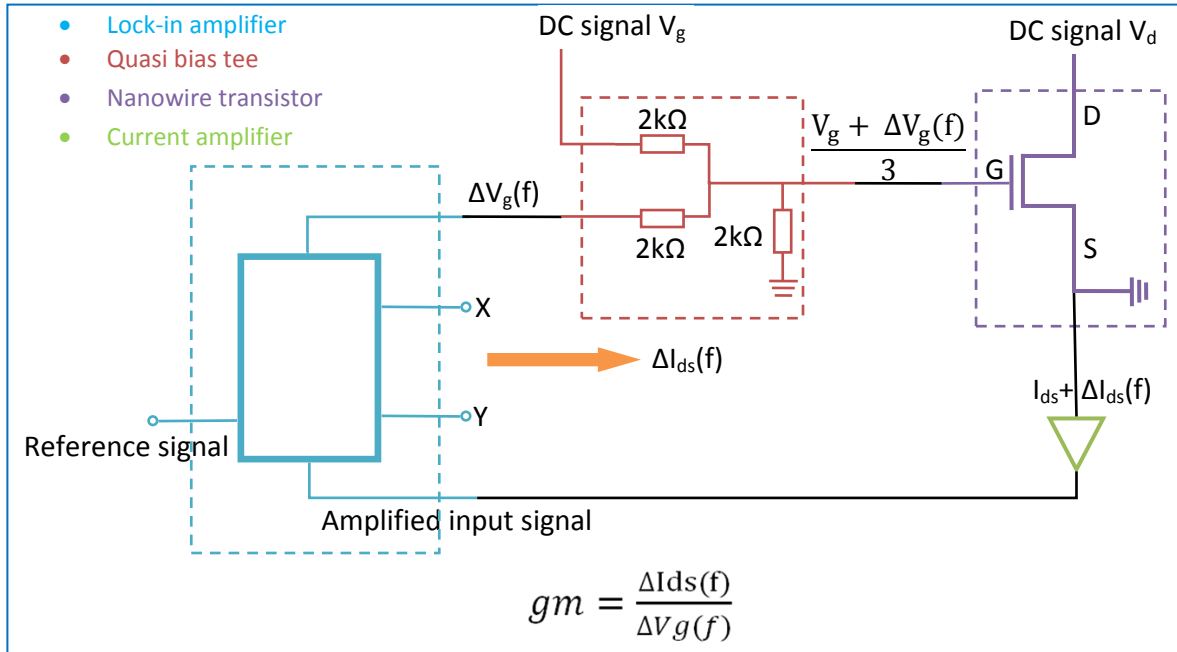


Figure 5 A schematic of the circuit design for the AC current measurement $\Delta I_{ds}(f)$ at low frequency between mHz to 100 kHz.

In figure 5, there are 4 major modules: (1) the lock-in amplifier, which serves as the AC voltage signal ΔV_g output as well as the tool to measure the amplified current ΔI_{ds} ; (2) the quasi-bias tee, consisting of 3 resistors with 2 kΩ each, combines the $\Delta V_g(f)$ and the DC voltage V_g into ΔV_g

(f)+ V_g ; (3) the InAs nanowire transistor is the sample; (4) the current amplifier, through which the current signal of ΔI_{ds} can be converted into readable voltage signal for lock-in amplifier.

3.2 High frequency measurement (20 kHz ~ 1 GHz)

Due to limitations of the instrument, the lock-in amplifier can only measure up to 100 kHz, however the increase of the curve does not stop at this frequency. Besides, for signal from 20 kHz above, we cannot test the sample with the applied voltages and then measure the corresponding currents flowing out of it as we did in the low frequency section.

Instead a VNA was used for this small signal, high frequency AC current measurement. The reason is that it is extremely hard to detect the absolute voltages and currents under such high frequencies. Therefore, we used RF signals, in which the reflection (b_1 in the figure 6 below) and transmission (b_2) of the incident waves (a_1 and a_2) were measured.

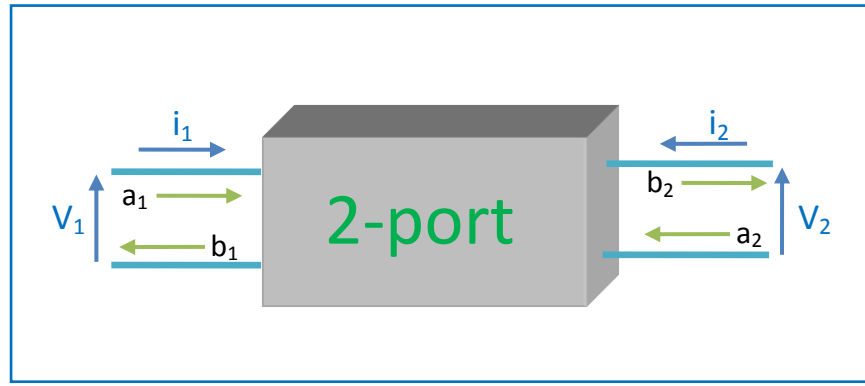


Figure 6 A schematic of waves of transmission b_2 and reflection b_1 with the incident signal a_1 to the 2-port object, similarly for a_2 , from which the g_m can be obtained from equation (6) below.

As shown in the figure 6, the signals a_1 and a_2 generated from the VNA with a certain frequency, phase and amplitude are applied on the 2-port object; the reflection and transmission signals b_1 and b_2 would be measured at the same time by VNA itself.

There is a matrix relationship relating the input (a_1 and a_2) and output (b_1 and b_2) signals, written as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (4)$$

where S-parameters (S_{11} , S_{12} , S_{21} and S_{22}) can be obtained by the equation below:

$$\begin{aligned} S_{11} &= \left. \frac{b_1}{a_1} \right|_{a_2=0} & S_{12} &= \left. \frac{b_1}{a_2} \right|_{a_1=0} \\ S_{21} &= \left. \frac{b_2}{a_1} \right|_{a_2=0} & S_{22} &= \left. \frac{b_2}{a_2} \right|_{a_1=0} \end{aligned} \quad (5)$$

Since the S-parameters contains complete information of both phase and magnitude for the signal at each frequency, the conversion of S-parameter to Y-parameter gives the tranconductance G_m by the relations (6) ~ (8) ^[9]:

$$g_m \approx y_{21} = \left. \frac{i_2}{v_1} \right|_{v_1=0} \quad (6)$$

where y_{21} can be expressed in equation (7) as below:

$$y_{21} = \frac{1}{R_0} \cdot \frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12} \cdot S_{21}} \quad (7)$$

where the resistance R_0 is with standard value of 50 ohm. That the approximation (6) is valid is provided that in equation (8) below, where the last term (parasitic campacitance) on the right side are very insignificant to be considered

$$y_{21} = \left. \frac{i_2}{v_1} \right|_{v_1=0} = g_m - \omega^2 C_{gd} R_g (C_{gs} + C_{gd}) \quad (8)$$

Therefore, the extraction of the transconductance is valid unless the frequency goes up very high, where effects from frequency dependent term can be omitted.

4 EQUIPMENT

4.1 Current amplifier

We used the MODEL SR 570 Low Noise Current Preamplifier in the Radio laboratory. Before the current from the source is put into the lock-in for analysis, it must be converted to the voltage information first so that the lock-in amplifier is able to read that out. The mode for the measurement we used is the high bandwidth mode, the amplifier fail to work properly above the frequency of 1 MHz though. This problem is that all measurements turn out to be 0 above 1 MHz, and then the high frequency measurements follow up from 20 kHz.

4.2 Lock-in amplifier

We used the MODEL SR 830 DSP Lock-in Amplifier in the Radio laboratory.

4.3 Quasi-bias tee

It is a self-designed joint circuit where each of the triple 2 k Ω resistors is connected to the DC signal, AC signal and ground respectively, so that the AC signal $\Delta V_g(f)$ and DC signal of V_g can be combined, as can be seen in the red dash rectangular in figure 5 and figure 7 (c).

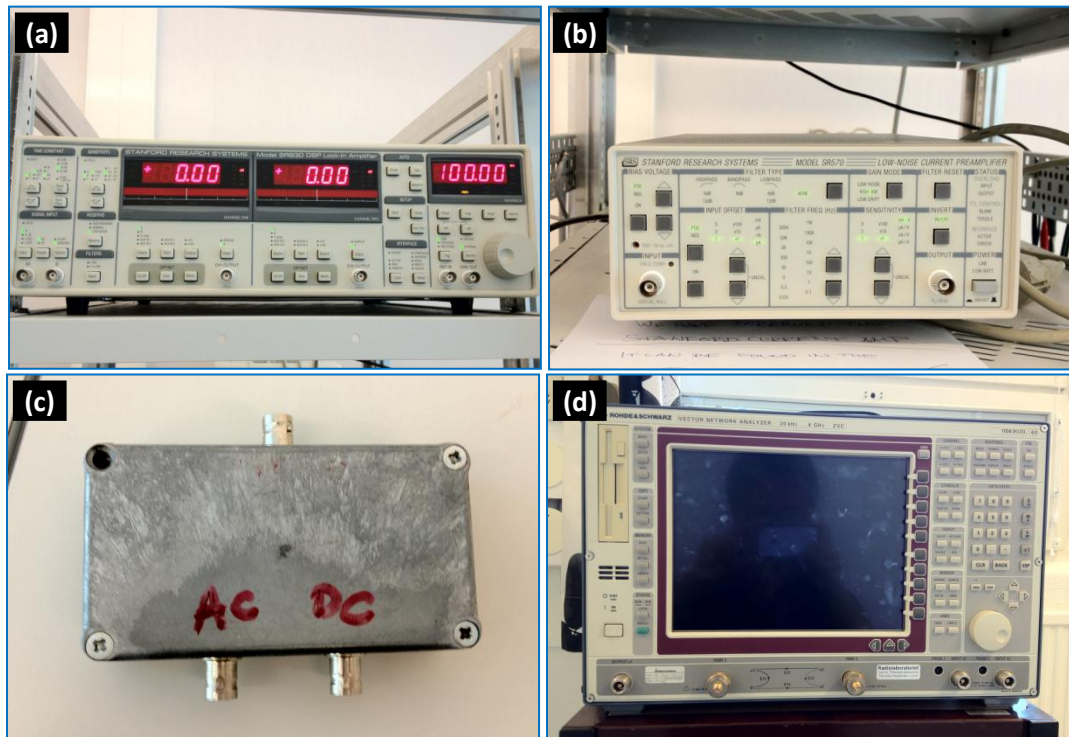


Figure 7 The major tools we used for the low and high frequency measurements: (a) lock in amplifier (b) current amplifier (c) quasi bias tee and (d) VNA.

4.4 VNA

We used the VNA in the Radio laboratory with the model of **VNA: ROHDE & SCHWARZ Vector NETWORK Analyzer 20 kHz till 8 GHz ZVC**. The tricky part about the measurement was that there were some of the cables broken, and the measurement result is put out with linear frequency scale, instead of the logarithm scale due to the inefficiency of the software, which was corrected manually later on.

Another trick with the VNA is the probing method incorporates extra parallel source contact resistances into the circuit. Those extra resistances will decrease the total resistance, leading to an increase in the transconductance measurement and finally contribute to a discontinuity between curves for low and high frequency, see figure 9 (a).

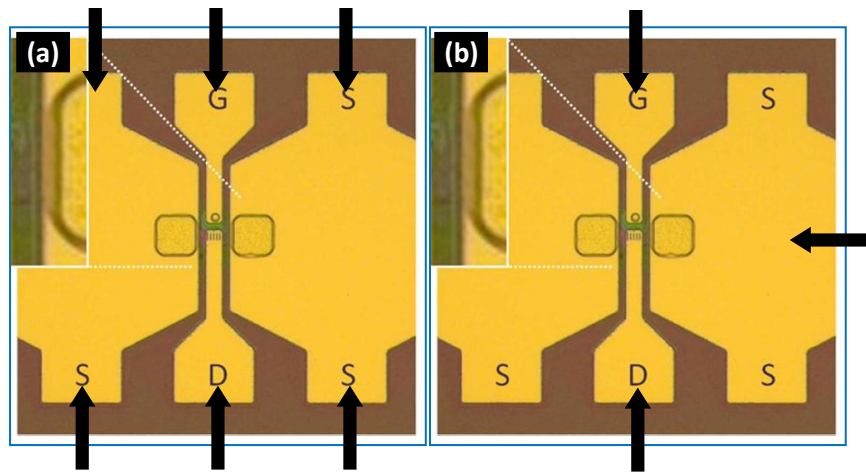


Figure 8 The contact methods for (a) VNA measurement at high frequency; (b) probe station measurement for low frequency. The black arrows represent the probe needles on the pads. The contact resistances from the semiconductor for both source and drain pad are estimated as $5 \sim 7.5 \Omega$.

5 EXPERIMENTAL RESULTS

5.1 Disconnection and Normalization

5.1.1 Disconnection

With the lock-in amplifier for the low frequency measurement, the frequency can go as high as to 100 kHz and the transconductance can be plotted as a function of frequency from the measured current. With VNA, the measurement goes from 20 kHz to 1 GHz, the S-parameters are measured and converted to transconductance by equation (6) and (7), and therefore the result is plotted as below in figure (7) for device of S06A-E2.

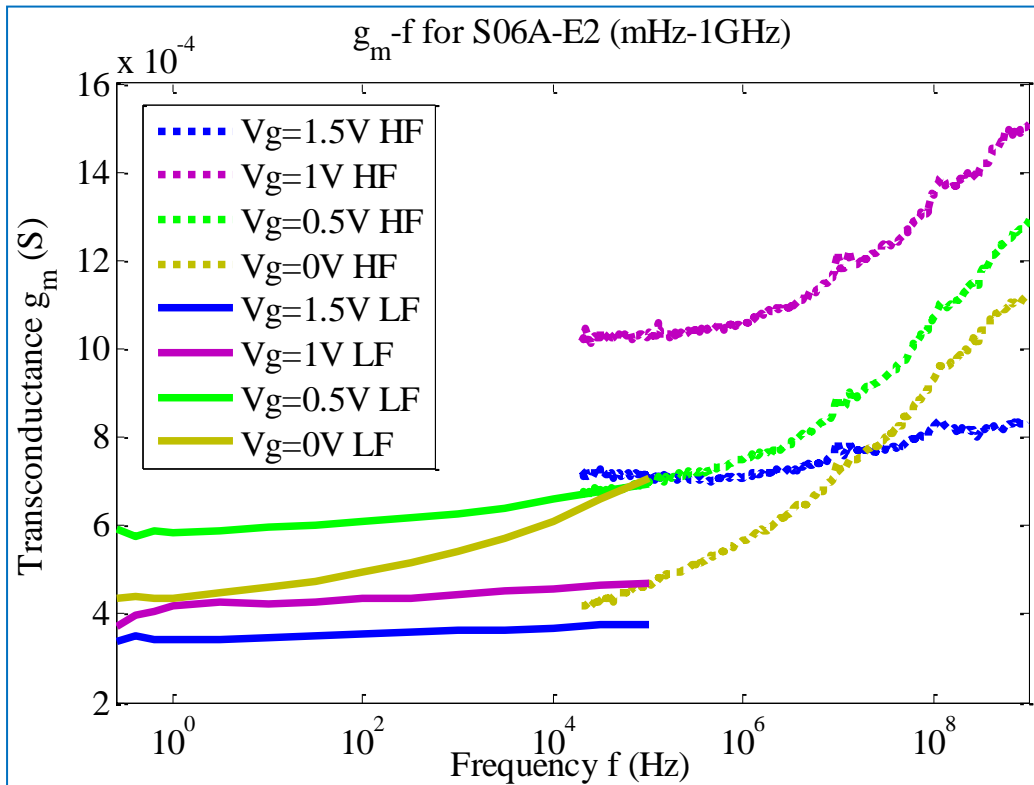


Figure 9 The transconductance is plotted as a function of frequency for InAs nanowire transistor S06A-E2 at different DC gate biases with fixed AC gate bias of 20 mV, where the solid curve indicates the low frequency measurements and dashed lines for high frequency. The drain current is fixed at $V_d=1V$.

There is a disconnection of the curves for low and high frequency measurements, due to two possible reasons: (1) because of the current drift in the nanowire transistor, which was observed in the measurement showed below in figure 10, where there are different transconductances obtained for the same sample measured with exactly same conditions; (2) since the contact methods of the probe needles are different for lock-in and VNA measurements (see figure 8), where the contact resistance will be reduced for the VNA measurement as there are parallel resistance incorporated.

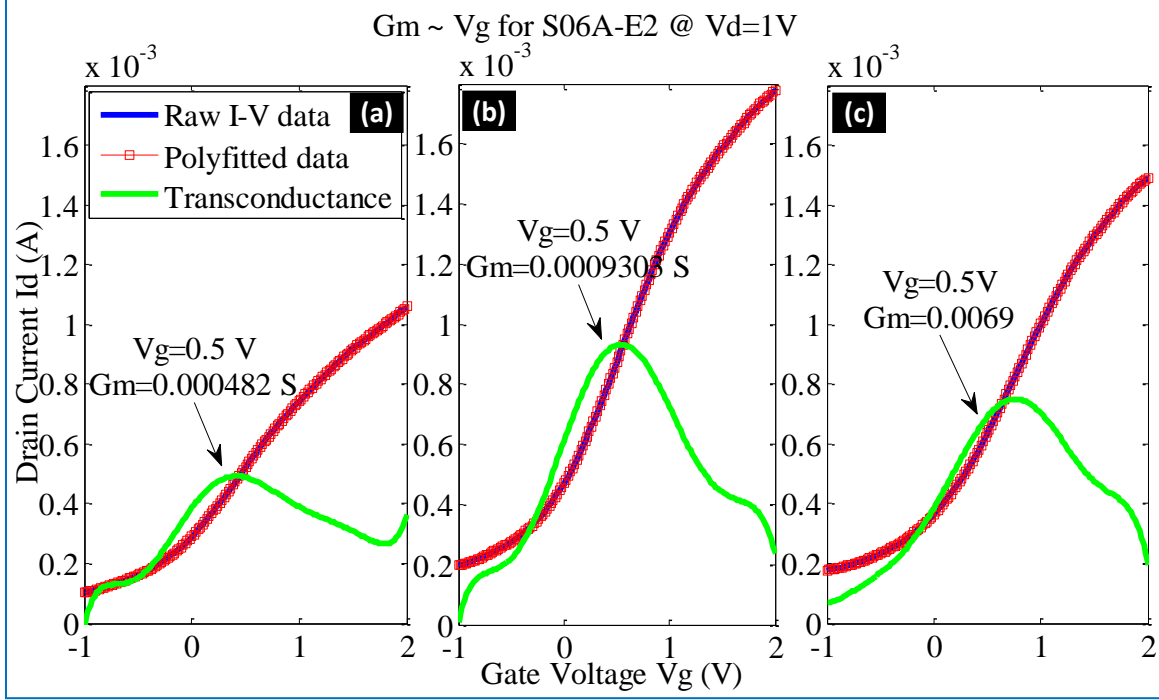


Figure 10 Above shows the I_{ds} as a function of V_g at $V_d=1V$ together with extracted transconductance for S06A-E2 sample. (a), (b) and (c) shows the same sample with same measurement conditions but turned out with different results due to current drifts.

Besides, the transition between the low and high frequency measurements should be smooth and we are more interested in the margin of the transconductance for low and high, the curves were normalized to be well connected afterwards.

5.1.2 Normalization

In order to make the measured curves of figure 9 to be as well connected and smooth as expected in figure 2 (b), normalization of those curves should be conducted. In convenience, the high frequency measurements will be normalized based on the low frequency measurements. Here by normalization it means that the high measurement results will be altered by a factor, which is ratio of transconductances from the high and low frequency measurements at $f=20$ kHz.

The same normalization methodology will be applied for both S06A-E2 and KMP-1B-B1 samples, as the disconnection happens for KMP-1B-B1 sample.

5.2 S06A-E2

As can be seen in figure 11, the transconductance starts to have a significant increase above frequency of 10 kHz after a slow increase. The measurements stops at 1GHz and may not be continued further up, since the transconductance deduction is under the assumption of approximated equation (8) that the terms on the right side are too small to consider.

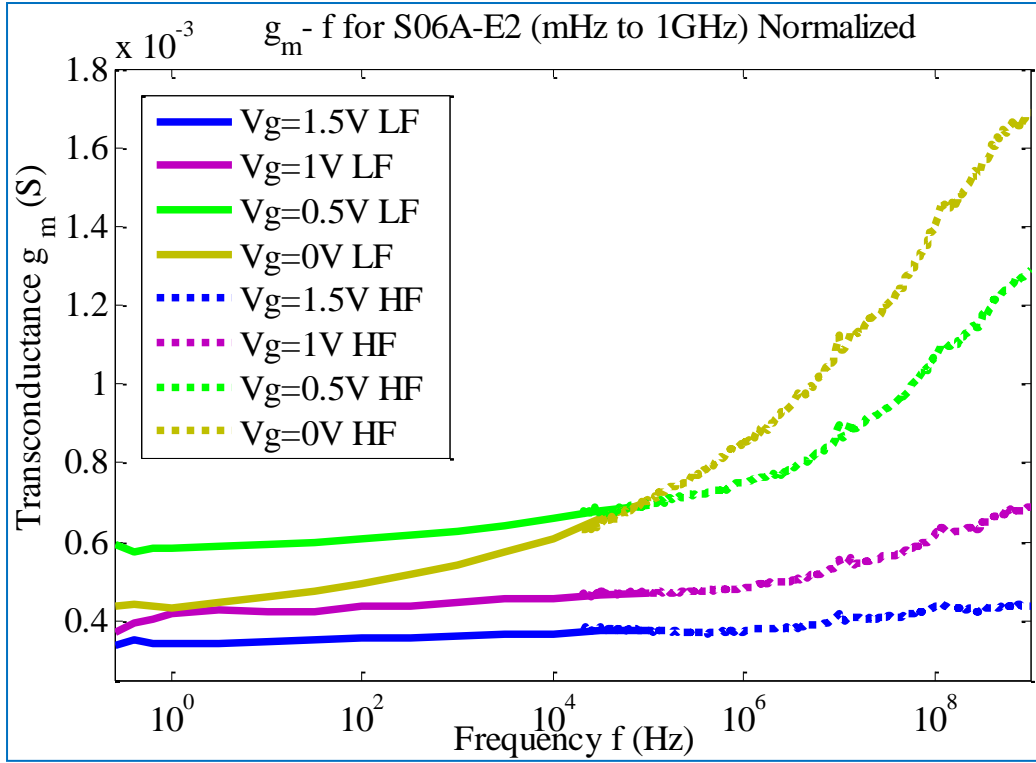


Figure 11 The transconductance as a function of frequencies for different gate voltages and fixed drain voltage of 1V, the curves are normalized according to the low frequency curves. The solid lines indicate the low frequency measurement and dashed lines for high frequency.

There is an increase slope as we expected in transconductance, but the traps in this device have a very strong ability and actually trap signal up to 67 GHz can be still leaked out. Table 1 shows the measured transconductances at starting and ending frequencies for different gate voltages.

Table 1 A displace of the measured transconductances at starting and ending frequencies for different gate voltages.

V_g (V) \ G_m (10^{-3} S)	$f=0.2512$ Hz	$f=1$ GHz	Increase (%)
0	0.4369	1.69	286.8
0.5	0.5934	1.286	116.7
1	0.3708	0.6889	85.8
1.5	0.3366	0.4375	30

The transconductance margin along the frequency varies very much from 287 % to 20 % with gate voltages, the reason is that gate biases drag down the band structure of semiconductor very differently, leading to the different trapping-site positions to be measured as can be seen below.

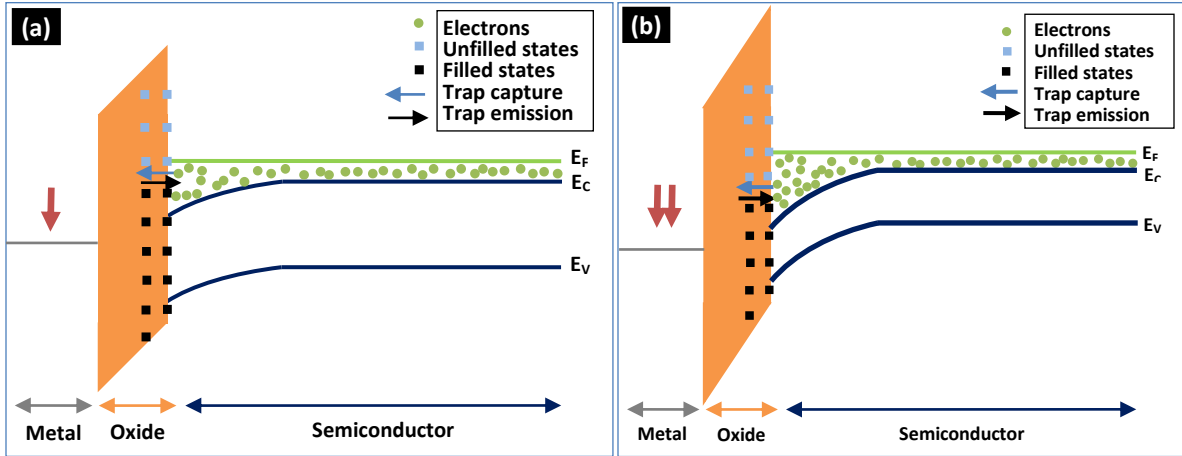


Figure 12 Band structure of the MOS transistor with different gate biases. (a) with less positive bias (see the red arrow); (b) with more positive bias.

The more positive bias it is, the more band structure can be stretched down, and thus the defecting sites in the oxide will be different with different gate biases.

5.3 KMP-1B-B1

KMP-1B-B1 sample was measured in a similar way and the high frequency was also normalized with the low frequency curves. Figure 13 and table 2 shows the relation of transconductance with frequency.

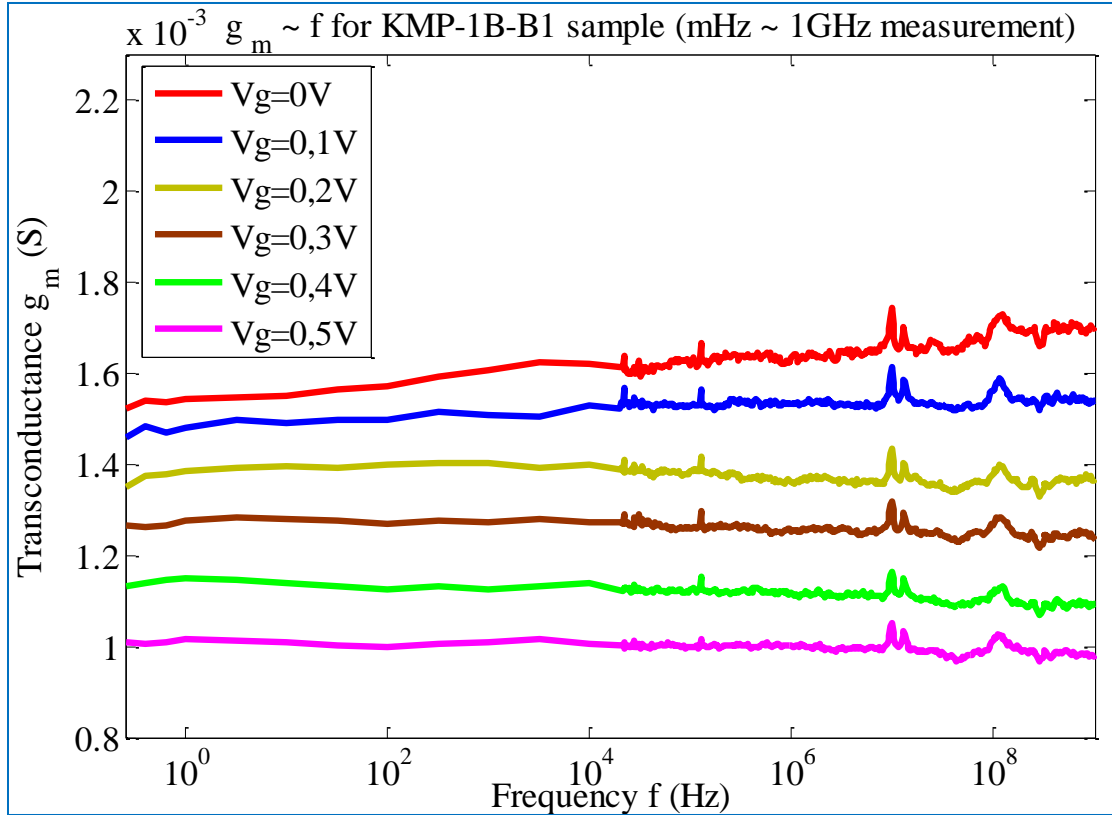


Figure 13 The transconductance is plotted as a function of frequency for InAs nanowire transistor KMP-1B-B1 at different DC gate biases with fixed $\Delta V_g = 20$ mV, where the solid curve indicates the low frequency measurements and dashed lines for high frequency, the low frequency curves are normalized. The drain water is fixed at $V_d=0.5$ V.

Table 2 A displace of the measured transconductances at starting and stopping frequencies for different gate voltages.

V_g (V) \ G_m (10^{-3} S)	$f=0.2512$ Hz	$f=1$ GHz	Increase (%)
0	0.00154	0.001692	9.9
0.1	0.001482	0.001547	4.4
0.2	0.001373	0.00137	0
0.3	0.001263	0.00125	0
0.4	0.00114	0.001095	- 4.1
0.5	0.001008	0.0009841	- 2.4

The results for this sample from the figure and the table are very different from the S06A-E2 in the following ways:

- (1) there is a much smaller increase of the transconductance with the frequency;
- (2) the curves for $V_g = 0$ V and $V_g = 0.1$ V, there a slight increase;
- (3) the curves for $V_g = 0.2$ V and $V_g = 0.3$ V, they are quite flat;
- (4) there are slight decreases for the rest curves at higher frequencies.

The phenomenon in table 2, where there is negative increase of the transconductance over the frequency, is a good example of how the high frequency can affect the validation of equation (6) and (7).

In the meantime, we find that there are less border traps in the KMP-1B-B1 as the slope of the g_m - f is much more flat. Therefore, we can already conclude that the bilayer structure plus the ALD temperature of 100 °C can substantially reduce the border traps in the HfO_2 .

6 ANALYSIS

In order to calculate the border trap density N_{bt} from the transconductance, the last step is to relate N_{bt} with the ΔG_m we measured before. The relation we will use is equation (9),

$$N_{bt} = \frac{C_{ox} \cdot \alpha}{(1 - \frac{x_m}{t_{ox}}) \cdot g_m^2(\omega) \cdot q \cdot \lambda} \cdot \frac{\partial g_m}{\partial \ln(\omega)} \quad (9)$$

where the oxide capacitance $C_{ox} = \frac{\epsilon_r \cdot \epsilon_0}{t_{ox}}$,

$$\alpha = \frac{C_s + C_{ox}}{C_{ox}} \cdot g_m(\infty) \approx 2 \cdot g_m(\infty)$$

$$\text{probing depth } x_m = \lambda \cdot \ln \frac{\omega_0}{\omega}$$

T_{ox} is oxide thicknes, $g_m(\infty)$ is transconductance at infinitely high frequency, q is the elemental charge and λ is attenuation factor for the oxide traps.

6.1 S06A-E2

After inserting the parameters for S06A-E2 and relation of $g_m(f)$ into equation (9), it comes to the border trap density result as a function of the probing depth x_m .

Values Parameter	λ (Å)	HfO ₂ ϵ_r
S06A-E2	2.84	25

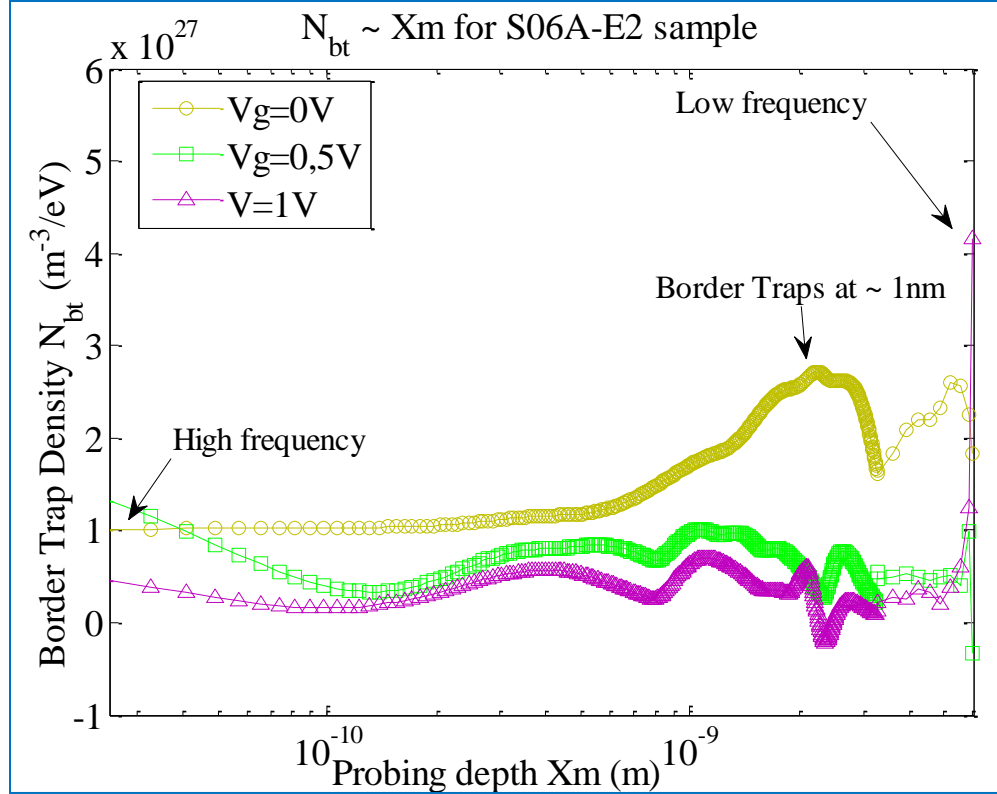


Figure 14 Border trap density calculated as a function of the probing depth X_m (f) at different gate biases for S06A-E2.

In figure (14), the yellow bump for $V_g = 0$ V means that there are large number at order of $\sim 10^{27}$ m^{-3}/eV of border traps at around 1 ~ 2 nms from the interface. However, for the rest of the two curves at gate voltages of 0.5V and 1V, there is too much noise from the measurements as well as the fact that the slope of the transconductance (f) is not very deep.

In order to make the comparison between the 2 samples in terms of the high frequency performance, the sample of KMP-1B-B1 is analyzed as the following.

6.2 KMP-1B-B1

For the bilayer oxide structure of Al_2O_3 and HfO_2 , we used the same attenuation factor λ for KMP-1B-B1 sample. However, the relative permittivity of the bilayer is estimated to be 15, where there is good fitting of the result between the modeling and experimental data [8].

Values Parameter	λ (Å)	HfO_2 ϵ_r
KMP-1B-B1	2.84	15

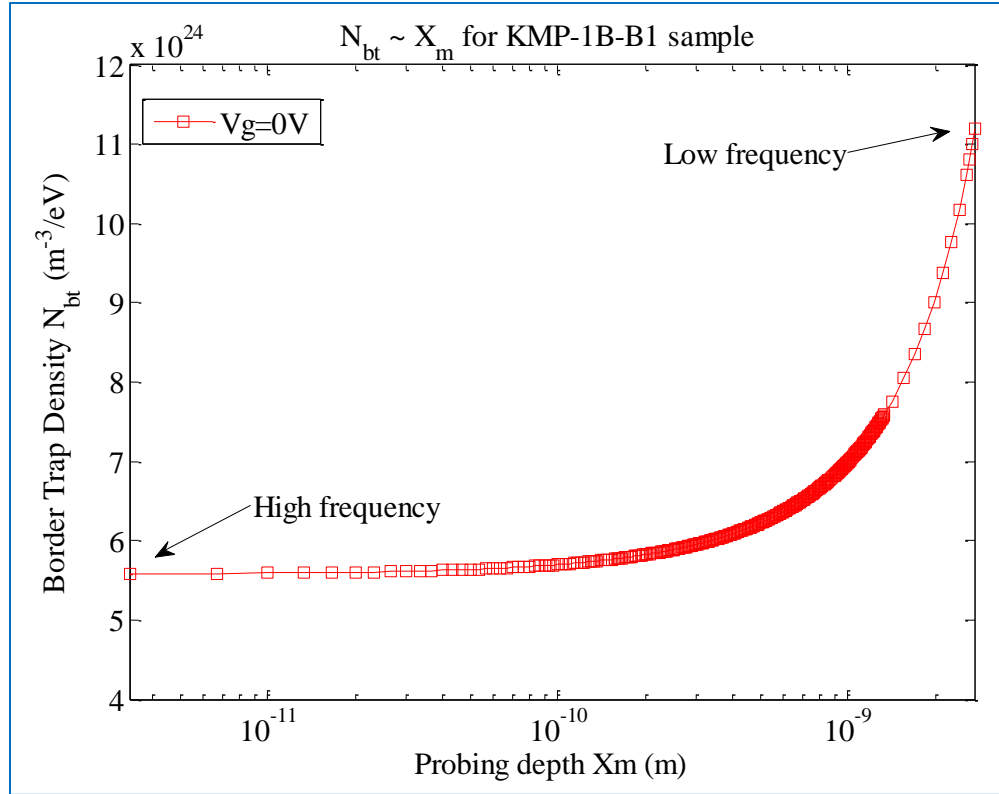


Figure 15 Border trap density calculated as a function of the probing depth X_m (f) at different gate biases for KMP-1B-B1.

In figure 15, the border trap density reaches its maximum level at the probing depth of 2.67 nm, which turns to be around $10^{25} \text{ m}^{-3}/\text{eV}$ and thus 2 orders less compared with S06A-E2 sample. This further approve that the bilayer structure has less border traps in the oxide interface.

The difference between figure 14 and 15 is that the measured probing depth X_m has a different scale (10^{-11} m to 10^{-8} m for S06A-E2 and 10^{-12} m to 10^{-9} m for KMP-1B-B1), it is due to the noise problem when processing the data for S06A-E2 sample.

7 CONCLUSION

In this thesis, we have successfully built up a new type of electrical circuit with lock-in amplifier to measure the transconductance at low frequency up to 100 kHz and VNA from 20 kHz upwards, from which we obtained the border trap density at the order of $\sim 10^{27} \text{ m}^{-3}/\text{eV}$ for HfO₂ gate wrapped InAs nanowire transistor S06A-E2 at 1 ~ 2 nm far from the interface.

In the meantime, we proved that bilayer structure of HfO₂ with internal layer of 0.5 nm of Al₂O₃ can effectively reduce the border trap density for an InAs nanowire.

Through transconductance to frequency method with lock in amplifier, the measurement can go down to mHz, meaning that the very slow traps are able to be detected compared with the capacitance method. However, the disadvantage about the circuit is that due to the noise measured in the VNA, which will affect the result when we need to calculate the derivative of the transconductance to frequency. This is very obvious when we analyzed the data for sample S06A-E2 at $V_g=0.5\text{V}$ and $V_g=1\text{V}$.

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