Master's Thesis

NWFET Ring Oscillator Simulations

By

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Abstract

In this work, a simulation model has been developed for a Nanowire Field-Effect Transistor (NWFET), which has been used in simulations of ring oscillators made up of a series of inverters, implemented in ratioed logic. The simulations have been benchmarked to FETs operating in the ballistic regime (BFET). The initial goal was to investigate how NWFETs manufactured at the Nanoelectronics Research group in Lund would behave in a digital environment. Comparing them to a BFET of the same dimension gives us an idea of how improvements to the device will benefit the digital circuit and what the ultimate limit may be. The simulations show that the original design of the ring oscillator does not work, and modifications to the design are proposed.

Acknowledgements

This project work would not have been finished without the help from the initiators of this project, Professor Lars-Erik Wernersson and Professor Peter Nilsson. I would like to thank Karl-Magnus Persson and of course my supervisor Anil Dey for help and guidance during my work. I would also like to thank my friend Samuel Bengtsson for encouragement and a more personal thanks go to my girlfriend Tove Bäckström for support and patience.

Svante Wikander

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CHAPTER 1

1. Introduction

1.1 Report outline

This report starts with a brief description of the research area and why this thesis is of importance. A description of the fundamentals needed to understand the principal points of this thesis will then be presented; mainly covering transistor parameters and digital design implementations. Further on, you will find descriptions of the two main areas of the thesis; electrical models of the transistors and the simulations performed with the model. Lastly, the results will be presented and will be followed by a discussion, together with brief thoughts on the future of the field of research.

1.2 Project background

This project was initiated by the author and the Nanoelectronics research group at LTH, Lund, Sweden. The area of interest is the work with Nanowire Field-Effect Transistors (NWFET) and their potential in digital circuits. The main supervisor of this project has been Anil Dey, Ph.D. student at LTH.

The project planning involved setting up goals, both primary and secondary, and also making a schedule for the project as a whole, estimating the time needed for different parts of the work.

1.3 Goals

The primary goal of this project has been to simulate the implementation of Nanowire Field-Effect Transistors into a ring oscillator. This work supports the current and future work of implementing NWFETs into digital circuits

by working out issues regarding layout design as well as transistor performance at an early stage and a step on the way towards real production and testing.

Secondary goals during the project include:

- Development of transistor models that work in an electrical environment.
- Evaluate the layout design for the ring oscillator.

CHAPTER 2

2. Theory

In this part, the fundamentals of the field necessary for understanding the project will be discussed. For those working within the field, this section can be browsed lightly.

2.1 Nanowire Field-Effect Transistor

The Nanowire Field-Effect Transistor (NWFET) is built around a nanowire channel. The NWFET is one of the big research areas within the Nanoelectronics Research group in Lund. The benefits of the NWFET compared to other technologies lie mainly in the material choice and favorable electrostatics. Combinations of III-V materials are well suited to be used as channel material, and they have some very favorable electronic properties. Nanowires are well suited to accommodate different III-V materials because of the reduced strain, from lattice mismatch, compared to the bulk. The nanowire studied in this thesis is made of InAs, and the structure of a device providing the experimental data used in the modeling can be seen in Fig. 1.

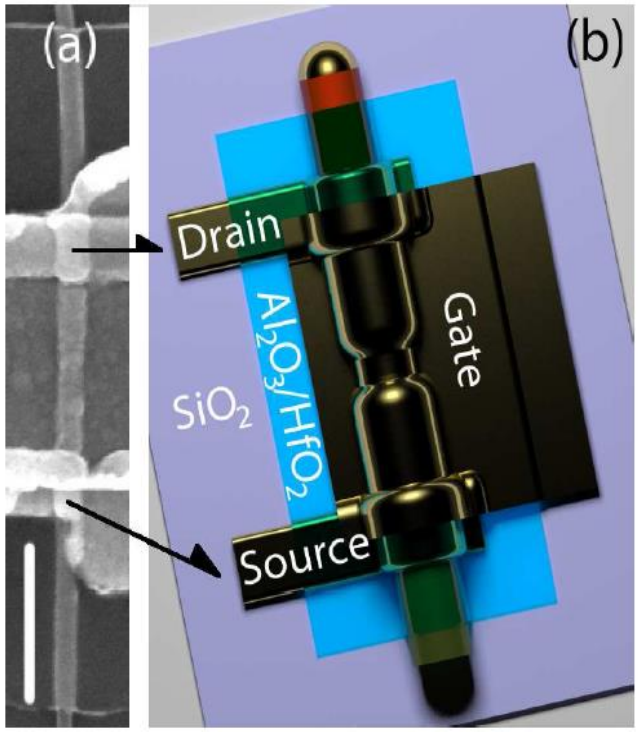

Figure 1. (a) Top view scanning electron microscope (SEM) image of the NWFET. The scalebar is 250 nm.

(b) Schematic image of the NWFET. [1]

2.2 Ballistic Field-Effect Transistor

This work is based on the comparison of the performance in a manufactured NWFET and an optimal case; this optimal case is considered in the Ballistic Field Effect Transistor (BFET). The BFET is a NWFET with ballistic transport in the channel.

2.3 Inverter

An inverter is one of the most basic logic building blocks in digital technology. It inverts a digital 0 to a digital 1 and vice versa. In regular complementary metal-oxide semiconductor (CMOS) technology the inverter is implemented by one NMOS used as pull-down network and one PMOS

as pull-up. The inverter schematic is shown in Fig. 2. The Voltage Transfer Characteristic (VTC) of a typical CMOS inverter is shown in Fig. 3.

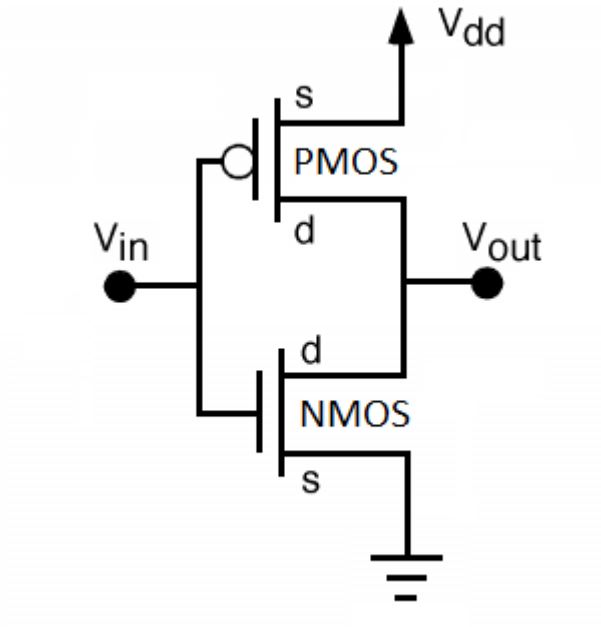

Figure 2. Schematic of a CMOS inverter.

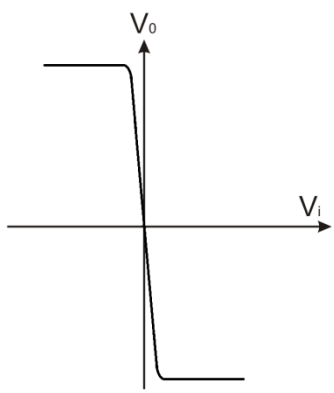

Figure 3. Voltage Transfer Characteristic of a CMOS inverter.

In this thesis, the inverter was implemented with ratioed logic, since the project did not cover any PMOS transistors. Here we use a NMOS as the pull-down transistor just like in a regular inverter, but the pull-up function differs from regular CMOS. Using ratioed logic, the pull-up network is implemented by an NMOS where the gate is connected to the supply voltage V_{DD} (hence it functions as a fixed resistance). Ratioed logic has the drawback of a reduced swing and the power consumption is affected in a negative way compared to a CMOS design, mainly due to increased static power dissipation. The schematic of a ratioed logic is shown in Fig. 4. The VTC of the ratioed logic is shown in Fig. 5.

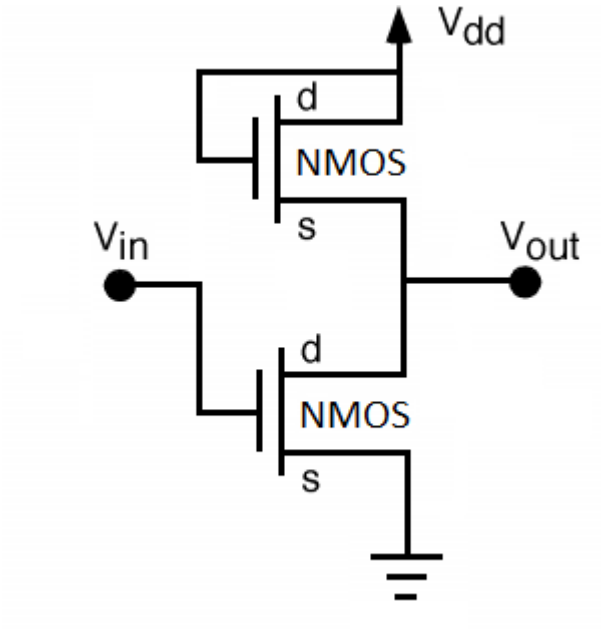

Figure 4. Schematic of a ratioed logic inverter.

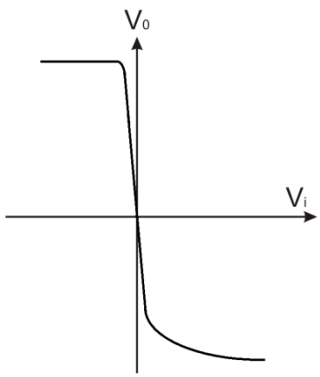

Figure 5. VTC of a ratioed logic inverter (with NMOS transistors)

2.4 Current mode logic

Another way of implementing digital circuitry is the use of Current Mode Logic (CML). Instead of measuring the voltage to get either a zero or a one, a differential current is used to distinguish between the two states in CML. The most simple digital function, the inverter, is built up by two NMOS transistors with the two input signals connected to the gates. The drain contacts are connected to the supply voltage through one resistance each, and the source is connected to a biasing network providing a bias current through both transistors. The output signals are generated between the drain and the resistance on either transistor. When a signal is applied to one of the gates, the high input increases the current through that transistor, thus decreasing the voltage on that output node. The opposite happens on the other side of the inverter. The output signal is now reversed. This can be seen in Fig. 6.

The CML has the general advantage of higher switching speed, with the cost of increased energy consumption. Looking at the VTC of the CML in Fig. 7 the features such as low swing (suitable for high speed), constant current drawn from power source and static power dissipation can be realized.

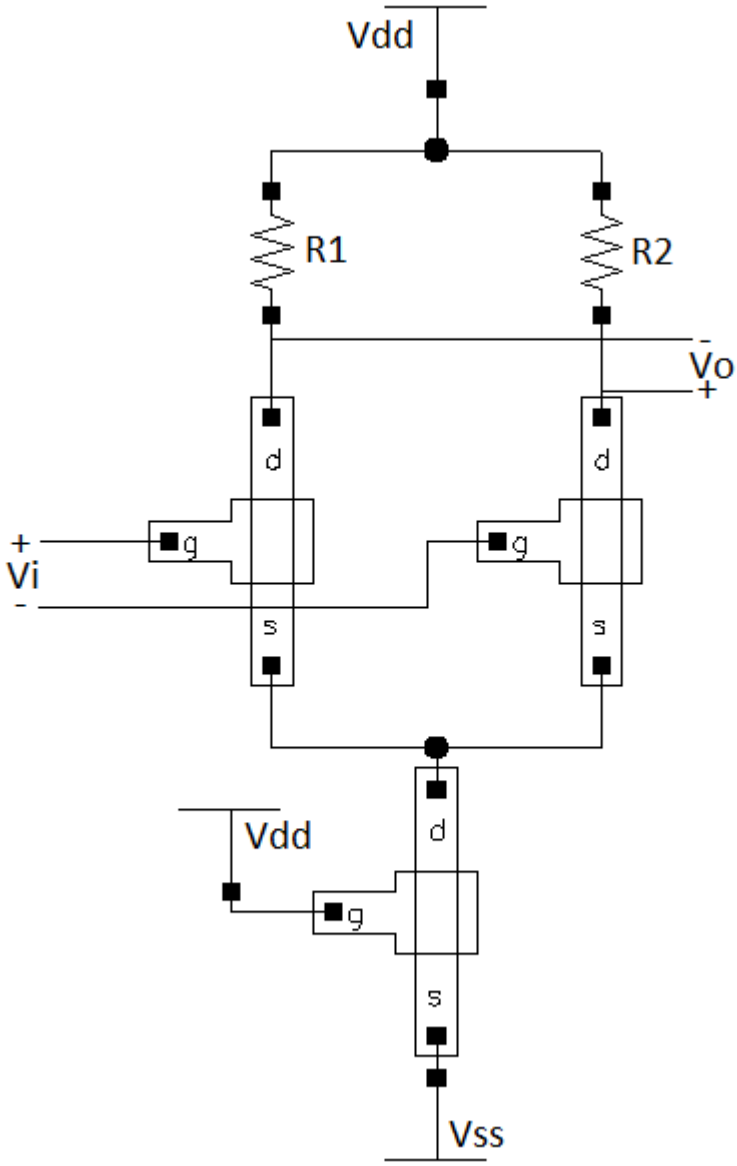

Figure 6. Schematic of the CML inverter, where the bottom transistor operates as a current source. The input V_I and the reversed output signal V_O is marked in the figure.

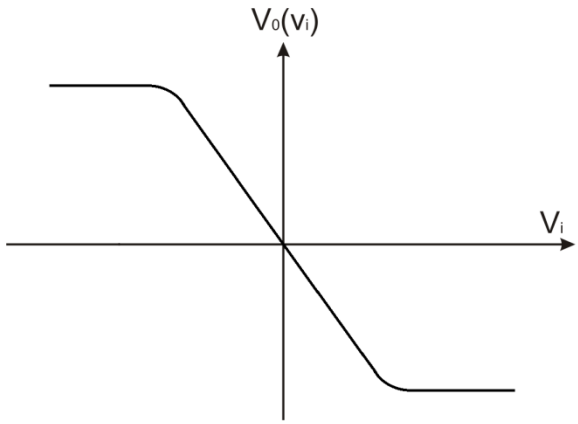

Figure 7. The VTC of the CML inverter.

2.5 Ring oscillator

A ring oscillator is made up of an odd number of inverters connected in series; the output of the last stage is connected to the input of the first stage. The natural delay of the inverter will force the circuit to oscillate. The oscillation frequency is dependent on the technology that has been used in making the inverter transistors.

All this makes ring oscillators ideal for comparing different transistor technologies. They are used in modern technology as standardized benchmarking tools to evaluate the performance of emerging technologies.

CHAPTER 3

3. Models

This chapter will explain the work put into developing the models of the NWFET and the BFET. First, the transistor parameters and their relation to the model parameters are investigated as well as their influence on electrical simulations. Subsequently, the model structure and the development of the model will be discussed.

The models needs to fulfill several different requirements;

- Smoothness: Edges and cracks in the curves will lead to poor simulation performance in Cadence.
- Accuracy: Having the models to follow the experimental data points is essential to the whole project.
- Comparability: Having the models for the BFET and NWFET with similar structure ensures that a comparison between the two can be made.

These important factors also facilitate the model development, since the adaptation of the models does not have to have a physical relation but can be done to suit the need for hand calculations. The optimal model would have all parameters comparable to the physical parameters, in this project the focus has instead been on full model behavior and its simulation properties.

3.1 NWFET and BFET

The models are based on initial data obtained by measurements on a 15-nm-diameter NWFET with a gate length of 100 nm[1] and for the BFET, the data points are taken from ballistic simulations of the channel. The

experimental data of a NWFET is taken from a device in a horizontal geometry. The model is planned to demonstrate nanowire circuitry in a vertical geometry, although this is mostly demonstrated when looking closer at the layout design (see chapter 4.1). An NWFET based circuitry will be implemented in a vertical design due to the favorable electrostatics; however, electrical data from the lateral version of the NWFET are still used as the base for the model. The main difference being a reduced gate perimeter of the lateral device compared to a vertical geometry where the gate would be a gate-all-around.

3.2 Model structure

The models' mathematical structures are focused around the transconductance (g_m). The transconductance is the amount of current change in the transistor when we change the gate voltage at a fixed drain-source voltage. Here the aim is to have a good small-signal model describing the derivative of the currents, and hence an accurate large-signal model for the real current values. By investigating the g_m plots an initial model for describing the transconductance was introduced. This work was already provided by Karl-Magnus Persson (Ph.D. student) for the BFET when this project started and his model is the base of the final model, which was modified to fit the NWFET and BFET simulations. The model is based on the fact that g_m first increases with increasing V_g, it then reaches a plateau and is followed by a linear decrease with increasing gate voltage. The model introduces two functions f_1 and f_2 that changes the values of the plateau length and slope.

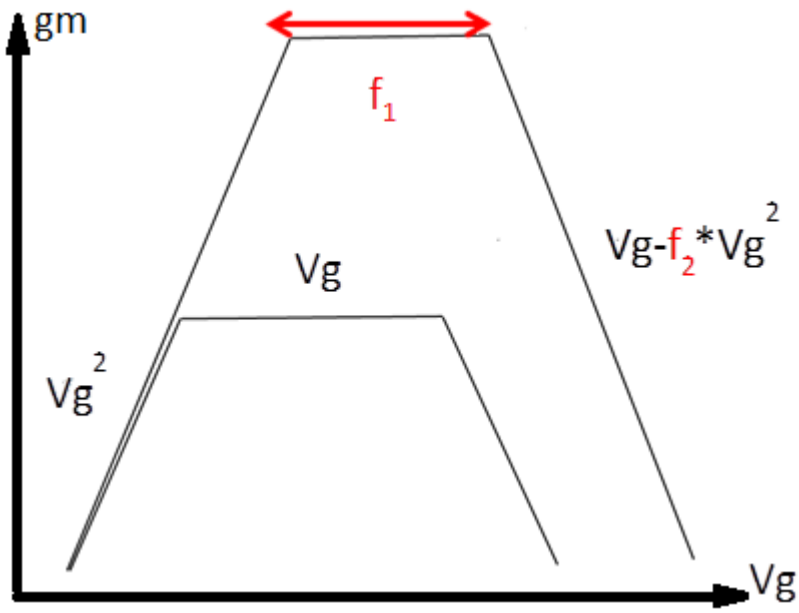

Figure 8. The modeled transconductance behavior when the two functions f_1 and f_2 are implemented [2].

The two functions are dependent on the drain voltage and built up by parameters that can be adjusted to fit the needs at hand.

$f_1 = A + B \cdot V_d$

$f_2 = C + D \cdot V_d$

Tuning the values A, B, C and D gives great flexibility for adjusting the model towards the NWFET/BFET data points.

3.2.1 Models after tuning

The following figure 9 and 10 show the results of the iterative process done in Matlab to modify the models towards the BFET and NWFET respectively. The red dashed lines indicate the initial data points and the green are calculated by the models. These results give us the final parameter values for the functions f_1 and f_2 as well as the values that match the current levels in a more general way.

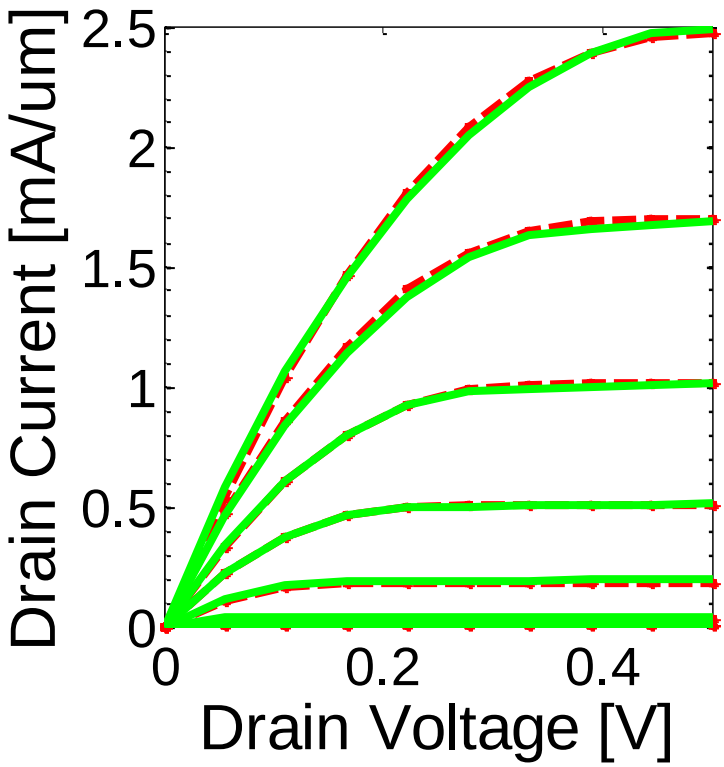

Figure 9. The data points (dashed red curves) and the calculated curves from the models (green) of the BFET.

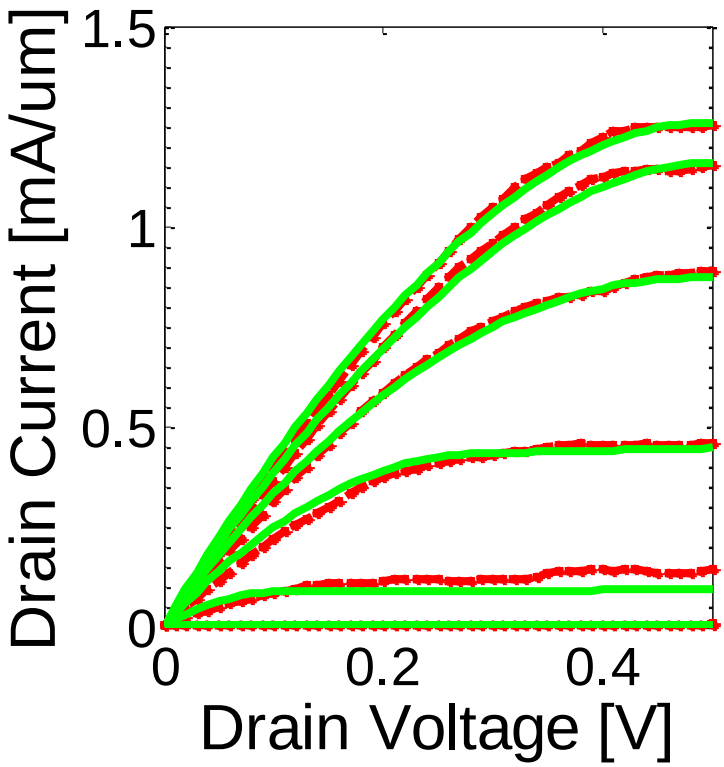

Figure 10. The data points (dashed red curves) and the calculated curves from the models (green) of the NWFET.

3.3 Model development in Matlab

While investigating the data points of the NWFET a minor issue was discovered regarding the amount of data points available. Hence, the transconductance plots do not give us the complete picture due to the limited number of gate voltages. The general idea of a peak in transconductance at a certain V_G does still apply.

The development of the model in Matlab started by evaluating the I_D-V_D curves for both the NWFET and the BFET to form a general understanding of the transistor behavior. At this stage, the BFET model was adapted by a few fitting parameters to describe the NWFET's output characteristics. This

type of development was suitable since having the two models to share a similar base-structure would make further development easier in several areas, including the transfer to Verilog-A and circuit simulations in general. Running more complex simulations with two fundamentally different models for the BFET and NWFET might give skewed results.

A Matlab code was developed and optimized to iterate through the different parameters that tuned the model towards the data points. With multiple parameters being tested simultaneously, the test code became quite substantial. Every tested parameter was evaluated in an interval with a fixed amount of points. After finding the best value for the interval, it was shifted and the procedure was repeated.

3.4 Transfer to Verilog-A

Once the different model parameters where found, and the shape of the model curves followed the initial data points, the model was transferred from Matlab code into Verilog-A code. Cadence is a powerful tool specialized at running electrical circuit simulation tests and Verilog-A code. The difference between Matlab code and Verilog-A code is minor, but as with all computer languages there are some minor differences.

CHAPTER 4

4. Simulations

Once the models where developed in Matlab and the code was successfully transferred to Verilog-A. Only one more addition was necessary before they could be used in Cadence for circuit simulations. Cadence required the addition of parasitic resistances and capacitances to run correctly. The main reason behind this being a consequence of how Cadence handles electrical signals. Without any capacitive effect, Cadence has trouble with different voltage levels on the nodes (wires) contacting the transistor and it will give an error that hinders all simulations.

4.1 Electrical parasitic implementation

The idea to implement parasitics into the model was planned at an early stage in the project, even before it was realized that they were crucial, but how they would be implemented was not exactly clear until the code was readily converted to Verilog-A. Previous work in the field of parasitics has been done within the department and the results were included for the NWFET and BFET in the Verilog-A models. The parasitic values implemented can be seen in table 1, and they can be related to Fig.11 of the NWFET. The parasitic effects are classified by their source; wire(w), internal(i), external(e), nanowire(N) and contact(C/c).

Parameter	16 nm node	Parameter	16 nm node
$C_{gg,i,N}$ (aF)	47.2	$g_{m,N}$(mS)	1.16
$C_{gs,e,C}$ (aF)	67.1	$g_{d,N}$ (mS)	0.116
$C_{gd,e,C}$ (aF)	25.5	$R_{S,w,N}$ (Ω)	171
$C_{ds,e,C}$ (aF)	41.5	$R_{D,w,N}$ (Ω)	171
$C_{gs,e,N}$ (aF)	3.15	$R_{S,c,N}$ (Ω)	231
$C_{gd,e,N}$ (aF)	2.47	$R_{D,c,N}$ (Ω)	231
$C_{ds,e,N}$ (aF)	0.976	$R_{S,e,C}$ (Ω)	2.49
$C_{gs,wi,N}$ (aF)	3.40	$R_{S,e,N}$ (Ω)	0.147
$C_{gd,wi,N}$ (aF)	3.08	$R_{D,e,N}$ (Ω)	22.3
		$R_{G,e,N}$ (Ω)	114

Table 1. Parasitic table for the 16 nm diameter NWFET/BFET, the values where integrated into the Verilog-A model [3].

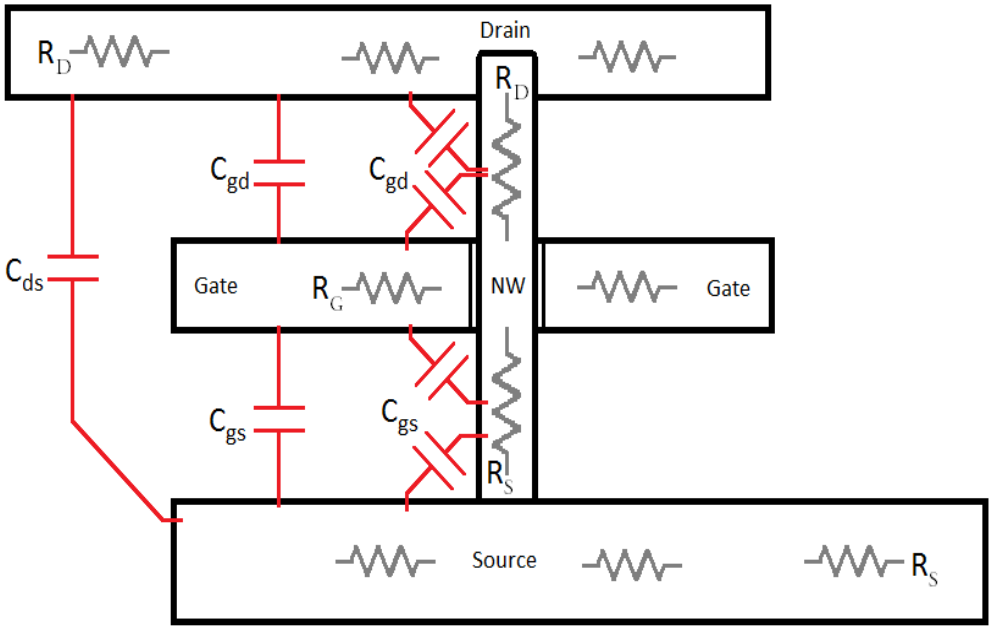

Figure 11. Side-view of the layout for the NWFET/BFET in a vertical geometry.

I will refer to these parasitic values as intrinsic parasitics since we will later also include wire parasitics (extrinsic parasitics) from the circuit layout.

4.2 First Circuit simulations

The first tests of the Verilog-A code were of a simple fashion, with the purpose to make sure the implementation as a whole was successful. The initial stage focused on two things; checking the I_d-V_g sweeps and comparing them to the Matlab model and investigating if the internal parasitics were working according to the plan. Checking the parasitic implementation was simple once oscillation was achieved. Increasing the parasitics by a factor of two led to a decrease in oscillation frequency by the same factor, hence indicating a correct implementation. The test circuit for the first sweeps is shown in Fig. 12.

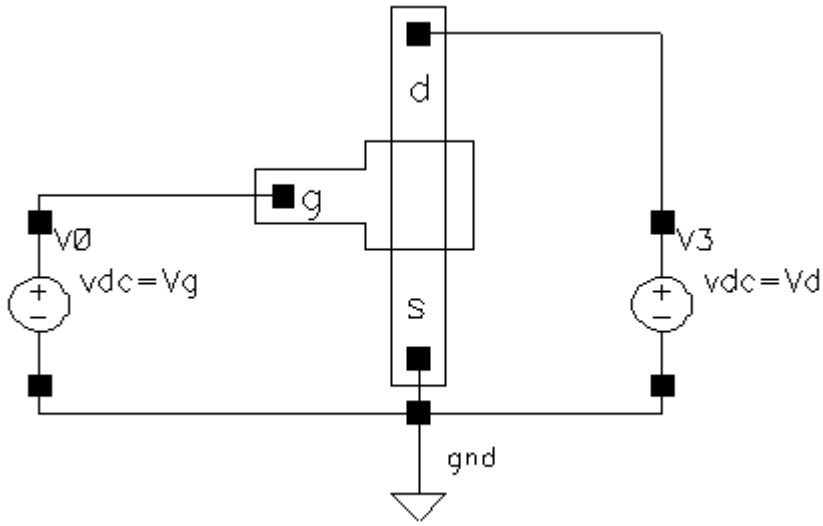

Figure 12. Layout of the first test circuit, able to do sweeps of the drain and gate voltages of the transistor.

With this setup we can sweep the drain voltage at different gate biases. At this stage the transistors behaved as expected and the Verilog-A code was returning the same current levels as the Matlab counterpart.

The project had reached an important milestone where the first major part; the goal to make a working model of the transistors capable of handling electrical signals was completed.

4.3 Ring oscillator

4.3.1 Biasing

The next step in preparation for the simulation of the ring oscillator was how to correctly bias the circuit. This work was done in close relation to the ring oscillator tests, and at times there was no difference between the two. Biasing was the key to get a working ring oscillator.

There have been many different setups during the circuit simulation part of the project where several different parameters have been modified.

Type of transistor

All tests have been done with both NWFET and BFET as the test device.

Number of wires

The model has the ability to handle multiple nanowires per transistor. This changes the current level and in general an increase in wires enables an easier operation of the oscillator due to higher drive currents. Normally, there is a difference in number of wires in the pull-up and the pull-down side of the inverter with more wires in the pull-down network.

Inverter types

Both ratioed logic (RL) inverters and current mode logic (CML) inverters have been evaluated.

All these differences have an effect on the ring oscillator performance as well as the needed biasing network to get oscillations in the first place.

4.3.2 Threshold voltage

When simulating the ring oscillator with all setups, apart from the CML ones, there was a major change made to the model, namely that the threshold voltage was shifted (350 mV for the NWFET and 150 mV for the BFET) to push the negative threshold voltage to a new positive value. This was performed to make sure the ratioed logic inverters would work properly. In real tests, similar tweaks can be done by instead tuning the bias network accordingly.

4.4 Wire parasitics

The following figure shows the initial layout of the five stage ring oscillator with ratioed logic inverters. Here we observe the top view of the layout, where the output of the fifth stage is connected to the input of the first. The connection bypasses all five stages and this overlap causes a parasitic capacitance. Another thing to note is the addition of a sixth stage intended as a buffer stage. This should not have any effect on the signal and thus it is not covered in any of the simulations.

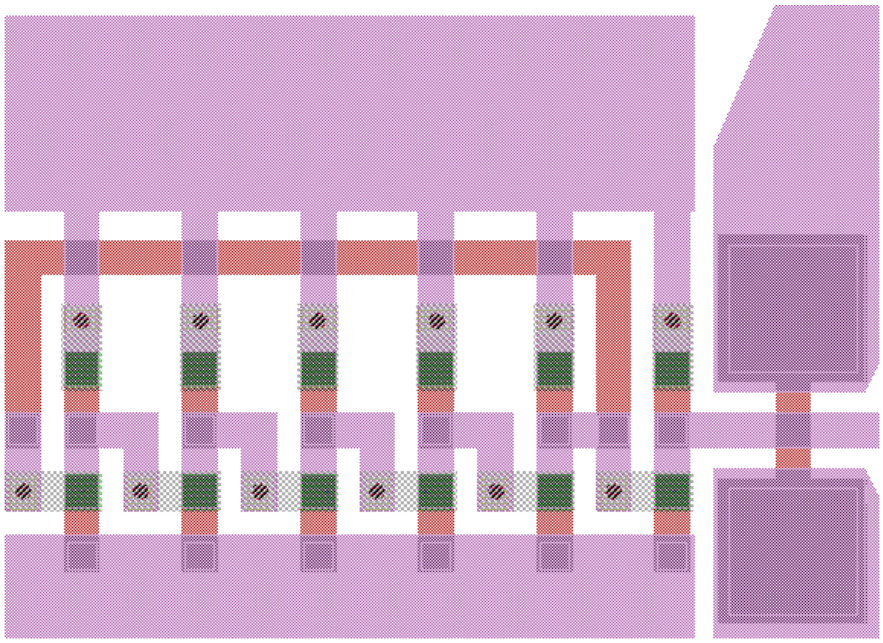

Figure 13. A Layout, developed by A. Dey, of the 5-stage NWFET ring oscillator.

The investigation of the external nanowire parasitic started by evaluating the parasitic values obtained in this layout, where both resistive and capacitive parasitic were considered for testing. However, in the end, only the capacitive effect was evaluated since it made a much more significant impact. The main capacitive contribution is the overlap of the wire from the output of the last stage when it passes the supply rails of the other five stages. The value of the capacitances was calculated in COMSOL Multiphysics in two dimensions and the result is very close to that of a simple parallel plate capacitor. For the initial design the value in COMSOL was calculated to C = 12.14 nC/m, compared to 12.09 nC/m for the same parallel plate capacitor, this indicates that the fringe field contribution is relatively small. The fact that the COMSOL calculated value is so close to the more simple parallel plate capacitor calculation is useful when interpreting the results for the wire parasitic simulations, as discussed later on.

4.5 CML ring oscillator

Further simulations were performed on 5-stage ring oscillators made up of CML inverters, which have the benefit of greater speed but with a drawback of a higher energy consumption. The benefit of the CML ring oscillator from a simulations point of view is the fact that the CML ring oscillator can operate correctly even with a negative threshold voltage. This was important in order to produce an as realistic result as possible. The simulations were just as the previous ones performed on both the NWFET and the BFET to get the important comparison between the two cases.

CHAPTER 5

5. Results

5.1 Result interpretation

Two main parameters were evaluated during the tests of the ring oscillators, namely the wavelength, corresponding to an oscillation frequency, and also the signal swing. The results are presented in the following graphs:

Figure 14 displays the transient signal analysis that was performed in Cadence. In the figure, the output signals from all five stages can be seen, and it can be observed that the oscillation is stable. From this type of graph, information was gathered about the signal swing and the wavelength. All stages have equal performance and the arrows in this case indicate the output of the second stage. The swing is the difference in voltage levels between the peak and the low point according to the vertical arrow indicated in the figure. The wavelength is shown by the horizontal arrow.

This is a great example of the type of simulated results that have been handled during the project. This example is of a NWFET with 50/100 nanowires in the pull-up/pull-down networks of the inverter respectively. Here we have not implemented any external parasitics and therefore the resulting frequency is quite high, 77 GHz. The swing is measured to 227 mV with the initial bias value set to 500 mV.

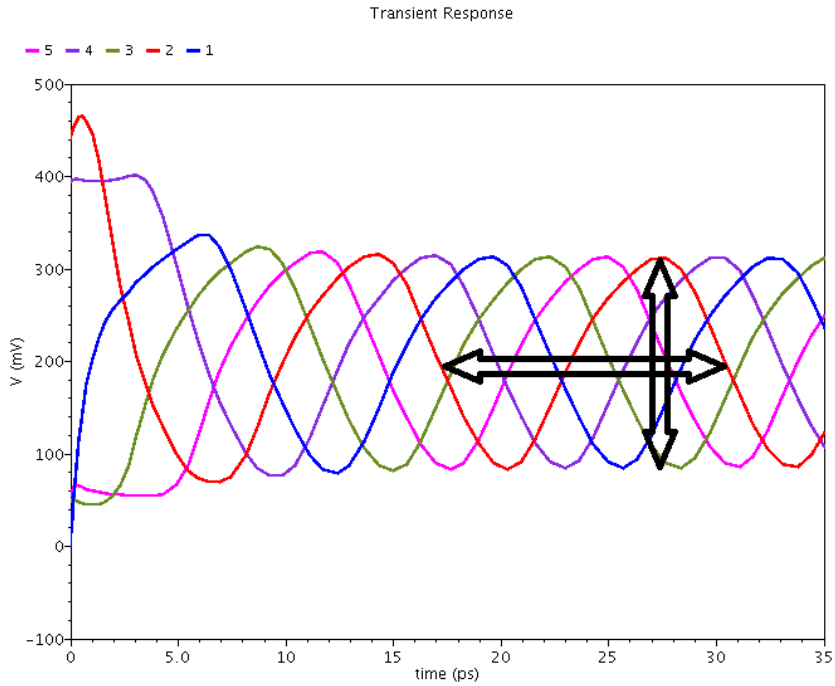

Figure 3. Transient response from a typical ring oscillator simulation in Cadence, the voltage is plotted for all the five stages. The arrows indicate how measurements of the wavelength (horizontal) and the swing (vertical) were observed.

5.2 Compact graphs

Instead of showing numerous variations of the previous graphs, the results are presented in a more compact way. In the following figures the results of several simulations with varying external parasitic values can be seen. On the left Y-axis and the blue line we see the frequency in GHz and on the other side the green line indicates the swing in mV. The X-axis shows the change of the external capacitance in fF.

5.2.1 NWFET

The two graphs, figure 15 and 16, of the simulated NWFET ring oscillators show that we get higher frequencies with more wires in the inverters; they

have the necessary power to drive the oscillation faster. For both cases the oscillation dies out when the parasitic capacitance approaches 25 fF. Improving the development process of the wire, combined with smart layout it is possible to increase the amount of wires.

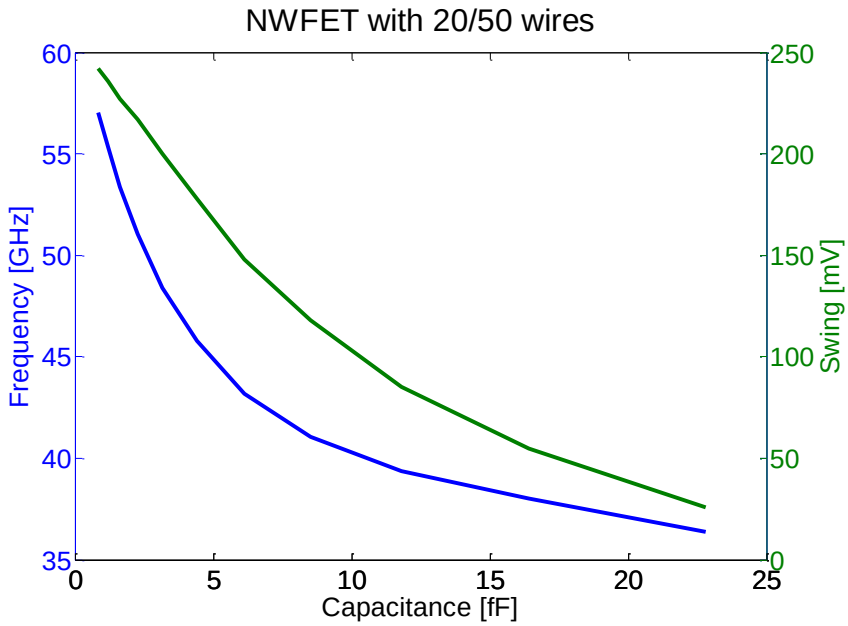

Figure 4. Resulting Frequency (blue) and Signal Swing (green) plots of the NWFET ring oscillator with 20 (PUN) / 50 (PDN) wires per inverter stage.

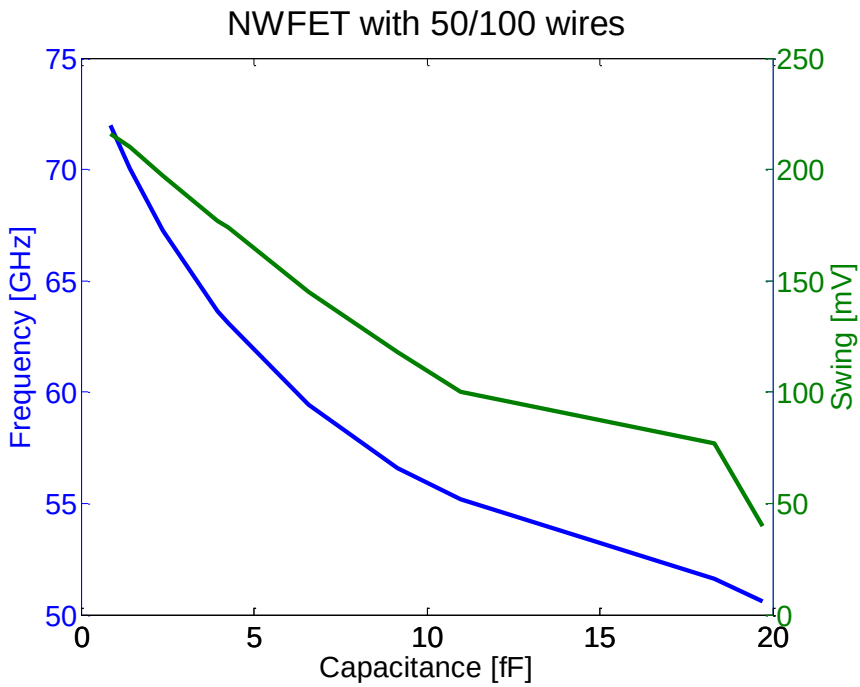

Figure 5. Resulting Frequency (blue) and Signal Swing (green) plots of the NWFET ring oscillator with 50 (PUN) / 100 (PDN) wires per inverter stage.

5.2.2 BFET

The next two graphs show the performance of the BFET ring oscillator; here we can conclude that the frequency is higher than in the NWFET case. The case with 600 wires per stage is clearly performing very well with oscillations occurring even when the parasitic capacitance approaches 500 fF. This example gives a clear view of what is necessary to drive the ring oscillator with higher parasitics.

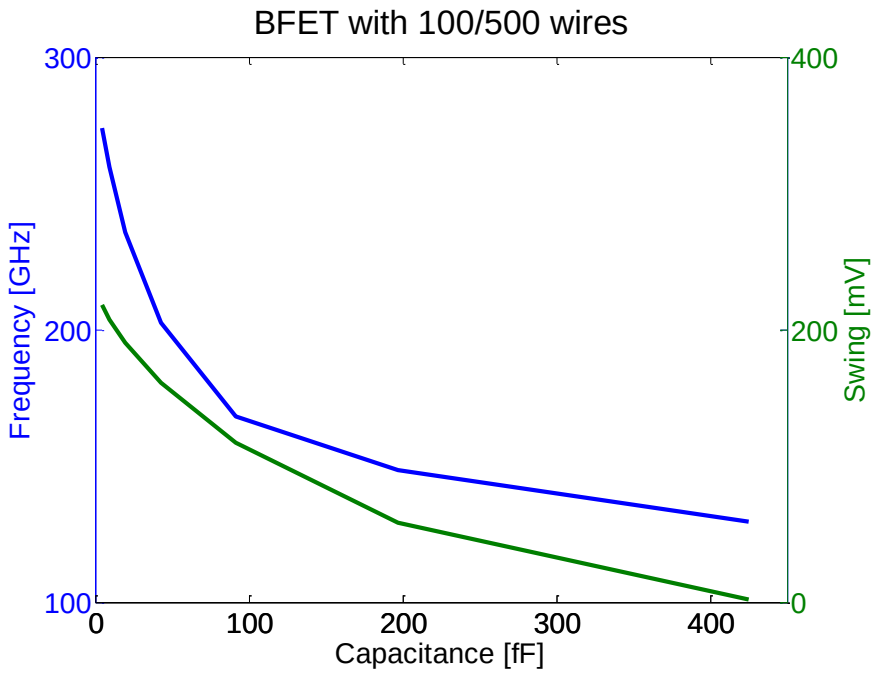

Figure 6. Resulting Frequency (blue) and Signal Swing (green) plots of the BFET ring oscillator with 100 (PUN) / 500 (PDN) wires per inverter stage.

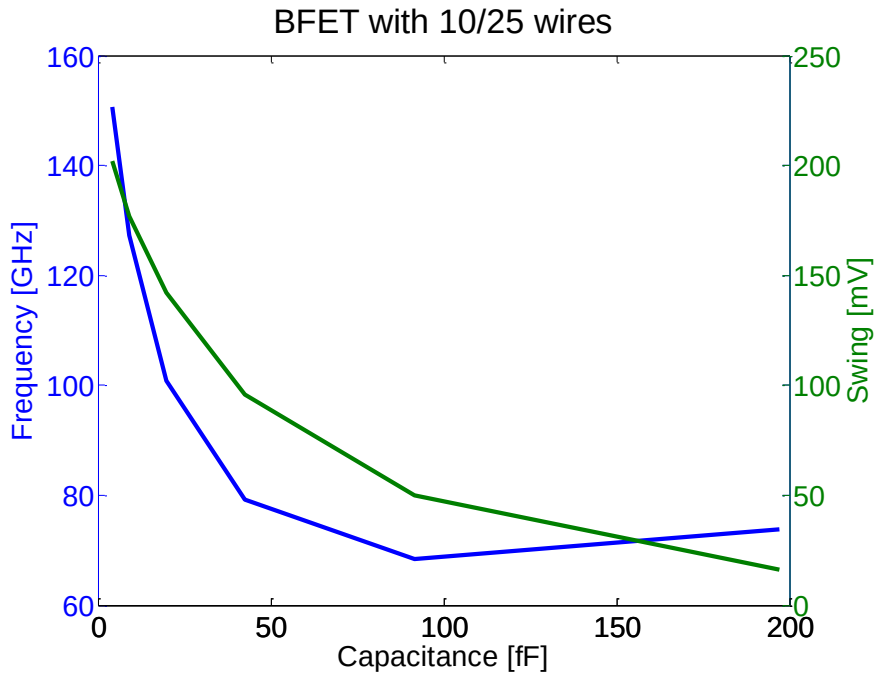

Figure 7. Resulting Frequency (blue) and Signal Swing (green) plots of the BFET ring oscillator with 10 (PUN) / 25 (PDN) wires per inverter stage.

5.2.3 CML

Since the inverter layout is different, in the simulations of the CML ring oscillator, the parameters that were changed between simulations were firstly the number of wires in the paired transistors and secondly the value of the two resistors connected to the transistors.

The results from the CML ring oscillator simulations are shown in the following figures.

In CML, the benefit of the ballistic transport properties is even more clear, frequencies four times higher than the NWFET are common. The four plots with the CML results does not vary much in general. It would be interesting to test the CML in a more complex circuit where losses could be monitored more in detail. Unfortunately, there was no time to continue with the CML in the scope of this project.

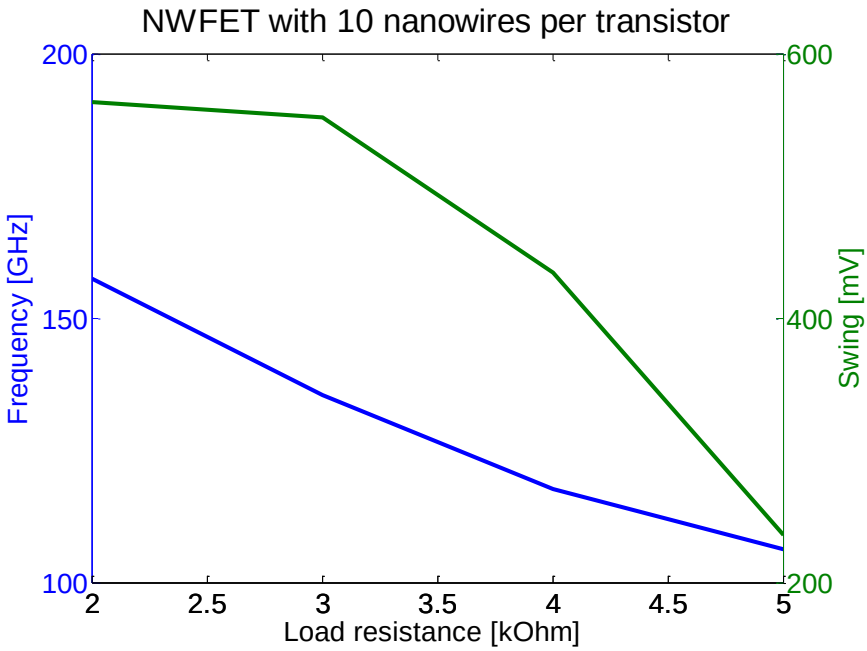

Figure 8. Frequency and swing is plotted for the NWFET (10 nanowires) for varying load resistances.

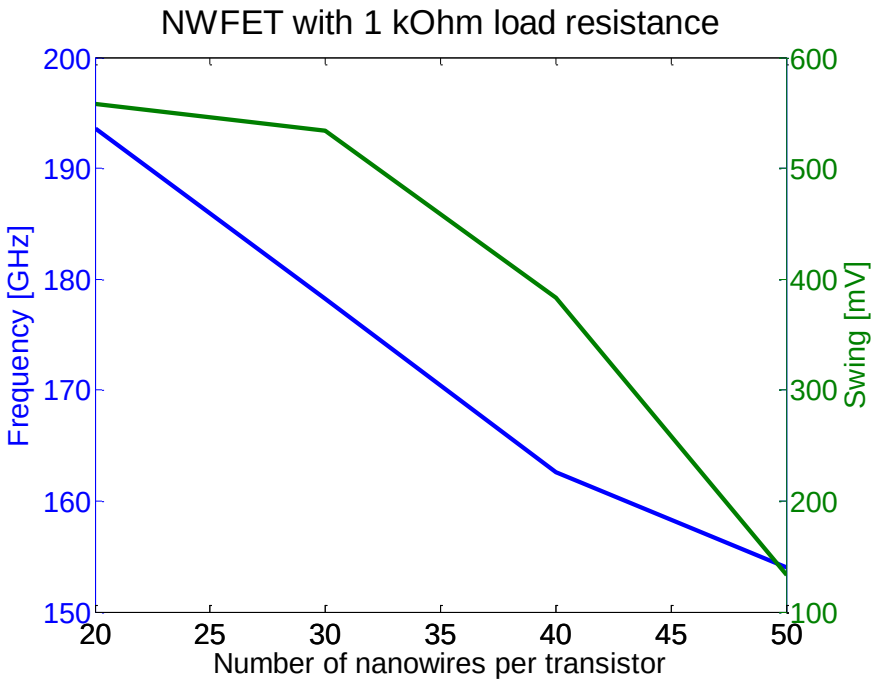

Figure 20. Frequency and swing is plotted for the NWFET (1 kOhm load resistance) for varying number of nanowires.

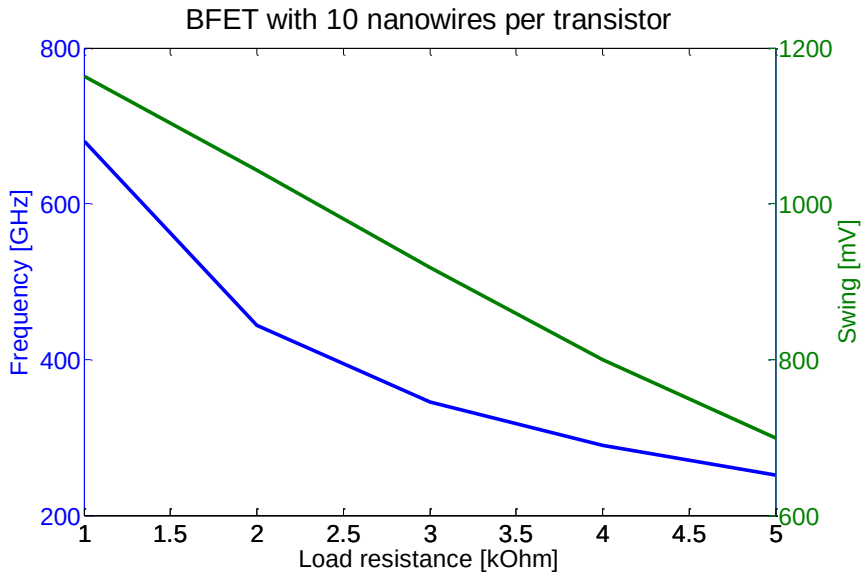

Figure 21. Frequency and swing is plotted for the BFET (10 nanowires) for varying load resistances.

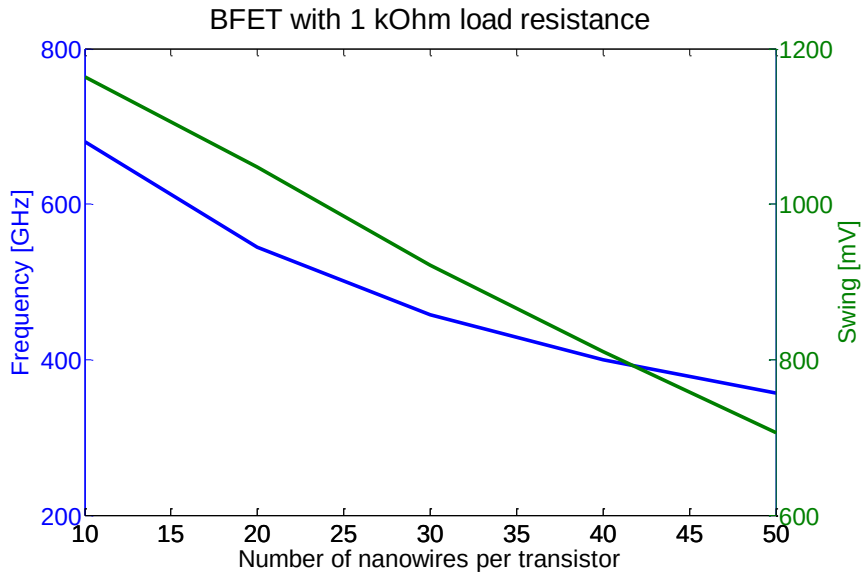

Figure 9. Frequency and swing is plotted for the BFET (1 kOhm load resistance) for varying number of nanowires.

CHAPTER 6

6. Discussion

The NWFET does not perform as well as the BFET in general; showing lower frequencies and equal or worse swings in all setups. This was expected and it is clear that improvements to the transistor performance will benefit the circuits in many ways. Although, there is another factor that in some cases has an even bigger effect on the circuit performance, the circuit layout and biasing structures. Circuit design and bias network are also key to overall circuit performance and are in need of constant design improvements as devices dimensions shrink. The results of the ring oscillator simulation show that the proposed layout has parasitic levels that cannot be handled by the current NWFET inverters. This needs to be addressed before any manufacturing of ring oscillators takes place.

The results of the CML are expected. It reflects the increased performance of the BFET compared to the NWFET well. One important aspect is the fact that there was no implementation of external parasitic that effects in the CML simulations; this would most likely lower the gap between the two design layouts. This also highlights the fact that taking as many aspects as possible into the simulations, minimizing the risk of skewed results.

6.1 Improving the layout:

Upon the realization of the need to lower the wire parasitics, a new layout that lowers the overlapping wires by a factor five was developed. This was obtained by twisting the ring oscillator into more of a physical ring, with two stages at the top and three at the bottom. The layout can be seen in Fig. 23.

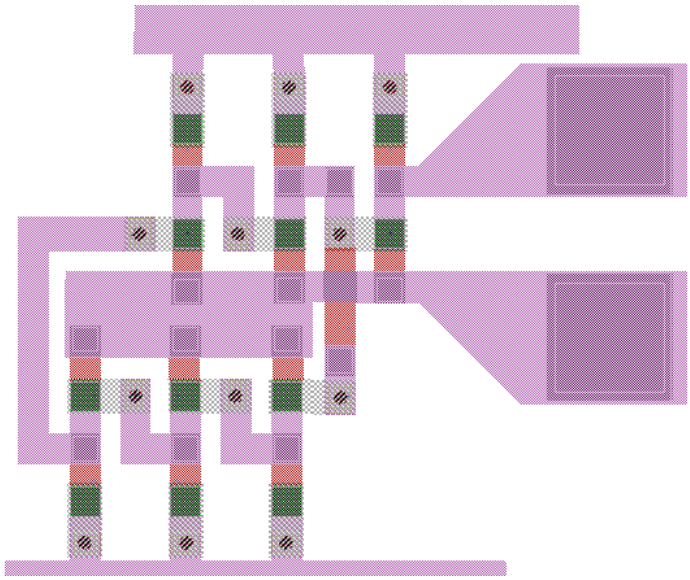

Figure 23. Proposed new layout for the Ring oscillator, reducing the wire overlap.

This is a great example of improvements that can be made in design and layout. More things can be done to improve the results further.

6.2 Improved interconnects

Lowering of the external parasitic capacitance can also be done by decreasing the size of the wires (reducing the overlap) or alternatively increasing the distance between the wires. This is not a favorable approach because of decreased wire performance and increased size. The simulations show that the external parasitic capacitance needs to be lowered by roughly a factor of 100 from the initial design to get oscillations. My suggestion is to do a combination of reduced metal wire width and an increased distance between wire layers. A simple parallel plate capacitor calculation gives us an idea of the quantity of the changes.

Increase the distance between the layers from 20 nm to 200 nm and decrease the wire width from 7 μm to 5 μm while also using the new design gives:

$$C = \epsilon_R \epsilon_0 \frac{A}{d} = 3.9 * 8.85 * 10^{-12} \frac{5 * 10^{-6} * 5 * 10^{-6}}{200 * 10^{-9}} = 4.32\ fF$$

This is roughly a factor 100 lower than the capacitance calculated in the original design. Even if these new calculations are of a simple character it still shows that the parasitics can be lowered with quite small actions.

CHAPTER 7

7. Conclusion

Simulations of NWFET ring oscillators and comparing them to the optimal case with BFET transistors show that there are improvements to be made in regards to the transistor performance and they will greatly improve the performance in a digital design. The project work has also shown that the external wire parasitic effects might give even more benefits at the moment. Small changes to the original design will help the ring oscillator achieve frequencies of approximately 50 GHz.

The project work has also given insight in the importance of a perfected biasing structure to the digital design. Improvements to transistor performances require improvements in circuit layout as well as contact wiring.

CHAPTER 8

8. Future Work

The results of this thesis show that improvements to transistor performance is beneficial to circuit performance, this is of course true since it is the driving point for all the development that goes into the digital industry today. The project has shed more light onto the fact that there is a lot of work that needs to be done regarding the supporting circuitry when looking at an emerging technology. For the implementation of Nanowire Field-Effect Transistors the supporting work regarding biasing is crucial for a successful digital circuit.

The future for the digital industry is bright, which leads the author to believe that the need for new technologies is increasing. The next step in this specific area is probably the implementation of NWFET in small scale circuits. One important thing that needs to be addressed as soon as possible is the negative threshold voltage, which has to be resolved before any circuits can be successfully manufactured. Other than that the author sees no trouble in implementing NWFETs into small-scale digital circuits in the near future.

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