

An Interface State Density Monitoring Circuit for Built-In Self-Test Applications

Viktor Sahlström

June 24, 2012

Abstract

A Verilog-A model to be used when simulating interface state current effects on MOS-devices is developed. Furthermore a circuit measuring the same on chip is presented. The Verilog-A model together with a SPICE model is used to test and prove the functionality of the circuit. The result will be used to monitor the performance of circuits. The model uses an engineering approach and the feasibility is tested using simulations. The result of the project is a circuit able to measure interface state concentrations with an accuracy good enough to determine if a circuit with particular low interface state density requirements should be used or not.

Acknowledgements

This project was done at the Chair of Sensors and actuators at Technische Universität Berlin during spring 2011.

I would like to thank my supervisor Prof. Roland Thewes for his continuous support and for showing great interest in my work.

I would also like to thank Anouar Laifi for helping me get started and later for helping me with the circuit design. Also thanks to Gabriel Bertotti for giving me valuable advice and guidance on the handling of cadence.

Berlin June 24, 2012
Viktor Sahlström

Contents

1	Introduction	5
1.1	Objective	5
1.2	Assignment Directive	5
1.3	Method	5
1.3.1	Transistor Equivalent Model	6
1.3.2	Circuit Design	6
2	Interface states	7
2.1	Physical Description	7
2.1.1	Bonds on an Atomic Level	7
2.1.2	Effects on Band Structures	8
2.1.3	Interface States in MOSFETs.	9
2.2	Impact on Device Behavior	11
2.2.1	Degradation of Off-State Current due to Interface States .	11
2.2.2	Degradation of On-State Current due to Interface States .	13
2.2.3	1/f Noise	15
3	Charge Pumping Interface State Density Determination Method	18
3.1	Basic Principle	18
3.2	Model Weaknesses	19
3.3	Current Model	19
4	Interface State Model Used for Circuit Simulation	23
4.1	Physical Model	23
4.1.1	Verilog-A model	23
4.1.2	Charge Determination	24
4.1.3	Determination of Design Parameters V_{init}, r, τ_1 and τ_2 . .	24
4.2	Input Parameter Generation	26
4.3	Combination of Verilog-A Model with SPICE Model	27
4.4	Model Feasibility Check	28
5	Circuit Design	32
5.1	Topology	32
5.2	Comparator and Delay Line	32
5.2.1	Measuring Stage	32
5.2.2	Comparator	33
5.2.3	Comparator - Scaling	34
5.2.4	Inverters	34
5.2.5	Inverter - Scaling	34
5.2.6	Choice of Capacitor Value	35
5.3	Operational Amplifier and Source Follower for Voltage Regulation	36
5.3.1	Functionality	36
5.3.2	Operational Amplifier	37
5.4	Transistors	39
5.4.1	Miller Effect	39
6	Results	44
6.1	Transient Behavior	44
6.2	Evaluation of Interface State Density	44

1 Introduction

1.1 Objective

This project is meant to address the problem of interface states in high performance sensors and to create an easy to use diagnostic tool to be used to identify the bad sensors. More precisely a circuit will be designed to measure leakage currents through a transistor originating from interface states. In this project the design will not move beyond simulation level. If successful, this circuit will later be built and tested before hopefully going in production. The goal is to implement this circuit on the high performance sensor chips and thereby improve their reliability.

1.2 Assignment Directive

The project consists of two major parts.

- Modeling a transistor containing the interface state related currents.
- Designing and dimensioning a circuit to measure related currents occurring in the transistor.

The measuring circuit must be able to distinguish interface state densities in the order of $10^{10} - 10^{12} cm^{-2}$. The measuring circuit will be based on the charge pumping method [1] [2].

1.3 Method

Since the charge pumping current is a purely physical phenomenon an understanding of the mechanics behind it must be retrieved. To keep the project on a not too complex scale it is important to make certain approximations and simplifications of the pure physical model. Concerning the transistor model it is most important that it works under the conditions used when actually measuring.

The process flow is seen in figure 1.

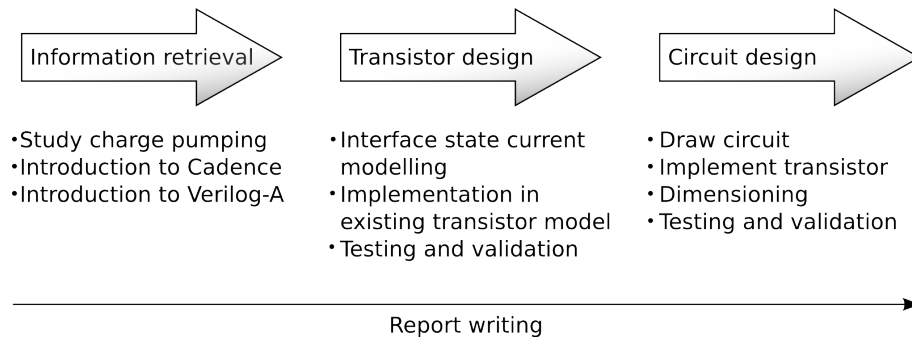


Figure 1: Process flow.

1.3.1 Transistor Equivalent Model

The transistor equivalent model was presumed to be the most challenging part of the thesis. It contained three different parts.

- Modeling interface state currents in Verilog-A
- Determination of threshold and flat band voltage
- Combining the interface state current with usual transistor behavior.

To keep the complexity low it was decided to model the interface state current in Verilog-A but then use a transistor model from Cadance to provide the rest of the transistor functionality.

The Verilog-A model was created bit by bit. The first part was creating the current behavior using a mathematical model. The approximate transient behavior was known and recreated using Verilog-A code and the mathematical model for the interface state density.

This code was then combined with known ways of determining MOSFET threshold voltage and flat band voltage using circuits. So far the model contained the interface state currents and the possibility to determine threshold and flat-band voltage. To incorporate usual transistor behavior this was connected in parallel with a SPICE transistor model.

1.3.2 Circuit Design

The design concept of the circuit was already decided before the project was started. The main task was now to actually get the circuit running and to solve the problems arising. The plan how to do this was the following:

1. Build circuit with ideal elements.
2. Get the circuit running with a normal current source instead of the transistor.
3. Get the circuit running with a transistor without interface state related current.
4. Get the circuit running with the transistor model containing interface states.
5. Dimension circuit elements.
6. One by one, replace the ideal elements with real elements. Make adjustments to the circuit if needed.
7. Optimize.
8. Add extensions if needed/wanted/possible. One example of a possible extension is a clock to control the comparator.

On every level simulations were run and adaptations of the previous parts were done when needed. The results of the different parts can be seen in the respective section and the final results in section 6.

2 Interface states

2.1 Physical Description

2.1.1 Bonds on an Atomic Level

In the description of dangling bonds from [3] it is described how the orbitals around an atom will be affected by surface formation. Through separating atoms the orbitals connecting them will appear as unbonded orbitals directed out of the surface. When interface states are mentioned in this report, these dangling hybrids are that, what is referred to. This approach to describe the phenomena of dangling bonds is different from the ones used by Shockley [4] and Tamm [5]. Although it has been proven that this method, called the dangling orbital model, does not really apply for open surfaces, since the dangling orbitals are eliminated after surface reconstruction [6]. It has been shown, first just as an assumption, later with spectroscopic pictures, that this reconstruction does not necessarily occur when the surface is in contact with another surface, for example as in the case of the Si/SiO₂ interface. Because of this the model described in this text is the dangling orbital model.

Considering an atom with the four bonding possibilities, or orbitals, it can be understood that the alignment of the surface will affect the possible amount of dangling bonds. As seen in figure 2 the cutting plane (111) can give two different results, one containing one unbonded orbital, one containing three unbonded orbitals. For the first case only one bond needs to be broken, whilst connected to the bulk with the remaining three bonds. This case is considered far more probable then case number two, requiring three bonds to be broken while only connected by one last orbital. For this reason only the first case is commonly considered.

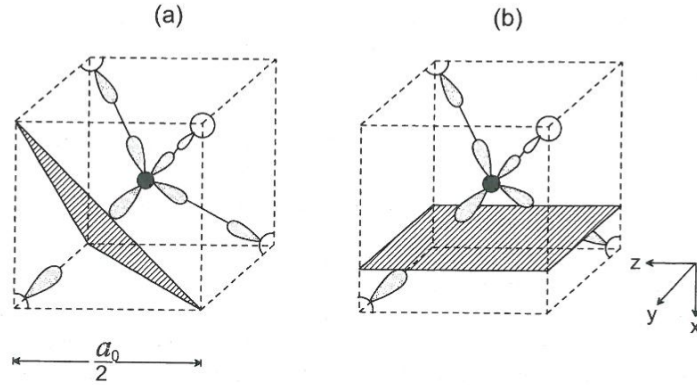


Figure 2: The two different way to create free orbitals. Figure taken from [6]

Creation of the surface in (100) direction would only result in one possible case with two orbitals truncated and two remaining back bonds bonding to the next atomic layer.

During later studies with electro paramagnetic resonance (EPR) only the case with one unbonded orbital and three back bonds has been detected. In later studies it has been referred to as P_b centers [7].

2.1.2 Effects on Band Structures

On an ideal surface the dangling bonds will give electrons a possibility to bond where, in the bulk, it would be impossible. This effect translates to pockets of allowed states in the bandstructure of the material. Investigating such a bandstructure clearly distinguishes the bulk from the surface.

In figure 3 the bandstructure of silicon in (111) and (100) direction is shown. Furthermore the bands of bound surface states are shown as solid lines.

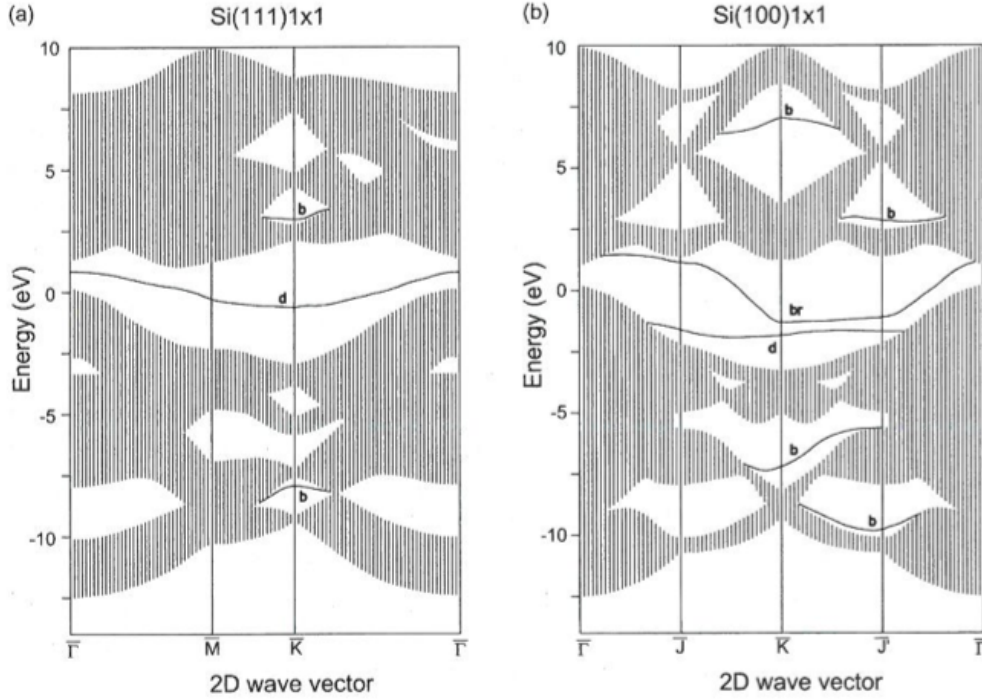


Figure 3: The band structure with the two different cutting planes. Figure taken from [3].

In the case of Si(111) the most obvious effect on the surface is the band marked 'd' in the figure. This is a result of the dangling sp^3 orbitals. It is also seen that this band is located in between the conduction and the valence bands. One also notices the 'b' bands in pockets around K-vector. These are not results of the actual dangling bonds but rather of the interaction between the bonds still connected to the bulk.

As one might expect the effect on the Si(100) is by far more drastic than the

Si(111) case. This mainly because of the fact that now two bonds instead of one are unbonded. When these bonds are first created they are not perpendicular to the surface. For symmetry reasons they are split up into bridge-bond orbitals, notated 'br' in figure 3 and dangling bonds, notated 'd'. These bridge-bonds will be parallel to the surface while the dangling bonds, as before are perpendicular to the surface. This is of course results in a change in how the orbitals look. To split the sp^2 orbitals into three orbitals, where two must be the same, they need to be split into two p orbitals and one sp orbital, see figure 4.

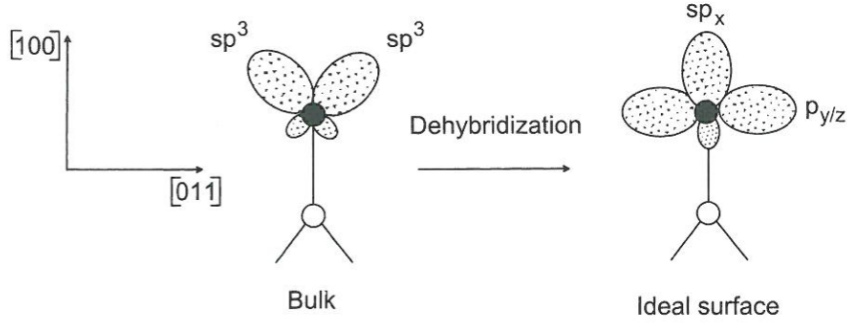


Figure 4: Schematic plot showing how two sp^2 orbitals split into one dangling orbital and two orbitals parallel to the surface. Figure taken from [3].

2.1.3 Interface States in MOSFETs.

It has been investigated and proven by Shockley [4], Tamm [5] and others that interface states in MOSFETs exist. It has also been shown, using ultra-high-vacuum systems, that the concentration of Q_{it} can be very high, approaching the concentration of surface atoms [10]. Such an amount of interface-trapped charge would indeed be troublesome for the behavior of the device. Fortunately, through well optimized anneal this number can be reduced down to about $10^{10} cm^{-2}$.

The interface-trapped charge can be divided into two groups, donors and acceptors. These may trap holes and electrons respectively. The spread of these states in space can be described by the distribution functions below [9].

$$F_{SD}(E_t) = \left[1 - \frac{1}{1 + \frac{1}{g} \exp\left(\frac{E_t - E_f}{kT}\right)} \right] = \frac{1}{1 + g \cdot \exp\left(-\frac{E_t - E_f}{kT}\right)} \quad (1)$$

$$F_{SA}(E_t) = \frac{1}{1 + \frac{1}{g} \exp\left(\frac{E_t - E_f}{kT}\right)} \quad (2)$$

F_{SD} and F_{SA} is the occupancy of the donor and the acceptor interface states respectively. E_t is the energy of the interface trap and g is the ground-state degeneracy (2 for donors and 4 for acceptors).

As the applied voltage shift the voltage difference between the interface states and the respective band will remain constant. Since a voltage shift moves the conduction and valence band while the Fermi level stays constant, the interface states will move in relation to the Fermi level. As the voltage needed to charge the interface states crosses the Fermi level the traps will of course experience charging or discharging depending on type of state and on the voltage change. As the charges on these states change the capacitance between the metal and the semiconductor, the MIS capacitance, will also follow. The MIS curve is no longer ideal and thereby the transistor behavior will also be less ideal. The change in capacitance has been described using the equivalent circuits in figure 5 by Nicollian and Goetzberger [11].

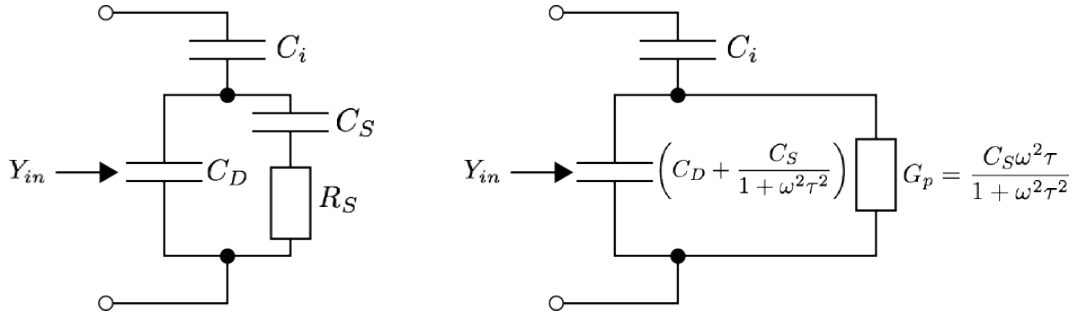


Figure 5: Equivalent circuit of the MIS capacitance including the charge from interface-traps represented by C_S and R_S .

In the figure C_D is the depletion layer capacitance, C_i is the insulator capacitance and C_S is the capacitance arising because of interface-trapped charge. Also the resistance R_S is related to the interface states and they are both a function of surface potential. The time constant $C_S R_S$ is in this case defined as the trap lifetime. This is an important aspect when considering the frequency behavior of charging and discharging process of the interface states.

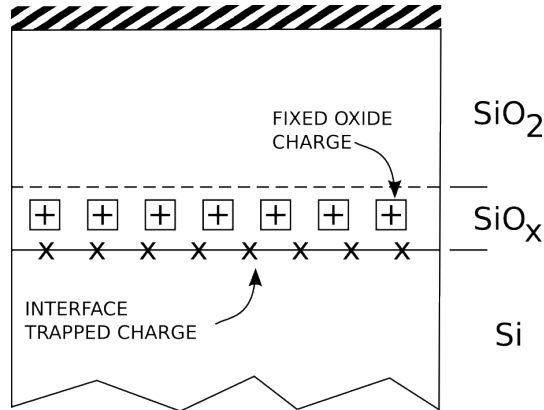


Figure 6: Schematic picture of interface states on a Si/SiO_x surface.

2.2 Impact on Device Behavior

2.2.1 Degradation of Off-State Current due to Interface States

Band-to-band tunneling and tunneling via grain-boundary traps were both early reported as important leakage currents. Realizing this, the next natural step was an investigation of how high densities of interfaces could influence the leakage [12]. In [12] interface states are created through Fowler-Nordheim tunneling current through the oxide. Measurements were made as the interface state concentration was increased. Thereafter the sample was annealed in low temperature (300° 20min) to remove the interface states and the measurements were once again run. In figure 7 one notices mainly two important findings. Firstly, the total leakage current is above the band-to-band tunneling at low-field. This implies that other leaking mechanisms are really present. Secondly one notices how the leakage increases with an increase of the interface state concentration. These results are today considered to be known and are being taken into account when designing new devices. The concentration of interface states needed to have an actual impact on the device is important to know so that one can distinguish between devices where this is a problem, and devices where it is not.

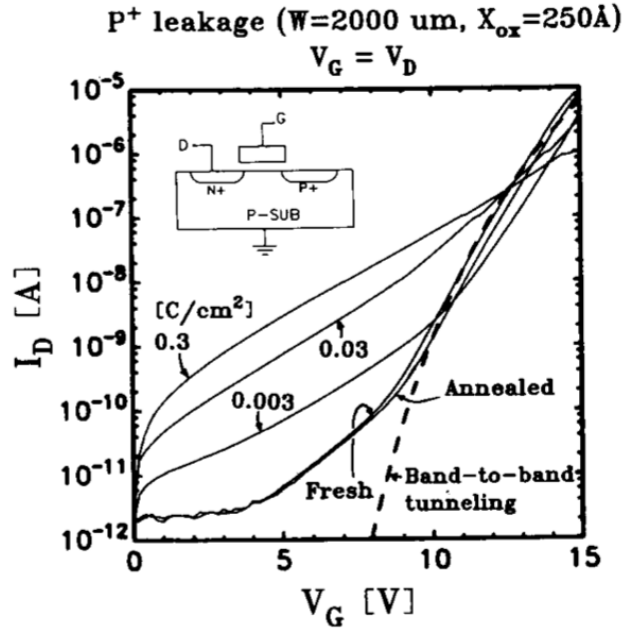


Figure 7: Gate-induced leakage I_D as a function of gate voltage V_G . The leakage was generated at the p^+ edge. The low voltage leakage strongly deviate from the expected Band-to-band tunneling. Thermal annealing can almost bring the leakage back to the unstressed level. Figure taken from [12].

The mechanism involving interface states leading to a larger drain leakage current is band-trap-band tunneling [13]. Here the charge carriers are excited from the valence band to the interface trap and then tunneling into the conduction band. The quasi-Fermi level is of importance since it decides if charge carriers

can be excited into the interface traps. Since the band bending affects the interface traps energy in relation to the quasi-Fermi level a sufficient increase in V_{dg} will result in thermal excitation no longer being an dominant reason for charge carrier occupation in the interface traps. On the other hand, a sufficiently low V_{dg} will make the tunneling harder and thereby make thermal excitation from the trap to the conduction band the mechanism of most importance.

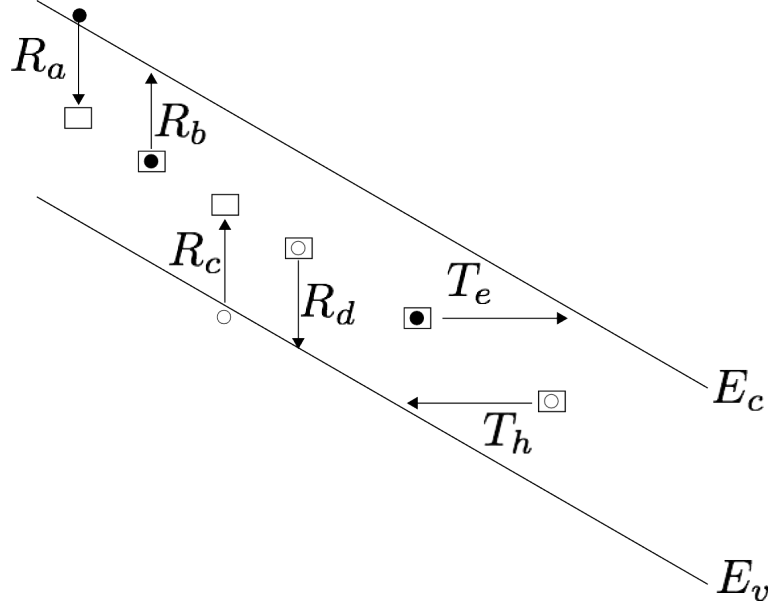


Figure 8: Schematic plot showing different possibilities for a charge carrier to enter or leave the bandgap. Electrons are represented by the black dots while the white dots represent holes. R_a , R_b , R_c and R_d are the possibilities for charge carriers to recombine as shown by the arrows. T_e and T_h are the possibilities for charge carriers to tunnel out of the bandgap.

For a more quantitative discussion of the leakage introduced by interface traps these mechanics are investigated one by one. In figure 8 one notices the different possible processes for tunneling (T_e and T_h) and thermal excitation ($G_e = R_a - R_b$ and $G_h = R_d - R_c$) for electrons and holes. The four contributions from recombination is simplified using two expressions for generation, one for electrons (G_e) and one for holes (G_h). Using Shockley-Read-Hall theory [9] the thermal excitation can be expressed as,

$$G_e = v_{th}\sigma_n \left[n_i \exp\left(\frac{E_t - E_i}{kT}\right) f_t - n_s(1 - f_t) \right] \quad (3a)$$

$$G_h = v_{th}\sigma_h \left[n_i \exp\left(\frac{E_i - E_t}{kT}\right) (1 - f_t) - (p_s f_t) \right], \quad (3b)$$

where v_{th} is the thermal velocity, σ_n and σ_p are the capture cross-sections of electrons and holes, n_i is the intrinsic carrier density, E_i is an intrinsic Fermi level, E_t is the trap energy, f_t is the electron occupation factor of interface traps,

and n_s , and p_s , are the electron and hole densities at the interface. Furthermore the tunneling is described as follows.

$$T_e = (f_t - f_c) / \tau_e \quad (4a)$$

$$T_h = ((i - f_t) - (1 - f_v)) / \tau_h \quad (4b)$$

There τ_e is the time constant for electron tunneling, τ_h is the time constant for hole tunneling. f_c and $(1 - f_v)$ are electron and hole occupation factors in the conduction band and in the valence band. To reach steady state the current at the valence band must equal the current on the conduction band, that means

$$G_e + T_e = G_h + T_h. \quad (5)$$

Insertion from equations (3) and (4) in (5) makes it possible to derive f_t . After doing this the drain leakage current is evaluated [14] and the result is seen below.

$$\Delta I_d = qW \int_{channel} \int_{bandgap} \Delta N_{it}(x, E_t) (G_e + T_e) dE_t dx, \quad (6)$$

where N_{it} is the interface state density and W is the width of the channel. The shape of the interface state distribution suggests a uniformity close to the intrinsic Fermi level which gives the possibility to simplify this expression further.

$$\Delta I_d \propto \int_{bandgap} G_e(E_t, x_t) dE_t + \int_{bandgap} T_e(E_t, x_t) dE_t = G'_e + T'_e \quad (7)$$

In (7) x_t is the location of the ΔI_d maximum and the G'_e and T'_e represent the integration between the valence- to the conduction band of G_e and T_e respectively. When V_{ds} increases, it would seem reasonable to assume that the drain leakage current would increase, since that would bring the conduction and the valence band closer together and thereby make the tunneling easier. This means that the effect described above has a greater impact when the transistor is in off-state. This also shows that there is a linear relation between the interface state concentration and the drain leakage current because arising from them.

2.2.2 Degradation of On-State Current due to Interface States

The dominating reason for a degradation of the on-state current caused by interface states is the lowering of the mobility that occurs. To quantify this effect a model using the gradual-channel approximation (GCA) is used. In this model one can clearly see the change in threshold voltage as well as a reduction in transconductance. To charge one interface state we need to have a potential above the interface trap energy in that specific point. The GCA model gives us [15],

$$dV_c = I_D dR_c = -\frac{I_D dy}{W \mu Q'_n(y)}, \quad (8)$$

with

$$Q'_n(y) = -C_{ox} [V_g - V_{TO} - V_c(y)] + qN_{it}(y). \quad (9)$$

Here V_{TO} is a linear extrapolation of the threshold voltage. To express this as a drain current (μ_0/L) is multiplied on both sides and the entire expression is integrated along the channel. We now have

$$\int_0^L \frac{\mu_0 I_d dy}{\mu L} = \int_0^{V_D} C_{ox} [V_g - V_{TO} - V_c(y)] dV_c - \frac{\mu_0 W}{L} \int_0^{V_D} q N_{it}(y) dV_c. \quad (10)$$

The two parts on the right-hand side consists of, firstly the normal current in a MOSFET

$$I_D = \frac{\mu_0 W}{L} C_{ox} \left(V_g - V_{TO} - \frac{V_D}{2} \right) V_D \quad (11)$$

while the second part is the mobility degradation as a function of interface state density. This can also be expressed using the empirical relationship established by Sun and Plummer [16].

$$\mu = \frac{\mu_0}{1 + \alpha N_{it}} \quad (12)$$

where $\mu_0 = 3490 - 164 \cdot \log(N_a) V_s / (Am)$, $\alpha = -0.104 + 0.0193 \cdot \log(N_a) m^2$ and with N_{it} in units of ($10^{12}/cm^2$). Using this, and the newly defined,

$$\bar{N}_{it} \equiv \frac{1}{L} \int_0^L N_{it}(y) dy. \quad (13)$$

the left side of (10) can be written as $I_D (1 + \alpha \bar{N}_{it})$. Furthermore, if V_D is sufficiently small, we could approximate the part of (10) containing the mobility degradation to

$$\frac{\mu_0 W}{L} \int_0^L q N_{it} \left(\frac{dV_c}{dy} \right) dy \approx \frac{\mu_0 W}{L} \left(\frac{V_0}{L} \right) \int_0^L q N_{it} dy = \frac{\mu_0 W V_D}{L} q \bar{N}_{it} \quad (14)$$

Combining (10) - (14) results in,

$$(1 + \alpha \bar{N}_{it}) I_D = \frac{\mu_0 W}{L} C_{ox} \left(V_g - V_{TO} - \frac{V_D}{2} \right) V_D - \frac{\mu_0 W V_D}{L} q \bar{N}_{it} \quad (15)$$

To move on we first need to consider the relation between the threshold voltage and the gate voltage of the device. Having a threshold defined at a specific drain current results in the change in V_T following V_g . This can easily be understood through comparing the input characteristic of the same MOSFET but with a shift in V_T . The result is the curve moving along the voltage axis, a shift in V_g thereby directly correlates to a shift in V_T . In this case that shift, ΔV_T , can be found through subtracting the current after degradation from the current before degradation.

$$\begin{aligned} (1 + \alpha \bar{N}_{it}) I_D - I_D &= I_D \alpha \bar{N}_{it} = \frac{\mu_0 W}{L} C_{ox} \left(V_{g,after} V_{T0} - \frac{V_D}{2} \right) V_D \\ &\quad - \frac{\mu_0 W V_D}{L} C_{ox} q \bar{N}_{it} - \frac{\mu_0 W}{L} C_{ox} \left(V_{g,before} V_{T0} - \frac{V_D}{2} \right) V_D \quad (16) \\ \rightarrow [V_{g,after} - V_{g,before} = \Delta V_T] &\rightarrow \Delta V_T = \left(\frac{L \alpha I_D}{V_D \mu_0 W C_{ox}} + \frac{q}{C_{ox}} \right) \bar{N}_{it} \end{aligned}$$

Here the left term describes the lower mobility in the device while the right term describes the smaller amount of mobile charge. Furthermore the degradation of the transconductance can be derived. With

$$G_m = \left. \frac{dI_D}{dV_g} \right|_{V_D} \quad (17)$$

15 turns into

$$(1 + \alpha \bar{N}_{it}) G_m = \frac{\mu_0 W}{L} C_{ox} V_D. \quad (18)$$

To reach a linear relationship between the transconductance and the interface state concentration the difference of the inverse transconductance before and after degradation is calculated.

$$\frac{\Delta G_m}{G_{m0} - \Delta G_m} = \alpha \bar{N}_{it}. \quad (19)$$

As a result two simple linear models, (16) and (19), have been derived to describe the relation between threshold voltage, mobility and interface state concentration in the device.

2.2.3 1/f Noise

It has been shown by [18] that the $1/f$ noise in MOS devices has different dependencies depending on the type of device. In a nMOS the interface traps are shown to be the dominant reason for $1/f$ noise, while the mobility degradation is the biggest cause in the case of pMOS devices.

It has been accepted for quite some time that $1/f$ noise is related to the capture and emission of charge by the interface traps really close to the Si/SiO_2 -interface. The work of John H. Scofield presents a model explaining the $1/f$ noise in MOS-devices [19].

Starting of with the energy band diagram shown in figure 9 we need to make some definitions. First we define the number of accepting interface traps to $n_{ot}(E, x) dx dE$ where their energy lies between E and $E + dE$ and they are situated a distance between x and $x + dX$ away from the interface. The probability of occupation is described through the Fermi factor

$$F(E) = \frac{1}{\exp\left(\frac{E - E_f(T)}{kT}\right) + 1} \quad (20)$$

There, E_f is the fermi level. The goal is the determination of mean concentration on trapped electrons over an area, $\langle N_t \rangle$. We can calculate that through integrating $\langle n_t(E, x) \rangle$ over the bandgap energy and the oxide thickness. $\langle n_t(E, x) \rangle$ is given by:

$$\langle n_t(E, x) \rangle = n_{ot}(E, x) F(E) \quad (21)$$

The integral of this would then be:

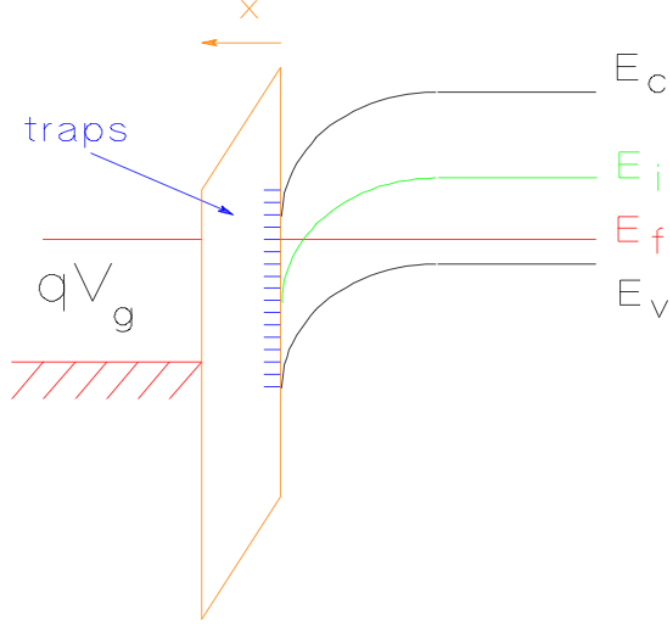


Figure 9: The energy bands near the Si/SiO_2 interface in a n-channel MOSFET in inversion.

$$\langle N_t \rangle = \int_{E_v}^{E_c} \int_0^{t_{ox}} n_{ot}(E, x) F(E) dx dE \quad (22)$$

with the integration limits in energy set by the valence band, E_v and the conduction band E_c and the limits in space set by the oxide edges. Because the system will be in thermal equilibrium and because electrons can move between the traps and the channel through tunneling certain fluctuations ($\delta n_t(E, x)$) in the concentration of trapped charge is assumed. The variance of these fluctuations is given by [20]

$$\langle \delta n_t^2(E, x) \rangle = \frac{\langle n_{ot}(E, x) \rangle}{LW} F(E) [1 - F(E)]. \quad (23)$$

Through integrating this over energy and space the variance in the total number of trapped charges can be obtained.

$$\langle \delta N_t^2 \rangle = \frac{1}{LW} \int_{E_v}^{E_c} \int_0^{t_{ox}} n_{ot}(E, x) F(E) [1 - F(E)] dx dE \quad (24)$$

The power spectral density is now given from [19]. It has been obtained using the results from above and the Wiener-Khintchine theorem and the result is shown below.

$$S_{n_t}(f) = \frac{4\tau \langle \delta n_t^2 \rangle}{1 + (2\pi f\tau)^2} \quad (25)$$

Finally equation (23) is inserted in equation (25) and the result is integrated over E and x. The final result is:

$$S_{N_t}(f, T) = \frac{1}{LW} \int_0^{t_{ox}} \int_{E_v}^{E_c} n_{ot}(E, x) F(E) [1 - F(E)] \frac{4\tau(E, x)}{1 + [2\pi f\tau(E, x)]^2} dE dx \quad (26)$$

Here the dependence from the interface state concentration on the $1/f$ noise is clearly shown. Seeing that the an increase in the interface state concentration would linearly worsen the noise, this effect is indeed something that needs to be taken into account.

3 Charge Pumping Interface State Density Determination Method

3.1 Basic Principle

There have been numerous suggestions how to measure the concentration of interface states in a MOS-device. Many of them contain methods where the MOS-capacitances are measured. Another technique to measure the concentration of interface states using charge pumping was developed and published by Paul Heremans, Johan Witters, Guido Groeseneken and Herman E. Maes [1].

The basic setup used for interface state measurements through charge pumping is seen in figure 10. A pulse is applied on the gate while the source and drain are connected to each other. In [1] the source and drain are also connected to the bulk through a voltage source applying a small negative voltage to the source node, this is of course not obligatory. When the voltage on the gate increases and the transistor reaches inversion electrons will fill the channel and thereby charge the interface states accepting electrons. As the transistor moves towards accumulation the electrons in the channel floods out through the source, drain and bulk. The charges trapped by the interface states recombine with holes in the channel. This means that a net flow of current into the transistor arises.

The charge absorbed during one charge/discharge of the interface states can easily be described by

$$Q_{pulse} = WLN_{it}q, \quad (27)$$

where Q_{pulse} is the charge every pulse, W and L is the width and length, N_{it} is the concentration of interface states per square centimeter and q is the elementary charge.

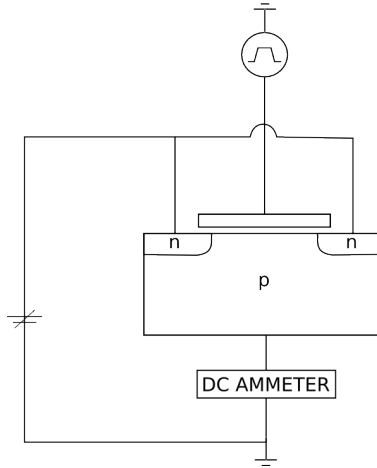


Figure 10: Basic configuration used to measure the interface state concentration using the charge pumping technique as shown in [?]

With a direct relation between charge and interface states everything one needs

to do to get a value for the interface state concentration is to measure the net charge through the transistor over time, the current. What is important is that the voltage on the gate translates into both inversion and accumulation in the channel region. Otherwise the charge carriers might stay in the traps and not contribute to the measured current. The method used in our case, since it is suitable when only the total amount of interface states is of interest, is to keep the pulse base voltage constant in accumulation and then to switch the gate to inversion.

The second method keeps the amplitude of the pulse constant while the base level of the pulse moves in relation to the threshold voltage. Through doing this one can determine the concentrations of interface states in different energy regions. This because the traps with the lowest energy will be reached before the traps of higher energy.

3.2 Model Weaknesses

Even though the charge pumping technique has been used for interface state measurements it was not always the dominating technique. The reason for this is a number of deviations from the simple model given above.

1. Dependence of the Pulse Shape: the current measured depends on whether the pulse is for example squared or triangular.
2. Current Increase with Increasing Gate Voltage: the V_{GH} , maximum gate voltage during one pulse, affects the current measured.
3. Nonlinear Frequency Dependence on Triangular Pulses: when using triangular pulses the linear relation of f is not shown.
4. Current Decrease with Increasing Reverse Voltage: by applying a reverse voltage on source and drain the charge pumping current is decreased.

To avoid these artifacts some decisions had to be made about the pulse before moving on to a more thorough investigation of the current. Firstly, it is decided to use a square pulse in order to avoid pulse shape deviations and the nonlinear dependence of f with triangular pulses. The dependence on increasing gate voltage can be neglected simply from using a V_{GH} sufficiently high since the increase is fairly slow.

By designing the measurement setup using these demands for the pulse the measurement will be accurate enough for this particular project. In order to gain a better understanding why the next section describes what happens as the gate voltage is shifting more carefully and also derives a more precise expression of the interface state current.

3.3 Current Model

This section more thoroughly discusses the mechanisms resulting in current as the gate voltage is changed. An nMOS is used as example for simplicity. A square pulse is applied on the transistor gate with the rise time t_r , fall time t_f , amplitude $\Delta V = V_{GH} - V_{GL}$ and the period T_p . The discussion is taken apart

into six different parts which relates to six different stages of one pulse. They can be seen in figure 11.

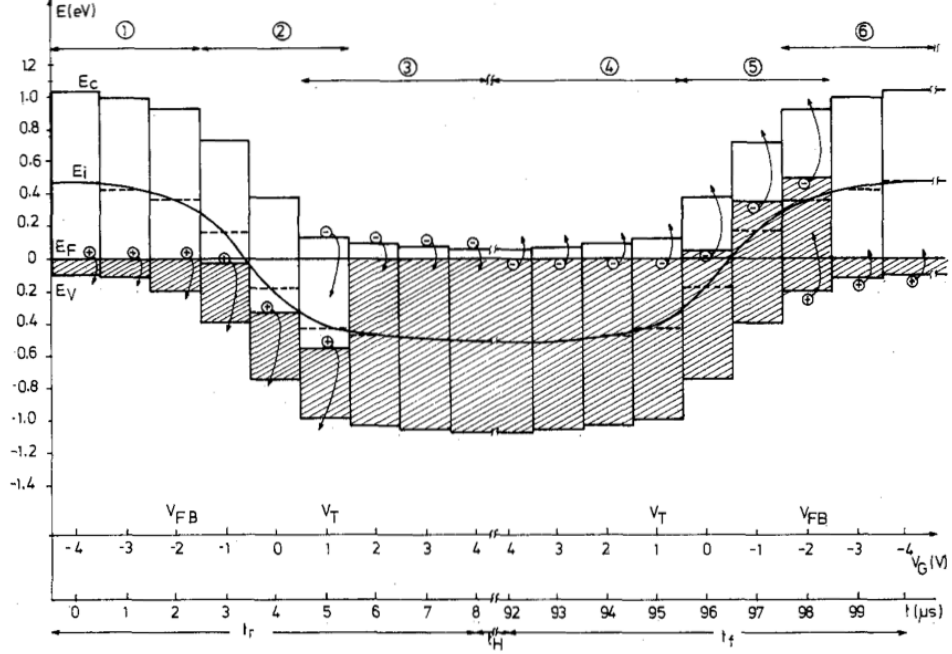


Figure 11: The different stages occurring as one gate voltage pulse passes. Plot taken from [2]

1. The gate voltage is now increasing. This results in holes moving from the interface states to the valence band and then flowing into the substrate. This automatically happens to maintain equilibrium. To obtain this equilibrium [17]

$$\left. \frac{dQ_t}{dt} \right|_{em} > \left. \frac{dQ_t}{dt} \right|_{ss}. \quad (28)$$

where $\left. \frac{dQ_t}{dt} \right|_{em}$ is the real change in charge trapped in the interface states and $\left. \frac{dQ_t}{dt} \right|_{ss}$ is the change in charge trapped needed to obtain equilibrium. These can also be written as

$$\left. \frac{dQ_t}{dt} \right|_{em} = -q^2 \overline{D_{it}} \frac{d\Psi_s}{dt}, \quad (29a)$$

$$\left. \frac{dQ_t}{dt} \right|_{ss} = -q \frac{d}{dt} n_t(t), \quad (29b)$$

where $n_t(t)$ is the hole density, in this case with nMOS.

2. When the condition in (28) is no longer true the relation moves from a regime where the traps were linearly discharged into a regime where the flow is only depending on the emission process. The function describing the occupied traps in this case, closely follows the Fermi-Dirac distribution. One difference is the time dependence for the traps. The gate voltage needed to reach this point can of course be calculated using the demands given in equation (29a). A more detailed investigation of this demand will show that this point will, always lie very close to the flat-band voltage [1]. This can be explained by considering the amount of charge carriers. When moving from flat-band towards strong inversion the amount of charge carriers in the channel is going to be very low. To be able to move charge some type of carrier has to be present. The only way to supply carriers in this case is by the hole emission that is always present, which makes the time constant for the flow very close to the emission time constant. Since the voltage on the gate changes very quickly the device will enter a stage where it can not emit holes fast enough to charge the interface states. This happens shortly after flat-band. Because of this it is a good approximation to say that the flat-band voltage is the border between the steady state and the nonsteady-state regime.
3. As the gate voltage now gets closer to the threshold voltage, electrons start to charge the neutral traps. This change can be described using the trapping time constant,

$$\tau_t \simeq \frac{1}{v_{th}\sigma_n n_s}, \quad (30)$$

where v_{th} is the thermal velocity of the carriers, σ_n is the capture cross section of electrons and n_s is the surface concentration of minority carriers. When the gate voltage is close to the threshold voltage the remaining traps will be filled with electrons and the previous equilibrium is regained.

4. In the final steps the behavior is similar to that explained before. First there is a flow of electrons into the source and drain until a voltage close to the threshold voltage is reached. The nonsteady-state is once again reached in the depletion region and finally the trapping time constant of holes gain importance close to the flat-band voltage and holes will thereby fill the remaining states containing electrons.

Now the currents can be described as four different currents using the description above. For simplicity we set D_{it} to constant and equal to $\overline{D_{it}}$. In this case the equations are,

$$I_1 = -q^2 \overline{D_{it}} \cdot \Delta \Psi_e \cdot f \cdot A_G, \quad (31a)$$

$$I_2 = q^2 \overline{D_{it}} \cdot \Delta \Psi_{ee} \cdot f \cdot A_G, \quad (31b)$$

$$I_3 = -q^2 \overline{D_{it}} \cdot \Delta \Psi_h \cdot f \cdot A_G, \quad (31c)$$

$$I_4 = q^2 \overline{D_{it}} \cdot \Delta \Psi_{he} \cdot f \cdot A_G. \quad (31d)$$

$$(31e)$$

Since the charge carriers entering and leaving through the channel through the source and drain are electrons, the currents through these can be described as

$$I_{S/D} = I_{CP} = I_2 + I_1 = q^2 \overline{D_{it}} (\Delta \Psi_{ee} - \Delta \Psi_e) f \cdot A_G, \quad (32)$$

whilst the current through the substrate is the current provided by the holes,

$$I_{SUB} = I_{CP} = I_4 + I_3 = q^2 \overline{D_{it}} (\Delta \Psi_{he} - \Delta \Psi_h) f \cdot A_G. \quad (33)$$

From [1] following relations are given

$$E_{em,e} - E_i = -kT \ln \left(v_{th} \cdot \sigma_n \cdot n_i \cdot t_{em,e} + e^{(E_i - E_{F,inv})/kT} \right), \quad (34)$$

$$E_{em,h} - E_i = kT \ln \left(v_{th} \cdot \sigma_n \cdot n_i \cdot t_{em,h} + e^{(E_{E,acc} - E_i)/kT} \right), \quad (35)$$

where the time for emission in nonsteady-state is represented in $t_{em,h}$ and $t_{em,e}$ for holes and electrons respectively. The exponential terms are describing the case when the emission levels are close to the band edges. Furthermore, the previous assumptions lead to expressions for these emission times.

$$t_{em,e} = \frac{|V_{FB} - V_T|}{|\Delta V_G|} \cdot t_f, \quad (36)$$

$$t_{em,h} = \frac{|V_{FB} - V_T|}{|\Delta V_G|} \cdot t_r. \quad (37)$$

One can now describe the more exact and reliable charge pumping current as

$$I_{CP} = 2q \overline{D_{it}} f \cdot A_G \cdot kT \left[\ln (v_{th} n_i \sqrt{\sigma_n \cdot \sigma_p}) + \left(\frac{|V_{FB} - V_T|}{|V_G|} \sqrt{t_f \cdot t_r} \right) \right]. \quad (38)$$

4 Interface State Model Used for Circuit Simulation

4.1 Physical Model

4.1.1 Verilog-A model

It was decided to model the interface state current with a Verilog-A code instead of an equivalent circuit since it would make the behavior and the manipulation of the circuit easier. Using Verilog-A one can easily create the current shape one wants just by using equations.

The Verilog-A model written in this case consists of two mayor parts. One part that charges the interface states and one part that discharges them. Since the shapes of these currents are not well investigated, we decided to treat the charge and discharge shapes similar to the ones of a capacitor. We also decided that the interface states start charging as $V_{gb} > V_{th}$ and discharging as $V_{gb} < V_{fb}$, a motivation can be found in section 3.

Seeing that the charge and discharge are depending on the threshold voltage, somehow the threshold voltage needs to be determined. Since the threshold voltage changes as a function of source voltage this must be done continuously. The solution for this is explained in section 4.2.

Since the interface states have opposite charges, the charging/discharging will occur at different times. Charging of the interface states that trap electrons will occur when the channel is filled with electrons i.e. in strong inversion. The discharge of those traps will occur when the gate voltage is below flat band voltage. Interface states that traps holes works the same but the other way around.

This means that the current provided by an interface state trapping holes and an interface state trapping electrons is the same. Different is the shape of the current charging and discharging the interface states. This is because from the difference in mobility between electrons and holes.

Since the shape of the current does not really affect the charge drawn through the transistor, it will be enough to consider one of the cases above as an engineering approach in this investigation. In reality the concentration of interface states could be a result of both types.

The interface states do not only vary in type but also in energy distribution. The interface states can be situated anywhere in the bandgap. Since one wants to measure all the interface states when investigating the concentration, we must make sure to have a gate voltage large enough to be above the conduction energy, in strong inversion, which means that all our interface states are filled. By doing this, all the states, disregarding were they are on an energetic scale, will contribute to the current. Therefore the energy of the traps does not have an impact in this case.

4.1.2 Charge Determination

It was decided to design the current using two exponential functions. As the time increases the current will first increase until it reaches a maximum and then starts decreasing. To be able to modulate how fast the current increases/decreases and to calculate the resulting charge the factors τ_1 and τ_2 were added. The resulting function is shown below.

$$I(t) = \frac{V_{init}}{r} \cdot \left(1 - e^{-\frac{t}{\tau_1}}\right) \cdot e^{-\frac{t}{\tau_2}} \quad (39)$$

$$= \frac{V_{init}}{r} \cdot \left(e^{-\frac{t}{\tau_2}} - e^{-\left(\frac{t}{\tau_1} + \frac{t}{\tau_2}\right)}\right) = \quad (40)$$

$$= \left[\frac{t}{\tau_1} + \frac{t}{\tau_2} = \frac{t(\tau_1 + \tau_2)}{\tau_1 \cdot \tau_2}\right] = \quad (41)$$

$$= \frac{V_{init}}{r} \cdot \left(e^{-\frac{t}{\tau_2}} - e^{-\left(\frac{t(\tau_1 + \tau_2)}{\tau_1 \cdot \tau_2}\right)}\right) \quad (42)$$

To get a value of the charge one pulse contributes, this function needs to be integrated from zero to infinity, shown below.

$$Q_{pulse} = \frac{V_{init}}{r} \int_0^\infty \left(e^{-\frac{t}{\tau_2}} - e^{-\left(\frac{t(\tau_1 + \tau_2)}{\tau_1 \cdot \tau_2}\right)}\right) dx = \quad (43)$$

$$= \frac{V_{init}}{r} \left[-\tau_2 \cdot e^{-\frac{t}{\tau_2}} + \frac{\tau_1 \tau_2}{\tau_1 + \tau_2} e^{-\left(\frac{t(\tau_1 + \tau_2)}{\tau_1 \cdot \tau_2}\right)}\right]_0^\infty = \quad (44)$$

$$= \frac{V_{init}}{r} \left(\tau_2 - \frac{\tau_1 \cdot \tau_2}{\tau_1 + \tau_2}\right) \quad (45)$$

The result is a simple function of τ_1 and τ_2 with V_{init}/r as a prefactor to make the amount of charge easy to modulate. As this equation is later used, τ_1 and τ_2 are kept constant and the prefactors are changed to alter the behavior of the current. This means that the time needed to charge/discharge is not depending on the interface state concentration. An approximation made to make simulations easier and less time consuming.

4.1.3 Determination of Design Parameters V_{init} , r , τ_1 and τ_2

The next step is determining V_{init} , r , τ_1 and τ_2 from the dimensions of the transistor. The charge stored during one complete charging of the interface traps depending on the dimensions of the transistor is

$$Q_{pulse} = 2WLN_{it}q \quad (46)$$

$$\frac{V_{init}}{r} \left(\tau_2 - \frac{\tau_1 \cdot \tau_2}{\tau_1 + \tau_2}\right) = 2WLN_{it}q \quad (47)$$

which can easily be solved. However, to get a good and realistic time behavior of the current one needs to make some further considerations. As seen in (42) the maximum current is increasing with V_{init}/r which means the pulse duration is decreasing with the same. Considering the time constants τ_1 and τ_2 one notices that the length of the pulse is increasing with τ_2 while the maximum current is

increasing with increasing τ_2/τ_1 .

To determine the pulse width one first needs to define what the pulse width is. Here it is defined as the time when $I(t) = \frac{1}{20} \cdot I_{max}$. To be able to investigate this one firstly needs to be able to calculate the maximum current. This is done by differentiating (42) with aspect to time.

$$\frac{\delta I}{\delta t} = \frac{V_{init}}{r} \cdot \left(-\frac{1}{\tau_2} e^{-\frac{t}{\tau_2}} + \frac{\tau_1 + \tau_2}{\tau_1 \cdot \tau_2} e^{-\left(\frac{t(\tau_1 + \tau_2)}{\tau_1 \cdot \tau_2}\right)} \right) \quad (48)$$

This expression has the only non-trivial solution at a time t_{max} when

$$0 = \frac{\tau_1 + \tau_2}{\tau_1 \cdot \tau_2} e^{-\left(\frac{t_{max}(\tau_1 + \tau_2)}{\tau_1 \cdot \tau_2}\right)} - \frac{1}{\tau_2} e^{-\frac{t_{max}}{\tau_2}} \quad (49)$$

$$t_{max} = -\ln\left(\frac{\tau_1 + \tau_2}{\tau_1}\right) / \tau_1 \quad (50)$$

Insertion of (50) in (42) results in

$$I_{max} = \frac{V_{init}}{r} (C + D) = \frac{V_{init}}{r} (e^A - e^B) \quad (51)$$

$$A = -\frac{t_{max}}{\tau_2} = \frac{\ln\left(\frac{\tau_1 + \tau_2}{\tau_1}\right) \cdot \tau_1}{\tau_2} \quad (52)$$

$$B = -\frac{t_{max} \cdot (\tau_1 + \tau_2)}{\tau_2 \cdot \tau_1} = \frac{\ln\left(\frac{\tau_1 + \tau_2}{\tau_1}\right) \cdot (\tau_1 + \tau_2)}{\tau_2} \quad (53)$$

$$C = \left(\frac{\tau_1 + \tau_2}{\tau_1}\right)^{\frac{\tau_1}{\tau_2}} \quad (54)$$

$$D = \left(\frac{\tau_1 + \tau_2}{\tau_1}\right)^{\frac{\tau_1 + \tau_2}{\tau_2}} \quad (55)$$

$$I_{max} = \frac{V_{init}}{r} \left[\left(\frac{\tau_1 + \tau_2}{\tau_1}\right)^{\frac{\tau_1}{\tau_2}} - \left(\frac{\tau_1 + \tau_2}{\tau_1}\right)^{\frac{\tau_1 + \tau_2}{\tau_2}} \right] \quad (56)$$

Finally the combination of (42) and (56) gives

$$e^{-\frac{t_{pulse}}{\tau_2}} - e^{-\left(\frac{t_{pulse}(\tau_1 + \tau_2)}{\tau_1 \cdot \tau_2}\right)} = \frac{1}{20} \left[\left(\frac{\tau_1 + \tau_2}{\tau_1}\right)^{\frac{\tau_1}{\tau_2}} - \left(\frac{\tau_1 + \tau_2}{\tau_1}\right)^{\frac{\tau_1 + \tau_2}{\tau_2}} \right] \quad (57)$$

which cannot be easily solved with analytical methods but according to MATLABs "solve"-function.

$$t_{pulse} = -\tau_2 \cdot \log \frac{1}{20} \left[\frac{\frac{\tau_1 + \tau_2}{\tau_1} \left(\frac{\tau_2 + 1}{\tau_1 \cdot \tau_2}\right) - \frac{\tau_1 + \tau_2}{\tau_1} \frac{1}{\tau_1 \cdot \tau_2}}{\frac{\tau_1 + \tau_2}{e^{\frac{\tau_1 + \tau_2}{\tau_1}} - 1}} \right] \quad (58)$$

Equations (47) and (58) do now provide 2 equations with 2 unknown parameters. With Q_{charge} and t_{pulse} given, values for τ_1 and τ_2 can be calculated. Starting with the extraction of τ_1

$$Q_{pulse} = \frac{V_{init}}{r} \left(\tau_2 - \frac{\tau_1 \cdot \tau_2}{\tau_1 + \tau_2} \right) \quad (59)$$

$$\frac{Q_{pulse} \cdot r}{V_{init}} = \tau_2 - \frac{\tau_1 \cdot \tau_2}{\tau_1 + \tau_2} \quad (60)$$

$$\left(\tau_2 - \frac{Q_{pulse} \cdot r}{V_{init}} \right) \frac{\tau_1}{\tau_2} + \left(\tau_2 - \frac{Q_{pulse} \cdot r}{V_{init}} \right) = \tau_1 \quad (61)$$

$$\tau_2 - \frac{Q_{pulse} \cdot r}{V_{init}} = \tau_1 \frac{Q_{pulse} \cdot r}{V_{init}} \quad (62)$$

$$\frac{V_{init} \cdot \tau_2^2}{Q_{pulse} \cdot r} - \frac{1}{\tau_2} = \tau_1 \quad (63)$$

Insertion of (63) in (58) would do no good since no solution for τ_2 can be found. Instead τ_2 should be chosen to set the pulse time and then τ_1 can be calculated in order to get the correct value for Q_{pulse} .

Below, in figure 12 the charge as a function of time is plotted for different values of τ_1 and τ_2 . There you can clearly see that the dependence that was expected surely is true. Still an easy method to choose time constants from transistor dimensions lacks.

When using the model for simulation the τ_1 and τ_2 was used to set the shape of the current pulse while $\frac{V_{init}}{r}$ was used to set the amount of current. This is of course not the best solution since it changes the amount of current without taking possible physical effects into account. For example the current charging the interface state might not increase linearly depending on the concentration of the states, but somehow change the time dependence of the charging. Though the lack of literature regarding this makes it hard to estimate such an effect, and, even if done with success, such a model would not make any real difference in this work since the only limitation is that the charge/discharge of the interface states are faster then the pulse. If an increase in interface states would increase the charge time to that point were not all the states were charged and discharged every pulse this would, of course, lead to a change in charge drawn from the circuit and thereby give false measurement results.

Thinking more about this one realizes that this would result in a nonlinear relation between interface state density, and time needed to discharge the measurement capacitor. To avoid this the frequency of the voltage pulse on the interface state transistor needs to be low enough to fully charge and discharge our interface states.

4.2 Input Parameter Generation

To determine the threshold voltage by means of simulation a transistor (T_1) in diode configuration, as in figure 13. The source on T_1 is fed the source voltage

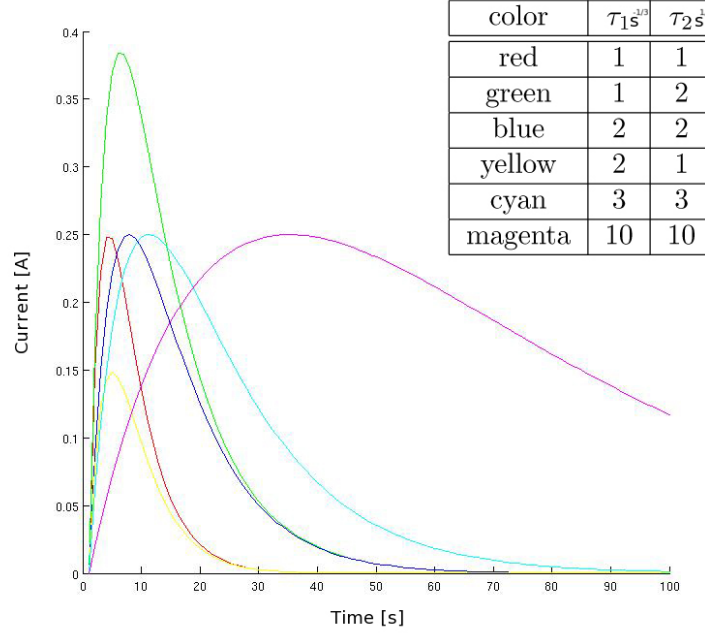


Figure 12: The current over time for different time constants.

from the transistor under test and the current source provides a current corresponding to the drain current of this particular transistor when the gate voltage equals the threshold voltage. To determine this current a separate simulation is run, plotting the input characteristics.

Under these conditions, using a transistor in diode configuration at a specified current, $V_{GS} = V_{th}$. The gate source voltage on T_1 is measured and used to modulate the threshold voltage of the transistor under test.

The modulation of the flat band voltage is not the most crucial issue in this case. Important is that the flat band is reached when applying the pulse and that the flat band voltage somehow follows the threshold voltage as the source voltage is modulated. This can easily be done by using the threshold voltage already modulated and defining the distance between the two. A standard value for this, using this technology, is around $0.6V$, so the flatband voltage is defined as $V_{fb} = V_{th} - 0.6V$.

4.3 Combination of Verilog-A Model with SPICE Model

As the interface state current model now is complete, the next step is to combine it with the SPICE model of a transistor. It is decided to use a $3.3V$ isolated nMOS with $W = 10\mu m$ and $L = 2\mu m$. Any type of nMOS could be used but it is important that the same type is used everywhere in the model.

To get the contribution from the SPICE model, this transistor model was connected in parallel with the interface state current source. Since $V_{SD} \approx 0$ when

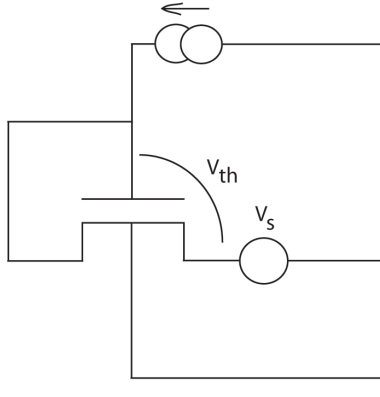


Figure 13: Use of an extra transistor to determine the V_{th} .

using the charge pumping measurement method, the most important contribution from this transistor is the current from the charge and discharge processes of the channel. These needs to be taken into consideration since a too big change in voltage could affect the functionality of the circuit.

The result of these three parts is shown as a circuit in fig 14. There the blackbox connecting everything provides the interface state current and adds it to the normal transistor behavior provided by the transistor connected in parallel to the right. The top part of the circuit only provides the threshold voltage to the interface state model.

4.4 Model Feasibility Check

To be able to consider the model as finished, some testing was done. The model was tried out as a normal transistor and as a transistor with different concentrations of interface states. To do this the transistor was put into a really simple testbench as shown in figure 15 and simulations were run. The results from one of these simulations are shown in figure 16.

This is the interface state current that occurs when the gate voltage of the transistor goes from high to low. The negative sign means that the current moves into the transistor.

What we see in figure 17 is supposed to be charge moving into the channel as the gate voltage is increasing but also the interface state current. This flow into or out of the channel occurs anytime the field over the channel is changed in any direction. In the case where we go from high to low voltage we have the opposite current. As seen in this plot the current charging the channel is a lot larger than the interface state current (the interface state current cannot be seen in this figure, compare to figure 28). This could lead to problems when measuring. To circumvent this a trick will be used that is discussed in chapter 5.2.

To more thoroughly investigate the results a quantitative analysis of the results

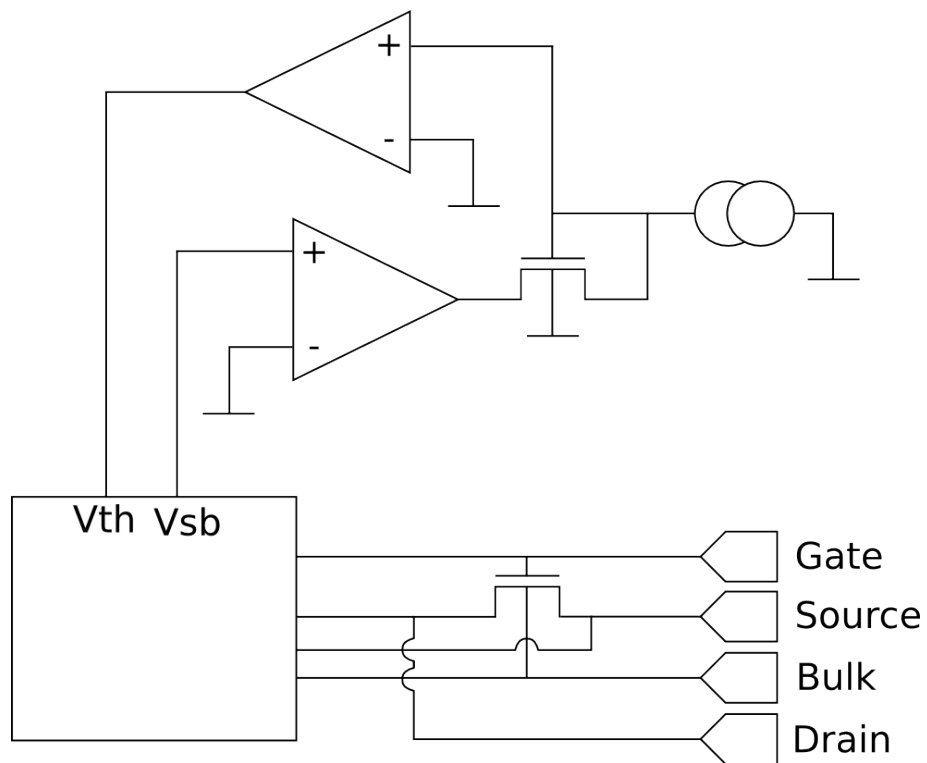


Figure 14: Blackbox used as transistor.

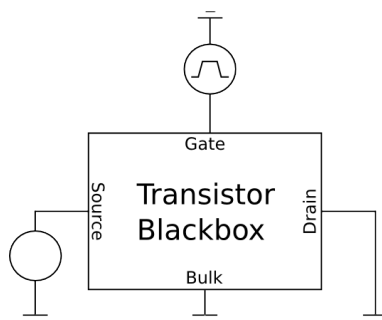


Figure 15: Testbench used to prove the functionality of the modeled transistor.

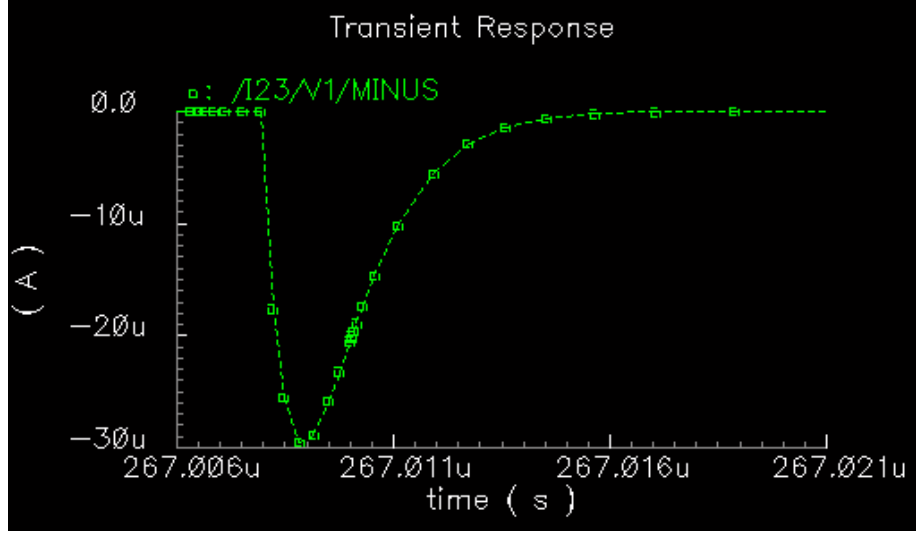


Figure 16: Zoom in on the interface state current at the drain node as the gate voltage moves the transistor's operation point from saturation to depletion.

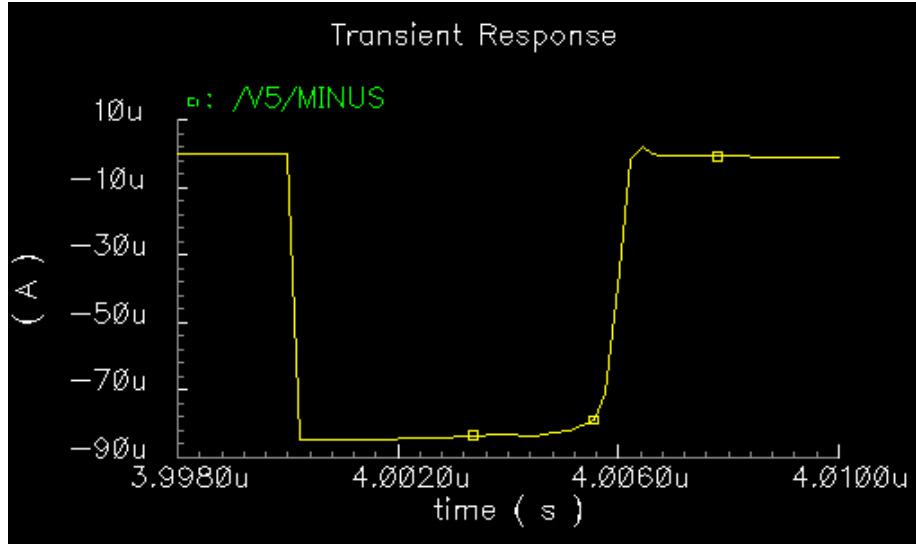


Figure 17: Combination of the interface state current and the channel charge at low concentration of interface states ($N_{it} = 10^{10} cm^{-2}$).

needed to be done. The goal is an interface state density in order $10^{10}cm^{-2}$, since this is the smallest value in range it is also going to be the smallest value measured. This gives a charge of

$$Q_{pulse} = W \cdot L \cdot q \cdot N_{it} = 10^{-5} \cdot 10^{-5} \cdot 1.6 \cdot 10^{-19} \cdot 10^{10} \cdot 10^4 = 1,6 \cdot 10^{-15}C \quad (64)$$

When trying to find values for our variables that would give a nice shape and a charge close to the one in 64 the values below was found.

$$Q_{pulse} = \frac{V_{init}}{r} \cdot \left(10^{-9} - \frac{20 \cdot 10^{-9} \cdot 10^{-9}}{20 \cdot 10^{-9} + 10^{-9}} \right) = 4,76190 \cdot 10^{-15}C \quad (65)$$

This current is approximately 3 times the value calculated in 64. The order of magnitude is good so the simulation is run with this value. The results from the simulation are shown in figure 17. The charge contribution from interface states are calculated using the integrator function in Cadence. The integration is done over multiple periods. The result is

$$4.76190... \cdot 10^{-15}C \quad (66)$$

This means that the simulation and the theoretical values are the same to an accuracy of 6 digits. Furthermore, one would like to compare this to the charge needed to charge the channel of the transistor. To do this, the gate capacitance C_G is calculated.

$$C_G = W \cdot L \cdot \frac{1}{t} \cdot \epsilon_0 \cdot \epsilon_r = \frac{10^{-5} \cdot 10^{-5}}{5 \cdot 10^{-9}} \cdot 3.9 \cdot 8.85 \cdot 10^{-12}F = 0.69pF \quad (67)$$

$$Q_{channel} = C_G \cdot \Delta V = 0.69pF \cdot 3.3V \approx 2.3pC \quad (68)$$

This shows that the charge needed to charge the gate capacitance under these conditions is about a thousand times bigger than the interface state charge. If we would consider the other case, the biggest interface state charge we would get, it would be roughly a hundred times bigger. That is still smaller then the charge from charging the channel but big enough to show in the plots, see figure 16.

5 Circuit Design

5.1 Topology

In figure 18 the circuit used for interface state density characterization is shown. The circuit consists of three major parts:

- the comparator and delay line,
- the operational amplifier and source follower for voltage regulation,
- and the transistors under test.

The transistors of course draw the current measured, the interface state related current from the source-drain nodes. This lowers the voltage in the same node. The task for the operational amplifier is to keep the voltage in the source-drain nodes of the transistors under test at a constant value. This is achieved through opening the source follower as the voltage decreases and thereby draw current from the capacitor C which is also connected to the input node of the comparator. This of course also lowers the voltage in that node. The comparator compares the voltage at the capacitor with a reference voltage and switches from high to low as this reference is reached. With a slight delay the transistor at the end of the delay line opens and the voltage drop at the capacitor C is reset. The delay line is needed to make sure that the circuit has enough time for a complete reset. As a consequence of the reset also the comparator output shows high again.

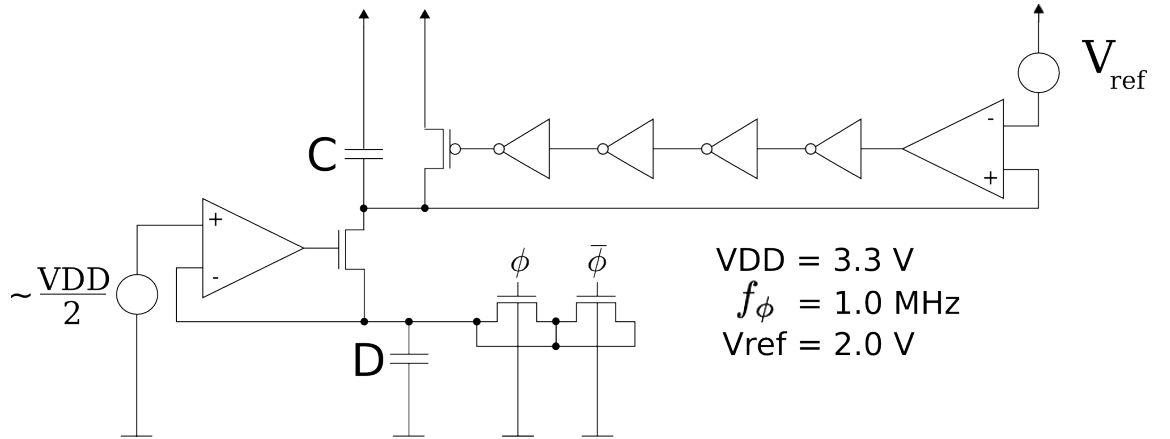


Figure 18: Circuit for measuring the interface state concentration.

5.2 Comparator and Delay Line

5.2.1 Measuring Stage

The measuring stage consists of one capacitor to be discharged by the interface state related current, one part to decide when a certain voltage drop has been achieved.

1. As long as the voltage at the non-inverting input of the comparator is above the reference voltage, the output voltage of the comparator is high.
2. As the interface state related current flows, the voltage at the non-inverting input of the comparator decreases.
3. When the chosen reference voltage is reached, the output of the comparator switches from high to low which opens the pMOS reset transistor with a delay gathered by the four inverters between comparator output and pMOS transistor gate.
4. When the pMOS transistor is opened capacitor C is shut down and the voltage at the non-inverting input of the comparator is reset to its starting voltage. This also gives a "high" at the output.
5. Consequently the entire process is started again. The repetition frequency is proportional to the interface state related current.

5.2.2 Comparator

Here, a comparator with full voltage swing at the output and a steep change from high to low output is needed. This because the input voltage is going to change fairly slow and it will affect the measurement quite a lot if the comparator does not switch as soon as low voltage is reached. A commonly used comparator fulfilling these demands is the Miller operational amplifier operated as time continuous comparator. See figure 19.

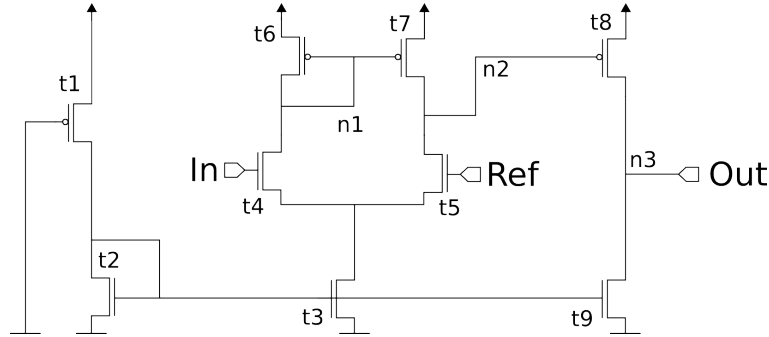


Figure 19: Miller opamp based comparator.

Functionality

Let's consider the case with input voltage \gg reference voltage.

1. The input transistor, t4, is now open.
2. This gives low on node n1, at the gates of the pMOS transistors t6 and t7.
3. That opens transistor t7 and thereby sets the voltage in node n2 to high.
4. This high voltage closes transistor t8 and thereby sets the voltage at the output on node n3 to low.

The other way around when input voltage is much smaller than reference voltage.

5.2.3 Comparator - Scaling

Scaling a commonly used device like the Miller Op-Amp can easily be done using standard methods and will not be discussed in detail in this text. What is done is to consider the relative driving capability of the transistors used to have a balanced and well working device. The major issue that will affect our circuit in this case is the input capacitance. Since it is going to be in parallel with capacitor C the interface state related current has to discharge both of them to lower the voltage enough to trigger the comparator. Knowing that the capacitance to be discharged is approximately $20pF$ the input capacitance has to be small in relation. On the other hand, a transistor with too small dimensions will suffer from process deviations that might affect the circuit performance.

Considering the second demand the length of the input transistor is set to $2\mu m$ and the width to $10\mu m$. Using these dimensions we now calculate the input capacitance. Since these are 3.3 V transistors, the oxide thickness is roughly 5 nm. Furthermore the dielectric constant of silicon oxide is approximately 4. The gate capacitance is then

$$C_{gate} = C_{ox} \cdot W \cdot L \quad (69)$$

$$\approx \frac{8.85 \cdot 10^{-12} \cdot 4}{5nm} \cdot 10\mu m \cdot 2\mu m \quad (70)$$

$$\approx 0.14pF. \quad (71)$$

This means that $0.14pF$ extra capacitance is going to be discharged every pulse. In comparison to the $20pF$ meant to be discharged this is a deviation of 0.7%. Such a small deviation in this case, is clearly acceptable.

5.2.4 Inverters

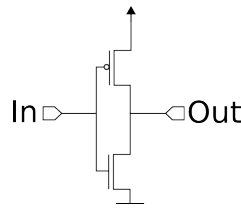


Figure 20: CMOS inverter.

Normal CMOS inverters as shown in figure 20 are used to provide a delay in the measuring part of the circuit long enough to completely reset the voltage drop over capacitor C.

5.2.5 Inverter - Scaling

When designing the circuit the number and size of the inverters was an open issue. An even number of inverters is needed to make sure that high voltage out

of the comparator provides high voltage at the pMOS after the inverter chain. At first four inverters were used where width and length for the nMOS were both one micrometer. The pMOS had a length of one micrometer but a width of two micrometers. During simulations these inverters turned out to be too fast, this is seen by looking at the starting voltage of the capacitor node. When the pMOS closes before the voltage drop at the capacitor is completely reset, a lack of delay can be assumed to be the problem. In order not to make the delay too big, the width of the pMOS can also be increased in order to increase its driving capability.

To increase the delay there are two possibilities. The inverter delay or the number of inverters can be increased. For simplicity the inverters were redesigned with the new length of ten micrometers. When the simulations were ran with these inverters, the delay was sufficient.

5.2.6 Choice of Capacitor Value

There are a few demands on the size of this capacitance.

- It should be not too large to make the time needed for measurement as small as possible. Still, to be able to measure properly a minimum amount of pulses needed to discharge should be defined.
- It should be big enough to make the input capacitance of the comparator small in comparison, since this capacitance would make the time needed to discharge the capacitance bigger, hence giving a bad result.
- It can not be too small in comparison to the capacitance of the interface state transistor sources, for the same reason as above.

Here, the first demand is of course the most critical as the others can be manipulated in another way, as discussed and done, earlier. Given is:

$$I_{CP} = 2WLN_{it}qf \quad (72)$$

$$C = Q/V \rightarrow V_{ref} = Q/C \quad (73)$$

$$Q = I_{CP} \cdot T \quad (74)$$

$$[T \neq \frac{1}{f}] \quad (75)$$

$$= 2WLN_{it}qfT \quad (76)$$

$$= 2WLN_{it}qn, \quad (77)$$

where n is the number of clock cycles needed to reach the reference voltage on the non-inverting input at the comparator. The demands on N_{it} is:

$10^9 cm^{-2}$	few $10^{10} cm^{-2}$	$10^{12} cm^{-2}$
excellent	good...fair	very bad

The capacitor must be big enough to measure the largest amounts of interface states, $10^{12}cm^{-2}$. Also the transistor is quadratic with the a side length of $10\mu m$ and the reference voltage drop measured on the comparator input is $300mV$. This gives the charge per pulse (one pulse is one charge and one discharge of the channel)

$$Q_{pulse} = WLN_{it}q \quad (78)$$

$$= 10\mu m \cdot 10\mu m \cdot 10^{12}cm^{-1} \cdot 1.602 \cdot 10^{-19}C \quad (79)$$

$$= 1.602 \cdot 10^{-13}C = 160.2fC. \quad (80)$$

To get a voltage drop of $\Delta V = 300mV$ with a capacitance $C_{discharge}$ the required charge is

$$Q = C_{discharge}\Delta V. \quad (81)$$

To measure one would like at lest tens of pulses. This while the measurements could start and stop within one pulse and thereby cause an error of up to one pulse. With less then ten pulses this is more then 10% deviation which in combination with other artifacts, is to much. With this in mind, a number of 40 pulses is chosen. The capacitance needed will then be

$$C_{measure} = \frac{40 \cdot Q_{pulse}}{\Delta V} \approx 20pF. \quad (82)$$

This was the extreme case in one direction. To get to the extreme case in the other one, ($N_{it} = 10^{10}$) there will be a hundred times as many pulses. With the frequency used, each pulse takes one microsecond. The time consumed to get one full discharge in this case is therefor

$$T = 40 \cdot 100 \cdot 1\mu s = 4ms. \quad (83)$$

This value is quite high but acceptable.

5.3 Operational Amplifier and Source Follower for Voltage Regulation

5.3.1 Functionality

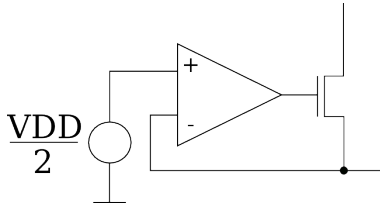


Figure 21: The regulation loop meant to keep the voltage at the source node of the transistor under test at a constant level.

Since the current generated by the interface states is only meant to affect the voltage at capacitor C (see fig 18) the voltage at the source node of the transistor

under test must be kept constant. To achieve this a regulation loop is added to the circuit. It consists of one operational amplifier with one input connected to a reference voltage and one to the source node of the transistors under test. The output is connected to the gate of the source follower. The function of this loop is described below.

1. The voltage at the source node of the transistor under test decreases.
2. the difference in voltage at the operational amplifier inputs increases which gives an increase in the gate voltage on the source follower transistor
3. More current flows through the transistor, from capacitor C towards the source of the transistor under test, since the potential in this node is always higher then at capacitor C.
4. This increases the voltage in node 1 until we reach the wanted voltage (the voltage on the positive input of the operational amplifier).
5. Now the two inputs are equal and the transistor is closed.

If the gain in the OP-amp is big enough, this will keep the voltage on the source drain node of the devices under test at a constant value.

5.3.2 Operational Amplifier

The operational amplifier is based on similar circuit topology as the comparator in section 5.2.3 and is shown in figure 22.

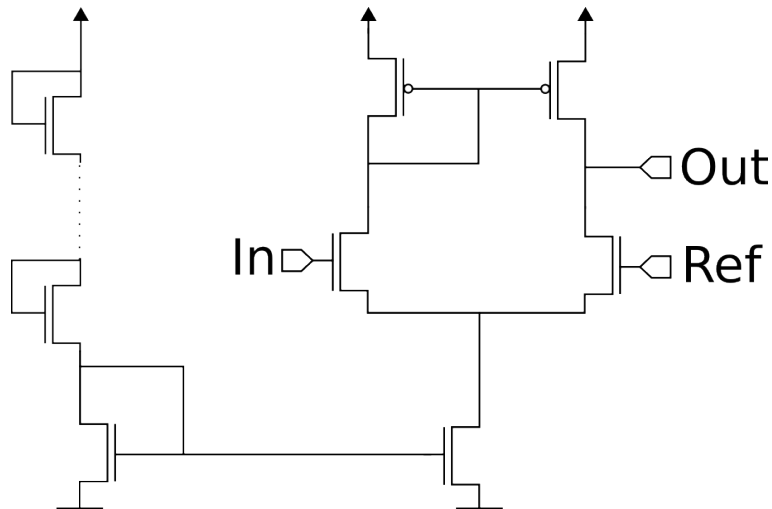


Figure 22: The operational amplifier.

When introducing this amplifier into the circuit it was soon realized that the OP-amp was reacting to much on the really fast voltage changes in the node. This could be solved by using a low pass filter. If the filter is placed on the changing input of the OP-amp it will also draw some current from the interface

state transistors which would affect the measurements. Another idea would be placing it on the OP-amp output which would solve the problem. This was tested with success. Still, since the capacitor needed to achieve this was quite big this solution was not totally satisfactory. Another way to have the amplifiers not react to really fast changes would be having the transistors in the subthreshold region. This was done by adding transistors in diode configuration in the OP-amp bias current generation path. The voltage was then divided evenly between them and the number of transistors determined the voltage at the gates of the transistors in the current mirror, $V_{G,CM} = V_{supply}/n_{trans}$. The threshold voltage of the transistors was known to be between 600 and 700 mV. To be sure that the devices are actually working in subthreshold a voltage about 100 mV smaller would be appropriate to stay clear of possible process variations. Because of this six transistors were used, from which 5 were arranged in series before the input of the current mirror.

To make sure that the OP-amp was not affected by fast changes in the circuit, bode simulations were run. The frequencies where the gain quickly falls can be modulated by adding capacitance on the output. The simulation results are shown in figure 23.

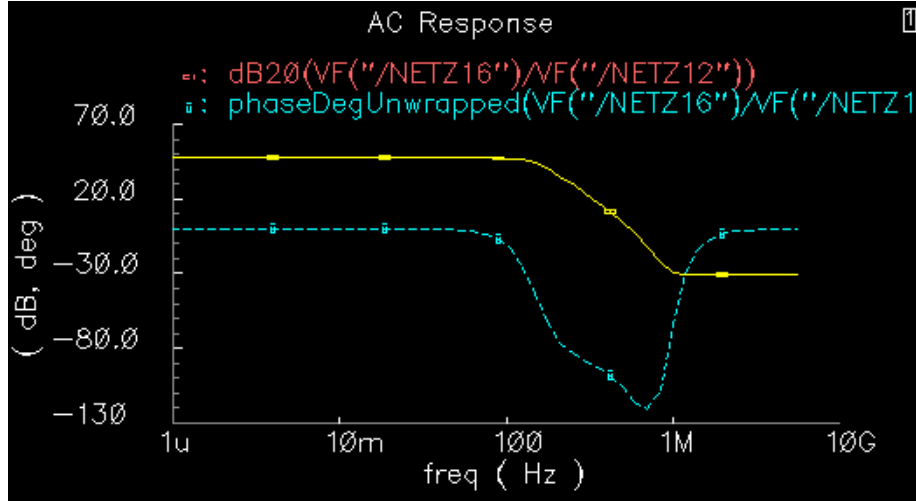


Figure 23: Bode plot of the operational amplifier.

As seen in plot 23, the gain is quite high, around 50dB, at low frequencies. At around 100Hz the gain decreases quickly until it reaches a minimum of approximately -30dB at around 1MHz. This means that the amplifier works as an amplifier with a built in low pass filter. The point where the gain drops can be modified by adding extra transistors at the biasing branch in the amplifier (see figure 22). One could thereby pushing the working point even further into subthreshold which would make the device even slower. Another way to make the amplifier slower would be adding capacitances on the amplifier output.

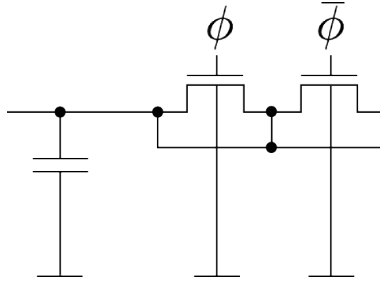


Figure 24: Two transistors with capacitance to prevent high voltage swing at the source-drain node under charge pumping operation.

5.4 Transistors

The transistor function is thoroughly described in chapter 4. When the measurement is run the voltage on the source drain is going to change due to charge and discharge of the transistor channel. To suppress this one can add two really simple parts to this node.

The first and most obvious solution is to add capacitance in this node. The capacitance would work as a buffer for the current and thereby lower the voltage swing. The larger the capacitance the lower the swing.

The second, not as obvious solution, is to add another transistor with the inverse V_{GS} -pulse, see figure 24. Then the current added from transistor one during channel discharge would be drawn from transistor 2 since its channel at that time is being charged. This would also make the interface state current twice the size which would make it easier to measure.

5.4.1 Miller Effect

In figure 25 a rather interesting behavior is shown. The current charging or discharging the transistor channel has a dip in the end of the cycle. This behavior was only observed when the capacitor on the source node of the transistor under test was sufficiently small, around $1pF$. This can be explained using the Miller effect.

To do this the transistors under test will be considered. The transistors are replaced with an equivalent circuit to make current derivation possible, see figure 26. The goal is to get an expression for i_1 depending only on capacitances and $v(t)$ and see how it changes over one cycle.

So, firstly the equations for the different currents are defined using figure 26.

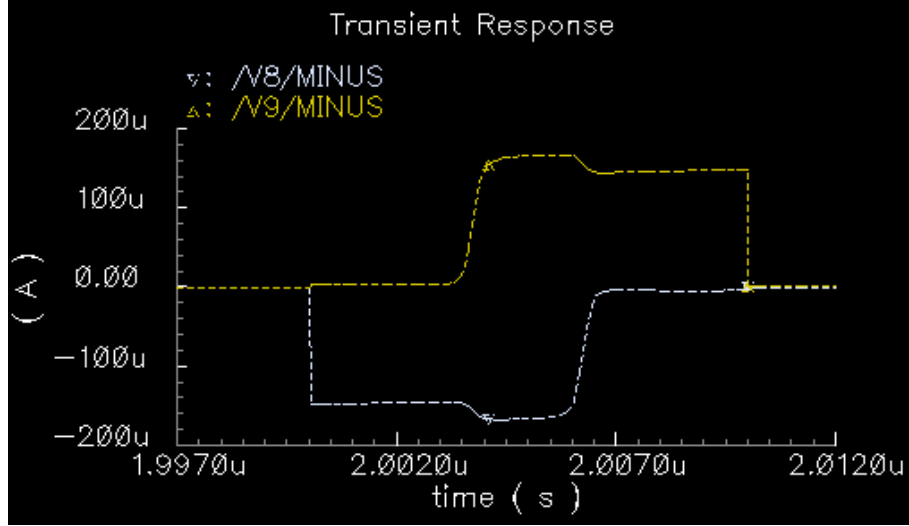


Figure 25: Current measured on the source node of the transistors. The current lowering on the positive current as the negative current approaches zero is caused by the Miller effect. Here $N_{it} = 10^{10} \text{ cm}^{-2}$ and capacitance $D = 1 \text{ pF}$.

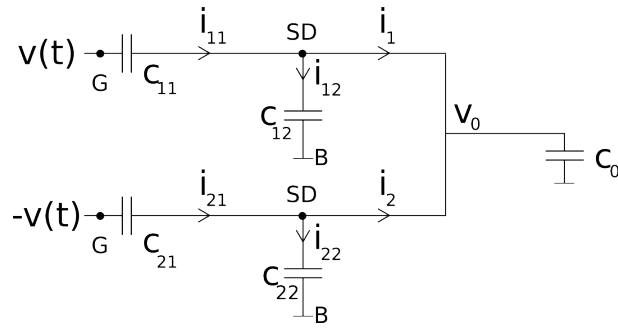


Figure 26: Equivalent small signal circuit of the transistors under test and the capacitance on their source/drain node.

$$i_{11} = C_{11} \frac{d}{dt} (v - v_0) \quad (84)$$

$$i_{12} = C_{12} \frac{d}{dt} v_0 \quad (85)$$

$$i_{21} = C_{21} \frac{d}{dt} (-v - v_0) \quad (86)$$

$$i_{22} = C_{22} \frac{d}{dt} v_0 \quad (87)$$

The second step is to set up equations for i_1 and i_2 .

$$i_1 = i_{11} - i_{12} = C_{11} \frac{dv}{dt} - (C_{11} + C_{12}) \frac{dv_0}{dt} \quad (88)$$

$$i_2 = i_{21} - i_{22} = -C_{21} \frac{dv}{dt} - (C_{21} + C_{22}) \frac{dv_0}{dt} \quad (89)$$

$$(90)$$

To get rid of the factor $\frac{dv_0}{dt}$ two equations for $i_{11} + i_{21}$ are derived, one from the formulas above, and one using the capacitance C_0 .

$$i_{11} + i_{21} = -\frac{dv_0}{dt} (C_0 + C_{12} + C_{22}) + \frac{dv}{dt} (C_{11} - C_{21}) \quad (91)$$

$$i_{11} + i_{21} = i_1 + i_2 + i_{12} + i_{22} = \frac{dv_0}{dt} (C_0 + C_{12} + C_{22}) \quad (92)$$

$$(93)$$

Combining these $\frac{dv_0}{dt}$ can be extracted.

$$i_{11} + i_{21} = -\frac{dv_0}{dt} (C_0 + C_{12} + C_{22}) + \frac{dv}{dt} (C_{11} - C_{21}) = \frac{dv_0}{dt} (C_0 + C_{12} + C_{22}) \quad (94)$$

$$\rightarrow \frac{dv_0}{dt} = \frac{dv}{dt} \frac{C_{11} - C_{21}}{C_0 + C_{12} + C_{22} + C_{11} + C_{21}} \quad (95)$$

Through replacing $\frac{dv_0}{dt}$ in the expression for i_1 the equation

$$i_1 = \left[C_{11} \frac{(C_{11} + C_{12})(C_{11} - C_{21})}{C_0 + C_{12} + C_{22} C_{11} C_{21}} \right] \frac{dv}{dt} \quad (96)$$

A schematic sketch of the simulated results is considered, see figure 27. This is divided into the three phases indicated in the figure, I, II and III. Firstly the capacitances in the three phases are defined. To do this we first define the three different capacitances that needs to be taken into account.

- C_{G-SD} : Capacitance of the extrinsic MOS transistor. Mainly the overlap capacitance between gate and source/drain.

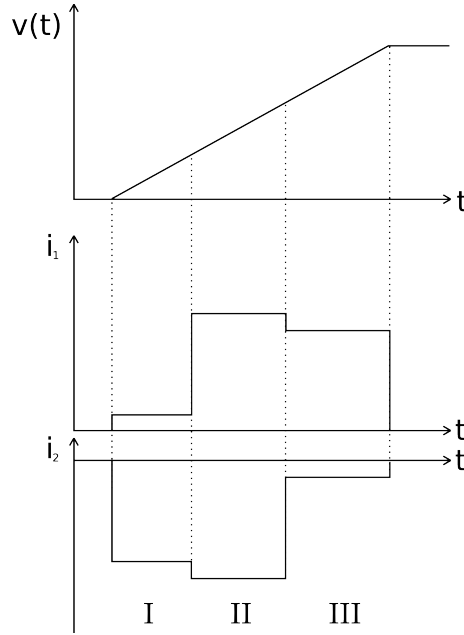


Figure 27: The three different time phases considered in the calculations.

- $C_{G,inv}$: Capacitance of the intrinsic MOS transistor in the region between source/drain and gate.
- C_{SD-B} : The junction capacitance between source/drain and bulk.

For the capacitance between gate and source/drain C_{G-SD} is always present. $C_{G,inv}$ is only present during inversion but is then dominant. The capacitance between source/drain and bulk is always dominated by the junction capacitance C_{SD-B} . Knowing this the capacitances in figure 26 can be replaced with physical capacitances.

- Phase I: T_1 in accumulation and T_2 in inversion:

$$C_{11} = C_{G-SD} \quad (97)$$

$$C_{12} = C_{22} = C_{SD-B} \quad (98)$$

$$C_{21} = C_{G,inv} \quad (99)$$

- Phase II: T_1 and T_2 in inversion;

$$C_{11} = C_{21} = C_{G,inv} \quad (100)$$

$$C_{12} = C_{22} = C_{SD-B} \quad (101)$$

$$(102)$$

- Phase III: T_1 in inversion and T_2 in accumulation:

$$C_{11} = C_{G,inv} \quad (103)$$

$$C_{12} = C_{22} = C_{SD-B} \quad (104)$$

$$C_{21} = C_{G-SD} \quad (105)$$

There C_{G-SD} is the overlap capacitance between gate and source/drain, C_{SD-B} is the joint capacitance between source/drain and bulk. $C_{G,inv}$ is the gate capacitance in inversion. By inserting these values into the expression for i_1 the current in the different stages can be compared.

- Phase I:

$$i_1 = \left[C_{G-SD} - \frac{(C_{G-SD} + C_{SD-B})(C_{G-SD} - C_{SD-B})}{C_0 + C_{G,inv} + C_{G-SD} + 2C_{SD-B}} \right] \frac{dv}{dt} \quad (106)$$

$$(107)$$

- Phase II:

$$i_1 = C_{G,inv} \frac{dv}{dt} \quad (108)$$

- Phase III:

$$i_1 = \left[C_{G,inv} - \frac{(C_{G,inv} + C_{SD-B})(C_{G,inv} - C_{G-SD})}{C_0 + C_{G,inv} + C_{G-SD} + 2C_{SD-B}} \right] \frac{dv}{dt} \quad (109)$$

$$\approx C_{G,inv} \left[1 - \frac{C_{G,inv}}{C_0 + C_{G,inv}} \right] \frac{dv}{dt} \quad (110)$$

A comparison between the expressions for the current i_1 in phase II and III shows the same behavior as observed during the simulations. In phase III i_1 will be smaller than in phase II, with a dependence on C_0 . Because of these results the capacitance C_0 was increased to suppress this behavior.

6 Results

6.1 Transient Behavior

In figure 28 one charging progress of the channel using a high concentration of interface states is shown. The interface state contribution can clearly be seen and has the shape previously defined. The integral of this current over a number of pulses gave the current expected from the calculations in previous sections. After doing this simulation, simulations over longer time periods were done and the input voltage at the comparator was plotted.

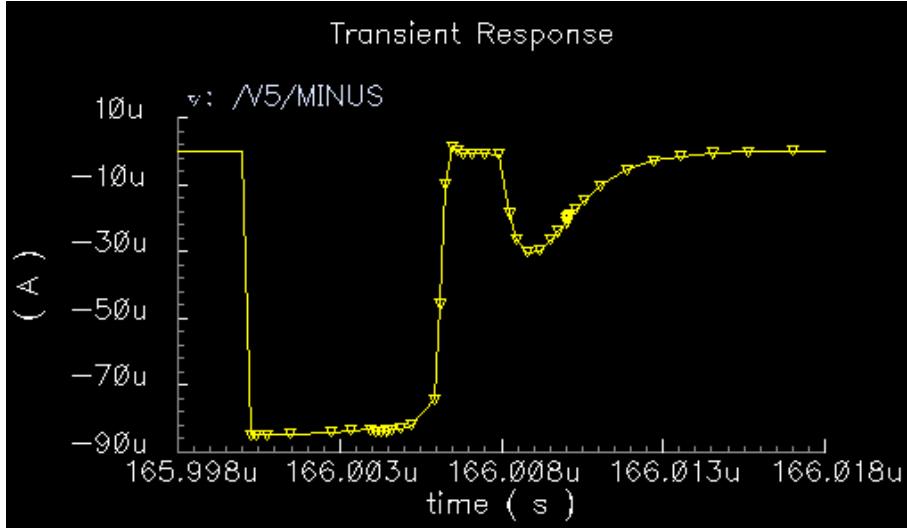


Figure 28: Charging of the channel with the effect from interface states in the worst case scenario, $N_{it} = 10^{12} \text{cm}^{-2}$. The current provided from the interface states can clearly be seen after the channel is charged. Compare to figure 17.

In figures 29 and 30 the voltage on the comparator input node is shown. For the discharge with $N_{it} = 10^{10} \text{cm}^{-2}$, $13.44 \text{ms} - 11.82 \text{ms} = 1.62 \text{ms}$ is needed to lower the voltage from starting voltage to the comparator's reference voltage. In the case of $N_{it} = 10^{12} \text{cm}^{-2}$ the time needed is $1.677 \text{ms} - 1.658 \text{ms} = 0.019 \text{ms} = 19 \mu\text{s}$. In the ideal case the difference between the two would have been exactly a factor 100. The deviation here arises because the number is extracted simply through readouts from the plots, but also because of nonidealities already discussed earlier in the report, for example the fact that the comparator input node only almost reaches the voltages 2.3 V and 2 V.

6.2 Evaluation of Interface State Density

Let's move on and compare these values to the calculated values. First the value $N_{it} = 10^{10} \text{cm}^{-2}$ is used.

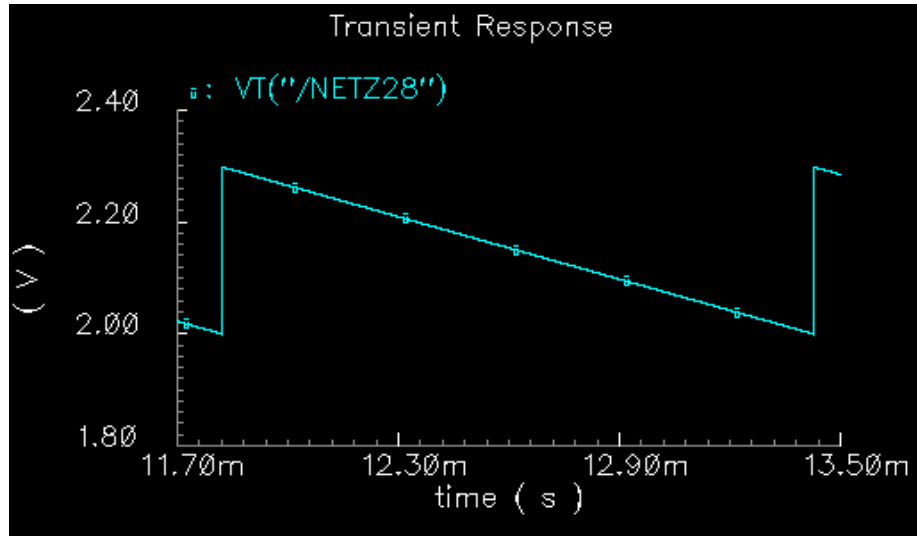


Figure 29: Voltage at the comparator input during one discharge cycle with $N_{it} = 10^{10} cm^{-2}$.

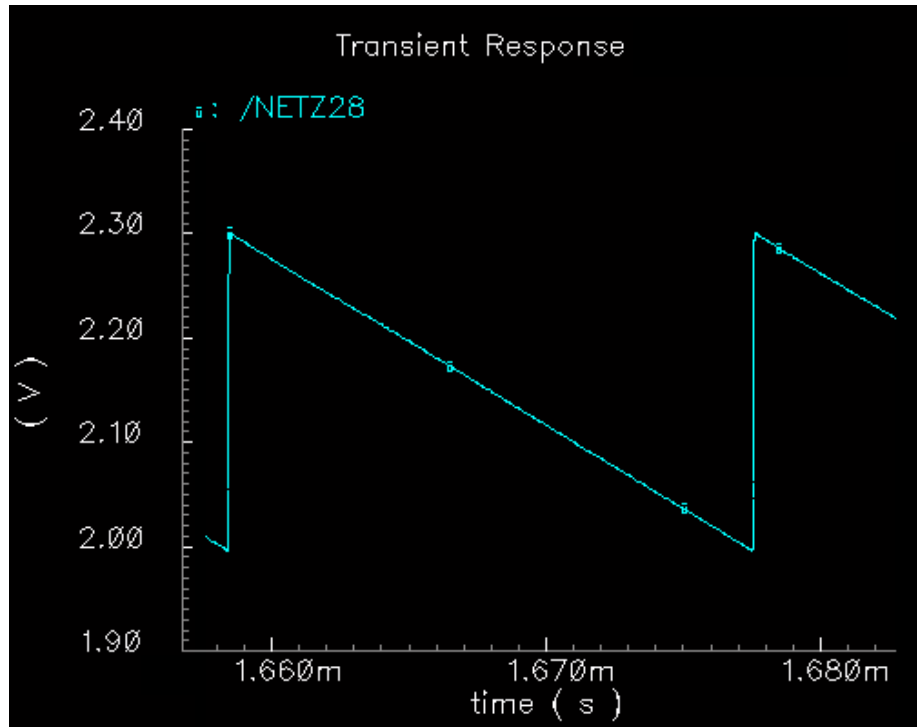


Figure 30: Voltage at the comparator input during one discharge cycle with $N_{it} = 10^{12} cm^{-2}$.

$$Q_{pulse} = LWN_{it}q = 10\mu m \cdot 10\mu m \cdot 10^{10}cm^{-2}1.609 \cdot 10^{-19}C = 1.602fC \quad (111)$$

$$Q_{discharge} = C_{discharge} \cdot \Delta V = 10pF \cdot 0.3V = 3pC \quad (112)$$

$$n_{pulses} = \frac{3pC}{1.602fC} \approx 1870 \quad (113)$$

$$t = \frac{n_{pulses}}{f} = 0.00187s = 1.87ms \quad (114)$$

where n_{pulses} and t are the number of pulses and the time needed for one measurement. For $N_{it} = 10^{12}cm^{-2}$ we should have 100 times less then that, i.e. $1.87\mu s$. According to these calculations the major abbreviation is the case with the least current. A reason for this could be a problem not discussed before which is the fact that these are results of a simulation. The simulations are limited by resolution of the simulator. When these simulations were run the simulator was set to do the simulation as accurate as it could handle. Nevertheless, since the time step can not be made too small, since that would make the simulations impossible to run, a small mistake will always occur.

A way to prove that simulation mistakes were the problem here, is to compare the integral of the current through the drain in the case of only interface state related current with the current through the drain when also charging and discharging of the transistor channels were considered. It was found that the first case gave precise and correct values without any bigger dependencies from simulator settings while the second case was more sensitive. This is because the larger range of currents used in the second range is much harder for the simulator to work with.

In figure 31 a bigger portion of the simulation is shown. One notices that some time is needed for the circuit to actually start measuring the interface states. This is not really a problem since it will only make the measurements a bit slower. After that the circuit starts working and a regular saw tooth shape is created.

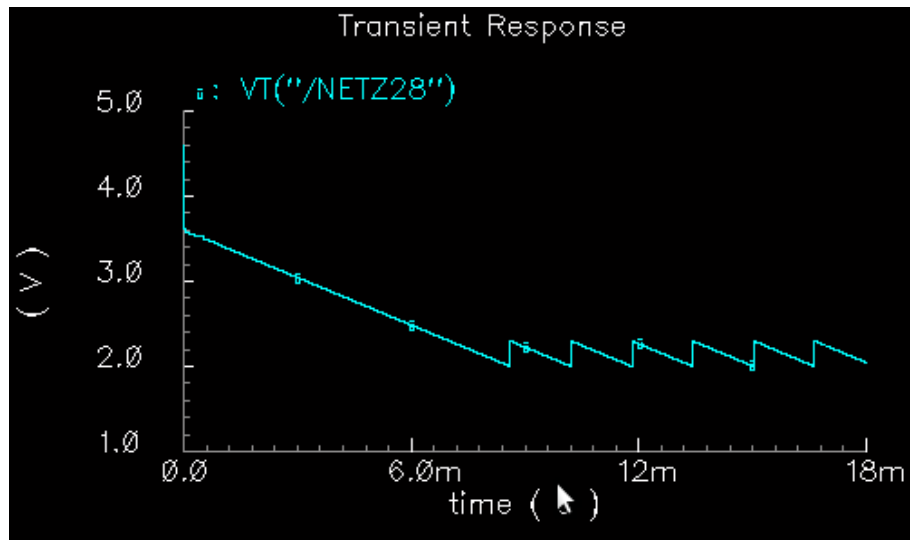


Figure 31: Voltage at the comparator input from simulation start until the circuit stabilizes. $N_{it} = 10^{10} cm^{-2}$

7 Conclusion

As a result of this project a circuit able to measure the interface state concentrations of a device is designed. The goal for this circuit is to be able to differ from interface state densities in the order of $10^{10}cm^{-2}$.

In this report a model usable for simulation of interface states in MOS-devices is created. In the model the current contribution is considered, and an engineering approach is used to give the interface states similar behavior to a capacitor. Also the threshold voltage and the flat band voltage are extracted. These are needed to trigger the charge and discharge of the interface states. This model is then combined with a SPICE transistor model to give full transistor behavior.

In the next part a circuit is designed using the charge pumping technique to measure interface states in MOS transistors. The circuit contains a measuring part with a delay stage, a regulator loop and the actual transistors under test. A number of adaptations are made to make the circuit work properly. Active elements are used to make the simulations more reliable.

References

- [1] P. Heremans, J. Witters, G Groeseneken and H. E. Maes: "Analysis of the Charge Pumping Technique and Its Application for the Evaluation of MOSFET Degradation", *IEEE Trans. Electron Devices*, vol. 36, p. 1318, 1989.
- [2] G. Groeseneken, H. E. Maes, N. Beltran and R. F. Dekeersmaecker: "A Reliable Approach to Charge-Pumping Measurements in MOS Transistors", *IEEE Trans. Electron Devices*, vol. ED-31, p. 42, 1984.
- [3] F. Bechstedt, "Principles of Surface Physics", *Springer, Berlin*, 1st end, 2003.
- [4] W. Shockley, "On the Surface States Associated with a Periodic Potential", *Phys. Rev.*, vol. 56, p. 317, 1939.
- [5] I. Tamm "Über eine mögliche Art der Elektronenbindung an Kristalloberflächen", *Phys. Z. Sowjetunion*, vol. 1, p. 733, 1933.
- [6] Davison S G and Levine J D, "Surface States", *Solid State Phys.* vol. 25, p.1, 1970
- [7] Edwards, Arthur H. "Theory of the Pb center at the $\langle 111 \rangle$ Si/SiO₂ interface", *Phys. Rev.*, vol. 36, p. 9638, 1987
- [8] Colin C. McAndrew and James J. Victory; "Accuracy of Approximations in MOSFET Charge Models", *IEEE Trans. Electron Devices*, vol. 49, no. 1, 2002.
- [9] S. M. Sze, "Physics of Semiconductor Devices", *Wiley-Interscience, New York*, 2nd edn, 1981.
- [10] F. G. Allen and G. W. Gobeli, "Work Function, Photoelectric Threshold and Surface States of Atomically Clean Silicon" *Phys. Rev.* vol. 127, p. 150, 1962.
- [11] E. H. Nicollian and A. Goetzberger, "MOS Conductance Technique for Measuring Surface State Parameters", *Appl. Phys. Lett.* vol. 7, p. 216, 1965.
- [12] I.-C. Chen, C. W. Teng, and D. J. Coleman, "Interface-Trap Enhanced Gate-Induced Leakage Current in MOSFET", *IEEE Electron Device Letter* vol. 10, p. 216, 1989
- [13] T. Hori, "Drain-structure design for reduced band-to-band and band-to-defect tunneling leakage", in Symp. V U I Technol., pp. 69-70, 1990
- [14] T. E. Chang, C. Huang, and T. Wang, "Mechanisms of Interface Trap-Induced Drain Leakage Current in Off-State n-MOSFET's " *IEEE Trans. Electron Devices*, vol. 42, p. 738, 1995.
- [15] R. S. Muller and T. I. Kamins, "Device Electronics for Integrated Circuits.", *Wiley, New York*, ch. 8, 1977.

- [16] S. C. Sun and J.D. Plummer, "Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces", *IEEE Trans. Electron Devices*, vol ED-27, p. 1497, 1980.
- [17] J. G . Simmons and L. S . Wei, "Theory of dynamic charge current and capacitance characteristics in MIS systems containing distributed surface traps", *Solid-State Electron.*, vol. 16, p. 53, 1973.
- [18] Motoyuki Sato, Takayuki Aoyama, Yasuo Nara, and Yuzuru Ohji, "Systematic Study of the Relationship Between 1/f noise, Interface State Defects and Mobility Degradation of High-K /Metal CMOSFETs on (110) And (100) Substrate", *IEEE CFP09RPS-CDR 47th Annual International Reliability Physics Symposium*, p.45, Montreal, 2009
- [19] John H. Scofield, "Physical Basis for Nondestructive Tests of MOS radiation Hardness", *IEEE Trans. Nuc. Science*, vol. 38, p.1567, 1991
- [20] R. Reif, "Fundamentals of Statistical and Thermal Physics", *McGraw-Hill, New York, 1965*, p. 351.