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MASTER OF SCIENCE THESIS

Hardware Implementation of a MIMO-OFDM Channel Estimator based on the Singular Value Decomposition technique

By

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Abstract

This thesis presents fixed point MATLAB® modeling and hardware implementation of a robust Multiple Input Multiple Output – Orthogonal Frequency Division Multiplexing channel estimator using a Singular Value Decomposition technique for frequency correlation of the channel.

Channel estimation has always been an important step at the receiver end in Multiple Input Multiple Output – Orthogonal Frequency Division Multiplexing system to approximate the channel effects. This unit is employed at the receiver end of a mobile device for highly reliable wireless data communication.

A robust channel estimation using the Singular Value Decomposition technique is chosen for the hardware implementation. A fixed point reference model is created using MATLAB® for floating point simulations. An input word-length of 20 bits is used for an Application Specific Integrated Circuit implementation.

The FPGA synthesis is targeted towards a Xilinx Virtex-5 board that provides a frequency of 10.9 MHz. The Application Specific Integrated Circuit design has been targeted towards both a ST 65 nm and a 130 nm UMC CMOS process technology. The power consumption has been simulated using the Primetime® tool.

In the 65 nm CMOS process technology, the high speed synthesis gives a maximum frequency of 50 MHz using an area of 0.107 mm^2 and an average power consumption of 88.2 mW, while low area synthesis provides an area of 0.097 mm^2 at a frequency of 20 MHz.

The low area synthesis for the 130 nm CMOS process technology provides an area of 0.152 mm^2 at a frequency of 15.87 MHz with an average power of 99.98 mW, while the high speed synthesis for 130 nm gives a frequency of 31.25 MHz with an area of 0.207 mm^2.

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Syed Zaki Uddin

Dedication

To my Family!

Table of Contents

CHAPTER 1

1 Introduction

Technology is advancing day-by-day making the world a better place to live in. Better technology provides better standard of living and ease of life. Wireless communication also undergoes a continuous phase of development providing better services. Wireless communication creates great ease of life for everyone by providing access to enormous services on mobile devices. Many exciting services can be accessed by mobile device users when it comes to either mailing, listening songs, watching movies, GPS services, online games and almost everything can be done wirelessly without any need of carrying laptops or computers, you can always have access to the services almost anywhere at any time. These application services on mobile devices requires huge need of high data rates along with reduced Inter Carrier Interference (ICI), Inter Symbol Interference (ISI) and power to provide better services. However, high data rates are restricted due to many factors such as restrictive regulations of spectral bandwidth for service providers, high loss rates due to interferences, high power [1]. These requirements have been successfully achieved by Orthogonal Frequency Division Multiplexing (OFDM) protocol. Further increase in bandwidth efficiency is carried by using MIMO-OFDM technology.

MIMO-OFDM protocol is designed to provide high data rate communication with much reduced ICI and ISI due to orthogonally between each subcarrier in Orthogonal Frequency Division Multiplexing (OFDM) protocol, and increased bandwidth efficiency by using Multiple Input Multiple Output (MIMO) protocol. MIMO-OFDM technology can also be employed in many products such as laptops, wireless modems, etc. to fulfill higher data need. MIMO-OFDM system without channel estimation will provide unreliable data communication due to unknown channel effects such as attenuation, diffraction, refraction, reflection, blocking and scattering from multiple paths. This creates extensive demand on channel estimation techniques at receiver end of mobile link for highly reliable data communication.

Several algorithms have already been developed to perform channel estimation for MIMO-OFDM systems. Different channel estimation techniques are analyzed and compared to choose best possible algorithm. One of the most efficient algorithms developed for hardware implementation is channel estimation using Singular Value Decomposition (SVD) technique. This thesis treats an Application Specific Integrated Circuit (ASIC) implementation of MIMO-OFDM channel estimator using SVD technique, not the complete receiver implementation for MIMO-OFDM system.

1.1 Background

Channel estimation has been strongly needed at the receiver end of mobile links for faithful communication of data over wireless channel. There is always great possibility of research in this field for efficient algorithms, both in terms of complexity and performance. Now-a-days, there are many research activities are being carried out to design low complexity highly reliable channel estimation techniques for future technologies. Channel estimation techniques had started getting attention in late 60's for digital communication systems. [7] [8] presents one of the first Least Square (LS) channel estimation techniques for mobile devices. Least square (LS) channel estimation technique as presented in [11] performs Pilot-signal aided channel estimation, where attenuation is calculated by correlation of the known transmitter reference signals with extraction of reference signals from the received signal. These reference signals, called Pilot signals, are random sequence values inserted at the transmitter end in some fixed arrangement order. They are needed at the receiver end for calculating the attenuation caused by the channel. An LMMSE channel estimation technique provides huge improvement in error calculation at the receiver end. In [12] LMMSE channel estimation by using frequency correlation of the channel is presented. LMMSE Channel estimation in both frequency and time domain is presented in [20], but practical realization of such two dimensional algorithm is too complex. Ye Li [5] proposed an efficient way to perform channel estimation in both frequency and time domain by calculating attenuation independently in time and frequency domain instead of calculating both at the same time. Low complexity based channel estimation techniques are proposed in [2] [5] by transforming LMMSE algorithm into Lower complexity algorithms with the small reduction of accuracy. One of the efficient low complexity channel estimation techniques is the Singular Value Decomposition (SVD) based channel

estimation as discussed in [2]. Singular value decomposition (SVD) channel estimation is used to transforms full length LMMSE algorithm into low complexity algorithm with the help of Singular Value Decomposition technique. This SVD based channel estimation technique proposed in [2] uses frequency correlation of the channel. This technique is considered to be one of the most efficient channel estimation techniques for practical implementation. The SVD channel estimation techniques provides only small amount of errors compensation compared to LMMSE estimator.

With the development of MIMO-OFDM communication system, many SISO channel estimation techniques have been extended to perform channel estimation for MIMO-OFDM system. A MIMO-OFDM channel estimation technique requires $NrxNt$ number of channel estimators concurrently to perform channel estimation, where *Nt* is number of transmitter antennas at the transmitter end and *Nr* is the number of receiver antennas at the receiver end. This will creates huge complexity at the receiver end of MIMO-OFDM system. This complexity at the receiver end can be reduced by using a single channel estimator with a specific pilot arrangement for MIMO-OFDM system. An idea has been presented in [3][4] for MIMO-OFDM system, where the pilots are scattered on each antenna with specific style so instead of performing channel estimation with many channel estimation units, with small loss of performance, estimation can be done using only single channel estimator. Many channel estimation techniques are analyzed and channel estimator is finally implemented using low complexity SVD technique for MIMO-OFDM system.

1.2 Specifications and Requirements

This thesis talks about hardware implementation of MIMO-OFDM SVD channel estimator by using both time and frequency correlation of the channel. The main tasks included for completion of this thesis work are:

- Evaluating different channel estimation techniques.
- Fixed Point MATLAB® simulations to choose best possible word lengths needed to use for hardware implementation.
- Propose hardware architecture for an SVD MIMO OFDM channel estimator.
- Synthesize the design for a Xilinx Virtex-5 board.
- ASIC implementation of hardware architecture for both UMC 130 nm and 65 nm CMOS processing technology.

- Analyzing different design trade-offs in terms of area, speed and power Consumption.

1.3 Organization of thesis

Chapter 2 deals with the theoretical framework of MIMO-OFDM protocol and different channel estimation techniques.

Chapter 3 explains MIMO-OFDM channel estimation using SVD along with its channel; transmitter and receiver characteristics are discussed in this chapter. Theoretical simulations along with conclusions are also presented here.

Chapter 4 discusses the complete hardware architecture and its implementation.

Chapter 5 presents different design Trade-Offs parameters of an ASIC implementation.

The conclusions are discussed in detail in the chapter 6.

Chapter 7 concludes this thesis with discussion on possibilities of future development.

CHAPTER 2

2 Channel Estimation Techniques

This chapter presents theoretical framework for MIMO-OFDM protocol and comparison of different available channel estimation techniques with their complexities and their performances. Section 2.1 describes in detail the theoretical model of MIMO-OFDM system. Section 2.2 presents the Least Square (LS) channel estimation technique followed by detailed study on Linear Minimum Mean Squared Error (LMMSE) estimator in section 2.3. Theoretical framework of SVD channel estimator concludes this chapter in section 2.4.

2.1 *Theoretical MIMO-OFDM systems*

One of the most promising protocols developed to provide high rate data communication is Orthogonal Frequency Division Multiplexing (OFDM) protocol.

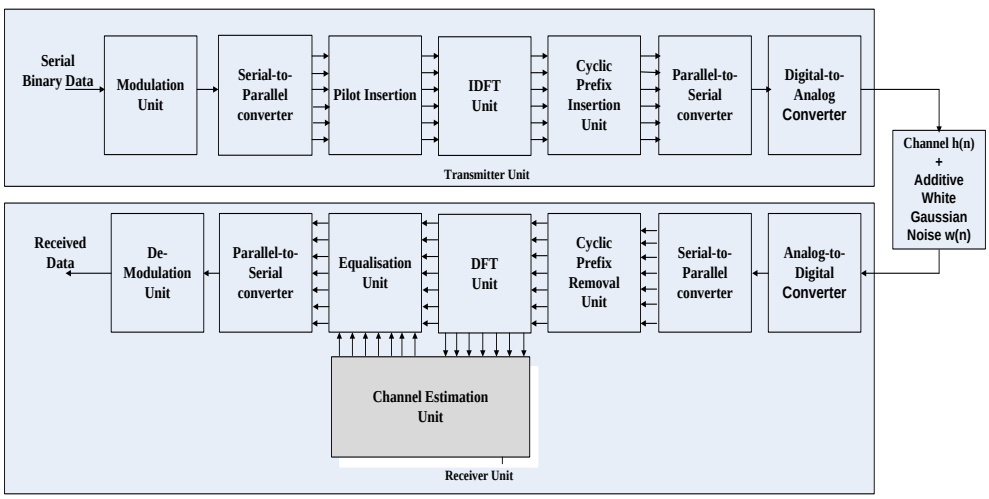

Figure 1.1. Typical Pilot based OFDM system model

An OFDM technology is a wideband digital communication technique used to carry data on orthogonal subcarriers. An OFDM system provides high spectral efficiency and also reduces the Inter-Symbol-Interference (ISI) and

Inter-Carrier-Interference (ICI) at the cost of small extra power and little bandwidth for both wired and wireless communication [6]. Typical OFDM system block diagram is shown in Fig 1.1.

At the transmitter unit, OFDM system consists of a Modulation unit to modulate serial binary information data into specific modulation scheme to produces serial modulated data. Serial modulated data will then be converted to parallel data by using a Serial-to-Parallel converter. This is followed by zero padding along with pilot signal insertion to create an *N*-point vector. The pilot signals are random sequence values inserted at the transmitter end that are needed at the receiver end to perform channel estimation. An Inverse Discrete Fourier Transform (IDFT) unit transform *N*-point vector into a time domain signal vector. This time domain signal vector will then be merged with Cyclic Prefix (CP) to avoid Inter Symbol Interference then followed by Parallel-to-Serial converter unit to convert a generated vector into a Serial Vector. Finally, the signal is passed through a Digital to Analog (D/A) low pass filter and transmitted through an Additive White Gaussian Noise (AWGN) channel.

At the receiver end, an Analog to Digital (A/D) low pass filter will convert the received serial data to a digital data signal. This digital signal is converted to parallel data using a Serial-to-Parallel converter. This parallel data will then pass through Cyclic Prefix (CP) removal unit to remove Cyclic Prefix which was added at transmitter end. The data will then get transformed into a frequency domain with the help of a Discrete Fourier Transform (DFT) unit. Due to fading channel, the received data will be completely distorted by the channel effects. A channel estimation unit is used to calculate distortion caused by the channel, and Equalizer unit is needed to remove the calculated distortion to extract correct information data. This data signal will then pass through a Parallel-to-Serial converter to convert the data stream into serial. Serial data will pass through demodulator unit to extract the serial binary information data [9]. Cyclic Prefix length (CP) is chosen such that OFDM system becomes orthogonal [13].

For an *N* subcarrier system with sub-carrier spacing *(Δf),* the total bandwidth *(B)* will be

$$B \cong N\ x\ (\Delta F) + (Guard\ Band) \quad (1)$$

In order to perfectly perform channel estimation for an OFDM protocol, pilot allocation should follow Nyquist theorem in both time and frequency. Nyquist limit must follow as [6]:

- Coherent time *(Tcoh)* must be greater than pilot spacing in time *(Δt).*
- Coherent Bandwidth *(Bcoh)* must be greater than pilot spacing in Frequency *(Δf).*

The spectral efficiency can be achieved by using OFDM technology along with MIMO system. MIMO is an important element for modern wireless communication standards such as IEEE 802.11n, Wi-Fi and Long Term Evolution (LTE). MIMO-OFDM system uses $NrxNt$ parallel antennas transmitting and receiving data concurrently providing higher data rates and better spectral efficiency but at the cost of extra power [10]. A brief MIMO-OFDM system block diagram is shown in Fig 1.2.

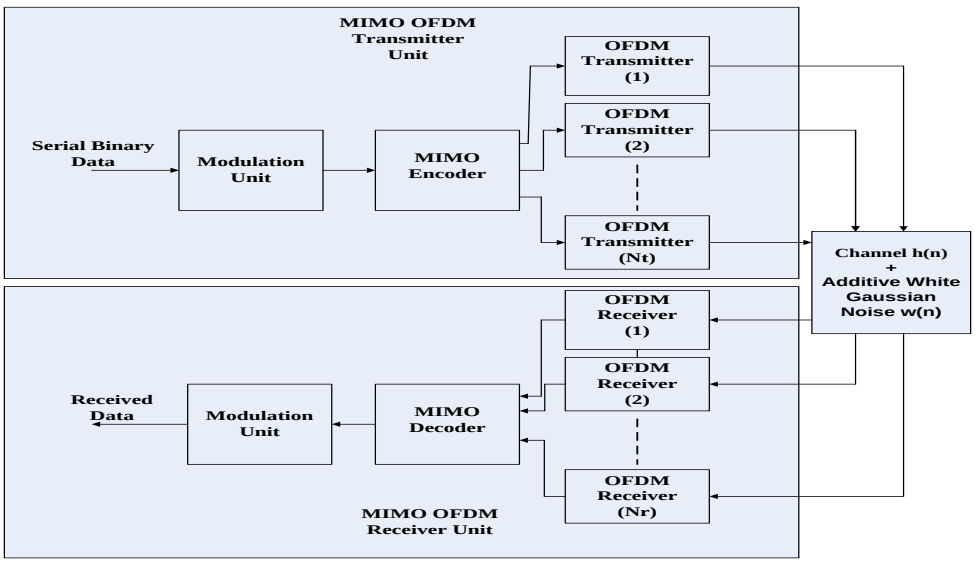

Figure 1.2. MIMO OFDM Baseband model

An $NrxNt$ MIMO-OFDM system consists of *Nt* number of transmitter antennas and *Nr* number of receiver antennas respectively. Each transmitter antenna can be corresponding to an independent OFDM transmitter system and each receiver antenna can be corresponding to an independent OFDM receiver system respectively. Due to different fading paths between

different transmitting and receiving antennas, the receiving antenna receives many replicates of the same signal. This makes the receiver to equip with channel knowledge every time for removing the channel effects from received data and synchronization due to delays [4].

2.2 The Least Square Channel Estimation

Channel estimation is performed by calculating an error using mathematical correlation algorithms. The fundamental algorithm for most of the channel estimation algorithms comes from the theory of the Least Square (LS) channel estimation technique. This LS channel estimator performs estimation by averaging the received pilot data that are arranged in some specific grid of the received signal to the transmitted pilot signal data that are usually known by the receiver. The LS channel estimation is given as (1).

$$h_{LS} = Y_p./X_p \quad (1)$$

Where h_{LS} is the LS channel estimation of the channel, Y_p is the received pilot signal data and X_p is the known pilot signal data.

This estimation technique is easy to implement and has very low complexity but it performs very poor. The Least Square channel estimation is suitable for systems that can have high BER, such as in services like IEEE 802.11n where high BER is negotiable. The Least Square channel estimation technique provides only small improvement in error calculation. Attenuation can be calculated more accurately using advance channel estimation algorithms such as the Linear Minimum Mean Square Error (LMMSE) channel estimation technique. For high data rate services such as LTE and DVB technologies, they requires advanced channel estimation techniques at receiver end to provide highly reliable data communication.

2.3 The LMMSE Channel Estimation

The LMMSE channel estimator provides much accurate channel estimation approximation when compared to the Least Square channel estimation technique. This technique employs calculation of channel effects along with the Least Square channel estimation. This technique shows very good performance but at the cost of too high complexity as it requires NxN

number of complex multiplications for an *N*-subcarriers OFDM system. The LMMSE channel estimation can be formulated as (2).

$$h_{LMMSE} = R_{hh}(R_{hh} + \sigma_n^2(XX^H)^{-1})^{-1}h_{LS} \cong R_{hh}\left(R_{hh} + \frac{\beta}{SNR}I\right)^{-1}h_{LS} \quad (2)$$

Here R_{hh} is the autocorrelation matrix of h, *SNR* is the signal to Noise Ratio used and β is the constant value for modulation techniques. It is 1 for BPSK and 17/9 for QPSK or 4-QAM modulation schemes. This technique provides much better results but generates a huge computational complexity as it includes many inverse operations and multiplication operations. Thus, a low rank approximation is carried out over LMMSE estimator using SVD technique to provide low complexity channel estimator with little reduced quality of estimates.

2.4 The SVD channel estimator

The Singular Value Decomposition channel estimator performs SVD on the LMMSE channel estimator to transform a high computational complexity operation into a low complexity operation. SVD algorithm concentrates the whole distributed energy of a matrix into first few Eigen value of the diagonal vector. Thus, by selecting only first few *k*-values of the diagonal vector, we can ensure that most of the energy of matrix is selected. This will result in a huge computational complexity reduction of the LMMSE channel estimator. By using the SVD channel estimator, complexity was reduced from NxN complex multiplications to only $2xNxK$ complex multiplications while giving almost same performance [2][4]. Moreover, if we fix the *SNR* and R_{hh} correlation Matrix to some known value [4], we can transform (2) to a low complexity Rank-*k* SVD channel estimation h_{KSVD} using frequency correlation of channel as shown in (3).

$$h_{KSVD} = UD_kU^Hh_{LS} \quad (3)$$

Here U is a unitary matrix, D is a diagonal matrix containing singular values on its diagonal vector, $(.)^H$ is the complex conjugate operation. In [2], it was discussed that after rank-*k*, magnitude of singular values on diagonal matrix become too small that it can be neglected without huge loss of accuracy. Since U and U^H are complex conjugate to each other, (3) can be further reduced to (4).

The new rank-*k* SVD channel estimation using the frequency correlation of channel is [4].

$$h_{KSVD} = \left(UD_k^{1/2}\right)\left(UD_k^{1/2}\right)^H h_{LS} \tag{4}$$

In [5], Ye Li has proposed that performing the channel estimation using both the time and frequency correlation of the channel independently will achieve better performance at the cost of little increase in complexity. A time filter *(Wg1)* using time correlation properties of the channel was calculated by Johan Löfgren and used along with the frequency correlation SVD channel estimation technique to achieve better accuracy. This Time-Frequency correlated SVD channel estimation was mathematically expressed as (5).

$$h_{KSVD} = \left(UD_k^{1/2}\right)\left(UD_k^{1/2}\right)^H h_{LS}\, Wg1' \tag{5}$$

A brief SVD based channel estimation system block diagram by using both the time and frequency correlation of the channel is shown in Fig 2.2.

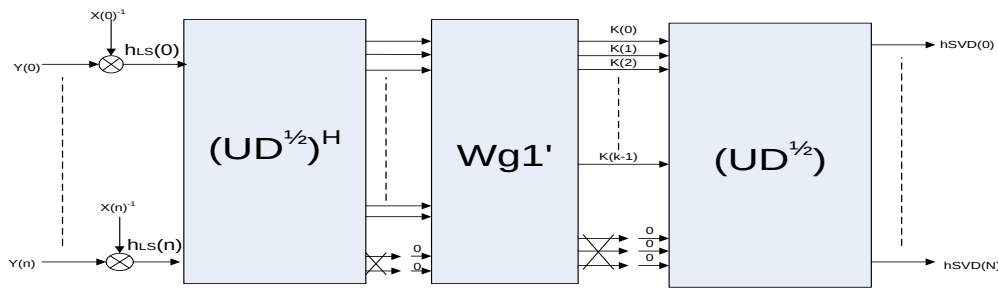

Figure 2.1. Block Diagram of the SVD based Channel Estimator

This Time Frequency correlated SVD based channel estimation technique provides much better BER that it is too reliable to be used for practical implementation.

CHAPTER 3

3 Robust Channel Estimator

This chapter discusses the complete theoretical simulation model used in the designing of a robust SVD channel estimator for an MIMO-OFDM system. Section 3.1 discusses the theoretical framework of a robust SVD channel estimation technique for an MIMO-OFDM system. In section 3.2, we present the system characteristics used for the theoretical simulations. The results obtained in the MATLAB® reference model simulations are discusses in section 3.3. This chapter is concluded with a discussion on fixed point simulation results obtained from MATLAB® in section 3.4.

3.1 *Robust SVD channel estimation for MIMO-OFDM system*

The robust channel estimation techniques are strongly needed at the receiver end of an MIMO-OFDM system to remove the ISI effects caused by the fading channels, and for successful high data rate communication. The high data rate multimedia services can be successfully implemented only if the receiver can decode the correct information from the received data. Since the channel changes continuously over time, the wireless digital communication systems using the coherent modulation schemes such as Quadrature Amplitude Modulation (QAM) and Quadrature Phase Shift Keying (QPSK) generally requires an effective channel estimation techniques at the receiver end [4]. For an MIMO-OFDM system, there will be $NrxNt$ complex frequency fading paths between the transmitter and the receiver as shown in Fig 3.1(a), where *Nt* is the number of antennas at the transmitter end and *Nr* is the number of the antennas at the receiver end of an MIMO-OFDM system respectively. The differential demodulation scheme can be used in the MIMO-OFDM system to remove the need of a channel estimator, but this will results in huge loss of 3-4 dB in Signal-to-Noise Ratio (SNR) as explained in [5]. An idea of using single channel estimator for an MIMO-OFDM system by Johan Löfgren as presented in [3][4] has hugely reduced the complexity of the channel estimation units. The pilot signals are arranged in specific way that for a given time and

frequency, only one antenna is transmitting and all other antennas are idle as shown in Fig 3.1(b).

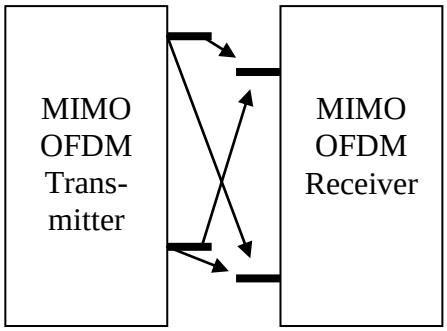

Figure 3.1(a). Different Fading paths between MIMO-OFDM transmitter and receiver

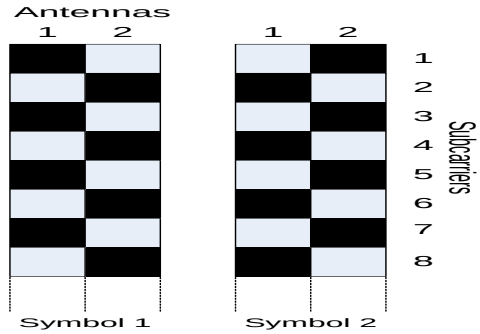

Figure 3.1 (b). Pilot arrangement using single estimation unit for MIMO-OFDM System

In wireless communication links, the channel changes too fast that designing a channel estimator for fixed environment such as Indoor, Outdoor, Urban and Sub-urban is not robust. The channel estimation techniques designed for worst case scenario is robust to be used for any kind of environment as studied by Ye Li in [5]. Such robustness is always needed for designing the reliable data communication systems for future technologies. Performing the channel estimation for an MIMO-OFDM system on all the receiver antennas concurrently will create a huge complexity at the receiver end. Such channel estimation techniques also requires high Signal to Noise Ratio (SNR) to work properly. This means that these channel estimation techniques works well only for a low data rate systems. The SVD based channel estimation technique as presented in [4] performs the channel estimation by using a single channel estimator unit for an MIMO-OFDM system. This technique has reduced huge complexity and provides much better Bit-Error-Rate (BER) ratio. Arranging the two pilot signals on start of each burst as shown in Fig 3.1.(b) creates the possibility of using only a single channel estimator for MIMO-OFDM system. Since, only a single antenna is the transmitting pilot signal at a given time and frequency, single channel estimator can be used for an MIMO-OFDM system. In Fig. 3.1.(b), black squares represent the pilot symbols transmitted at a given time and frequency, while white squares correspond to antenna is quite at that given time and frequency. In [4], Johan Löfgren discusses the SVD based channel estimation technique for an MIMO-OFDM system by using only frequency domain correlation of the

frequency selective fading channel. This work has been extended for both frequency and time correlation using the frequency response of a time dispersive channel. This channel estimation technique uses the Weiner FIR filters individually in both time and frequency directions. This MIMO-OFDM channel estimator uses a single Time Frequency correlated SVD channel estimator along with specific pilot arrangement. This pilot structure ensures that there should be only one antenna transmitting pilot data at the given time and frequency. This creates only single channel estimation unit sufficient to estimate channel for whole MIMO-OFDM system without extra need of channel estimation units.

3.2 *Theoretical Simulation Model*

A MIMO-OFDM System with only a single Time-Frequency correlated SVD channel estimator is analyzed for simulations. An MIMO-OFDM system with $Nt = 2$ number of transmitting antennas and $Nr = 2$ number of receiving antennas were used. As each antenna corresponds to one OFDM system, we used $N = 64$ subcarriers for each OFDM system with a cyclic prefix of $L = 8$. Cyclic Prefix was chosen sufficiently larger than the channel impulse response so that the orthogonally between the subcarriers in each OFDM system should not break [4]. Binary Phase Shift Keying (BPSK) modulation scheme was used. Moreover, simulations was carried out with robust factors such as *SNR* is chosen to be maximum and power delay profile is selected to be uniform so that the calculated parameters should be valid for worst case scenario. The system is considered to be full rate with each transmitting antennas transmits data independently. Moreover, antennas are decoupled completely so that it can be considered independently [19].

Due to multiple antennas at transmitting and receiving antennas in an MIMO-OFDM system, there will be $NrxNt$ different fading paths between the transmitting and receiving antennas. Factors such as, reflection, refraction, diffraction and attenuation creates reception of transmitted data signals at the receiver end with different magnitudes and with different delays for each antenna system. The Channel Impulse response of such a system was mathematically expressed as (6).

$$G_{i,j}(\tau) = \sum_{n=1}^{R} \alpha_{n,i,j} . \delta(T - \tau_{n,i,j}) \quad (6)$$

The frequency response of the channel was obtained by performing a Discrete Fourier Transform (DFT) over the time domain channel impulse response as (7).

$$h(k) = DFT\big(Gi,j(\tau)\big) = \sum_{l=0}^{N-1} \sum_{n=1}^{M} \alpha_n . \, e^{-j2\pi \frac{K}{N} \tau_n} \qquad (7)$$

3.3 *Simulation Model and Results*

Different channel estimation techniques are analyzed for complexity computation and Bit-Error-Rate (BER) performance as shown in Fig 3.2. For a 2x2 MIMO-OFDM system with N = 64 subcarriers, the LS channel estimation technique requires a $NxNrxNt$ complex multiplication operations. However, the LS channel estimator provides a high Mean Squared Error (MSE) that gives a very low accuracy. The LMMSE channel estimator requires a computation complexity of $NxNxNrxNt$ complex multiplications that makes it very complex. The LMMSE channel estimation has a low MSE that provides high accuracy but at the cost of a huge complexity. The SVD channel estimator, using both time and frequency correlation, provides low complexity of only $2xkxNxNrxNtxW$ complex multiplications while providing better MSE than LMMSE estimator. Here W is the number of time filter coefficients. This makes it perfectly suitable for practical implementation.

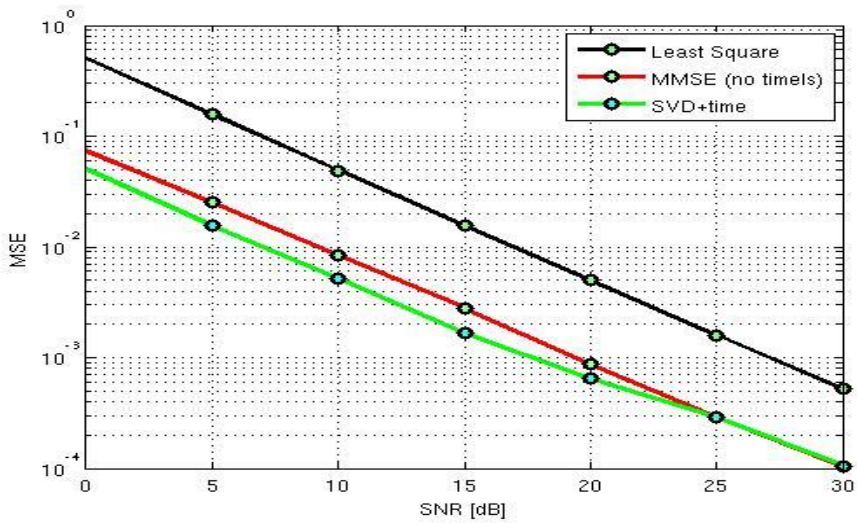

Figure 3.2 The MSE performance vs. the SNR

Finally, the channel estimation technique using SVD is chosen for the hardware implementation.

3.4 *Fixed point MATLAB® Model*

The fixed point model of SVD based algorithm is analyzed for calculating word-lengths required in hardware implementation as shown in Fig 3.3. Choosing an input word-length of 16 bits (8 bits for Real, 8 bits for Imaginary) gives too high MSE. This results in high Bit Error Rate (BER) for high SNR values. Input word-length of 20 bits (10 bits for Real, 10 bits for Imaginary) provides close enough performance compared to the ideal case. Full accuracy with input word-length of 24 bits (12 bits for Real, 12 bits for Imaginary) gives exact performance compared to ideal case. Additional 4 bits in 24 bits input word-lengths compared to 20 bits input word-lengths create huge hardware complexity.

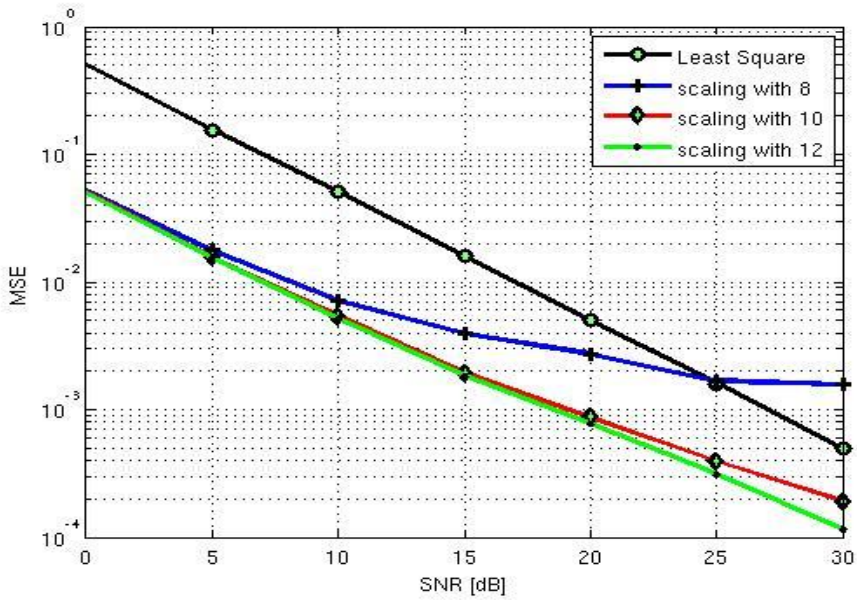

Figure 3.3 Fixed point simulation results

Fixed point simulation results are compared and input word-length of 20 bits (10 bits for real and 10 bits for imaginary) is chosen for the hardware implementation.

CHAPTER 4

4 ASIC Implementation

This chapter summarizes complete ASIC implementation of the proposed SVD algorithm with 20-bits input word-length. Section 4.1 describes the complete hardware design flow followed in this thesis. Section 4.2 discusses the complete architecture with a block diagram. Section 4.3 concludes this chapter with the complete details of the components used in the designed module.

The hardware implementation of the MIMO-OFDM channel estimator based on the SVD technique, by using both time and frequency correlation of the channel, is used for hardware implementation. There has been many channel estimation techniques already analyzed for an MIMO-OFDM system but there are only a few ASIC implementations of these channel estimation algorithms.

4.1 Hardware Design Flow

This section describes the design flow followed throughout the thesis dissertation. The computer simulations are carried out using MATLAB® tool. Comparison of different available channel estimation techniques and a fixed point model is created using MATLAB® tool. Designing and simulation of hardware unit is carried out using Modelsim® tool. The gate level synthesis is performed by using Synopsys Design Vision® tool for both ST 65 nm and 130 nm UMC technologies. The FPGA synthesis has been carried out on a Xilinx ISE® with module targeted toward a Virtex-5 board. Finally, the power results are measured using the Primetime® tool. A 20 bit word-length for the input and an output of 22 bits are chosen. The complete hardware design flow is shown in Fig 4.1.

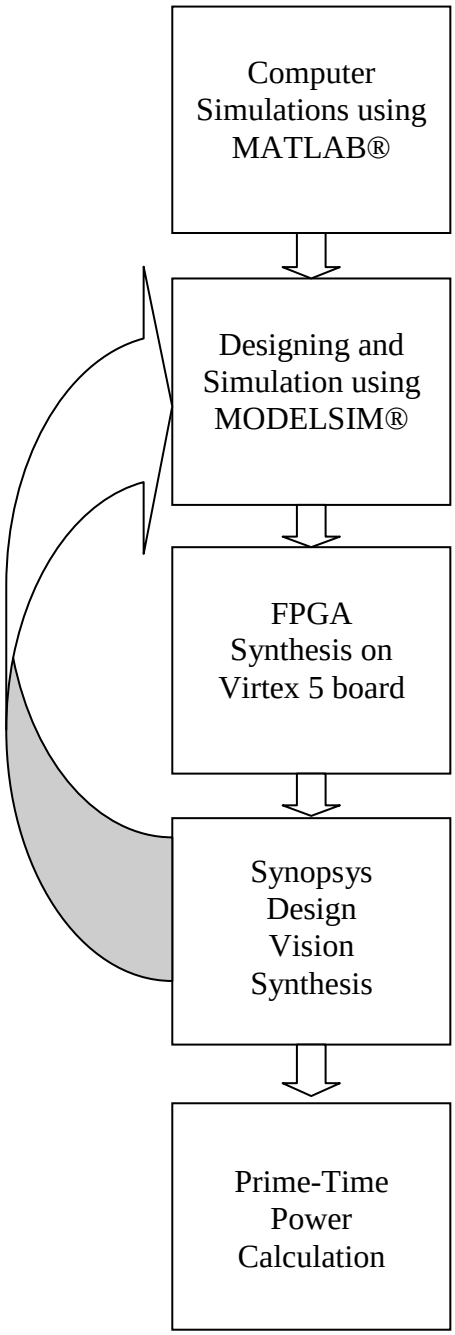

Figure 4.1 The Hardware Design Flow

4.2 Hardware architecture

This section describes complete hardware architecture used in this thesis for the ASIC modeling. The complete hardware architecture designed here is a time-multiplexed unit that runs in three different states. These three states are termed as Phase1, Phase2 and Phase3. Sub-section 4.2.1 discusses the Phase1 operation of the design, whereas Phase2 time filtering is discussed in sub-section 4.2.2. This section concludes with discussion on Phase3 operation of the designed module.

4.2.1 The Phase1 Operation

This state is used to calculate the matrix multiplication of $(UD^{1/2})^{H}$ matrix with the Least Square channel estimates. $UD^{1/2}$ ROM unit consists of a Conjugate Unit to give the complex conjugate values of the stored elements needed for matrix multiplication. Calculation of first product requires 192 CC that are generated and are controlled with the help of the control unit. Since, there are only 4 complex multipliers used for the hardware implementation. A matrix multiplication of $(UD^{1/2})$ Rom Unit (12x64) with Least Square channel estimates for single antennas (64x1) requires 192 clock cycles to perform the complete matrix multiplication. The complex multiplication results are added with the 4 previous values that are stored on the 12 42-bit delay elements. When all 64 Least Square channel estimates are multiplied with the $(UD^{1/2})^{H}$ matrix, the resulting 12 values are rounded and saved in the intermediate registers REG. The block diagram of Phase1 operation is shown in Fig 4.2.

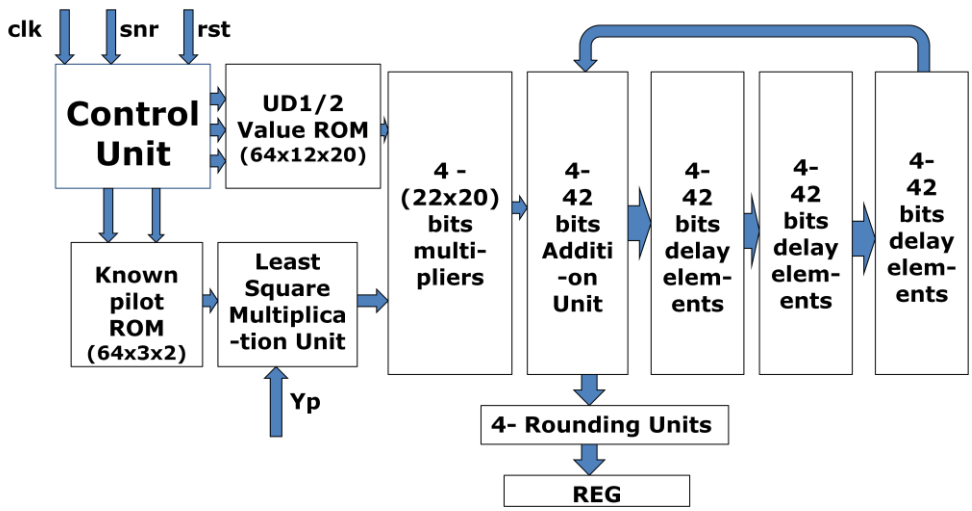

Figure. 4.2. The Phase1 operation of the Hardware Unit.

4.2.2 The Phase2 Operation

This phase is needed to perform time filtering of Phase1 results. The values generated from Phase1 are stored in intermediate registers REG. These three intermediate register values are then multiplied with the time filter coefficient ROM to produce Phase2 results. The filter design has been folded in order to reduce the number of required complex multiplications from 36 to 24. The folding of the filter is also advantageous in reducing the number of clock cycles from 12 to 6. The Phase2 operation block diagram for one value update is shown in Fig. 4.3.

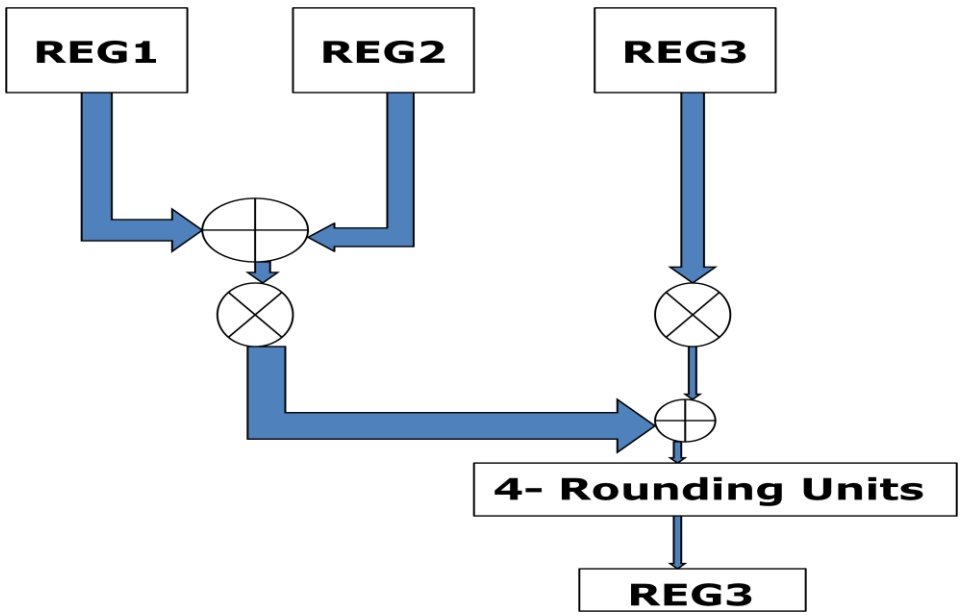

Figure. 4.3. The Phase2 operation of the Hardware Unit.

4.2.3 The Phase3 Operation

This phase also runs for 192 clock cycles to produce the final product of the $UD^{1/2}$ Rom unit with the Phase2 results. On every 3rd clock cycle of Phase3, one output SVD channel estimate is calculated and sends to the output port of an ASIC. The block diagram for Phase3 is shown in Fig. 4.4.

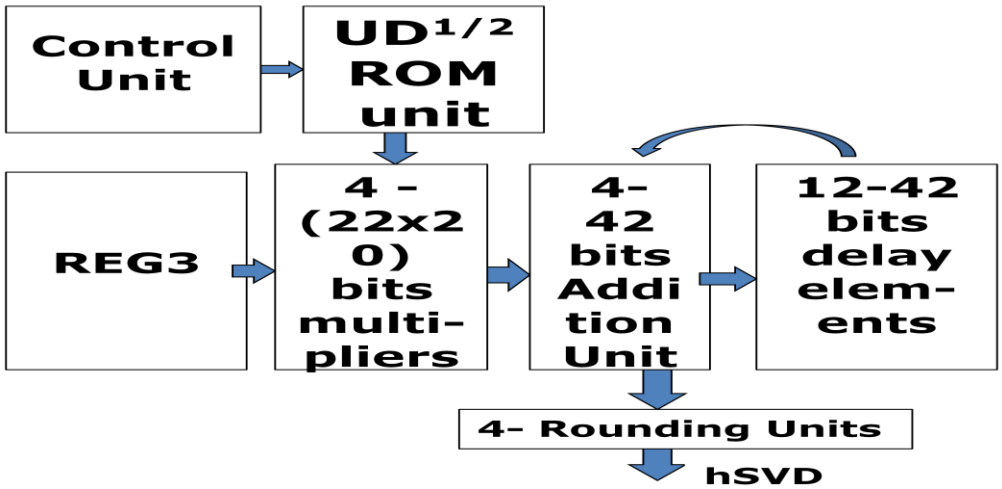

Figure. 4.4. The Phase3 operation of the Hardware Unit.

Moreover, a control signal of Signal to Noise Ratio (SNR) is used in hardware design to reconfigure the whole system to either perform both time and frequency correlation of the channel or only frequency correlation of the channel. When SNR is too large, only frequency correlation of channel is carried out otherwise channel estimation is calculated using both frequency and time correlation of channel.

4.2.4 Components used

The complete components used in an ASIC implementation are discussed in this section. The complete list of components used is

1) The control Unit.
2) The Least Square multiplication unit.
3) 4 – (20x22 bit) Complex multiplication unit.
4) Read Only Memories.
5) 4 – (42 bit) Complex addition unit.
6) 12 – (42 bit) Delay elements.
7) 4 - Rounding unit.
8) Multiplexer's.

4.2.4.1 The Control Unit

The control unit is the main unit in the whole design. It is needed to control the whole operation by generating the control counter signals. These control

signals are required to perform appropriate operation for that given instance of time. In addition to counter signals, there is also a phase signal generated by the control unit to select the module to work in a desired state. The state diagram of the control unit is shown in Fig. 4.5.

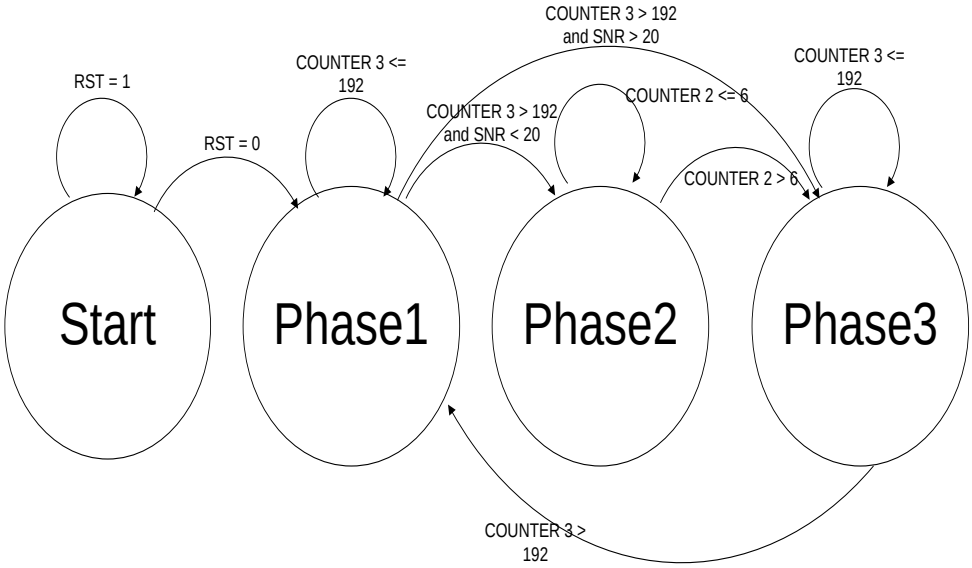

Figure. 4.5 The state diagram of the Control Unit.

The detailed state machine is given in Fig. 4.5. This state machine is generating three counter signals called as Count1, Count2 and Count4. The Count1 counter signal is needed in both the Phase1 and the Phase3 to select the first index value for the $UD^{1/2}$ ROM unit, the Pilot ROM, and the indexes for the delay elements. The Count2 counter signal is used to select the desired row elements of the $UD^{1/2}$ ROM unit and the Pilot ROM unit. The control counter signal Count4 is used to select the desired column value for the $UD^{1/2}$ ROM unit and the Pilot ROM unit. The phase signal is generated to select the desired working phase for the hardware module. The ready_out signal will assert high whenever data is ready to send to the output port (hSVD) of an ASIC. The SNR control signal will control the phase transition. If the SNR is too high, the phase signal will move directly from Phase1 to Phase3. Otherwise, the phase signal will be changed from Phase1 to Phase2 state.

4.2.4.2 The Least square Multiplication Unit

The Least Square multiplier designed here performs the complex multiplication operation of the Pilot ROM with the received data *(Y_p)*. The complex multiplication is performed by using only multiplexing, addition and subtraction unit. The truth table used for the Least Square multiplication unit is given as in TABLE 4.1. Here, Y_{real} is the real part of the received data Y_p and Y_{imag} is the imaginary part of the received data Y_p.

Table 4.1. The Least Square Multiplication

Known Pilot (-1 for 1, 1 for 0)	Out_Real	Out_Imaginary
00	$(Y_{real}-Y_{imag})$	$(Y_{real}+Y_{imag})$
01	$(Y_{real}+Y_{imag})$	$-(Y_{real}-Y_{imag})$
10	$-(Y_{real}+Y_{imag})$	$(Y_{real}-Y_{imag})$
11	$-(Y_{real}-Y_{imag})$	$-(Y_{real}+Y_{imag})$

4.2.4.3 Read Only Memories

1) Pilot ROM

The Pilot ROM is used to store the known pilot signal values. Since a BPSK modulation scheme is employed in this thesis, there could be only two possible values to store, i.e., either -1 or +1. Instead of using two bits values to store for each real or imaginary value, -1 is considered as 1 and +1 is considered as 0. This technique will reduce the size of the memory. Now, we need to store only 384 bits instead of 768 bits.

2) $UD^{1/2}$ value ROM Unit

This ROM unit stores 15360 bits. It also consists of a conjugate unit that gives complex conjugate values of the $UD^{1/2}$ ROM content in Phase1 and original values of the $UD^{1/2}$ ROM in Phase3.

3) Time Filter Coefficient ROM

This ROM is used to store the time filter coefficients.

4.2.4.4 The Complex Multiplication Unit

The complex multiplication unit is designed using a strength reduction algorithm. The strength reduction algorithm is an efficient way to calculate a complex numbers multiplication with much lower hardware complexity. Instead of performing a normal complex multiplication that requires 4 multiplication units and 2 adder units, the strength reduction algorithm requires only 3 multiplication units and 5 adder units. The strength

reduction algorithm is given in (4.1) [21]. A brief diagram of the strength reduction complex multiplier is shown in Fig. 4.6.

$$(a + jb)(c + jd) => Re = a(c - d) + d(a - b);\ Im = b(c + d) + d(a - b) \qquad (4.1)$$

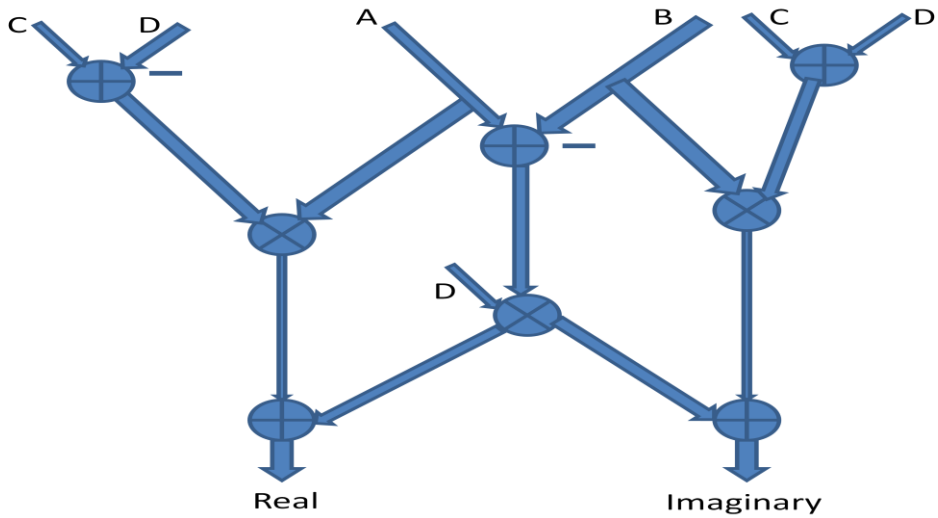

Figure. 4.6. Complex multiplication using the strength reduction algorithm.

4.2.5 Delay Units

In this design, we need a total of 12 42-bit delay elements to store the intermediate results until complete phase operation is done.

4.2.6 Rounding Units

A rounding unit is used to round the input values depending upon the received fractional part. If the fractional part is greater than 500, it will add 1 to the real value otherwise it will not add 1 to it.

4.2.7 Complex Addition Unit

In this design, we need a total of 4 42–bit full adder addition units to add the intermediate values.

Other small signals and multiplexer units are used for correct operation of the hardware module. The control unit is designed in a specific way that it will select the correct values and operation of the ASIC design.

CHAPTER 5

5 Implementation results

This chapter discusses the results obtained in an implementation of the hardware module. Section 5.1 discusses the results of synthesis for the ST 65 nm and the UMC 130 nm CMOS process technology. The results obtained in the FPGA synthesis are presented in section 5.2. This chapter is concluded with power simulation results in section 5.3.

5.1 Implementation results and Design Trade-Offs

The designed module has been targeted toward both the ST 65 nm and the UMC 130 nm CMOS process technology library for both the high speed and the low area synthesis. The final results obtained in the ST 65 nm technology for the high speed synthesis are tabulated in Table 5.1.

TABLE 5.1. High speed synthesis results for the 65 nm CMOS technology

Parameters	Parameter values
Maximum Clock Frequency (MHz)	50
Combinational Area (mm^2)	0.084
Non-Combinational Area (mm^2)	0.023
Total Area (mm^2)	0.107

The results obtained for low area synthesis in the ST 65 nm CMOS process technology are tabulated in Table 5.2.

TABLE 5.2. The low area synthesis results for the ST 65 nm CMOS technology

Parameters	Parameter values
Maximum Clock Frequency (MHz)	20
Combinational Area (mm^2)	0.074
Non-Combinational Area (mm^2)	0.023
Total Area (mm^2)	0.097

High speed synthesis results in the UMC 130 nm CMOS process technology are tabulated in the Table 5.3. It gives a maximum clock frequency of 31.25 MHz for an area of 0.207 mm^2.

TABLE 5.3. The results obtained in 130 nm technology for high speed synthesis

Parameters	Parameter values
Maximum Clock Frequency (MHz)	31.25
Combinational Area (mm^2)	0.169
Non-Combinational Area (mm^2)	0.038
Total Area (mm^2)	0.207

Table 5.4 presents the low area synthesis results obtained in the UMC 130 nm CMOS process technology. It provides an area of 0.152 mm^2 at a maximum clock frequency of 15.87 MHz.

TABLE 5.4. The 130 nm CMOS process technology results for low area synthesis

Parameters	Parameter values
Maximum Clock Frequency (MHz)	15.87
Combinational Area (mm^2)	0.114
Non-Combinational Area (mm^2)	0.038
Total Area (mm^2)	0.152

5.2 FPGA Synthesis

The FPGA synthesis is targeted towards a Virtex-5 board. The maximum achievable clock frequency from the FPGA simulations is 10.9 MHz. The Table 5.5 presents resources utilization in the FPGA Synthesis.

TABLE 5.5. The FPGA synthesis results

Name of the device	Device utilization	Percentage Used (%)
Number of Slice Registers	1370 out of 19200	7
Number of Slice LUTs	4479 out of 19200	23
Number of bonded IOBs	51 out of 220	23
Number of fully used LUT-FF pairs	406 out of 5443	7
Number of DSP48Es	12 out of 32	37

The critical path obtained along with the timing summary is reported in Table 5.6.

TABLE 5.6. The FPGA timing results

Timing Parameters	Parameter values
Minimum period (ns)	91.774
Maximum Frequency (MHz)	10.896
Minimum input arrival time before clock (ns)	0.929
Maximum output required time after clock (ns)	2.775
Maximum combinational path delay (ns)	No path found
Speed Grade	-3

5.3 Power Consumption

The power consumption has been estimated for both the technologies using the Prime Time® tool. The power results obtained for the high speed synthesis in the 65 nm CMOS process technology are tabulated in the Table 5.7.

TABLE 5.7. The power consumption results for the 65 nm CMOS process technology

Parameters	Parameter values
Clock Period (ns)	20
Combinational Power (mW)	26.65
Non-Combinational (mW)	61.59
Total Power (mW)	88.24

The power results obtained for the high speed synthesis in 130 nm CMOS process technology are tabulated in Table 5.8.

TABLE 5.8. The 130 nm CMOS process technology power estimated results

Parameters	Parameter values
Clock Period (ns)	32
Combinational Power (mW)	31.87
Non-Combinational (mW)	68.11
Total Power (mW)	99.98

CHAPTER 6

6 Conclusions

The computer simulations are carried out to compare different channel estimation techniques for an MIMO-OFDM system. An SVD channel estimation technique, by using both time and frequency correlation of the channel, is chosen for the hardware implementation. The fixed point MATLAB® simulation shows that an input word-length of 20 bits is suitable for the hardware implementation. The design has been simulated using the MODELSIM® tool and the obtained results match with the MATLAB® reference values perfectly. The FPGA emulation has been carried out using a Xilinx Virtex-5 board that achieves a maximum clock frequency of 10.9 MHz.

The hardware module has been mapped onto both the ST 65 nm and the UMC 130 nm CMOS process technologies. For the 65 nm CMOS process technology, a high speed synthesis gives a maximum clock frequency of 50 MHz using an area of 0.107 mm^2, while the low area synthesis provides an area of 0.097 mm^2 at a clock frequency of 20 MHz. In the 130 nm technology, the high speed synthesis results in a maximum clock frequency of 31.25 MHz with an area of 0.207 mm^2. The low area synthesis results in a maximum clock frequency of 15.87 MHz with an area of 0.152 mm^2. The design has been successfully implemented for both the technologies.

CHAPTER 7

7 Future Work

There has been many different channel estimation techniques already analyzed but only few hardware implementations of channel estimation techniques are reported.

The low complexity channel estimation algorithms are strongly needed to be analyzed for higher throughput and practical implementation in future technologies.

There is a strong need of improved algorithms to perform channel estimation for MIMO-OFDM concurrently on all the antennas.

Moreover, efficient complex multiplication algorithms are desired to reduce the huge area and to provide a high throughput in ASIC implementations.

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List of Figures

List of Tables

List of Acronyms (Not necessary)

MIMO	Multiple Input Multiple Output
OFDM	Orthogonal Frequency Division Multiplexing
SVD	Singular Value Decomposition
IEEE	Institute of Electrical and Electronics Engineers
ASIC	Application Specific Integrated Circuit
FPGA	Field-Programmable Gate Array
LTE	Long Term Evolution
DVB	Digital Video Broadcasting
WiMAX	Worldwide Interoperability for Microwave Access
HSPA+	Evolved High-Speed Packet Access
ICI	Inter Carrier Interference
ISI	Inter Symbol Interference
VLSI	Very Large Scale Integration
BER	Bit Error Rate
AWGN	Additive White Gaussian Noise
BPSK	Binary Phase Shift Keying
CP	Cyclic Prefix
DFT	Discrete Fourier Transform
IDFT	Inverse Discrete Fourier Transform
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
IFFT	Inverse Fast Fourier Transform
LS	Least Square
SNR	Signal-to-Noise Ratio
ROM	Read Only Memory
RAM	Random Access Memory
MMSE	Minimum Mean Square Error
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
GSM	Global System for Mobile Communications
PDA	Personal Digital Assistant
UWB	Ultra Wide Band Technology

Input-Output Pins

The pin diagram of the hardware implementation is shown in Fig I and the pin configuration is tabulated in TABLE II.

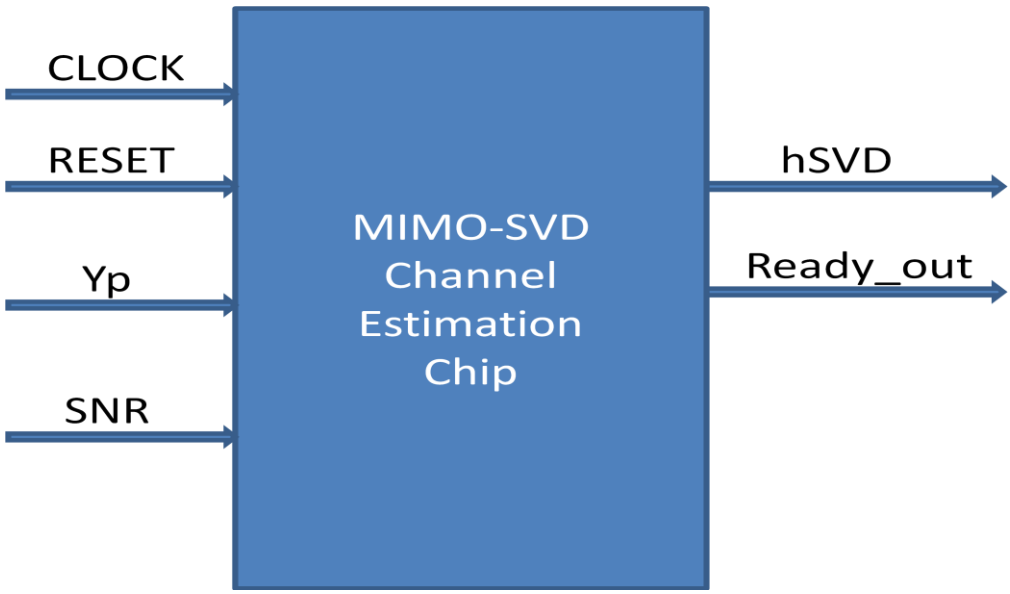

Figure I. The pin diagram of Top Model.

TABLE II. The Top Level Ports detail

Port Name	**Symbol**	**Direction**	**Number of bits**
Clock	clk	Input	1
Reset	rst	Input	1
Signal to Noise Ratio	SNR	Input	6
Received value	Yp	Input	20
SVD estimates	hSVD	Output	22
Output Ready	Out_ready	Output	1