Master's Thesis

Design and measurement of a cyclic ADC in 65 nm CMOS

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Abstract

This thesis report describes the implementation and measurement results for a cyclic ADC with a programmable resolution between 1 and 15 bits. The ADC is clocked at 10 MHz and converts 1 bit in three clock cycles. Thus for a 10 bit resolution the sampling frequency is 333 kHz. The main requirement is an ENOB better than 9 bits for 10-bit conversions. Measurements of the fabricated chip show an ENOB of 9.4 bits, a DNL of 0.25 LSB and an INL of 0.3 LSB. The power consumption is 6.24 mW and it is fabricated in a 65 nm CMOS process using 0.25 mm^2 of silicon area.

The ADC is part of an on-chip measurement system used for DC measurements during calibration, verification and test. It is important with a large input voltage range and a low input voltage offset to be able to measure both high and small signals accurately. To meet these requirements a cyclic ADC topology is used, that has an inherent insensitivity to capacitor mismatch and amplifier offset voltages. The operation of the ADC circuit topology is analyzed, the implemented circuit solutions are described and the results from simulations and measurements are reported.

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Chapter 1
Introduction

This thesis report describes the implementation of a cyclic ADC intended to be used as part of an on-chip analog test system on a radio transceiver chip. It is used for analog to digital conversion of DC signals such as regulator voltages, bias levels, sensor outputs and external voltages connected through the test system. For these purposes, an ADC with 10 bit resolution, low offset voltage and an input voltage range as large as the supply voltage are needed.

To meet these requirements an ADC solution, introduced by Onodera in [1], is used due to its insensitivity to capacitor mismatch, suppression of amplifier offset voltage and large input voltage range. The ADC implements a cyclic ADC architecture, see 1.1, with a switch-capacitor circuit topology that converts 1 bit in three clock cycles. Thus, for a 10 bit conversion the sampling frequency is equal to the clock frequency divided by the number of periods needed to finalize the conversion, $f_s = \frac{10M}{3 \cdot 10}$. This gives a sampling frequency of $333kHz$.

Since the ADC is intended to be used for measurement of DC signals or very low frequency signals, the control interface only supports single shot conversions. To trigger a conversion, a command is sent to the chip over a digital bus connection and when the conversion is finished the results can be read from the chip using the same connection.

1.1 Algorithmic/Cyclic ADC architecture

A 1 bit per cycle algorithmic ADC structure is shown in Figure 1.1. At the start of the conversion, the input voltage is sampled by the sample and hold, S/H. Next the sign of the sampled voltage, $V_{SH}(1) = V_{IN}$, is decided by the comparator. Then the residue voltage, $V_r(k)$, is calculated as the sum of the doubled sampled voltage and positive or negative reference voltage depending on the comparator output. The residue voltage at the end of the first cycle is $V_r(k) = 2V(k) + b(k) \cdot V_{ref}$. In the next cycles, the S/H samples the residue voltage from the previous cycle instead of the input voltage. Thus, the S/H voltage is now equal to $V_{SH}(k+1) = 2V(k) + b(k) \cdot V_{ref}$. This continues until all bits in the conversion are decided. The final residue voltage is then $V_r(n) = 2^n V_{IN} + V_{ref} \cdot \sum_{k=1}^{n} 2^{k-1} \cdot b(k)$.

The residue voltage is the difference between the amplified input signal and

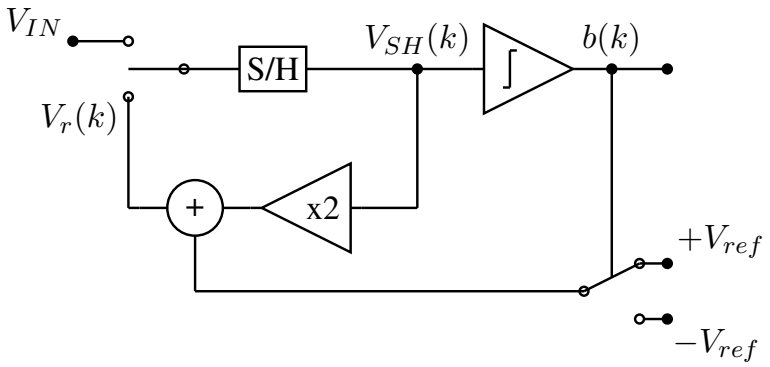


Figure 1.1: Algorithmic ADC architecture

the decoded digital value. For each decoded bit the input-related residue voltage is reduced by two and at some resolution it will be smaller than the errors caused by nonidealities of an actual circuit implementation. The main limiting factors are the multiplication by two accuracy, the reference addition/subtraction accuracy and the noise of the circuit implementation.

1.2 Organization

Following this introduction, chapter 2 discusses the function of the ADC circuit topology and why it is insensitive to capacitor mismatch and amplifier offset. Chapter 3 presents schematic, layout and simulation results of the circuit. Chapter 4 presents and discusses results from measurements and chapter 5 gives a conclusion.

Chapter 2

Cyclic ADC topology

The circuit topology used (Figure 2.1) consists of two switched-capacitor (SC) stages, each with an amplifier and associated switches and capacitors. The two stages implement all the functions needed to implement the cyclic ADC as described in section 1.1 (the sample and hold (S/H), multiplication by two, reference addition/subtraction and quantization).

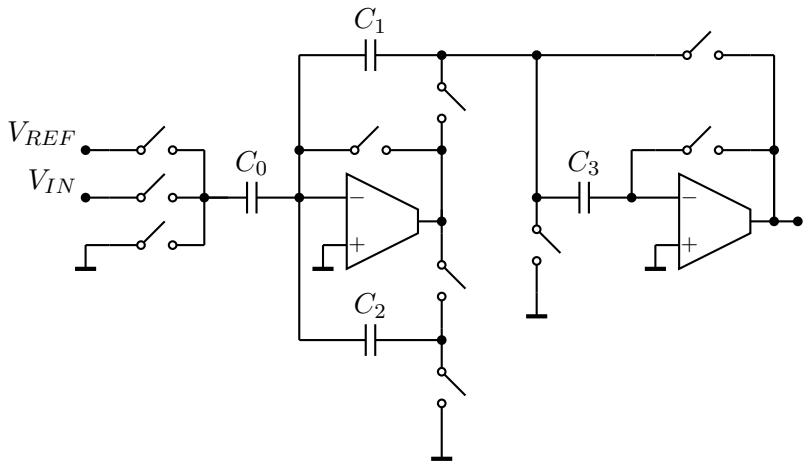


Figure 2.1: Cyclic ADC topology [1]

In the following sections the operation of the ADC circuit topology will be described and its functions analyzed (multiply by two gain, input voltage sampling, reference addition/subtraction and offset suppression).

2.1 Multiply by two

This section discusses the insensitivity of the used topology to capacitor mismatch and why it is desirable feature. A capacitor-ratio dependent gain stage and the ratio independent topology are analyzed and compared. First the ratio-dependent gain stage is analyzed in section 2.1.1 and then the ratio-independent in section 2.1.2

2.1.1 Ratio dependent SC gain

In switch-capacitor amplifiers a capacitance ratio between two capacitors is often used to achieve a certain gain. First the input voltage is sampled on one capacitor then the sampled charge is transferred to the other capacitor. If the second capacitor has half the capacitance of the first the output voltage will be doubled compared to the input voltage and a gain of two is achieved. As the gain is set by the capacitance ratio of the two capacitors the accuracy is limited by the mismatch between them. This will set a minimum capacitance for a certain accuracy as the mismatch decreases with increasing capacitor size.

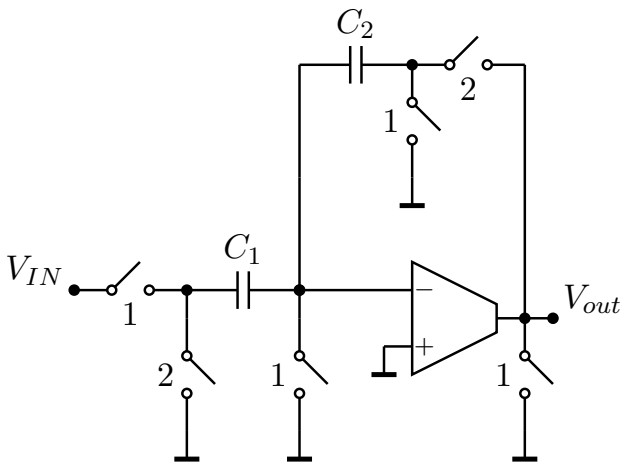


Figure 2.2: Simple switch-capacitor gain stage

A simple switch-capacitor gain stage that operates with two phases is shown in Figure 2.2. In the first phase the input voltage, v_{in}, is sampled on capacitor C_1, connected between the input and ground, and capacitor C_2 is discharged as both its terminals are connected to ground. During the second phase the charge stored on C_1, $Q_1^{p=1} = -v_{in} * C_1$, is discharged into the amplifier virtual ground as it is connected between ground and amplifier virtual ground. The discharge current through C_1 is supplied from the amplifier through C_2, why the charge on C_1 is transferred to C_2. At the end of the second phase the output voltage is.

$$V_{out} = -Q_1/C_2 = -v_{in} * \frac{C_1}{C_2}$$

From the equation above it can be seen that the gain is equal to the capacitor ratio $\frac{C_1}{C_2}$.

2.1.2 Ratio independent SC gain

The ratio independent topology in Figure 2.1 operates with two stages and three phases each. The first and second stages perform different operations during the three phases. The three operations in the first stage are named "Add", "Take

refuge" (TR), and "Store & sample" (SS), and in the second stage the three operations are named "Sample" (S), "Compare" (C) and "Hold" (H).

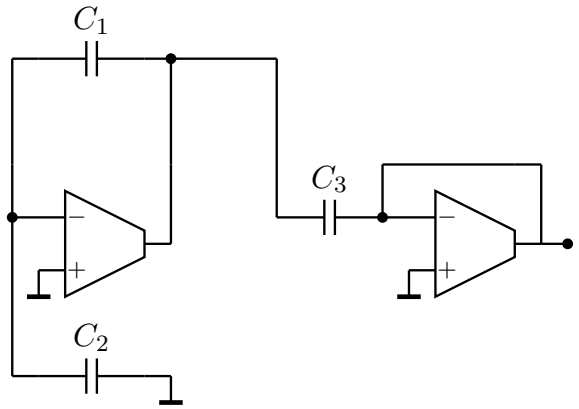


Figure 2.3: Topology phase 1, Add and Sample.

In phase 1, shown in Figure 2.3, capacitor C_1 is connected to the amplifier output and capacitor C_2 is connected to ground. The negative side of the capacitors are connected to the amplifier negative input throughout all phases. This forces charge on C_2 to be transferred to C_1 adding to any charge already stored on capacitor C_1. To analyze the gain of the topology it is assumed that the output voltage of stage 1 is V_O^1 at the end of phase 1, and that both amplifiers have infinite gain. In the second stage, the amplifier is connected in unity-gain feedback and capacitor C_3 is connected to the output of stage 1, sampling the output voltage. The capacitors charges at the end of phase 1 are:

$$Q_{C_1}^{ADD} = V_O^1 * C_1$$
$$Q_{C_2}^{ADD} = 0$$
$$Q_{C_3}^{S} = V_O^1 * C_3$$

In the second phase, see Figure 2.4, capacitor C_1 is connected to ground and C_2 is connected to the amplifier output. This causes the charge sampled on C_1 in the previous phase to be transferred from C_1 to C_2. In the second stage, C_3 is connected to ground and the feedback around the amplifier is disconnected. This leaves the charge on C_3 unchanged. The capacitors charges at the end of the phase are:

$$Q_{C_1}^{TR} = 0$$
$$Q_{C_2}^{TR} = -V_O^1 * C_1$$
$$Q_{C_3}^{C} = V_O^1 * C_3$$

In the third phase, see Figure 2.5, the amplifier in stage 1 is connected in unity gain feedback, C_1 is connected to the output of stage 2 and C_2 is floating. This causes the charge on C_2 to be unchanged and the voltage over C_1 to become

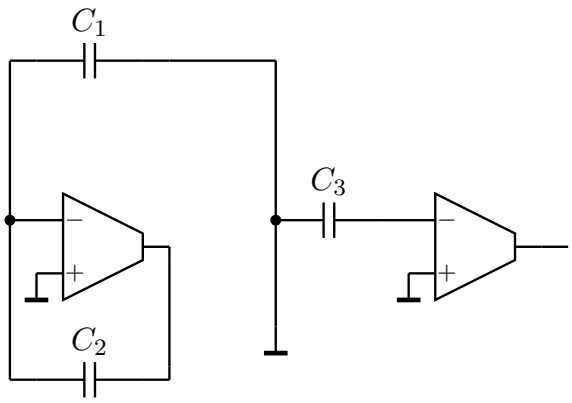


Figure 2.4: Topology phase 2, "Take refuge" and "Compare"

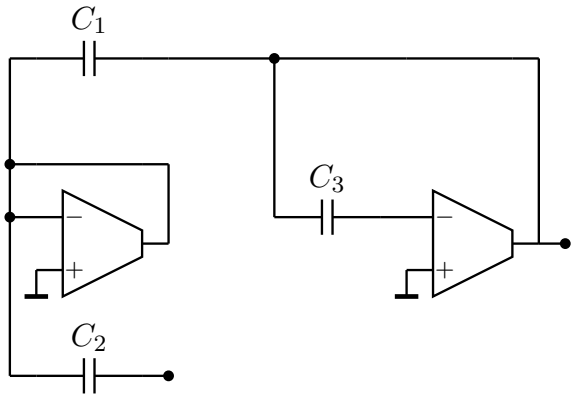


Figure 2.5: Topology phase 3, "Store and sample" and "Hold"

equal to output voltage of stage 2. In stage 2 C_3 is connected to the amplifier output making the output voltage equal to the previously sampled voltage in phase 1. The capacitors charges at the end of the phase are:

$$Q_{C_1}^{SS} = V_O^1 * C_1$$
$$Q_{C_2}^{SS} = -V_O^1 * C_1$$
$$Q_3^H = V_O^1 * C_3$$

Now the charges on C_1 and C_2 are of equal magnitude with opposite sign. As the circuit again enter phase 1 the charge on C_2 is transferred to C_1. The capacitors charges at the end of the phase are:

$$Q_{C_1}^{ADD_2} = 2 \cdot V_O^1 * C_1$$
$$Q_{C_2}^{ADD_2} = 0$$
$$Q_3^{S_2} = 2 \cdot V_O^1 * C_3$$

The ratio of the charge, $Q_{C_1}^{ADD2}$, on capacitor C_1 after one cycle of operation to the initial charge, $Q_{C_1}^{ADD}$, is

$$\frac{Q_{C_1}^{ADD2}}{Q_{C_1}^{ADD}} = \frac{2 * V_O^1 * C_1}{V_O^1 * C_1}$$
$$\frac{Q_{C_1}^{ADD2}}{Q_{C_1}^{ADD}} = 2$$

As the charge on C_1 is doubled in one cycle the voltage at the output of the amplifier is also doubled and a gain of two is achieved, independent of any capacitance ratio.

Comparing the two gain stages it obvious that the cost of the ratio independent gain is high. One extra amplifier, one extra capacitor, more switches and one more phase which generates costs in power consumption, area and complexity. For this ADC it was essential with a robust solution with reduced sensitivity to process variations, so the cost was considered acceptable.

2.2 Input voltage sampling

Here a capacitor C_0 is added. It is connected between the input voltage and the virtual ground of the amplifier in stage 1, see Figure 2.6. The input voltage can then be sampled on the capacitor and in the next phase the charge is transferred to C_1 to start the ratio independent gain cycle. This requires one extra phase before the ratio independent gain cycle in which all other capacitors are connected to ground.

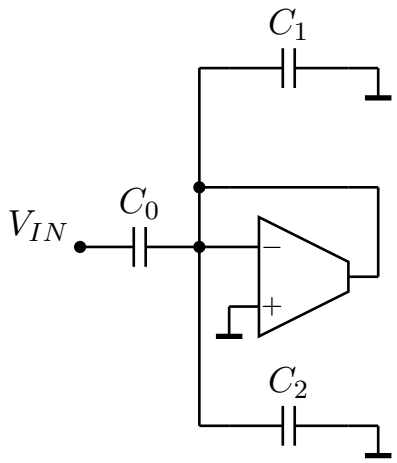


Figure 2.6: SC gain stage 1 with added capacitor, C_0, used for input voltage sampling

2.3 Reference subtraction/Addition

Capacitor C_0 is also used to do reference voltage subtraction or addition, depending on the sign from the previous bit decision. This is done in the same way as the input voltage sampling. Instead of connecting C_0 input side to ground it is connected to the reverse polarity of the reference voltage so that the charge subtracted (added) is $V_{ref_p} - V_{ref_n}$ $(V_{ref_n} - V_{ref_p})$. In the single-ended case this will be $V_{ref} - V_{gnd}$ $(V_{gnd} - V_{ref})$.

2.4 Quantization

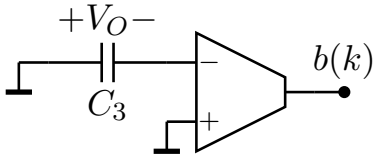


Figure 2.7: Amplifier in stage 2 used as a comparator

The second stage is used to perform the quantization. The input side of capacitor C_3 is grounded and the amplifier is in an open loop configuration, as shown in Figure 2.7. Then as C_3 is grounded the input of the amplifier will be forced apart by the charge stored on the capacitor in the previous phase. The output voltage of the amplifier will then either go to supply or ground depending on the sign of the voltage sampled on capacitor C_3 in the previous phase.

2.5 Amplifier offset voltage suppression

The circuit topology is insensitive to amplifier offset voltages, as long as they are small enough to not push the amplifier into nonlinear operation. This can be seen as a form of correlated double sampling (CDS) of amplifier offset voltage [6]. To explain this, a simpler switched-capacitor gain stage (see Figure 2.8) that uses the same method to suppress the amplifier offset voltage is analyzed.

The switched-capacitor gain stage operates with two phases: sampling and amplification. In the first phase the input voltage is sampled on capacitor C_0 and in the second phase the charge on C_0 is transferred to capacitor C_1. Assuming zero offset voltage, the charge sampled in the first phase is $Q_{sampled} = C_0 \cdot V_{in}$. After the charge transfer the voltage over C_1 is $-Q_{sampled}/C_1 = -C_0/C_1 V_{IN}$. Thus, the output voltage is equal to $V_{OUT} = -C_0/C_1 \cdot V_{IN}$. If the amplifier offset voltage is included in the analysis, the sampled charge on C_0 is changed and the voltage over C_1, during the sampling phase is no longer zero. So this charge must also be included in the analysis. The charges stored on capacitors C_0 and C_1 in

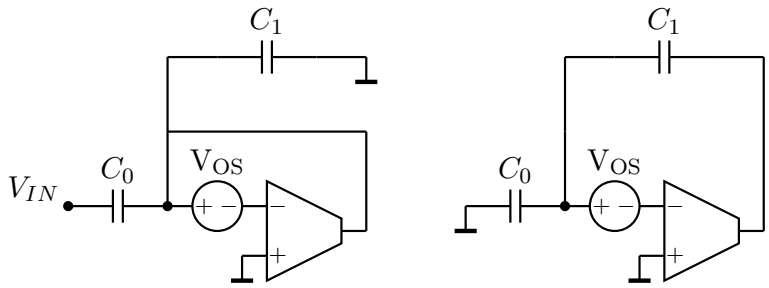


Figure 2.8: SC gains stage with CDS of offset voltage, sampling phase to the left and amplification phase to the right

the sampling phase are then:

$$Q_{C_0} = C_0 \cdot (V_{in} - V_{OS})$$
$$Q_{C_1} = C_1 \cdot (-V_{OS})$$

After the charge transfer in the amplification phase the charges are:

$$Q_{C_0} = -C_0 \cdot V_{OS}$$
$$Q_{C_1} = -C_0 \cdot V_{in} - C_1 \cdot V_{OS}$$

The output voltage can be calculated by adding the voltages over C_0 and C_1:

$$V_{OUT} = -Q_{C_0}/C_0 + Q_{C_1}/C_1$$
$$V_{OUT} = V_{OS} - \frac{C_0}{C_1} \cdot V_{in} - V_{OS}$$
$$V_{OUT} = -\frac{C_0}{C_1} \cdot V_{in}$$

From the equation above for the output voltage, it is clear that the amplifier offset voltage is suppressed as it does not affect the output voltage. In the ADC circuit topology the same principle is used. The additional capacitor C_2 does not change the conclusion of the analysis.

Chapter 3

Implementation

In this chapter the implementation and simulation of the main parts of the ADC are described. First comes the implementation and simulation of the ADC core, which implements a differential version of the previously described single-ended cyclic ADC topology, in section 3.1. Then comes the reference buffer implementation and simulation, in section 3.2, and after that the implementation and simulation of the common mode voltage buffer, in section 3.3. Other parts not described are a digital control block that generates control signals and a reference voltage generator that creates a reference voltage. Moreover, a bias current generator that creates a programmable bias current used by all amplifiers is also omitted. After that simulation results of the full ADC are discussed in section 3.4 and finally the layout of the ADC is shown in section 3.5.

3.1 ADC Core

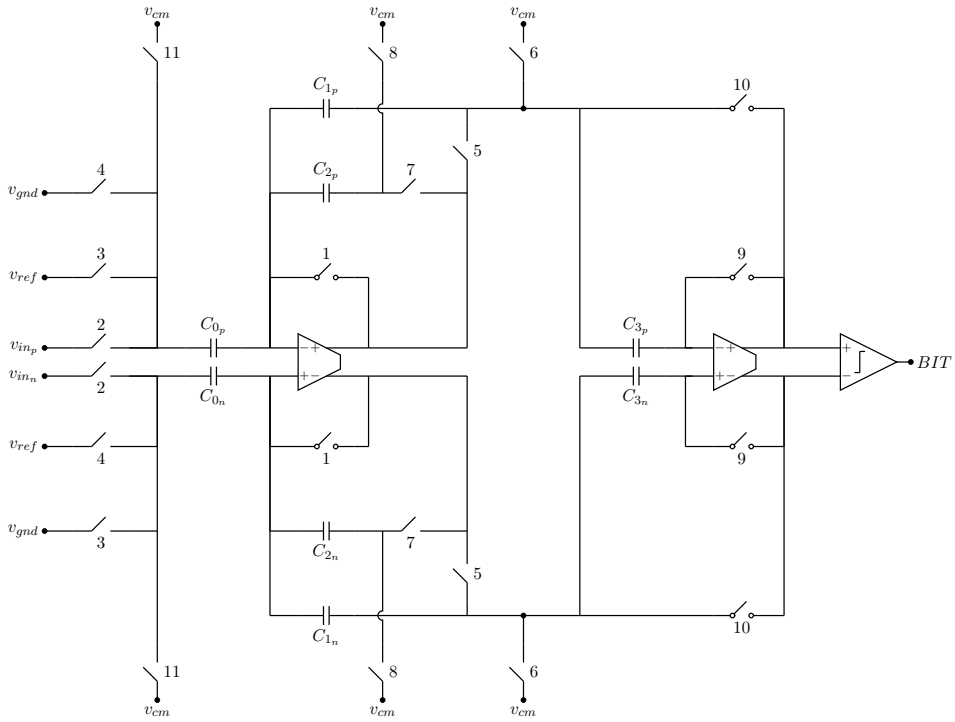


Figure 3.1: Differential implementation of ADC circuit topology.

The differential implementation of the single-ended ADC circuit topology described in chapter 2 is shown in 3.1 and capacitor sizes are listed in Table 3.1. The two amplifiers in stage one and two use the same implementation, described in section 3.1.1, but with different compensation networks as the load capacitance and feedback factor are different. After the amplifier in stage two a separate quantizer, described in section 3.1.2, is used to speed up the quantization decision and simplify the amplifier design. All switches are implemented as pass gates, i.e. using both PMOS and NMOS transistors for lower on-resistance. The current consumption of the ADC core is about 4.1 mA, of which the two amplifiers consume 2 mA each and the comparator less than 50 uA.

Capacitor	Capacitance (pF)	Capacitor	Capacitance (pf)
$C_{0_{p,n}}$	1.1	$C_{1_{p,n}}$	2.2
$C_{2_{p,n}}$	2.2	$C_{3_{p,n}}$	2.2

Table 3.1: Table of capacitor sizes in ADC Core, shown in Figure 3.1

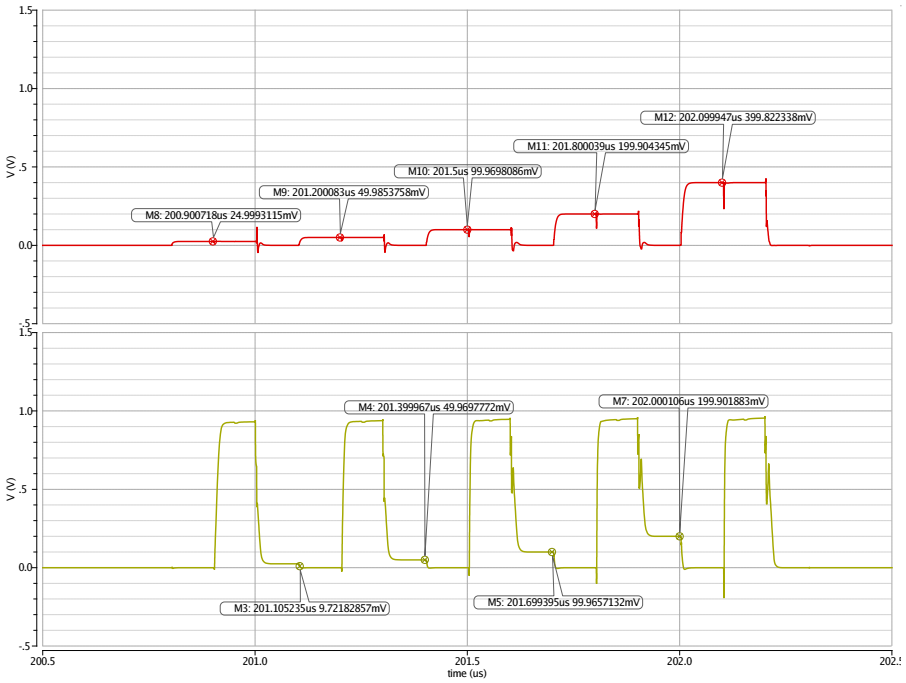


Figure 3.2: Simulation of ADC core stage 1 (upper plot) and stage 2 amplifier (lower plot) differential outputs with v_{ref} set to zero.

Figure 3.2 shows the output voltage of stages one and two from a simulation of a 5-bit conversion. The reference voltage input is set to zero to make it easier to estimate the cycle gain. The upper curve shows the output voltage from stage 1 and the markers show the voltage at the end of each "Add" phase for each conversion cycle, see section 2.1.2. For each conversion cycle the voltage at the end of each "Add" phase is doubled compared to the previous phase as intended. The ratio of the marked voltage at the start and end of each cycle are used to estimate the gain of one conversion cycle. The estimated gain in cycle 1 is 1.9995, cycle 2 is 2.0000, cycle 3 is 1.9996 and cycle 4 is 2.0001. The gain error (δ_1) in the first cycle is:

$$\delta_1 = \frac{\left|2 - \frac{49.9853758}{24.9993115}\right|}{2} = 265\mu$$

The input referred error from the first cycle is the gain error divided by the ideal gain of 2:

$$\delta_{input_1} = \frac{delta_1}{2}$$

By summing the input referred gain errors made in each cycles during the conversion, the total input referred error is:

$$\delta_{input} = \frac{delta_1}{2} + \frac{delta_2}{4} + \frac{delta_3}{8} + ... + \frac{delta_n}{2^n}$$

For 10-bit resolution, assuming that the gain errors are equal in all cycles, the above equation results in an input referred gain error of:

$$\delta_{input} = 0.999 \cdot delta$$

This shows that the total gain error is almost equal to a single gain error in one cycle. The gain error should be less than half of an LSB, to not degrade the conversion accuracy:

$$\delta_{input} < \frac{1}{2^{10+1}}$$

Thus, the input referred gain error of 265μ is almost a fourth of an LSB, which is accurate enough for a 10 bit resolution. As the voltages used to estimate the cycle gain accuracy are taken from a plot, it is assumed that the actual accuracy is better. In Figure 3.3 the capacitor output voltages from the stages are shown. Using this simulation the cycle gain can also be estimated by observing the voltage over capacitor C1 at the start and end of the first cycle. The estimated gain from the plot is 1.9991. From Figure 3.3 it also possible to observe the different phases

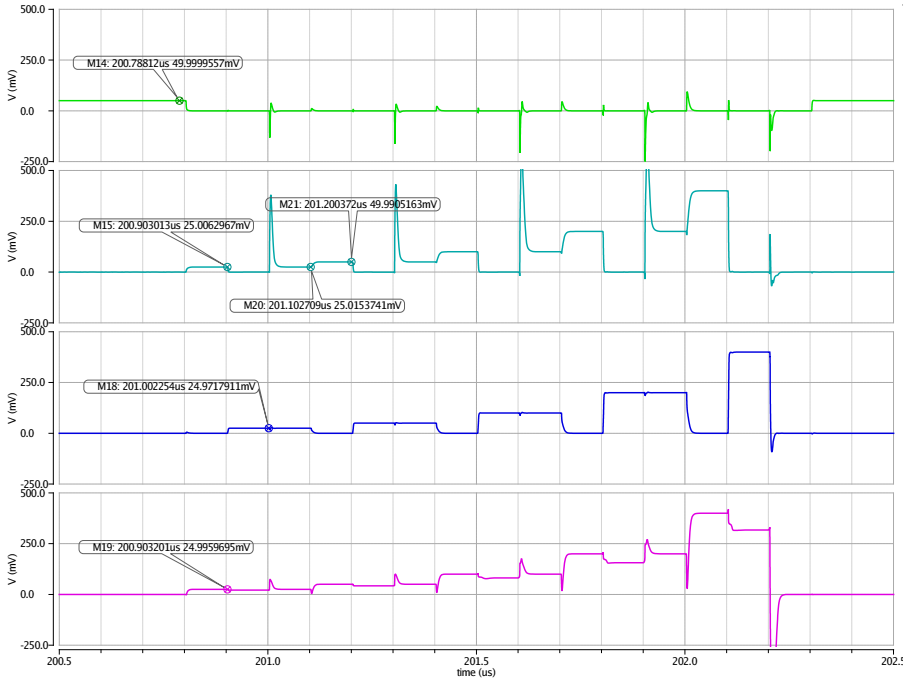


Figure 3.3: Simulation of ADC core capacitor voltages with v_{ref} set to zero. The capacitor voltages are shown in number order with C_0 in the top plot to C_3 in the bottom plot.

of operation. In the top curve showing the voltage over capacitor C_0, the marker displays the voltage, 50 mV, at the end of the sample phase. This charge is then transferred to capacitor C_1 resulting in a voltage of 25 mV, indicated by left-most marker on the second plot. The voltage is half that of the sampled voltage as capacitor C_1, C_2 and C_2 are twice as large as capacitor C_0. This is to reduce the internal swing in the ADC core compared to the sample voltage. At the same time the voltage is copied onto capacitor C_3 resulting in a voltage of 25 mV, shown by the bottom curve. Next is the "Take refuge" phase, in which the charge on capacitor C_1 is transferred onto capacitor C_2 resulting in a voltage of 25 mV, shown in the third curve. After that comes the "Sample and store" phase, in which the voltage copied onto C_3 is copied back onto C_1, resulting in a voltage of 25 mV, marked by the second marker from the left for capacitor C_1. Finally, the charge stored on C_2 is transferred to capacitor C_1, adding it to the charge from the previous phase. This results in a voltage of 50mV, indicated by third marker from the left, and thus the cycle is done and the voltage is doubled.

3.1.1 Amplifier

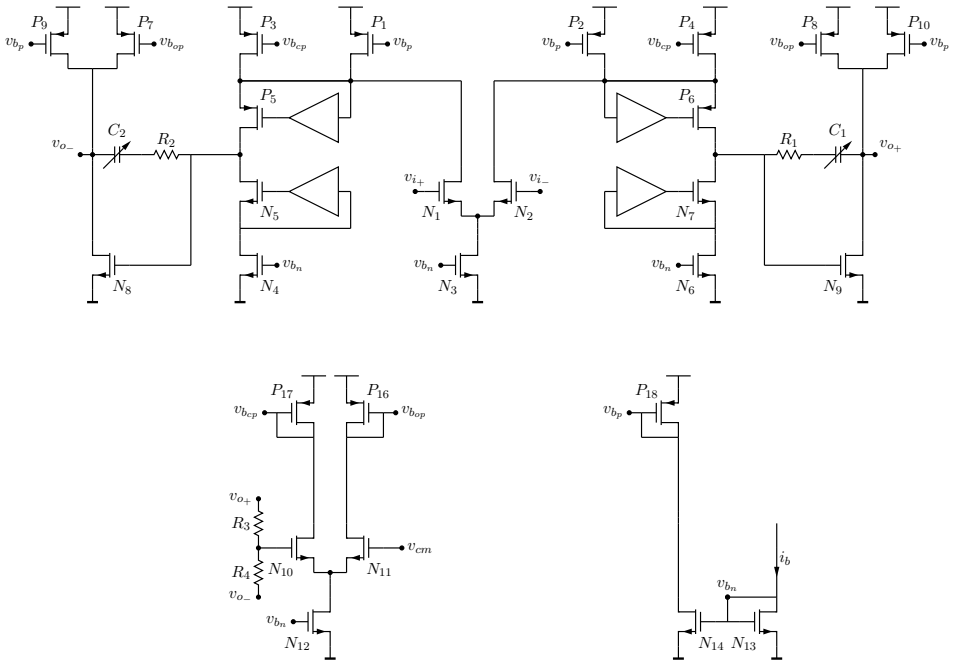


Figure 3.4: Two stage amplifier.

The amplifier in Figure 3.4 is implemented using a two-stage topology with a pole-split frequency compensation to achieve a high gain and a large output swing. This will however increase the settling time due to a lower bandwidth caused by the multiple amplifier stages. As the clock frequency of the ADC is modest, necessary bandwidth can still be obtained but at the cost of higher cur-

rent consumption. The first stage is using a folded cascode amplifier [2] to achieve a high gain without introducing a third stage. To increase the gain more, gain boosting is used [5]. This increases the output impedance of the first stage and thus the gain is increased. In Table 3.2 dimensions of the devices in the amplifier are listed. The amplifier pole-split frequency compensation is made using a Miller capacitor with a series resistor [2] to cancel the zero caused by unwanted feed forward path through the Miller capacitor. The compensation capacitor is programmable as the needed compensation capacitance to achieve good phase margin varies between the different phases of the cyclic ADC operation, due to the varying load capacitance and feedback factors depending how the capacitor are connected.

Transistor	Size (μm)	Transistor	Size (μm)
N_1	$16\frac{10}{0.2}$	N_2	$16\frac{10}{0.2}$
N_3	$10\frac{10}{1}$	N_4	$7\frac{10}{1}$
N_5	$4\frac{10}{0.2}$	N_6	$7\frac{10}{1}$
N_7	$4\frac{10}{0.2}$	N_8	$20\frac{10}{0.2}$
N_9	$20\frac{10}{0.2}$	N_{10}	$2\frac{20}{0.2}$
N_{11}	$2\frac{20}{0.2}$	N_{12}	$4\frac{10}{1}$
N_{13}	$2\frac{10}{1}$	N_{14}	$\frac{10}{1}$
P_1	$4\frac{20}{1}$	P_2	$4\frac{20}{1}$
P_3	$7\frac{20}{0.5}$	P_4	$7\frac{20}{0.5}$
P_5	$4\frac{20}{0.2}$	P_6	$4\frac{20}{0.2}$
P_7	$12\frac{20}{1}$	P_8	$12\frac{20}{1}$
P_9	$8\frac{20}{1}$	P_{10}	$8\frac{20}{1}$
P_{11}	$2\frac{20}{0.5}$	P_{12}	$2\frac{20}{0.5}$
P_{13}	$2\frac{20}{1}$		
Capacitor	Capacitance (pF)	Capacitor	Capacitance (pf)
C_1	2,3,4	C_2	2,3,4
Resistor	Resistance $k\Omega$	Resistor	Resistance $k\Omega$
R_1	1.3	R_2	1.3
R_3	42	R_4	42

Table 3.2: Table of devices in amplifier, shown in Figure 3.4

Figure 3.5 shows the loop gain for the three phases of operation for stage 1: "Add", "Take Refuge" and "Store & Sample". The nominal DC gain varies between 95 and 105 dB, the phase margin varies from 88° to 108° and the unity gain frequency from 47 to 76 MHz. In [1] the following equation, for the maximum absolute error of the multiply by two gain due to a limited DC gain is presented:

$$E_{gain,max} = \frac{3}{G_{DC}}(2^n - n - 1) + \frac{3}{G_{DC}}(2^n - \frac{2}{3})\frac{|V_{off}|}{V_{ref}}$$

In the implemented ADC capacitor C_0 has half the capacitance of capacitors C_1

and C_2. This increase the feedback factor from $1/3$ to $2/5$ and the above equation has to be modified to:

$$E_{gain,max} = \frac{\frac{5}{2}}{G_{DC}}(2^n - n - 1) + \frac{\frac{5}{2}}{G_{DC}}(2^n - \frac{2}{\frac{5}{2}})\frac{|V_{off}|}{V_{ref}}$$

In order to keep the error below $1/4$ LSB, assuming that the amplifier offset voltage (V_{off}) is equal to the reference voltage (V_{ref}), the gain (G_{DC}) must be higher than 94 dB for 10-bit and 100 dB for 12-bit conversions, respectively. As the DC gain reported above are from loop gain simulation, it needs to be multiplied with the feedback factor to be compared to the required DC gain. With the feedback factor taken into account the DC gain varies between 103 dB and 105 dB.

The amplifier DC gain is designed to achieve better than 12 bit accuracy in the nominal case to have margin for process variations and other error sources, while still achieving better than 10-bit accuracy. The bandwidth required can be estimated by approximating the amplifier transfer function with that of an ideal integrator, i.e. assuming infinite DC gain, $A(s) = \frac{\omega_{ta}}{s}$, where ω_{ta} is the unity-gain frequency of the amplifier. Thus, the closed loop system is given by:

$$H(s) = \frac{A(s)}{1 + A(s)\beta} = \frac{1}{\beta}\frac{1}{1 + \frac{s}{\omega_{ta}\beta}}$$

Where it can be seen that the time constant of the system is $\tau = 1/(\omega_{ta}\beta)$. The time domain step response of the closed loop system is:

$$h(t) = \frac{1}{\beta}(1 - e^{-\frac{t}{\tau}})$$

The relative error of the settling at time t_{clock} is:

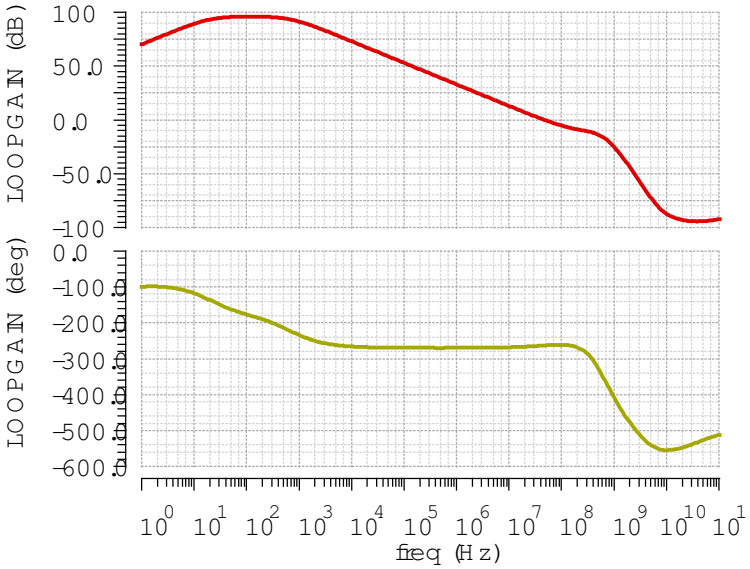
$$\varepsilon = \frac{h(t \to \infty) - h(t = t_{clock})}{h(t \to \infty)} = e^{-\frac{t_{clock}}{\tau}}$$

If the system should have an N-bit performance, then the relative settling error must be less than fourth of an LSB. As this circuit operates with three phases, it is assumed the error must be a third of one fourth of an LSB to account for the error made in each phase, this requires that:

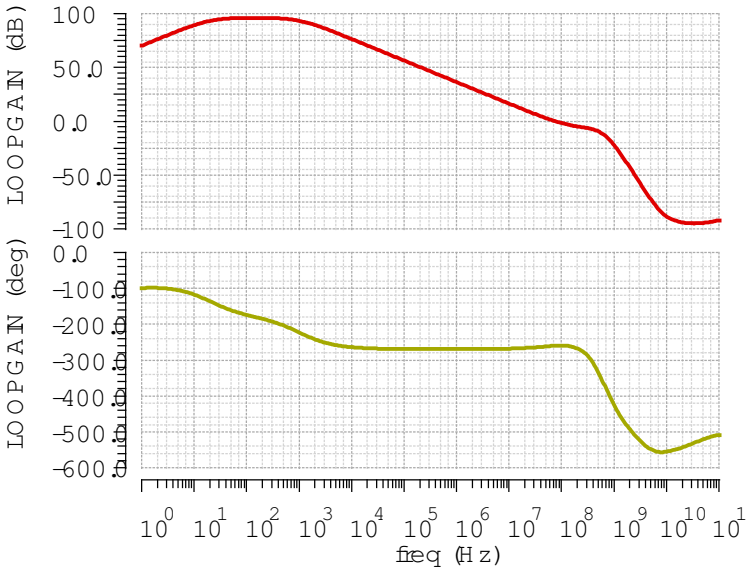
$$e^{-\frac{\omega_{ta}\beta}{f_{clock}}} < \frac{2^{-(N+2)}}{3}$$

Since $A(s)$ is the open loop transfer function of the amplifier, $A_s\beta$ is equal to the loop gain of the circuit. This gives, that the amplifier unity-gain frequency times the feedback factor ($\omega_{ta}\beta$) is equal to the unity-gain bandwidth (f_{UGBW}) of the loop gain. Given this, the above equation can be rewritten as:

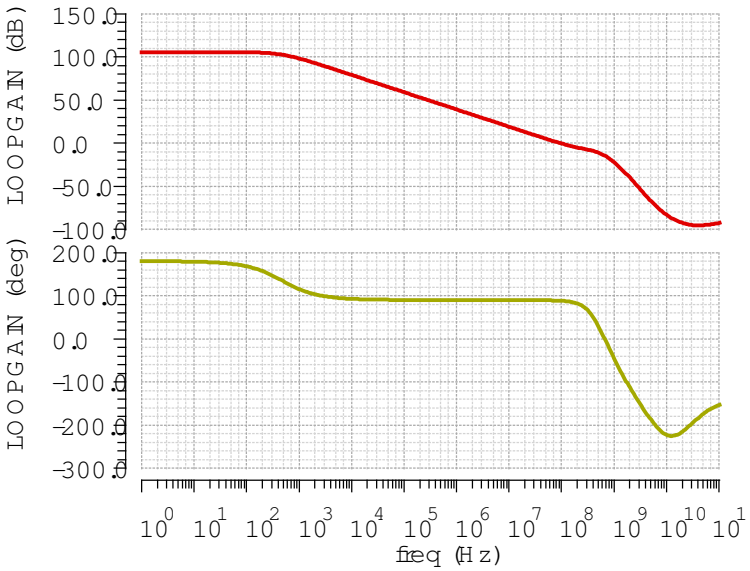
$$e^{-\frac{f_{UGBW}}{f_{clock}}} < \frac{2^{-(N+2)}}{3}$$



(a) Add



(b) Take refuge



(c) Store and sample

Taking the logarithm of both sides of the above equation, the required ratio of the unity-gain frequency of loop gain to the clock frequency is:

$$\frac{f_{UGBW}}{f_{clock}} > \frac{(N+2)ln(2)}{2\pi} + ln(3)$$

Thus, the required unity-gain bandwidth of the loop gain can be calculated with the equation above. For 10-bit accuracy the ratio is $\frac{f_{UGBW}}{f_{clock}} > 2.42$, thus a unity-gain bandwidth larger than 24.2 MHz is required. The nominal unit gain bandwidth of 47 MHz, in the phase with the lowest bandwidth, is twice that of the required bandwidth and the settling error are much less than $1/4$ LSB.

3.1.2 Comparator

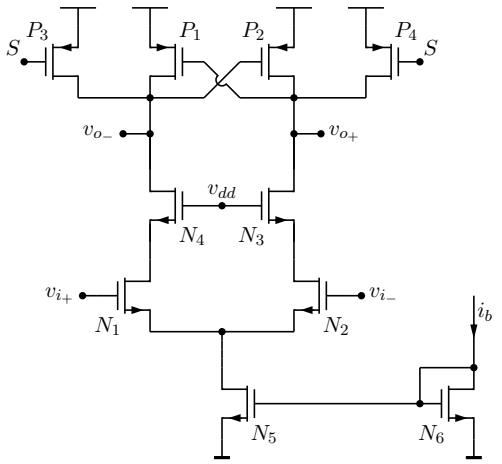


Figure 3.6: Regenerative comparator

Even though the amplifier can be used to perform the quantization, as shown in fig 2.4, a comparator is added after the amplifier in the second stage to reduce the bandwidth needed. This is because the amplifier does not need to resolve a small input voltage to logic levels in a short time interval. Instead, it acts a buffer before the comparator which increases the input voltage to the comparator. This makes it possible to use a simple regenerative comparator as the input offset voltage of the comparator is suppressed by the amplifier gain [4]. The amplifiers own offset voltage is suppressed as explained in section 2.5.

The regenerative comparator (Figure 3.6) consists of an input NMOS differential pair, a cross-coupled PMOS pair as load and PMOS reset switches. Dimensions of the devices in comparator are listed in Table 3.3. The comparator operates in two phases, reset and compare. In the reset phase the output is shorted to the supply to make the differential output voltage zero. In the compare phase the shortcut to supply is disconnected and the outputs are pulled down by the currents through the differential pair which are proportional to the input voltage.

Transistor	Size (μm)	Transistor	Size (μm)
N_1	$8\frac{5}{0.4}$	N_2	$8\frac{5}{0.4}$
N_3	$\frac{4}{0.18}$	N_4	$\frac{4}{0.18}$
N_5	$4\frac{9.6}{1}$	N_6	$\frac{9.6}{1}$
P_1	$2frac40.4$	P_2	$2\frac{0.4}{0.4}$
P_3	$frac20.08$	P_4	$\frac{2}{0.08}$

Table 3.3: Table of devices in comparator, shown in Figure 3.6

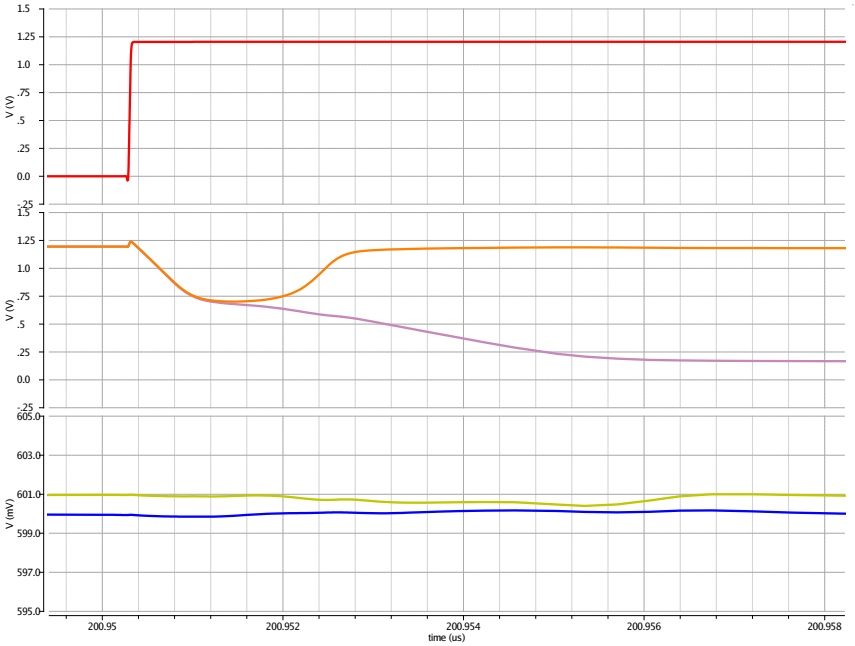


Figure 3.7: Comparator simulation

As the cross coupled pair is off at the start, the output voltage difference is only due to the current trough differential pair. As soon as the voltage is pulled low enough the cross couple pair is turned on and the outputs are pulled apart towards supply and ground. This can be seen in Figure 3.7 that shows the sample signal, upper curve, the voltages at the output of the comparator, middle curves, and the input voltages, lower curves. First the voltage is shorted to the supply then it is released and pulled down. Then, as the cross-coupled pair turns on, the outputs are pulled apart towards supply and ground.

3.2 Reference buffer

As the reference voltage is created by a resistive divider between the supply and ground the output resistance is relatively high. This would cause slow settling if

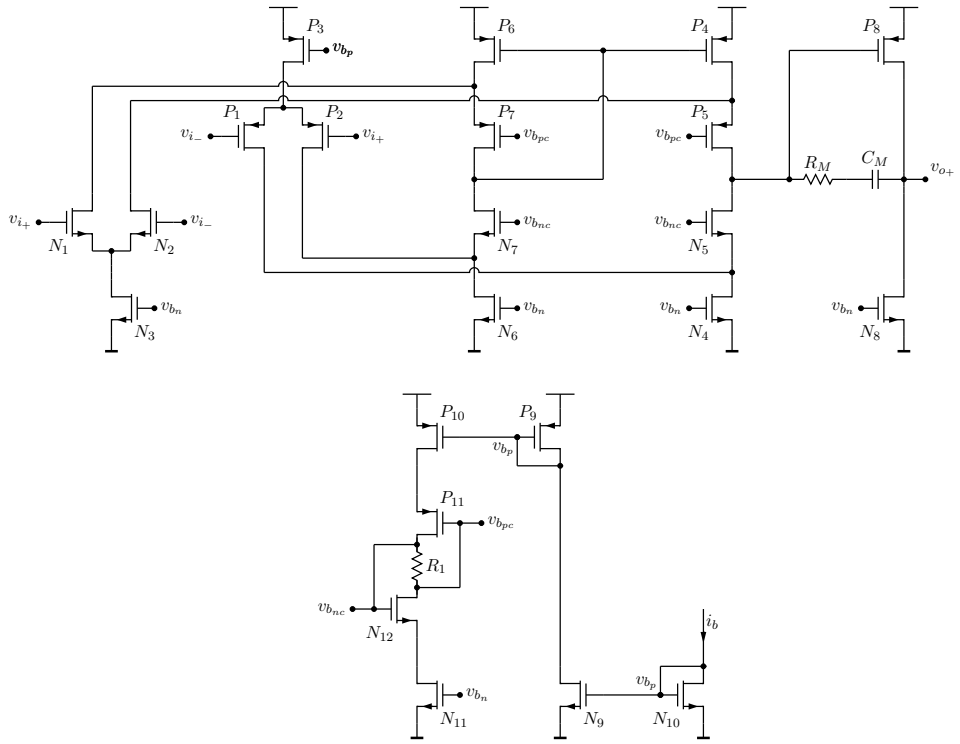


Figure 3.8: Reference buffer amplifier, schematic

it was connected directly to the ADC. Instead, a unity gain buffer is used between the reference divider and the ADC. The reference buffer implementation is shown in Figure 3.8 and device sizes are listed in Table 3.4. It uses a two stage amplifier topology with a first stage folded cascode amplifier with complementary differential pairs at the input to handle the reference voltage range. A common source second stage using a pole-split with a Miller capacitor as frequency compensation to get a stable amplifier is also used.

Figure 3.9 shows magnitude and phase of the loop gain in the reference buffer. The DC gain is 81 dB, the bandwidth is 218 MHz, the phase margin is 81° with a current consumption of less than 900 uA. The bandwidth of the reference buffer is substantially higher than the bandwidth of the amplifiers in the ADC core, not to degrade the total settling of the ADC core.

3.3 Common mode voltage buffer

As the capacitors are connected to signal ground in several of the phases of operation, a buffer amplifier is used to protect the common mode source from the switching load of the ADC Core. The common mode voltage buffer implementation is shown in Figure 3.10. A single-stage amplifier is used since the common mode voltage does not need to be a very accurate copy of the common mode

Transistor	Size (μm)	Transistor	Size (μm)
N_1	$4\frac{10}{0.2}$	N_2	$4\frac{10}{0.2}$
N_3	$12\frac{5}{0.8}$	N_4	$9\frac{5}{0.8}$
N_5	$\frac{10}{0.2}$	N_6	$9\frac{5}{0.8}$
N_7	$\frac{10}{0.2}$	N_8	$30\frac{5}{0.8}$
N_9	$\frac{5}{0.8}$	N_{10}	$\frac{5}{0.8}$
N_{11}	$3\frac{10}{0.2}$	N_{12}	$\frac{10}{0.2}$
P_1	$8\frac{10}{0.2}$	P_2	$8\frac{10}{0.2}$
P_3	$12\frac{10}{0.8}$	P_4	$9\frac{10}{0.8}$
P_5	$3\frac{10}{0.2}$	P_6	$9\frac{10}{0.8}$
P_7	$3\frac{10}{0.2}$	P_8	$20\frac{10}{0.2}$
P_9	$\frac{10}{0.8}$	P_{10}	$3\frac{10}{0.8}$
P_{11}	$3\frac{10}{0.2}$		
Capacitor	Capacitance (pF)		
C_M	1		
Resistor	Resistance Ω	Resistor	Resistance $k\Omega$
R_M	740	R_1	6.6

Table 3.4: Table of devices in reference buffer, shown in Figure 3.8

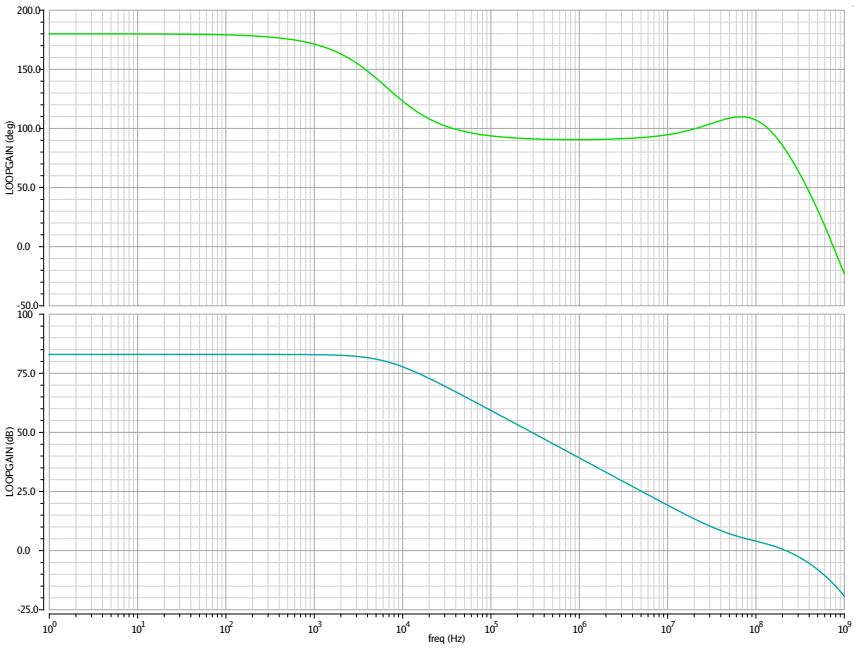


Figure 3.9: Reference buffer amplifier loop gain simulation.

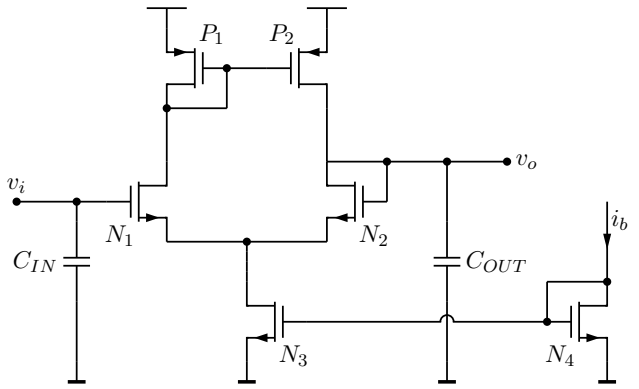


Figure 3.10: V_{cm} buffer amplifier schematic

voltage derived from the resistive reference generator.

Transistor	Size (μm)	Transistor	Size (μm)
N_1	$10\frac{10}{0.2}$	N_2	$10\frac{10}{0.2}$
N_3	$10\frac{15}{1}$	N_4	$\frac{15}{1}$
P_1	$10\frac{30}{0.6}$	P_2	$10\frac{30}{0.6}$
Capacitor	Capacitance (pF)	Capacitor	Capacitance (pf)
C_{IN}	3.4	C_{OUT}	3

Table 3.5: Table of devices in V_{cm} buffer, shown in Figure 3.10

Figure 3.11 shows the phase and magnitude of the loop gain for the common mode voltage buffer. The DC gain is 30 dB, the bandwidth is 28 MHz, the phase margin is 85° with a current consumption of 140 uA. All capacitors connected to the buffered common mode voltage are connected in differential pairs. So the discharge or charge current cancel each other out to the first order, which reduces the bandwidth and gain required by the common mode buffer, compared to the reference buffer. This makes it possible to use a single-stage amplifier with low bandwidth.

3.4 Simulation results

In this section simulation results of the full ADC with on-chip linear supply regulators and decoupling are presented. In section 3.4.1 results from applying a DC ramp to the input are discussed. Section 3.4.2 describes the noise simulation and in section 3.4.3 the current consumption is discussed.

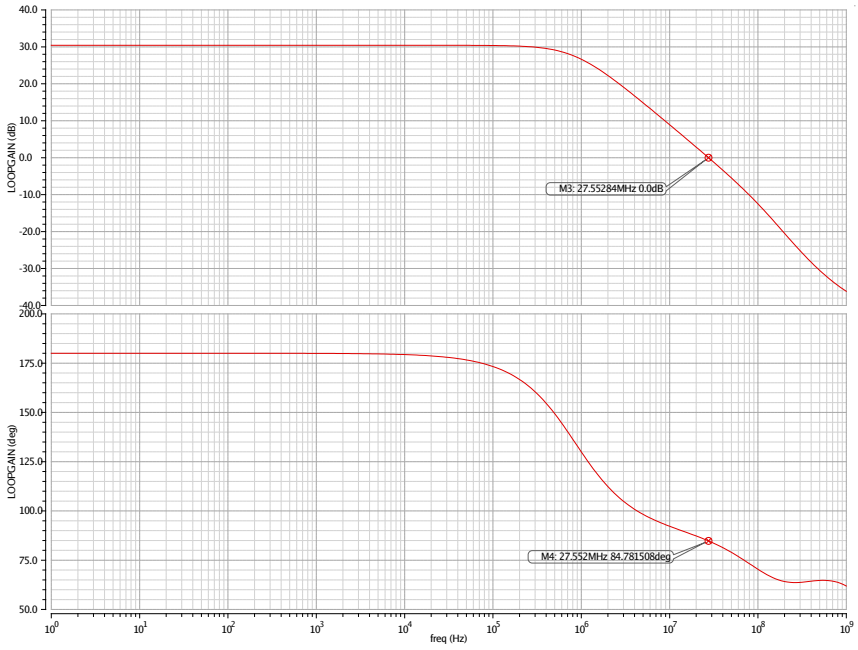


Figure 3.11: V_{cm} buffer amplifier loop gain simulation

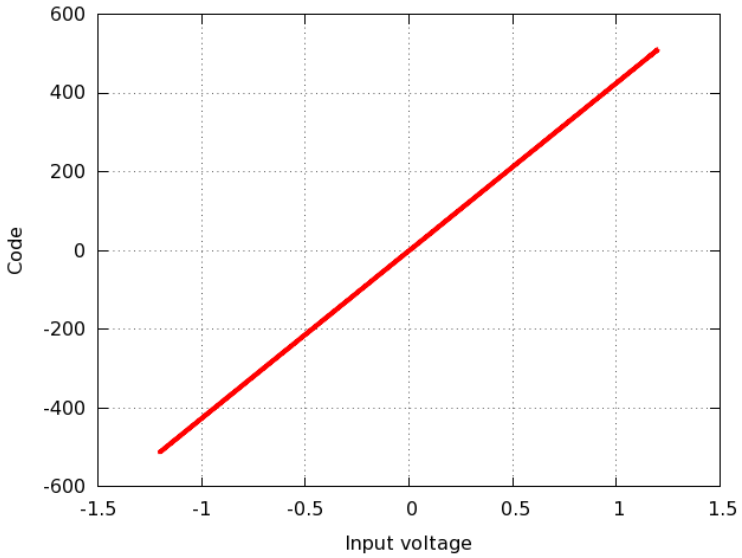


Figure 3.12: Output code vs full range input ramp

3.4.1 Ramp input

A ramped input voltage is used to determine linearity of the ADC but as the ADC control interface does not support continuous sampling, it is approximated by a series of DC values with a higher resolution than the ADC resolution. Figure 3.12 shows the simulation result of a 10-bit conversion in a nominal process corner. Since the error is expected to be less than an LSB, no nonidealities are visible at this scale. To find the error for each code hit during the ramp, a line has been fitted to the data in Figure 3.12 and the difference between the fitted line and data is shown in Figure 3.13. The errors shown in Figure 3.13 are in the order of half an LSB, which is expected as the quantization step is half an LSB. To give a better estimate of the errors, a shorter ramp with smaller step size centered around zero differential input voltage is used, see next section.

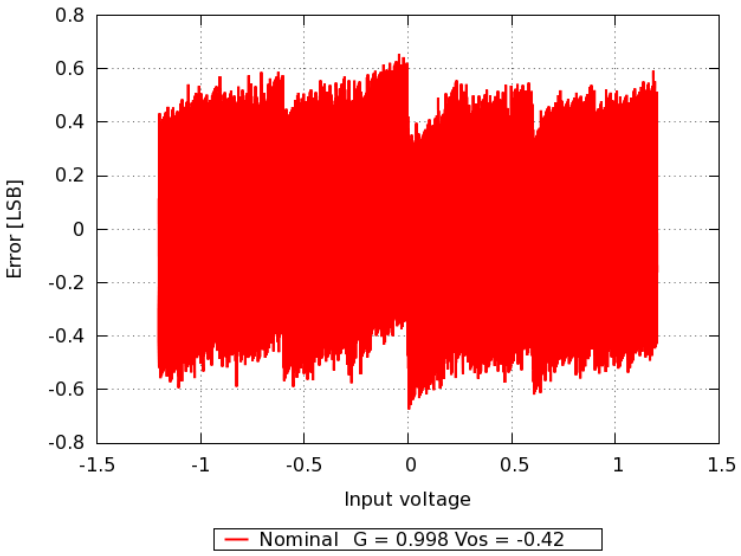


Figure 3.13: Output code error vs full range ramp input voltage

Small range ramp

Figures 3.14 and 3.15 shows the results from the simulation with a small voltage ramp centered around zero differential voltage as input. Due to the small input voltage range, only four output codes, the quantization of the ADC is clearly visible. The errors shown in Figure 3.13 show that the additional errors compared to the quantization step are small, which indicates that the errors due to settling and DC gain are below the design target of $1/4$ of an LSB.

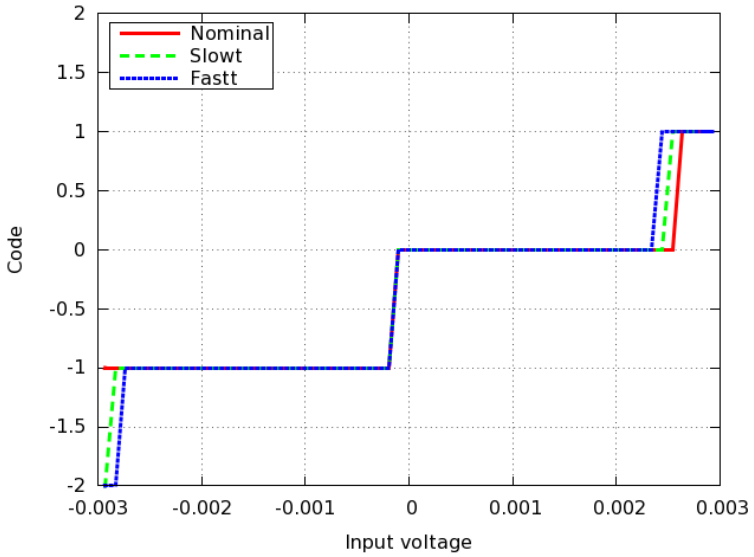


Figure 3.14: Output code vs. small range ramp input voltage

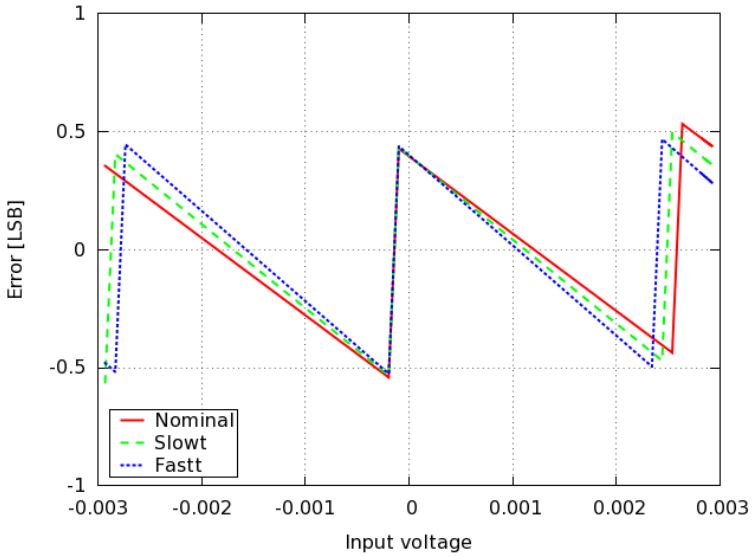
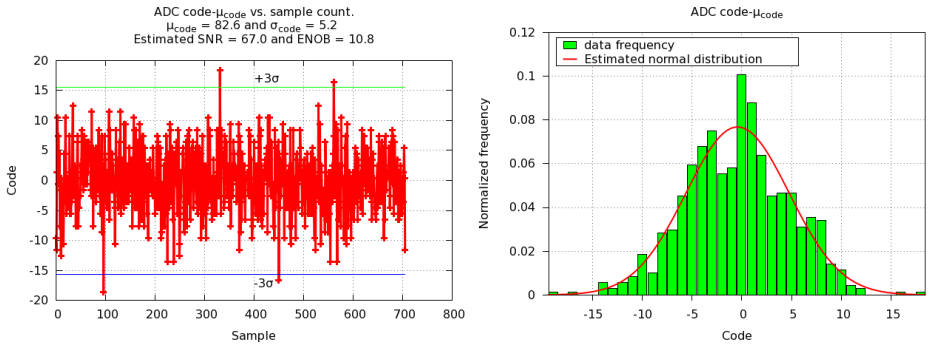


Figure 3.15: Output code error vs small range ramp input voltage

3.4.2 Noise

To estimate the noise of the ADC, transient simulations with noise were used. Several conversions were run with 15-bit resolution to estimate the standard deviation of the noise at the output of the ADC. The results for nominal process corner and temperature are shown in Figures 3.16a and 3.16b. Figure 3.16a shows a

plot of ADC output code vs sample number, with the mean value deducted from the output value. Figure 3.16b shows a histogram of the same data. The estimated standard deviation of the ADC output code is 5.2 LSB at 15-bit resolution, which correspond to a 0.16 LSB standard deviation at 10 bit resolution.



(a) Output code vs sample number **(b)** Histogram of output codes

Figure 3.16: Noise simulation result with 15-bit resolution

3.4.3 Current Consumption

The simulated current consumption of the ADC is shown in Figures 3.17 and 3.18. In Figure 3.17 the total current consumption of the ADC over temperature and process corners is shown. Figure 3.18 shows the current consumption in the nominal process corner per block. The nominal power consumption is 5.2 mA at 40 °C

3.5 Layout

Figure 3.19 show the layout of the ADC. The area of the ADC is 0.25 mm^2 with width 570 μm and height 440 μm. The blocks described in the previous sections are marked with names and it can be seen that majority of the area is used by the ADC core, which includes amplifier 1, amplifier 2, comparator, switches and capacitors. Most of the other area is used for decoupling capacitors for reference voltage and supply voltage. It is also worth mentioning that the digital part of the design is located to the left in the layout to separate it from the analog part.

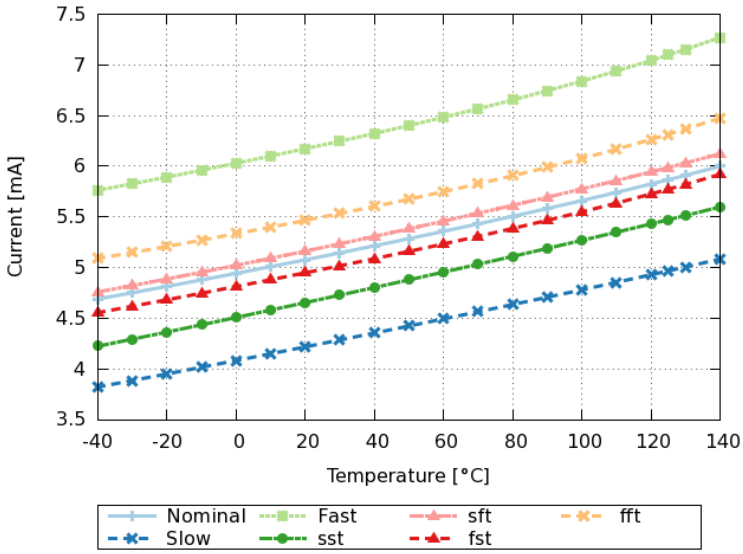


Figure 3.17: Current consumption over temperature and process corners

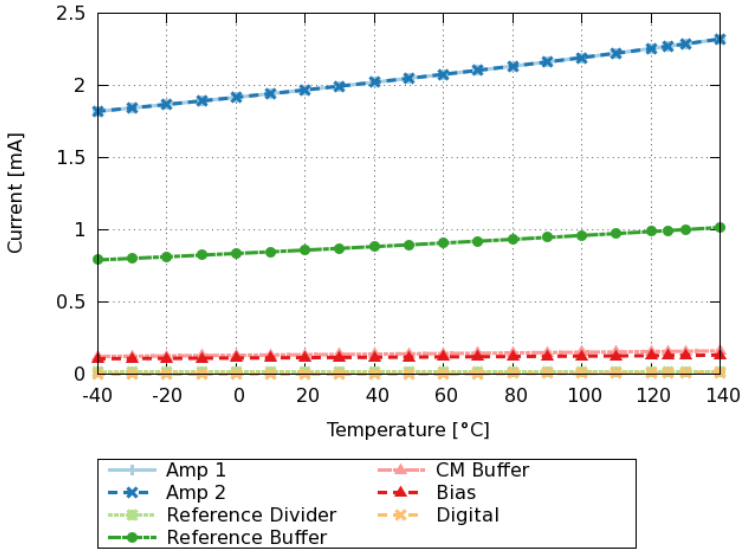


Figure 3.18: Current consumption per block

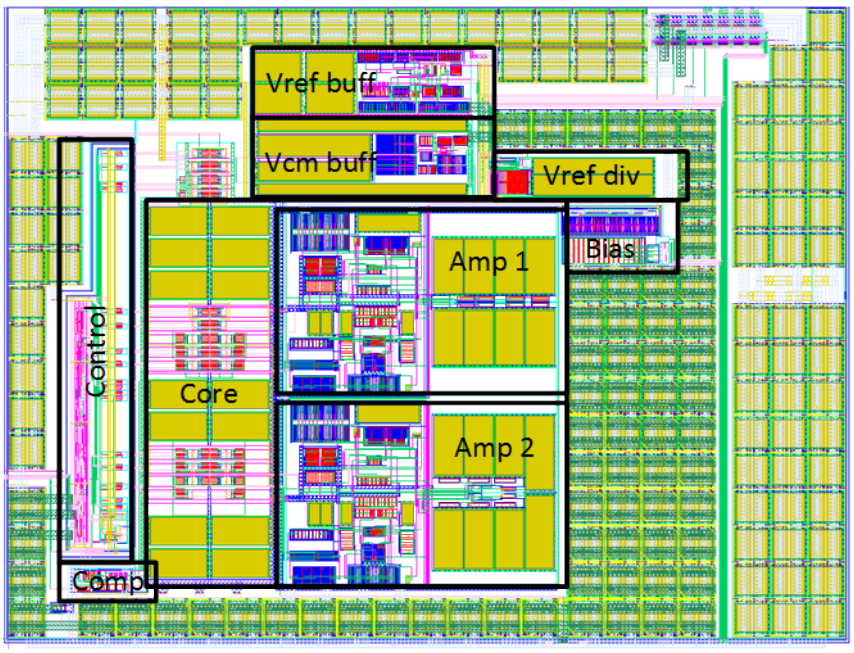


Figure 3.19: ADC Layout ($540\ \mu m\ x\ 440\ \mu m$)

Chapter 4

Measurement Results

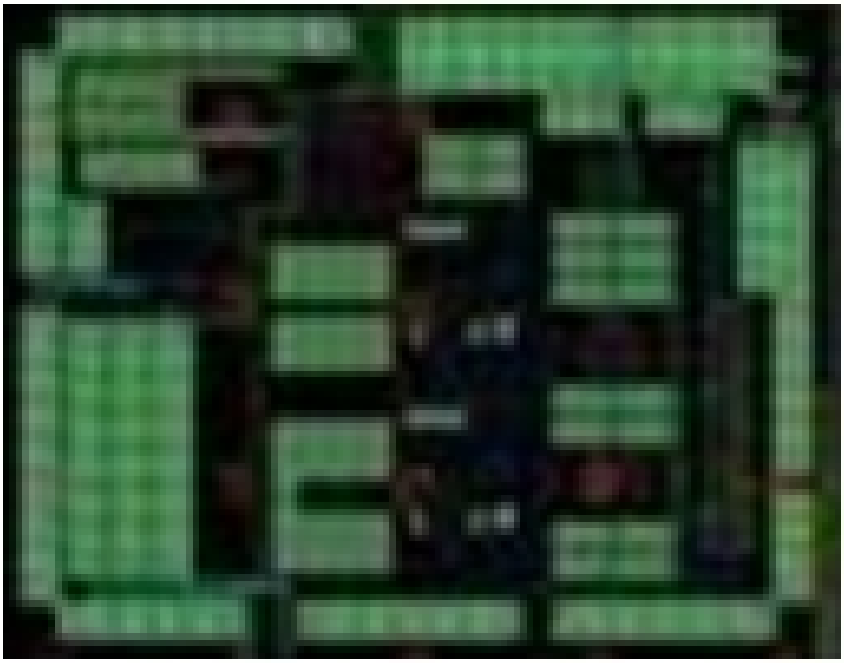


Figure 4.1: Chip photo (Only ADC part shown)

The measurements presented here were done on the fabricated chip, see photo shown in Figure 4.1. It was fabricated in a 65 nm CMOS process at TSMC. In the following sections measurement results are discussed. Section 4.1 presents results from applying a voltage ramp to the input of the ADC. Section 4.2 presents results for the ADC noise. Section 4.3 presents results for performance measures such as INL, DNL and ENOB [3].

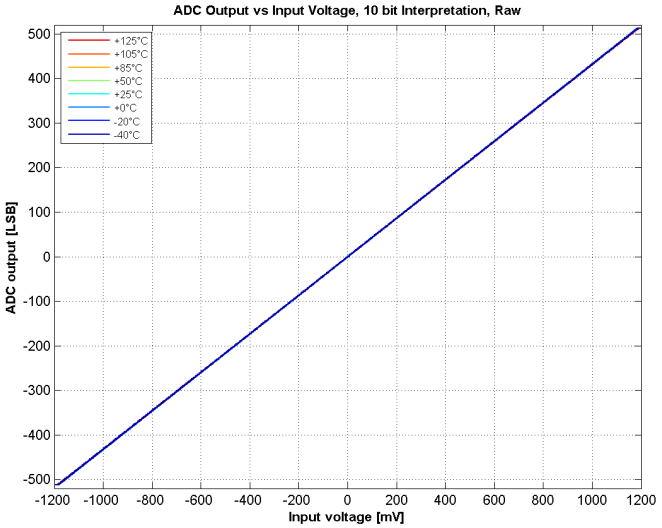


Figure 4.2: Measurement of output code vs. ramp at input

4.1 Ramp input

A voltage ramp input is used to determine the linearity of the ADC. As the ADC control interface does not support continuous sampling, it is approximated by a series of DC values with higher resolution than the ADC resolution. Figure 4.2 shows measurement results from a DC ramp applied to the ADC and as in the simulation results in Figure 3.13, no deviation from a straight line is visible. The difference between the ADC data and a fitted line is shown in Figure 4.3. The errors are slightly worse than the simulation data in Figure 4.3, but this is due to the noise present in the measurement.

4.2 Noise

Figure 4.4a and 4.4b show results from a noise measurement done with 15-bit resolution. Figure 4.4a shows the ADC output code vs. sample count with the mean value deducted. Figure 4.4b shows a histogram of the same data. The standard deviation estimated from the measurement is 7 LSB at 15-bit resolution that correspond to 0.22 LSB at 10-bit resolution.

4.3 Performance metrics

This section discusses measurements of INL, DNL and ENOB [3]. Figure 4.5 and Figure 4.6 shows INL and DNL calculated from a DC ramp applied to the ADC as described in section 4.1. Both INL and DNL are calculated using a so called

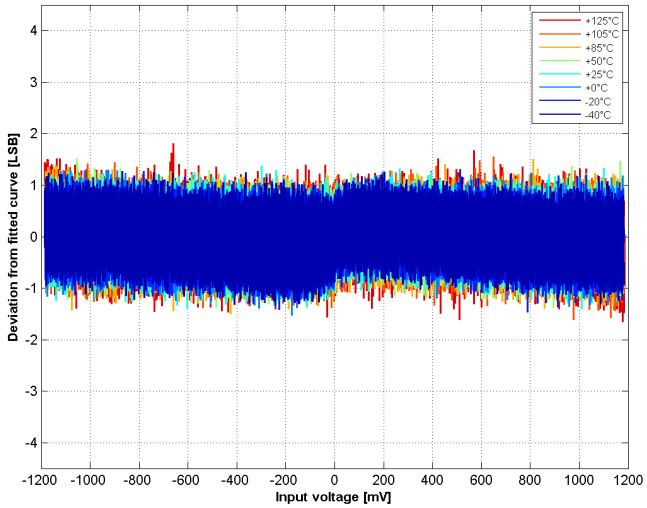
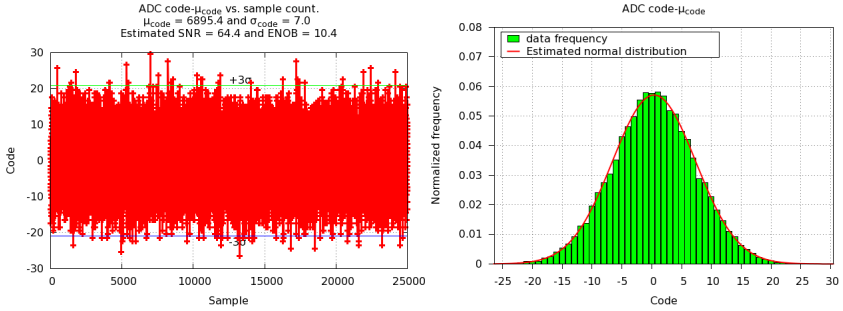


Figure 4.3: Error between measured output code and fitted linear curve.



(a) Output code vs sample count **(b)** Histogram of output codes

Figure 4.4: Noise Measurement result with 15-bit resolution

best line fit [3]. The worst measurement of INL and DNL are 0.3 LSB and 0.25 LSB respectively.

Figure 4.7 shows performance metrics DNL, INL, ENOB and offset voltage over a temperature range from -40 to +125 °C. The offset voltage stays below 0.2 LSB over the temperature range as expected due to the suppression of offset voltage in the ADC topology (see 2.5). The DNL decreases with temperature from a maximum of 0.25 LSB at -40 °C to 0.1 LSB at 105 °C, and then increases to 0.12 LSB at 125 °C. The INL is below 0.2 LSB for temperature up to 105 °C and above that increases to 0.33 LSB at 125 °C. The INL is dominated by codes at the edges of the input range for high temperature and at the middle code at low temperatures.

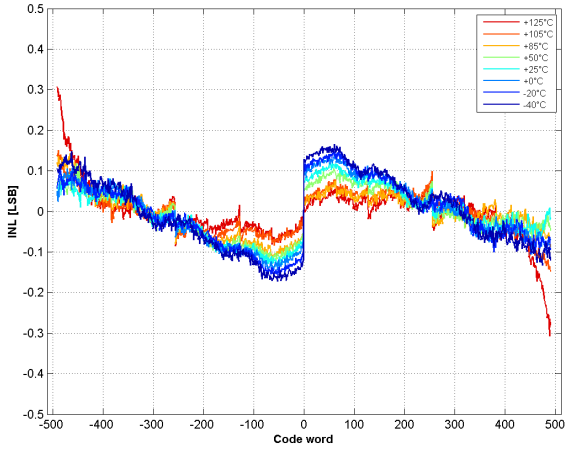


Figure 4.5: Integral Nonlinearity (INL)

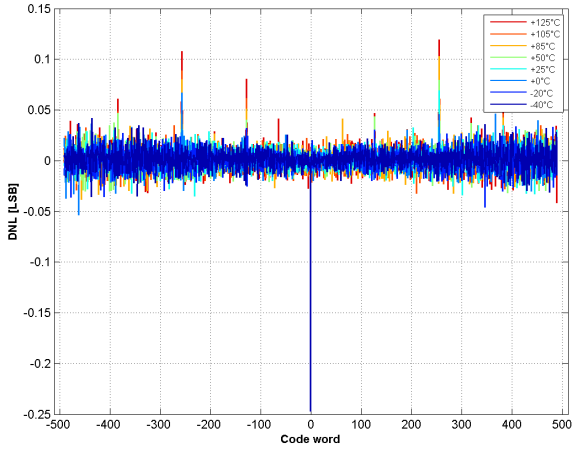


Figure 4.6: Differential Nonlinearity (DNL)

ENOB is almost flat over the temperature range, but drops from 9.55 bits at low temperature and to 9.40 bits at high temperature.

4.4 Averaged measurements

If averaging of several conversions per measurement point is done the noise present in the measurement result can be reduced. This can be seen by comparing the plots in Figures 4.8a and 4.8b. Both figures show the results of measurements of a voltage ramp applied to the ADC input and zoomed in around the center

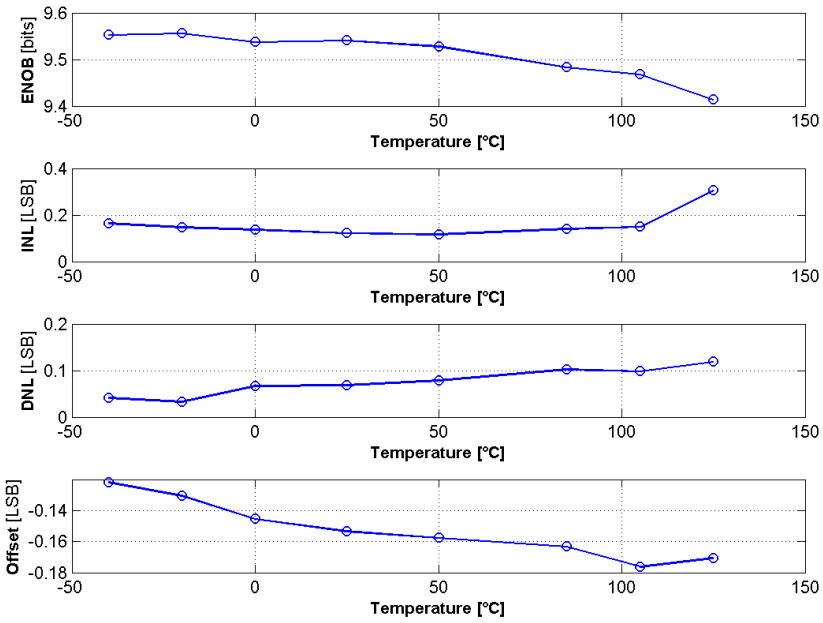
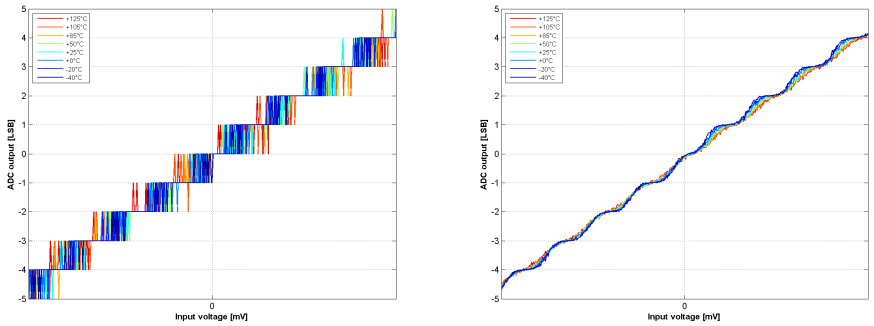


Figure 4.7: Performance metrics over temperature

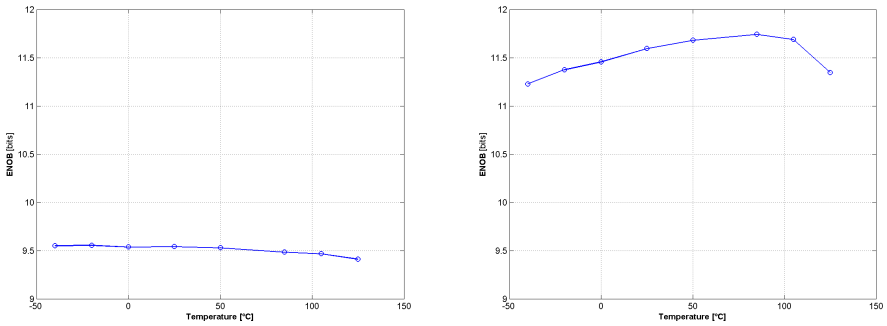
code. In Figure 4.8a the quantization levels are clearly visible, as well as the ADC noise. The noise causes the output to toggles between different codes for input voltages close to each other. When using averaging (Figure 4.8b) the quantization levels are not visible anymore, instead a small ripple is visible around the slope. This is caused by the combination of noise and averaging [7]. The noise causes each input voltage to correspond to several output codes and together with averaging, an output value closer to the input voltage than quantization noise is achieved. For this to work the averaging must be done with a higher precision than the conversions, otherwise only the ADC device noise will be suppressed and not the quantization noise.

The ENOB of the ADC measurements, without and with averaging, are shown in Figure 4.9. The ENOB for nonaveraged measurement Figure 4.9a peaks at almost 9.56 bits and the averaged measurement (Figure 4.9b) peaks at almost 11.75 bit. Thus, an improvement of over 2 bits is achieved with averaging of 100 measurements. As the ADC is intended to be used for DC measurements, this effect can be utilized to improve the measurement accuracy. It also shows that the linearity of the ADC is better than necessary for 10 bit accuracy, as linearity can not be improved by averaging.



(a) No averaging **(b)** With averaging sampling

Figure 4.8: Close-up of ADC output code vs input voltage



(a) No averaging **(b)** With averaging

Figure 4.9: ENOB: Nonaveraged and averaged

Chapter 5
Conclusion

In this thesis project a 10 bit ADC with an equivalent sampling frequency of 333 kHz has been implemented, simulated, fabricated and measured. The functions of the ADC cyclic topology is investigated and the inherent insensitivity to capacitor mismatch and amplifier offset voltage are analyzed and discussed. Schematic implementation and simulation results of the individual major blocks as well as the entire ADC are presented. Also, the layout and photo of the chip are shown.

Measurement results on the fabricated chip show that the ADC achieves an ENOB between 9.4 and 9.5, dominated by noise. The measured INL is better than 0.33 LSB, the DNL is better than 0.2 LSB for temperatures below 100 °C and below 0.25 LSB for temperature up to 125 °C. The offset voltage is below one LSB. Measurements using averaging show that the ENOB can be improved by over 1.5 bits if lower output data rate is acceptable. The averaged measurements also show that the inherent linearity of the ADC is better than 10 bits. This indicates that the ADC is over-performing for 10 bit accuracy.

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