Master of Science Thesis

A 90nm Digital Phase-Locked Loop based on a Multi-Delay Coarse-Fine Time to Digital Converter

By

Ying Wu

Supervised by Dr. Ping Lu, Lund University
Examined by Prof. Pietro Andreani, Lund University

Department of Electrical and Information Technology
Faculty of Engineering, LTH, Lund University
SE-221 00 Lund, Sweden

Abstract

Technology scaling and large-scale integration make the operating environment increasingly hostile for traditional analog design. In the area of frequency synthesis, Digital PLLs (DPLLs) provide an attractive alternative to conventional PLLs: their wide programmability allows for multi-standard application, and a digital intensive design means easy re-configurability and shorter design cycles.

In this paper, a 5GHz digital frequency synthesizer achieving a low noise for wireless RF application is presented. This architecture uses a multi-delay coarse-fine Time-to-Digital Converter (TDC) to achieve both the large detection range and fine resolution. A Digitally Controlled Oscillator (DCO) based on capacitive degeneration in LC-Tank is also implemented. The DCO achieves frequency quantization step of 300 Hz without any dithering.

Simulated phase noise at 5 GHz carrier frequency is -125 and -151 dBc/Hz at 1 MHz and 20 MHz offset, respectively. The Digital phase-locked loop (DPLL) is realized in 90nm CMOS process and consumes 14mA from a 1.2V supply.

Acknowledgments

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Ying Wu
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CHAPTER 1

1 Introduction

The integrated circuit (IC) has enjoyed an exponential growth in the last half century since it was invented in 1959. Following the famous Moore's law, the number of transistors in an IC or "chip" has doubled approximately every two years and reached more than 3.1 billion in 2011. IC products are now ubiquitous and universal in everyday life.

As the capability of the digital calculation keeps on improving in modern sub-micron CMOS processes, there is increasing interest in developing digital approaches to assistor even replace the analog functions that encounter design difficulties due to the degrading analog device characteristics such as decreasing supply voltage, and increasing leakage current and variation. People have demonstrated some successful results in various digitally-assisted analog subsystems including data converters, RF transceivers, and phase-locked loops (PLL).

Digital PLLs have recently emerged as an attractive alternative to the more traditional analog PLL, with recent results demonstrating that digital frequency synthesizers. One of the key advantages of digital PLLs over their analog counterparts is that they remove the need for large capacitors within the loop filter by utilizing digital circuits to achieve the desired filtering function. The resulting area savings are critical for achieving a low-cost solution, and the overall PLL implementation is more readily scaled down in size as new fabrication processes are utilized. Also, by avoiding analog-intensive components such as charge pumps, a much more attractive "mostly" digital design flow is achieved.

In this master work, we will explore the design and implementation of a DPLL from the basic simulink model to the transistor-level circuits in Cadence. Such DPLL achieves low phase noise comparable to analog approaches. The noise and power performance of the DPLL will be analyzed.

1.1 Organization

The ultimate goal of our research is to develop a fully integrated DPLL with low phase noise and with low power consumption.

Chapter 2 goes over the fundamental aspects of analog Phase-locked Loop and its different components such as Phase/Frequency Detector, Low-pass Loop Filter, Voltage-Controlled Oscillator and integral/fractional Divider. The two types of Digital PLL are also introduced. The basic operations of the DPLLs are also discussed.

Chapter 3 starts with the fundamental of Time-to-Digital Converter (TDC) used for DPLL. Next, the details of proposed Multi-Delay TDC and its resolution effects are presented.

Chapter 4 illustrates the Digitally Controlled Oscillator (DCO) and the methodology of different Oscillation Tuning Word (OTW). The frequency quantization effect on phase noise is analyzed.

Chapter 5 shows the structure of the DPLL. The other blocks of the DPLL, such as Digital Loop Filter (DLF), tuning bank controller, divider and TDC unwrapping circuit will be presented in details. The loop dynamics of the DPLL is also included.

Chapter 6 behavior models are built and the circuit simulation results are provided to show the noise performance and transient response.

Chapter 7 and 8 summary the thesis and further work is suggested.

CHAPTER 2

2 Phase-Locked Loop Basics

This chapter gives an overview of traditional analog Charge-Pump PLL architectures. At the same time, equations and original insights are supplied in the text. We start with the standard Integer-*N* technique. The properties of the PLL building blocks on the system level are then briefly reviewed. In addition, we will introduce the two types of Digital PLLs: Counter-assisted DPLL and Divider-assisted DPLL. The key blocks, such as Time-to-Digital Converter, Digitally Controlled Oscillator and Digital Loop Filter will be also briefly explained.

2.1 Charge Pump PLL

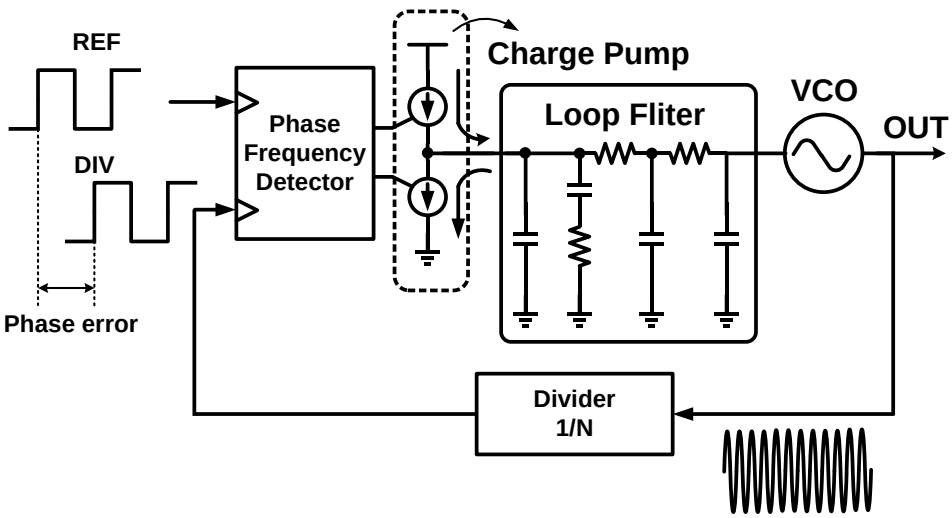


Figure 2.1. Conventional integer-N charge-pump PLL

The integer-*N* Charge Pump PLL architecture is depicted in Figure 2.1. This architecture is by far the most popular in the industry [1]. This is partly because of its simplicity in terms of external components and ease of application, but also because it can be produced with high reliability and occupy a relative small chip area. The PLL presented in Figure 2.1 consists

of a voltage-controlled oscillator (VCO), a programmable frequency divider with a divider ratio *N*, a phase frequency detector and charge-pump combination (PFD/CP) and a loop filter. In addition, the architecture also comprises a reference crystal oscillator. When the loop is locked the phase of the divided output signal accurately tracks the phase of the reference signal. The phase-lock process forces the frequencies of f_{div} and f_{ref} to be equal. Relating F_{out} to f_{div} and f_{ref} one readily obtains:

$$F_{out} = N.f_{ref} = N.f_{div} \tag{2.1}$$

If the division ratio *N* is programmable in steps of 1, then F_{out} can be stepped with a minimum step size equal to f_{ref}.

2.1.1 Phase/Frequency Detector

The phase detector compares the phase of f_{ref} and f_{div} signals (Figure 2.1) and generates an error signal which is proportional to their phase difference. The most commonly encountered phase detectors are the tri-state Phase/Frequency Detector (PFD), as shown in figure 2.2. It consists of two D-type flip-flops (D-FF) which have their D inputs connected to the active level. The main advantage of the D-FF based implementation is its compactness.

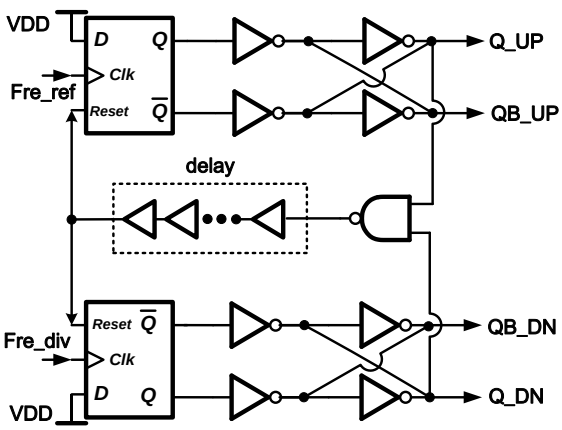


Figure 2.2. Circuit of Phase/Frequency Detector

The upper D-FF, which is clocked by generates the up signal *Q_UP*. The lower D-FF, clocked by generates the down signal *Q_DN*. The NAND gate

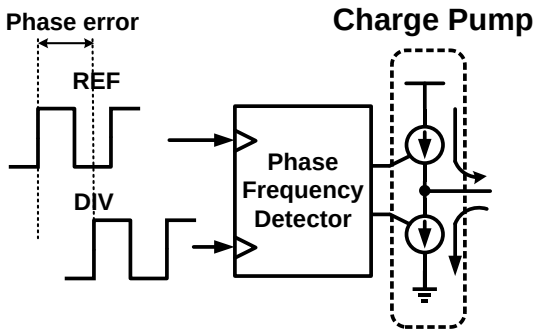


Figure 2.3. PFD combined with single-ended charge-pump

monitors the *up* and *down* signals and generates the *reset* signal for the D-FFs at the moment both outputs become active. The *up* and *down* signals are used to switch the current sources in the charge-pump CP, as illustrated in figure 2.3. When *up* is active, a current with magnitude of I_{CP} is sourced by the charge-pump; conversely, when *down* is active, current is sunk into the charge-pump. When both *up* and *down* are inactive, no current flows into or out the output node of the charge-pump. The output is a high impedance node, under all circumstances.

In the figure 2.3, that the duty-cycle of the *up* and I_{out} signals grow in proportion to the phase difference $\Delta\theta = \theta_{ref} - \theta_{div}$ of the input signals. The relationship between average current I_{out} and $\Delta\theta$ can therefore be written as follows

$$I_{out} = I_{cp} \frac{\Delta\theta}{2\pi} \tag{2.2}$$

The gain K_{pd} of the PFD/CP combination, defined as the average charge pump output current for a given phase difference at the input of the PFD, can then be simply expressed as

$$K_{pd} = \frac{I_{out}}{2\pi} = \frac{I_{cp}}{2\pi} \quad \text{[A/rad]} \tag{2.3}$$

2.1.2 Low-pass Loop Filter

The loop filter provides the current-to-voltage conversion from the charge-pump signal to the tuning voltage input of the VCO. The purity of the tuning voltage determines to a great extent the spectral components of the VCO output signal. The output of the charge-pump vanishes when the

phase difference between the input signals of the PFD is zero. This is the ideal locking position for the loop: there is no current injection into the loop filter, and therefore no degradation of spectral purity performance of the VCO. Phase lock with zero phase error, for all possible output frequencies, requires a loop filter with infinite DC gain. In other words, the loop filter must perform an integration operation on the charge-pump output signal. As the pump output is a node with an ideally infinite output impedance, a simple capacitor suffices to realize the integration function at the loop filter.

On the other hand, the loop "already" contains a perfect integrator—the VCO. So, the addition of another perfect integrator in the loop's transfer function leads to instability and oscillatory behaviour, unless further measures are taken to increase the loop's phase margin. In order to do that, very often a resistance is placed in series with the integrator capacitor. This adds a zero to the trans-impedance function of the loop filter. Hence, the RC combination causes a phase advance in the PLL open-loop response, potentially solving the stability problem

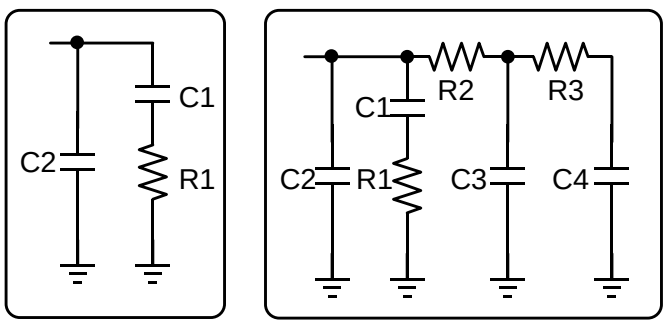


Figure 2.4. Types of passive loop filter: (a) 2nd order; (b) 4th order

Two passive loop filter configurations are shown in Figure 2.4. The trans-impedance function of 2nd order loop filter is given below.

$$H_{lp}(s) = \frac{1 + s(R_1(C_1 + C_2))}{sC_1(1 + sR_1C_2)} \tag{2.4}$$

2.1.3 Voltage-Controlled Oscillator

The voltage-controlled oscillator (VCO) generates the output signal of the PLL. The frequency of the VCO signal is dependent on the voltage at its tuning input. The relationship between the output frequency F_{out} and the

tuning voltage V_{tune} can be written as $F_{out} = f_{center} + K_{vco}(V_{tune}).V_{tune}$ where $K_{vco}(V_{tune})$ is the VCO gain factor in [Hz/V] and f_{center} is the output frequency when the tuning voltage is 0 Volt. In the basic PLL configuration of Figure 2.1 the frequency range of the VCO must cover the total tuning range of the intended application. The combination of a wide tuning range with good phase noise performance is a difficult task [2].

The control action of the loop is based on a phase error signal, namely the difference of the θ_{div} and θ_{ref} signals in Figure 2.1. The relationship of the phase θ_o of the VCO signal with the tuning voltage V_{tune} can be derived as follows

$$\theta_o = \int 2\pi F_{out}(t)dt = \int 2\pi(f_{center} + K_{vco}(V_{tune}).V_{tune})dt \tag{2.5}$$

After phase and frequency lock is achieved, the DC value of V_{tune} is (nearly) constant, so that the dependency of K_{vco} on V_{tune} can be neglected. Taking the Laplace transform of (2.5) yields

$$\theta_o = \frac{2\pi K_{vco} V_{tune}(s)}{s} \tag{2.6}$$

2.1.4 Frequency Divider

The digital frequency divider is responsible for frequency scaling within the loop. The frequency f_{div} of the output signal equals the frequency f_{in} of the input signal divided by an integer number. The effect of the frequency division on the phase relationship between input and output signals is derived next. We will calculate the effect of frequency division on a signal. From this information we may derive a model for the frequency divider in the phase domain. The phase of the input signal is given by

$$f_{div} = \frac{f_{in}}{N} \tag{2.7}$$

$$\theta_{div}(t) = \int 2\pi f_{div}(t)dt = \frac{2\pi f_{in} t}{N} \tag{2.8}$$

$$\theta_{div}(t) = \frac{\theta_{in}(t)}{N} \tag{2.9}$$

An important conclusion from (2.9) is that the frequency divider's phase transfer function $\theta_{div}(t)/\theta_{in}(t)$ is simply a gain factor with value 1/*N*.

2.1.5 Fractional-N Architecture

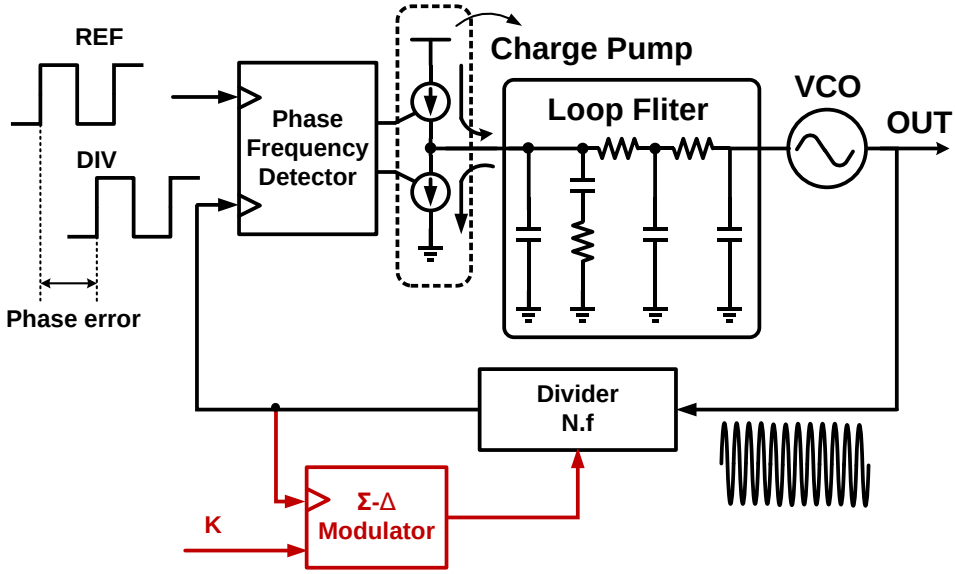


Figure 2.5. Fractional-N PLL Architecture

Fractional-*N* techniques enable a PLL synthesizer to generate output frequencies with a smaller step size than the loop's reference frequency [3]. The fundamental fractional-*N* PLL architecture is depicted in Figure 2.5. Suppose that the desired output frequency F_{out} is a non-integer multiple of the reference frequency f_{ref}.

$$F_{out} = (N + .f) \times f_{ref} \tag{2.10}$$

So, N is the integer and $.f$ is the fractional (decimal) part of the division ratio. Therefore, the average value of the divider ratio is

$$N_{avg} = N + .f \tag{2.11}$$

$\Delta\Sigma$ modulation techniques are widely applied to A/D conversion of narrowband analog signals [4]. The method is used in the digitisation of (narrowband) input signals with coarse quantization steps. To compensate for the coarse quantization levels, oversampling and noise-shaping principles are applied. In this way, quantization noise is pushed away from the frequency range of interest. The SNR and dynamic range at the relevant frequency range is therefore improved, and the shaped quantization noise can be eliminated by filtering.

A variation of the fractional-*N* principle employs a $\Delta\Sigma$ modulator (or a noise shaper) to implement the ratio control block, as depicted in Figure 2.5.

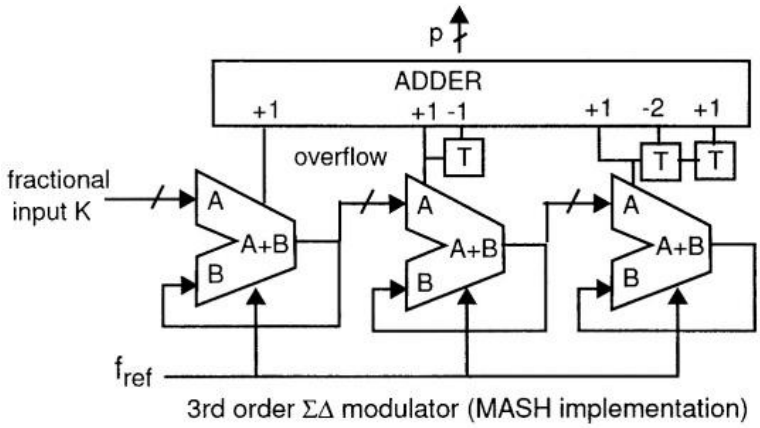


Figure 2.6. MASH implementation of a 3rd order $\Delta\Sigma$ modulator based on digital accumulators, on an output adder stage and on delay elements T

The divider operates as the coarse quantiser, as only integer division ratios can be realized. By switching of the division ratio between two (or more) integers, the average value of the division ratio is generated at the output of the PLL. In fact, it has been shown that an accumulator can be seen as an implementation of a first-order, digital $\Delta\Sigma$ modulator.

First-order modulators are known to generate spurious frequency components in their output signal, in response to a DC input signal. This is consistent with the observation of spurious signals at the output of a fractional-*N* PLL. With higher order modulators the switching of the divider ratio is randomised, such that the spurious signals are (ideally) no longer present in the output signal of the PLL. Instead, the designer has to cope with an extra source of phase noise in the loop — the shaped quantization noise generated by the $\Delta\Sigma$ modulator. The exposition proceeds with a short review of modulators which are based on a multi-stage noise shaping (MASH) structure. Such implementations have been extensively reported in the literature [4].

The main advantage of the MASH structure is that the hardware implementation is simply a cascade of digital accumulators as shown in Figure 2.6. In addition, the absence of feedback between the different accumulators ensures the stability of higher order modulators.

2.2 Digital PLL

Mainstream CMOS technology scaling in most modern silicon ICs has always favored digital circuits, as they allow for more flexibility and programmability compared to their analog counterparts. As a result, the

phase locked loop has been explored towards a mostly digital architecture for both wireless and wireline application. Unlike an analog PLL, the digital PLL potentially benefits from eliminating the area consuming passive elements and leakage current issues associated with a large MOS capacitor. This makes the digital phase-locked loop frequency synthesizer an attractive topic in both academic and industry fields [5].

Currently, there are two main types of DPLL architectures which are used for high performance frequency synthesis: counter-assisted digital PLL (CDPLL) and divider-assisted digital PLL (DDPLL).

2.2.1 Counter-assisted Digital PLL

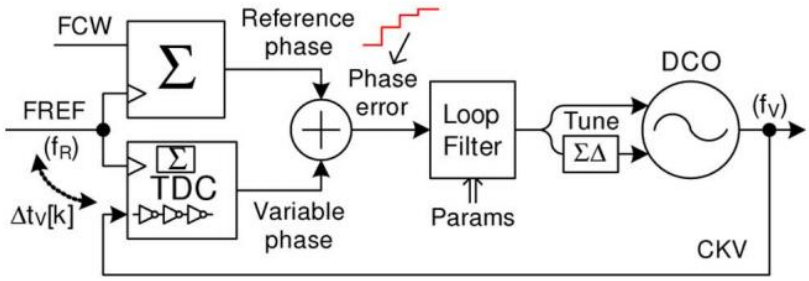


Figure 2.7. Counter-assisted digital PLL [6]

Beyond the classical analog approach, several DPLL-based architectures have been recently proposed. A step forward to more digital operation is done replacing the combination of multi-modulus divider and PFD-CP by a TDC, which means the TDC is in the feedback path directly comparing the output signal with the reference signal. As shown in figure 2.7, the TDC is used to compute the ratio between the output and the reference frequency. This ratio is compared in the digital domain with the Frequency Control Word (FCW) which yields the frequency error, which is then integrated to provide a phase error that exactly corresponds to the phase difference between the output signal and the reference signal, except for a constant phase error offset arising from integration [6].

2.2.2 Divider-assisted Digital PLL

Another DPLL-based architecture is analogous to the conventional analog PLL [7]. The TDC replaces the PFD and Charge Pump; the digital loop filter replaces the analog RC loop filter and the Voltage-Controlled Oscillator (VCO) is replaced by the Digitally Controlled Oscillator (DCO). This topology reduces the synthesizer area cost and enables simple loop reconfigurability.

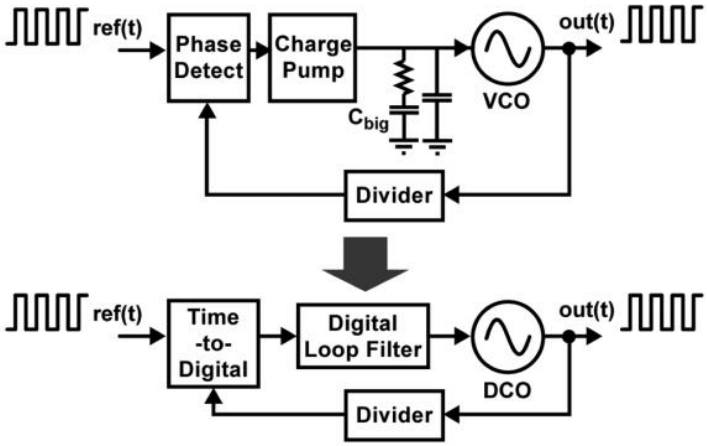


Figure 2.8. Progression from analog to divider-assisted digital PLL [7]

A disadvantage versus the analog counter-part is immediately evident. Two additional noise sources inside the loop degrade the output spectral purity, i.e. the quantization noise of both the DCO and TDC. Therefore, counter-measures to reduce the performance gap with analog synthesizers are thus required. The impact of DCO quantization noise can be reduced by means of reducing the frequency resolution. Similarly, the quantization noise of TDC can be reduced by minimizing the time resolution. We will discuss in the next chapters.

CHAPTER 3

3 Time-to-Digital Converter

Time-to-digital converters (TDC) – certainly most engineers link this expression with Digital phase-locked loops (DPLL) where a TDC serves as phase detector. Interestingly, TDCs have been used for more than 20 years in the field of particle and high-energy physics, where precise time-interval measurement is required. Other applications cover time-of-flight measurement, or measurement and instrumentation applications such as digital scopes and logic analyzers. Currently the micro-electronics community rediscovers time-to-digital converters and this is the justification for a complete book on this topic. While the digital PLL is the first and most famous TDC application others emerge rapidly [8].

3.1 Fundamental of TDC

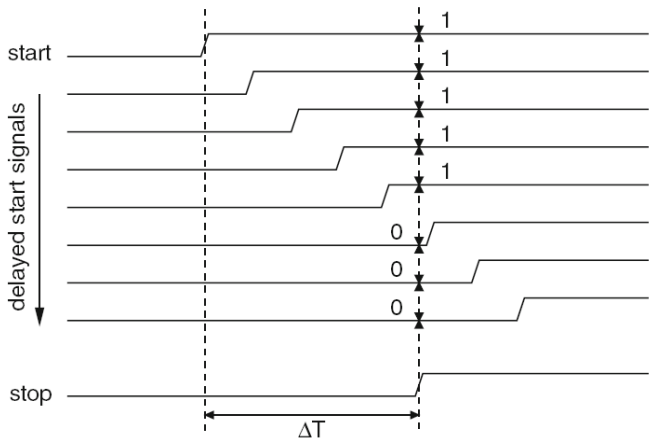


Figure 3.1 Operating principle of time-to-digital converter

Figure 3.1illustrates the operating principle of a TDC based on a digital delay-line. The reference clock which is in a more general sense an arbitrary start signal is delayed along the delay-line. On the arrival of the stop signal the delayed versions $start_i$ of the start signal are sampled in parallel. Either latches or flip-flops can be used as sampling elements. The sampling process freezes the state of the delay-line at the instance where the stop signal occurs. This results in a thermometer code because all delay

stages which have been already passed by the start signal give a HIGH value at the outputs of the sampling elements, all delay stages which have not been passed by the start signal yet give a LOW value. The position of the HIGH-LOW transition in this thermometer code indicates how far the start signal could propagate during the time interval spanned by the start and the stop signal. Hence this transition is a measure for the time interval. The number N of all sampling elements with a HIGH output is related to the measurement interval ΔT according to

$$N = \left\lfloor \frac{\Delta T}{T_{LSB}} \right\rfloor \tag{3.1}$$

where T_{LSB} is the delay of a single delay element in the delay-line. The time interval ΔT can be calculated from the number of HIGH outputs by

$$\Delta T = NT_{LSB} + \varepsilon \tag{3.2}$$

where ε describes the quantization error that arises as a delay element has been either passed by the start signal yet or not. Any intermediate state is not possible. The quantizer characteristic of a TDC and its non-idealities are discussed later in this chapter.

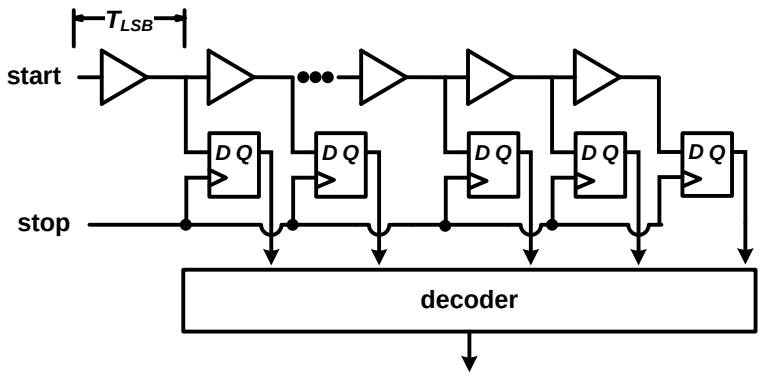


Figure 3.2 Implementation of basic delay-line based time-to-digital converter

An implementation of the basic delay-line TDC is shown in Fig.3.2. The start signal ripples along a buffer chain that produces the delayed signals start$_i$. Flip-flops are connected to the outputs of the delay elements and sample the state of the delay-line on the rising edge of the stop signal. The stop signal drives a high number of flip-flops so a buffer-tree (not shown) is required. Any skew in this buffer-tree directly contributes to the non-linearity of the TDC characteristics. For a correct thermometer code the skew between adjacent branches in this tree has to be smaller than T_{LSB} which makes the design challenging.

3.2 Multi-Delay Coarse-Fine TDC

The resolution of the delay-line based TDC discussed in the previous section is limited by the delay of the buffers. In order to achieve the resolution better than single buffer, a multi-delay coarse-fine high resolution TDC is proposed in this work.

The TDC has a coarse delay line with different delay cells [9]. In classical TDC [5], the delay cells should be matched to be as equal as possible. However, as we noted, only a number of delay cells will be used when the loop is in the locked state. The rest part of delay cells are used only at acquisition and will thus not affect the phase noise performance. Therefore, the multi-delay structure releases the requirement for a large number of delay cells which should cover the whole period of reference clock. This reduces the power consumption and saves the chip area. The highest time resolution of the coarse delay line is a single buffer delay (two inverters), approximate 20ps in 90nm CMOS process. In order to increase the time resolution which dominates the in-band noise of PLLs, a coarse-fine TDC based on time amplifier (TA) is introduced [10]. The TAs are utilized to amplify the time residue with a high gain in order to resolve the time interval better than a single buffer delay. As such, the combination of multi-delay and coarse-fine architectures achieves both the large detection range and high time resolution.

3.2.1 Multi-delay structure

In traditional TDC, the delay cells are matched as equal as possible. However, when the PLL is in the locked state, the loop is configured to type-II, which means that only a small part of the buffers are activated in maintaining the feedback. Therefore, a TDC with different delay-time cells is implemented, as shown in Fig.3.3. The complete delay chain has been divided into four segments. The first segment has the shortest delay-time cells, eight of which are used for the time amplification for the fine TDC (FTDC). The other three segments use current-starved inverters to increase the delay time and reduce the power consumption.

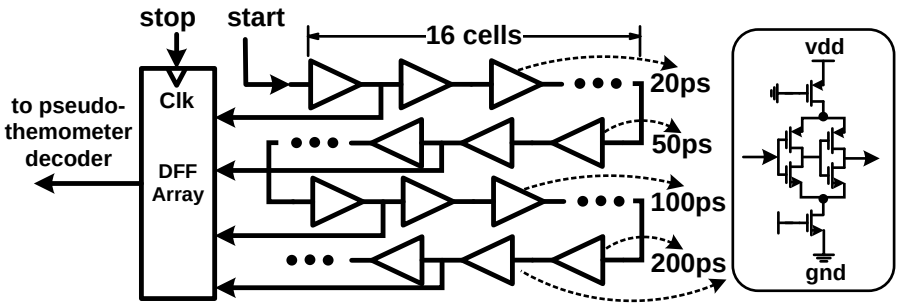


Fig.3.3 Multi-delay architecture of TDC

3.2.2 Coarse-Fine structure

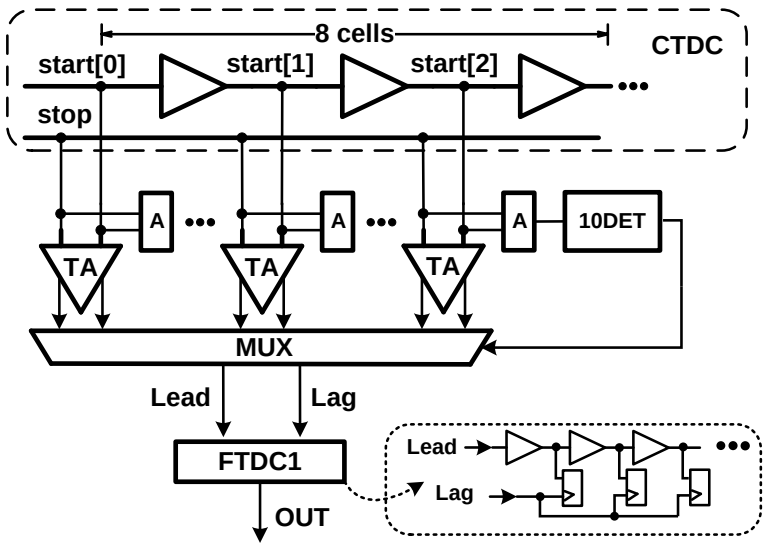


Fig.3.4 Coarse-fine architecture of TDC

The coarse-fine architecture resolves intervals less than a buffer delay by amplifying the time residue. The TAs used in this design have a high gain (=16 to use a 4-bit fine TDC) and a linear range large enough to cover the shortest delay (T_d = 20ps) of one stage in the coarse line. As shown in Fig.3.4, the time difference between the edge of each buffer, *start[k]*, and the edge of *stop*, creates every possible time residue. While the arbiters (A) determine which of the residues is the critical one, and then the detector (DET) identifies the critical amplified residue to be sent to the FTDC for the fine conversion. The FTDC consists of one buffer chain which is similar to the traditional TDC [5]. The time resolution of FTDC is equal to the

shortest delay cells in coarse line, about 20ps. Therefore, the final resolution of the TDC achieves 1.25ps (20ps/16).

3.2.3 Time Difference Amplifier

The Fig.3.5(a) details the circuit of TA. It exploits the metastability of SR latch to slow down the output [10]. The TAs used in this design must have a high gain (16 to use a 4 b fine-TDC) and a linear range large enough to cover the propagation delay ($T_{d=}$20ps) of one stage in a delay chain. In Fig. 3.5(a), we show the designed TA where T_{off} is due to two inverters. Realizing both T_{off} and T_d with inverters makes it easy to obtain the sought linear range across PVT variation. The value of is designed to be around 80ps, which is much larger than T_d in order to have better linearity. Another consequence of the large T_{off} is lowered gain, as depicted in Fig. 3.5(b). To recover the gain, the ratio C/g_m for each NAND gate is increased by adding more capacitance at the output of the latches and by reducing the g_m of the transistors, which provide a positive feedback during regeneration. This results in a new characteristic having a gain of 16 and a useful range of $\pm$80ps, which is adequate for our needs. The capacitors added to boost the gain are implemented with MOSFETs because they take up less space.

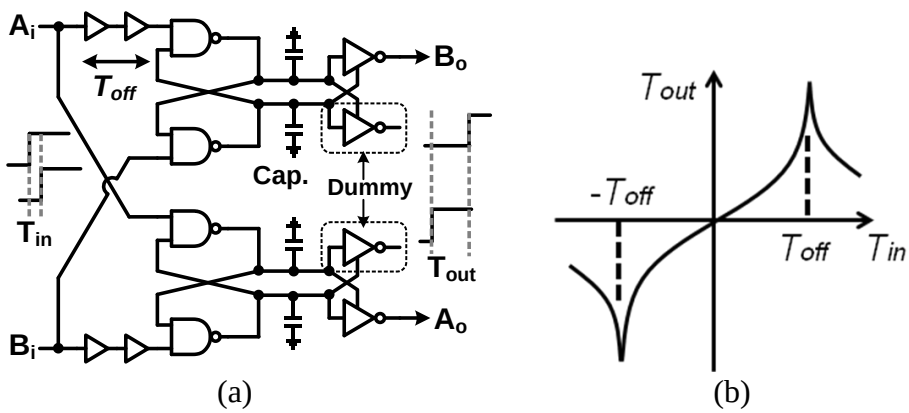


Fig.3.5 (a) Proposed TA. (b) Gain curve of TA

The gain of TA which is express as

$$A_T = \frac{2C}{g_m T_{off}} \tag{3.3}$$

3.2.4 Sense Amplifier Based Flip-Flop and Arbiter

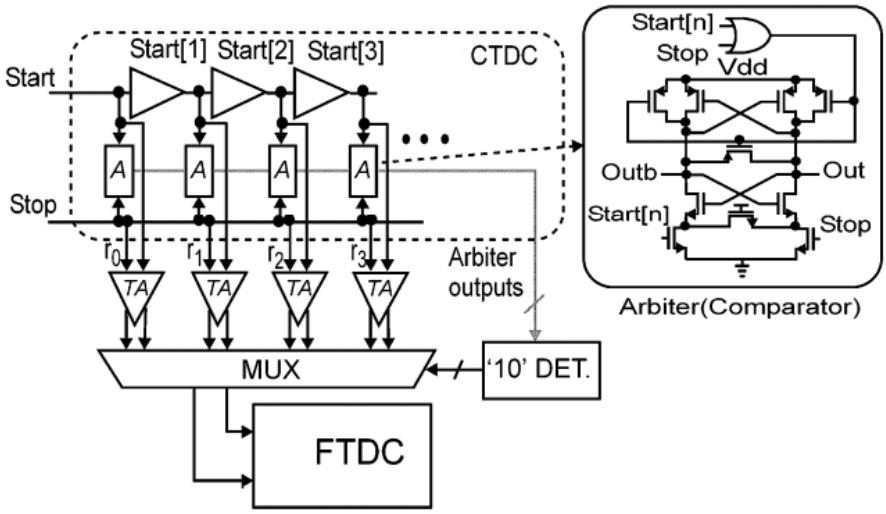


Fig.3.6 The arbiter used with TAs

Just as an ADC requires a latching comparator, so does a TDC. Either a flip-flop or an arbiter can be used as a comparator of which output determines the output codes of the TDC. However, conventional flip-flops, such as the sense-amplifier-based flip-flop in [10], create mismatch in the data and clock propagation path, which results in a large time offset. This time offset requires large over-range in FTDC, which means additional delay taps. To reduce the over-range, the arbiter in Fig.3.6 is used because it has equal delay from its two inputs, Start[n] and Stop, to the output .

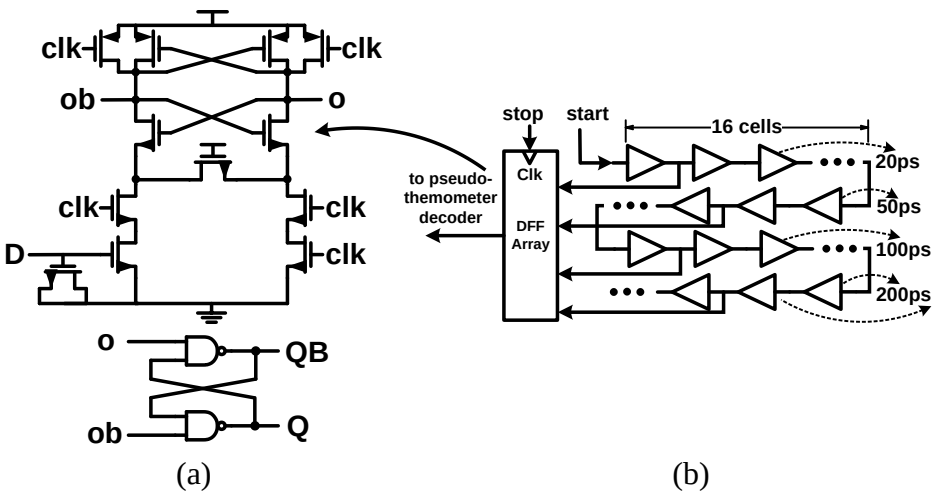


Fig.3.7 The small setup-time flip-flop in Coarse/Fine-TDC

The SR latch shown in Fig.3.6 is not appropriate choice for the Coarse/Fine TDC [11]. The time amplifier (TA), which amplifies the dissimilar metastable dynamics of two latches, produces meaningless results if the latch inputs change during regeneration. This is exactly what happens in our DPLL, where two different input frequencies are applied to the inputs of the TDC, one is reference clock and the other is feedback clock from divider. The flip-flop in Fig.3.7 has the small setup time which means the amount of time the data signal should be held steady before the clock event .

3.2.5 Residue selection MUX

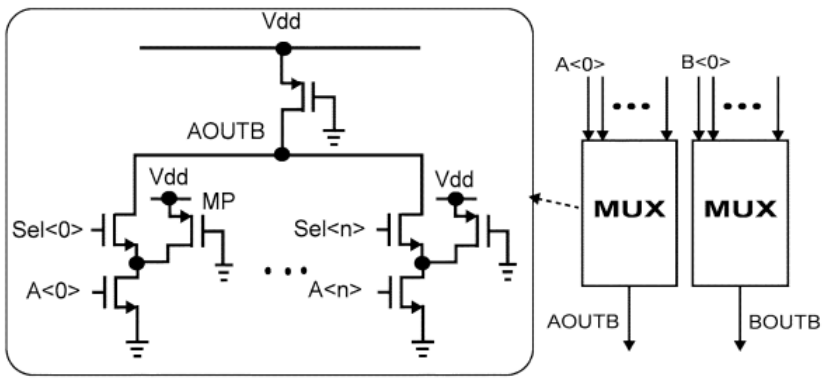
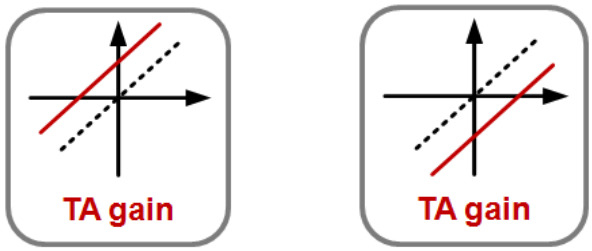


Fig.3.8 Residue selection MUX

The circuit detail of the residue selection MUX is shown in Fig.3.8. The MUX consists of an array of nMOS pull-down devices connected to a common pMOS pull-up, which is a ratioed logic circuit. The signal feedthrough from unwanted residues to the output causes timing uncertainty. The selection device on top of the input transistor blocks the signal feed-through from the input to output node. Also, the charge sharing between the output and the drain of input nMOS after the selection signal, *S[k]*, becomes active, can introduce timing error. This error is avoided by the weak pull-up transistors, MPs, which charge every node to a high level to obtain smooth transition at the output.

3.2.6 Digital Calibration Techniques for Time Offsets

As can be seen in the typical operational amplifier, the device mismatch in a TA shifts the zero crossing of the gain curve, which appears as a TA offset, as shown in figure 3.9. This offset can be corrected by calibration in the following way.



(a) (b)

Fig.3.9 (a) Positive time offset. (b) Negative time offset

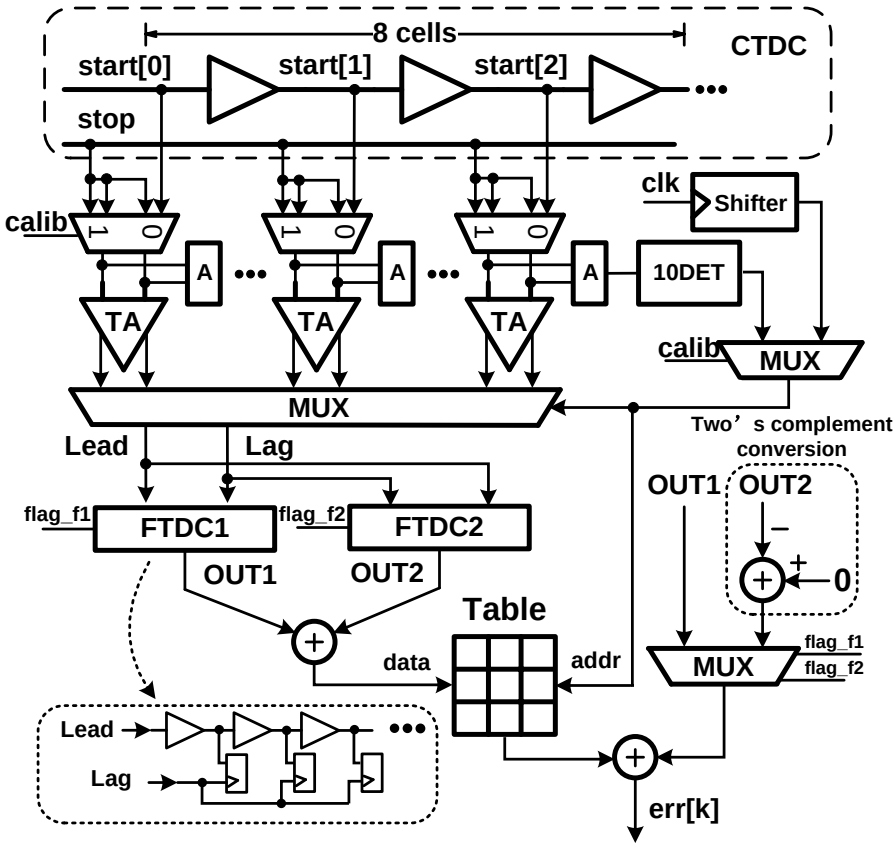


Fig.3.10 Coarse-fine TDC with calibration techniques

As shown in figure 3.10, the *Calib* switches the multiplexer (MUX) to feed though the same *stop* signal to both inputs of the TA, which creates zero input, and thus the amplified offset is quantized by the FTDC and stored in the look-up table, and then the value in the table will correct the output of the FTDC during normal operation. Since the offset value can be

positive or negative and also large enough to drive the FTDC into over-range, double FTDCs with opposite direction are introduced and the number of stages is doubled (4+1 bits). In particular, the outputs of two FTDCs are always expressed as absolute value. Therefore, the output from FTDC2 should be converted to two's complement. This offset calibration process is sequentially performed during the startup by shifting the control pulse signal to select each TAs.

3.2.7 Look-up Table

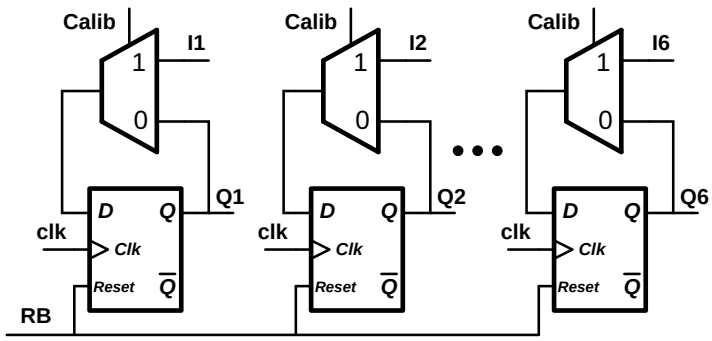


Fig.3.11 Data cell in look-up table

As illustrated in figure3.11, when the Calib is 'high', the data (time offsets) are stored in the DFFs. It will be updated on every rising-edge of the clock. However, during the normal operation, the DFFs are 'locked' by the MUX and the outputs of DFFs will not be changed on the rising-edge of the clock. In order to store the time offsets of eight TAs, we need the same number of the cells in look-up table. The address cells in look-up table consist of eight selectors, which are used to activate the corresponding data cell.

3.3 TDC Resolution Effect on Phase Noise

In closed-loop operation, the TDC quantization Δt_{res} of timing estimation affects the phase noise at the DPLL output [5]. Under a large-signal assumption (spanning multiple quantization levels), the variance of the timing uncertainty is

$$\sigma_t^2 = \frac{(\Delta t_{res})^2}{12} \tag{3.4}$$

The phase noise (rad) is obtained by normalizing the standard deviation of the timing error to the unit interval and multiplying by 2π radans:

$$\sigma_{\phi} = 2\pi \frac{\sigma_t}{T_V} \tag{3.5}$$

The total phase noise power is spread uniformly over the span from dc to Nyquist frequency. The single-sided spectral density is, therefore, expressed as

$$L = \frac{\sigma_{\phi}^{\ 2}}{f_R} \tag{3.6}$$

The TDC Noise contribution, within the loop bandwidth, at the DPLL RF output is [5]

$$S_{TDC} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{res}}{T_{DCO}}\right)^2 \frac{1}{f_{REF}} \tag{3.7}$$

where Δt_{delay} denotes the delay time of a buffer cell, T_{DCO} the period of RF output, and f_{REF} is the frequency of reference clock. For example, Δt_{res} =1.25ps, T_{DCO} =1/5GHz, f_{REF} =50MHz, we obtain S_{TDC}= -116dBc/Hz

CHAPTER 4

4 Digitally Controlled Oscillator

The digital solution to control the oscillating frequency could generally be summarized as follows [12]: A method of weighted binary switchable capacitance devices, such as varactors, is used. An array of varactors (Fig. 4.1) could be switched into a high or low-capacitance mode individually by a two-level digital control voltage bus, thus giving very coarse step control for the more significant bits, and less coarse step control for the less significant bits (LSBs). To achieve very fine frequency resolution, the LSB could possibly be operated in analog fashion.

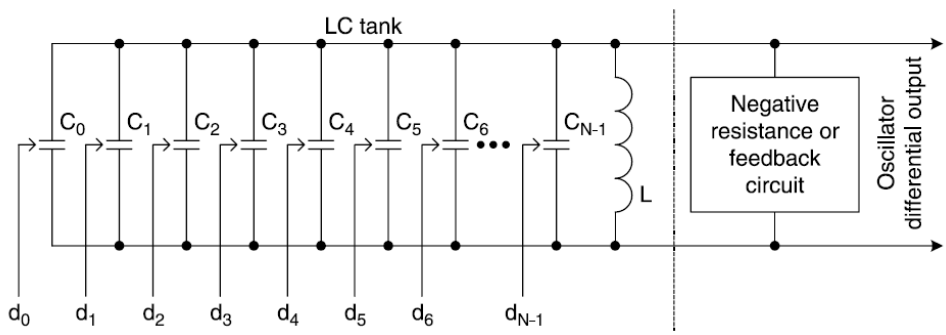


Fig.4.1 LC-tank based oscillator with switchable capacitors

4.1 Fully Digital Control of Oscillating Frequency

The idea behind a digitally controlled LC tank oscillator was shown from a higher system level in Fig.4.1. The resonant frequency of the parallel LC tank is established by the well-known formula

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{4.1}$$

The oscillation is perpetuated by a negative-resistance device, which is normally built as a positive-feedback active amplifier network. The

frequency f could be controlled by changing either the inductance L, the capacitance C, or some combination thereof. However, in a monolithic implementation it is more practical to keep the inductor fixed while changing the capacitance of a voltage-controlled device such as a varactor. Since the digital control of the capacitance C is required, the total capacitance is divided into N smaller digitally controlled varactors, which may or may not follow the binary-weighted pattern of their capacitance values. Equation 4.1 now becomes

$$f = \frac{1}{2\pi\sqrt{L\sum_{k=0}^{N-1} C_k}} \tag{4.2}$$

The capacitance difference between the high- and low-capacitative states of a single-bit k is $\Delta C_k = C_{1,k} - C_{0,k}$ and is considered the effective switchable capacitance. Since the frequency of oscillation grows with lower capacitance, increasing the digital control value must result in the increased frequency of oscillation. Therefore, the digital control state is the opposite of the capacitative state, so the digital bits need to be inverted such that the kth capacitor could be expressed as

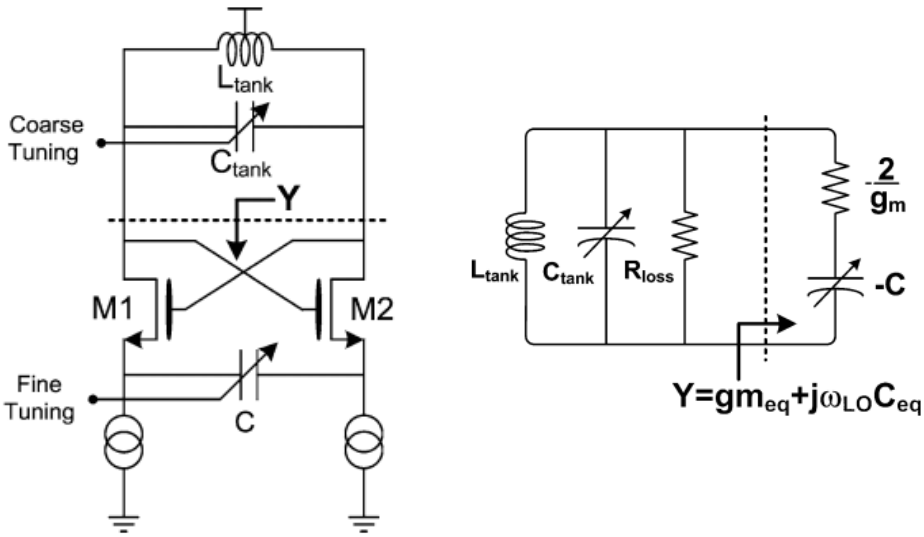
$$C_k = C_{0,k} + \overline{d_k}\Delta C_k \tag{4.3}$$

Equation 4.2 could be rewritten to include the digital control details:

$$f = \frac{1}{2\pi\sqrt{L\sum_{k=0}^{N-1}(C_{0,k} + \overline{d_k}\Delta C_k)}} \tag{4.4}$$

4.2 Principle of Capacitive Degeneration in LC Tank

The idea of this work is to move part of the tuning bank from the tank to the sources of the switching pair of the LC oscillator exploiting an intrinsic shrinking effect present in the structure (Fig.4.2) [13]. The portion of the capacitive array still in parallel to the tank (named coarse tuning bank) is used to compensate process and temperature variation, while the portion at the source of M1 and M2 (named fine tuning bank) is used for the DCO modulation inside the PLL. As it will be shown, this approach allows an easier design of both coarse and fine tuning banks, avoiding the use of dithering and without introducing any degradation in the DCO phase-noise.



(a) (b)

Fig.4.2 (a) Propose DCO scheme (b) DCO equivalent scheme

Since the circuit operates in a large signal regime, the structure has been studied using a small signal time variant analysis, where the MOS transconductance g_m was averaged over a time interval equal to one period of the oscillation frequency. Under these assumptions, the oscillator reported in Fig.4.2 (a) can be modeled by the scheme reported in Fig. 4.2 (b). In fact, the signal current that flows into transistor M1-M2 is the same as that flows into capacitance and is related to the voltage across the tank with an inversion of sign due the gate-drain cross-connections. The effect of on the DCO frequency tuning characteristic can be estimated evaluating the admittance Y using a series to parallel conversion in the circuit of Fig.4.2. The admittance Y can be expressed as follows:

$$Y = -\frac{g_m}{2} - j\omega_{LO}C \cdot (\frac{g_m}{2\omega_{LO}C})^2 \; ; \quad \text{for } g_m \ll 2\omega_{LO}C \tag{4.5}$$

Where the real part is the classical negative conductance that compensate the tank losses, while the imaginary part is equal to the capacitor *C* shrunk by a factor $g_m^2/(2\omega_{LO}C)^2$. Then we define the quality factor as follows.

$$Q_f = \frac{g_m}{2\omega_{LO}C} \tag{4.6}$$

Rewrite the equation 4.5

$$Y = -\frac{g_m}{2} - j\omega_{LO} C \cdot Q_f^{\,2} \tag{4.7}$$

If the quality factor Q_f is reduced, the equivalent capacitance at the tank diminishes. This capacitance is reflected in parallel to the tank shrunk by a factor proportional to the transconductance used in the cross-coupled pair. This allows to perform a fine frequency tuning with a resolution that is not limited by the unitary element present in the capacitor banks.

4.3 Oscillator Core

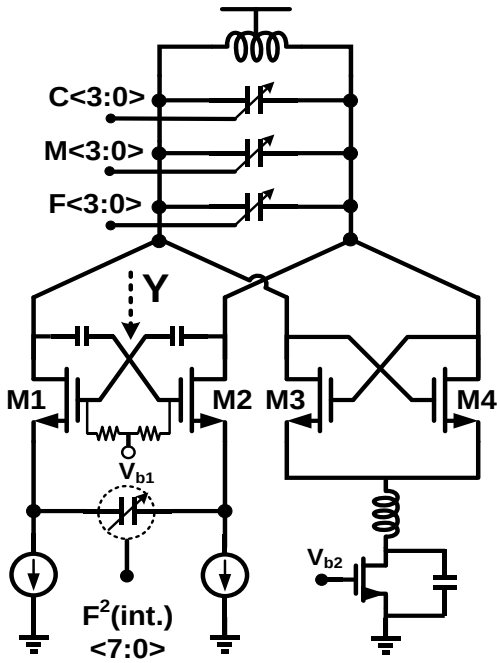


Fig.4.3 Core of DCO scheme with four banks

The Fig.4.3 illustrates the architecture of DCO, which consists of LC oscillator core and four tuning banks. Three 4-bit banks (named coarse, medium and fine tuning banks) are located in the LC-tank. Their frequency resolutions are 70MHz/LSB, 7MHz/LSB and 1MHz/LSB, respectively. However, the fine^2 bank (with frequency resolution 10kHz/LSB), in particular, moves from the tank to the source of the switching pair of the LC oscillator. As reported in [13], the capacitive degrading mechanism produces an equivalent scaled down replica of the fine^2 tuning bank in

parallel to the LC-tank. The effect of C on the DCO frequency tuning characteristic can be estimated by the admittance Y in Fig.4.2.

As the expression of equation 4.5, The value of g_m required to sustain the oscillation can correspond to a shrinking factor that makes the value of C excessively large. To solve the problem, a second cross-coupled transistors pair is added in parallel to M3-M4. The M1-M2 provides an extra degree of freedom to choose the shrinking factor. The M1 and M2 are biased to operate in Class-C resulting in reducing the phase noise and lowering the current necessary for a given shrinking factor [13]. To further improve the phase noise performance, the noise filtering technique with an inductor in the tail current source is also used [14].

4.4 Frequency Tuning Banks

As illustrated in Fig. 4.3, the DCO is composed of an LC oscillator core and four banks of switchable capacitors implementing the digital frequency tuning. The coarse and medium tuning banks ensure a wide frequency range, and the fine and fine^2 tuning bank provide the high frequency resolutions. Different types of capacitors and switches are used in the four banks for either wide frequency range or high resolution.

4.4.1 Implementation of Coarse, Medium and Fine Bank in LC Tank

As shown in Fig.4.4, the differential switched MIM capacitors were used in the coarse tuning bank to achieve a wide frequency tuning range, since this structure can have a large ratio between on and off capacitance, at the expense of reduced quality factor. Compared to single-ended structures, however, the quality factor is doubled [15]. Unfortunately this structure is not suitable for the other two banks, especially the fine bank, because it contains nodes with a large time constant and it could therefore not be used in fine frequency tuning.

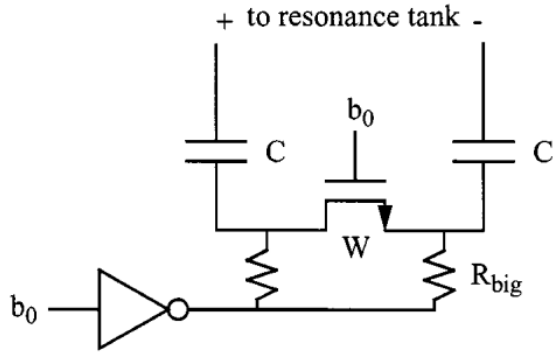


Fig.4.4 Improved differential switchable capacitor circuit for coarse bank

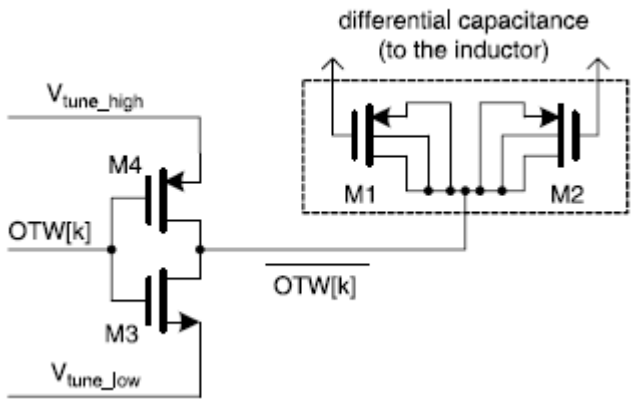


Fig.4.5 Differential varactor and an inverting driver in medium/fine bank

Figure 4.5 shows an implementation of the differential varactor and the preceding driver stage for medium and fine tuning banks. The V_{tune_high} and V_{tune_low} rail supply levels of the inverter are set to correspond with the two stable operating points, the off-state and on-state, respectively (V_{tune_high}=1.2V and V_{tune_low}=0 V). The varactor used in this work is a differential configuration. The balanced capacitance is between the gates of PMOS transistors M1 and M2 (Fig.4.5), whose source, drain, and back-gate connections are shorted together and tied to the M3/M4 inverter output. Because of the differential configuration, one-half of the single PMOS capacitance is achieved, which actually enhances frequency resolution.

4.4.2 Implementation of Fine^2 tuning Bank

The integral and fractional bits of fine^2 bank are realized as depicted in Fig.4.6. The 8 most significant bits (MSB) are used to control a matrix of 16×16 varactors. All elements except one are connected either to voltage supply or ground, generating a thermometric filling of the matrix. The remaining one varactor is connected to the output of a 5-bit digital-to-analog converter (DAC) [13]. It provides 32 additional voltage levels which realized as the fractional part of fine^2 bank, generating the finest resolution (10kHz/32) of DCO.

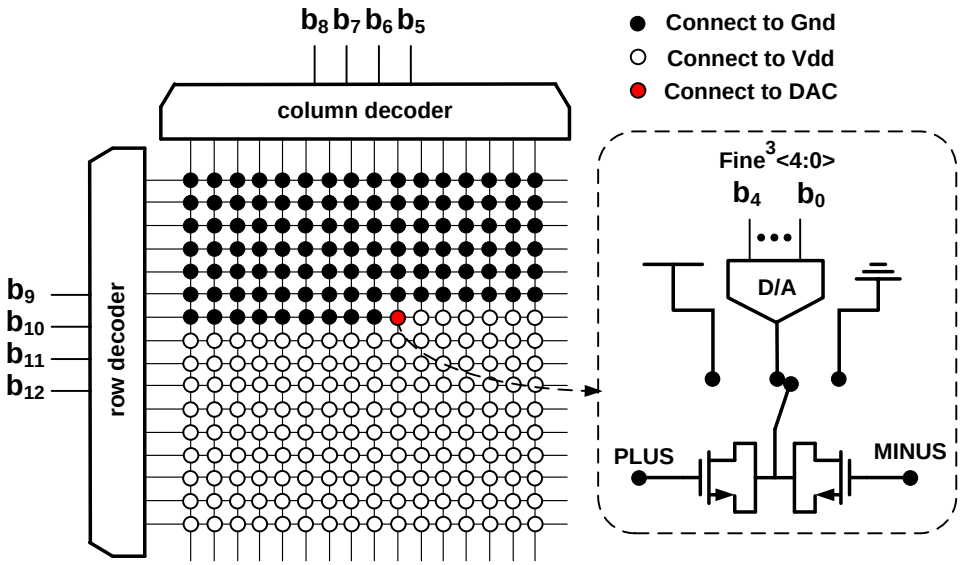


Fig.4.6 Fine^2 tuning bank

Fig. 4.7 displays a simplified circuit diagram of the proposed DAC structure, which provides 5-bit, 50-MHz operation with a full output range using a passive circuit structure [7]. The key idea of the proposed DAC structure is to perform a two step conversion process using a 3-bit resistor ladder in combination with a 2-bit capacitor array. In step one, as illustrated in Fig. 4.7(a), the resistor ladder is used to form two voltages of value $V_L = M/8 \cdot V_{DD}$ and $V_H = (M+1)/8 \cdot V_{DD}$, where M ranges from 0 to 7, and corresponds to the 1.2 V supply voltage. Simultaneously, V_H is connected to N unit cell capacitors, and V_L to *(4-N)* unit cell capacitors, where N ranges from 0 to 3. In step two, as illustrated in Fig. 4.7(b), the capacitors are first disconnected from the resistor ladder, and then connected to a common capacitor.

The unit resistance and the on-resistance of the switches should be designed to be low enough in value such that the unit capacitors completely settle to V_H and V_L during step one.

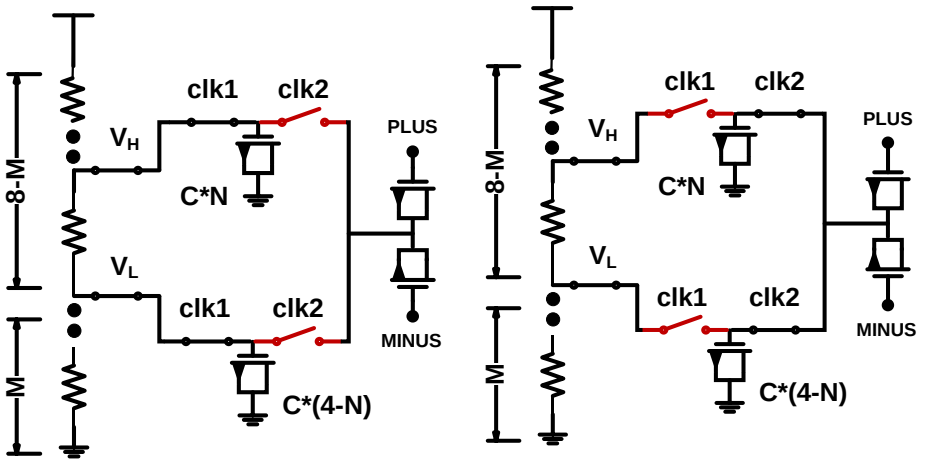


Fig.4.7 DAC operation: (a) step one: the unit capacitors are charged. (b) step two: the charges are redistributed and filtered.

A standard clock generator is used to produce the non-overlapping clocks to drive the switches [4]. The timing diagram of the non-overlapping clocks is shown in Figure 4.8.

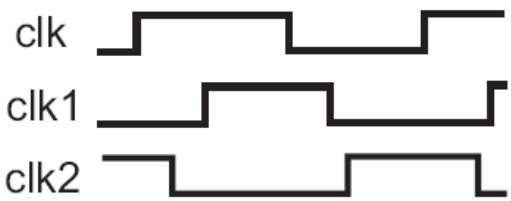


Fig.4.8 Timing diagram of the non-overlapping clocks

4.5 DCO Frequency Resolution Effect on Phase Noise

The DCO is accomplished by means of a quantized capacitance of the LC tank. Due to the natural discrete tuning of DCO, the quantization noise is inevitable, which will degrade the total noise performance. A reduced frequency step reduces the quantization noise [5].

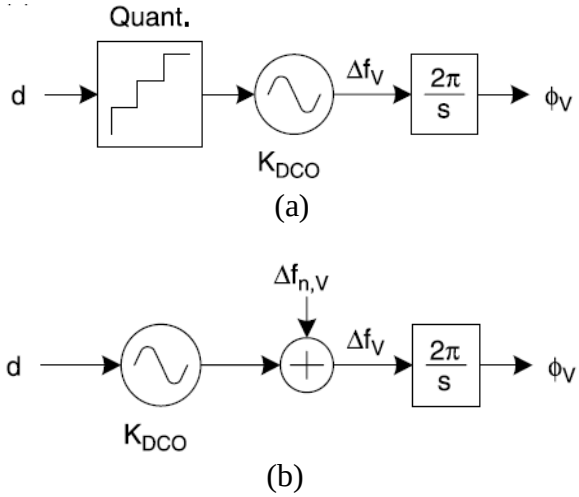


Fig.4.9 DCO quantization noise model

To gain insight into the quantization effects of the finite DCO frequency resolution Δf_{ref} on the RF output phase noise, consider its transfer function, shown in Fig. 4.8(a). The infinite-precision tuning signal *d* is quantized to a finite-precision tuning word such that it matches the DCO frequency resolution Δf_{ref} . The actual frequency deviation Δf_V will be within $\Delta f_{ref} / 2$ of from ideal. The frequency deviation is then converted to phase through the $2\pi / s$ integration. The 2π multiplication denotes the conversion of a linear frequency (hertz) to an angular frequency (rad/s).

Since the tuning word normally spans multiple quantization levels, the DCO frequency quantization error is modeled in Fig.4.8(b) as an additive uniformly distributed random variable $\Delta f_{n.V}$ with white noise spectral characteristics. The quantization error variance is

$$\sigma^2_{\Delta f_V} = \frac{(\Delta f_{res})^2}{12} \tag{4.8}$$

The total phase-noise power is spread uniformly from dc to the Nyquist frequency. The single-sided spectral density of $\Delta f_{n.V}$ is therefore flat at

$$\frac{1}{2} S_{\Delta f} = \frac{\sigma^2_{\Delta f_V}}{f_R} \tag{4.9}$$

Outside the loop bandwidth, the closed- and open-loop transfer functions from the frequency deviation $\Delta f_{n.V}$ to the phase Φ_V of the RF output are the same:

$$H_{ol,\Delta f_V}(s) = \frac{2\pi}{s} \tag{4.10}$$

So the single-sided power spectral density at the output is

$$L\ \Delta\omega\ = \frac{(\Delta f_{res})^2}{12 f_R}(\frac{2\pi}{\Delta\omega})^2 \tag{4.11}$$

It could be rewritten as

$$L\ \Delta f\ = \frac{1}{12}(\frac{\Delta f_{res}}{\Delta f})^2 \frac{1}{f_R} \tag{4.12}$$

For example, for $\Delta f = 1MHz$, $\Delta f_{res} = 300Hz$, $f_R = 50MHz$, $L\ \Delta f\ =$ -158dBc/Hz.

CHAPTER 5

5 Digital Phase-Locked Loop

Fig.5.1 shows the block diagram of the proposed DPLL. The key components of the proposed structure are a multi-delay coarse-fine high resolution TDC, a retiming flip-flop, unwrapping circuit which eliminates the phase wrapping at TDC output, digital loop filter, the asynchronous divider with a low-power implementation and the DCO achieving both the large tuning range and the fine frequency resolution.

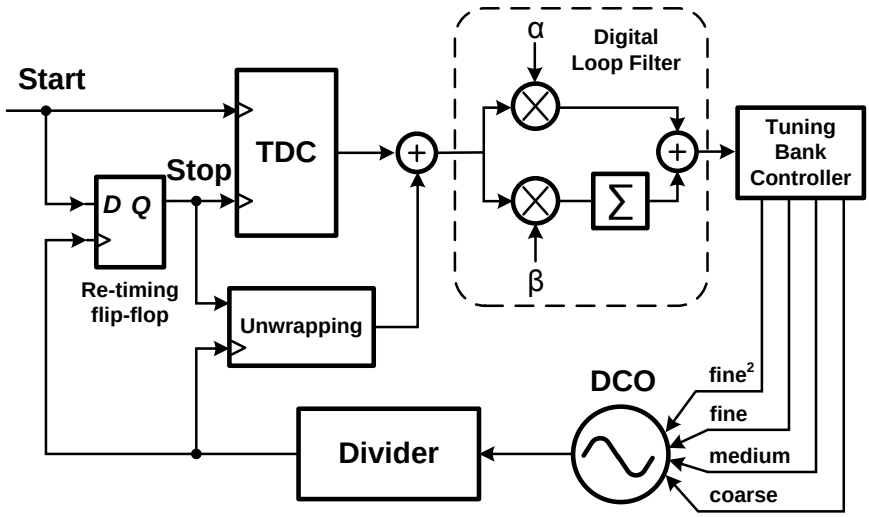


Fig.5.1 Block Diagram of proposed DPLL

5.1 Digital Loop Filter

To support type-II loop, the Digital Loop Filter (DLF) in Fig.5.1 consists of a proportional path and an integration path. The DLF can be easily configured to type-I or type-II PLL by disabling or enabling the integration path. In order to further speed up the setting time, the loop is to start with the ultra-wide acquisition bandwidth and to progressively narrow it down while traversing through finer DCO tuning banks. At the end of setting, the PLL switches its characteristic from type-I to type-II in order to filter out

the high frequency noise and ensure almost zero phase error between reference and feedback clock.

A type-II PLL is used in this work for its zero phase difference characteristic, which allows use of the multi-delay coarse-fine TDC. In the digital loop filter, this is accomplished by summing a proportional phase error (scaled by $\alpha=2^{-2}$) and an accumulated phase error (scaled by $\beta=2^{-11}$). The scaling factors are chosen as 1/2 to the power of *n*, where *n* is an integer. In order to speed up the setting time, the loop is to start from type-I corresponding to fast loop dynamics. The α value is changed several times during the frequency locking with an initial $\alpha=2^{-7}$, then $\alpha=2^{-5}$, $\alpha=2^{-3}$ and final $\alpha=2^{-2}$ values for coarse, medium ,fine, and fine^2, respectively. The final value of α is chosen to be the best phase noise performance. The integral loop factor β is activated after the fine bank is settled. It switches the PLL characteristic from type-I to type-II in order to effectively improve the phase noise.

5.2 Tuning Bank Controller

The tuning bank controller is needed to make to PLL work automatically when multiple frequency tuning banks are adopted in the DCO [9]. At frequency acquisition it lets the PLL tune the four different frequency tuning banks one by one, first the coarse, then the medium, fine and finally the fine^2 tuning bank. Figure 5.2 shows its block diagram. A detector measures the state of the control word. When the loop is locked the frequency control word is expected not to change outside a range of 3 different values. A long enough time of watching the control word can thus be used to determine whether the loop is locked and the next tuning bank should be activated. During the process, the judging counter will be reset once a $\Delta > 3$ occurs. Only if a stable control word is kept for enough reference cycles, lock is recognized and a pulse is sent to clock a flip-flop, starting the average frequency control value calculation. The average calculation is performed by halving the sum of the maximum and the minimum value during a period after lock is recognized. At the end of this calculation, a pulse from the second counter will drive an accumulator in the bank selector which puts out a 2-bit bank selecting signal to activate the next level bank. Meanwhile, the average control value will be fed to the last active bank. The details of the bank selector are illustrated in the left half of Fig.5.2. Internal signals sw0 and sw1 are bank selection bits, which are initialized to be ‘‘00’’ (coarse tuning) at power up. Once a positive pulse is present at port ‘‘pul’’, the value will be increased by one. sw0 and sw1

determines the active bank, and also control signals so that the average value avg_ctrl is stored in the flip-flops belonging to the correct bank at the moment of bank switching. The coarse and medium control words are always fixed by this operation when the loop has locked.

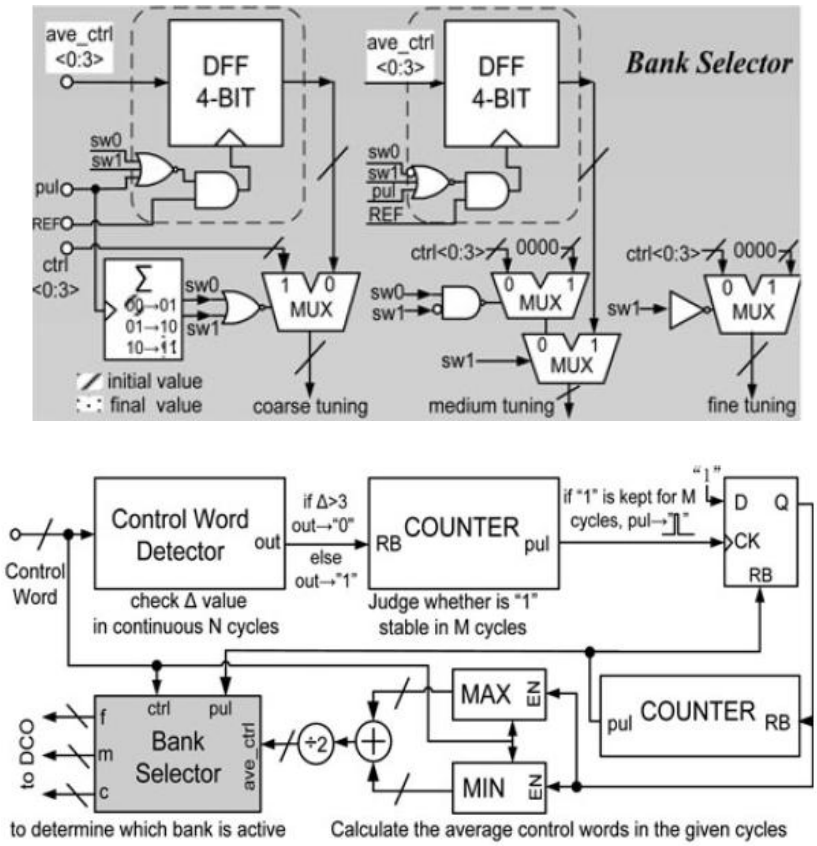
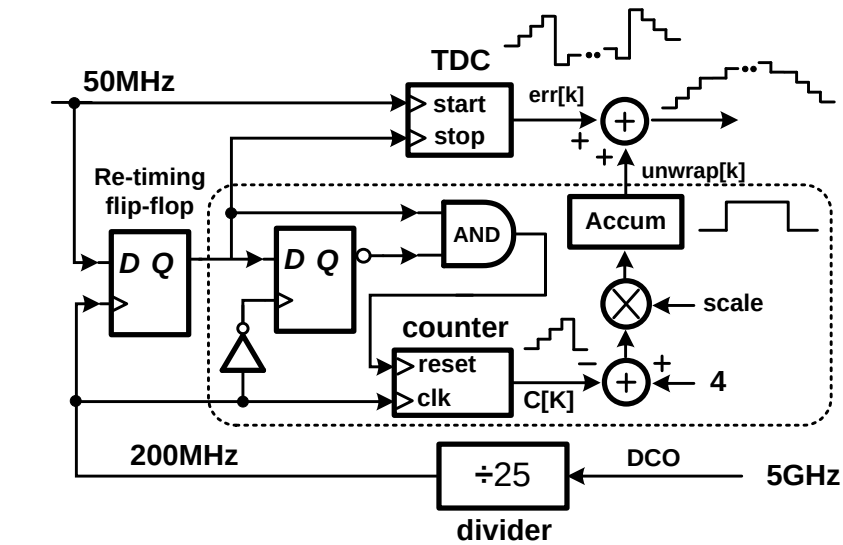


Fig.5.2 Tuning Bank Controller [9]

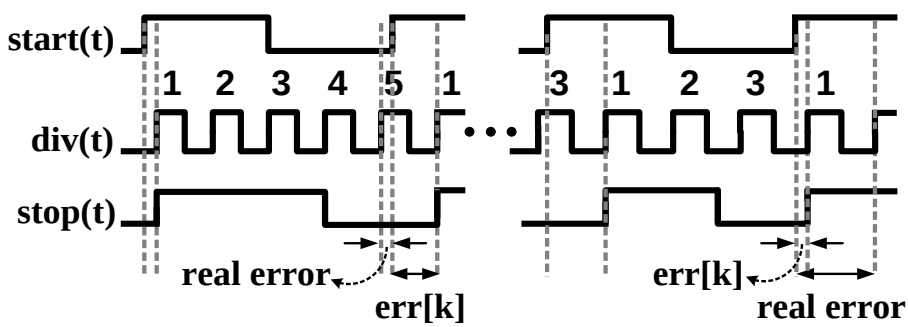
5.3 TDC Unwrapping Function

The TDC measures the phase error between the two inputs *Start* and *Stop*. Since a TDC cannot handle a negative phase error directly, the retiming flip-flop is needed to make *Start* always lead *Stop.* In addition, the retiming flip-flop is clocked at four times the reference frequency. As shown in Fig.5.3 the maximum time span seen by the TDC is 1/4 the reference period rather than the full reference period. In the case the phase error exceeds the detection-range, the "phase wrapping" will occurs, that is, the TDC

overestimates or underestimates the phase error *err[k]*, as shown in Fig.5.3(b) and Fig.5.3(c). Therefore, the idea is to switch in an offset *unwrap[k]* to eliminate the negative effect of the phase wrapping [7]. The unwrapping function in this prototype is implemented in Fig.5.3(a). The counter output is leveraged to indicate whether phase wrapping occurs. Its output compares with four, and their difference is scaled and accumulated to generate *unwrap[k]*, which provides the offset value to the TDC output. The scale factor is a digital word corresponding to the full range of TDC. Once the PLL is locked, no phase wrapping occurs, *c[k]* is four and nothing is accumulated.



(a)



(b) (c)

Fig.5.3 Phase unwrapping function

5.4 Asynchronous Divider

The divider core shown in Figure 4-4 is based on [16]. The beauty of this topology is the simple design resulting from the modular structure.

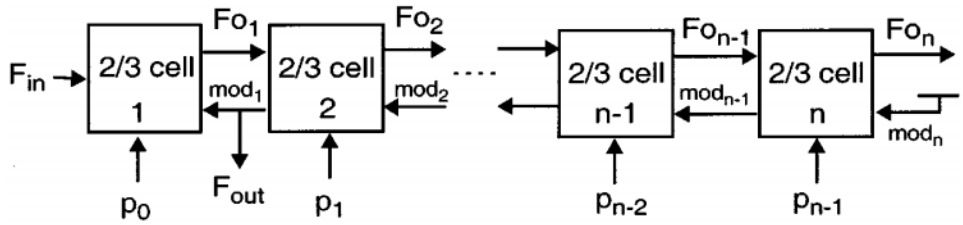


Figure 5.4 Basic architecture of divider

Different from the original implementation based on the current-mode logic in [16], the implementation of the asynchronous divider in this prototype is achieved with the full-swing TSPC logic in order to save the chip area and power dissipation. Figures 5.5 and 5.6 illustrate the original divide-by-two/three cell and the modified TSPC version used in this chip, respectively. The upper two latches in Figure 5.5 are combined as a TSPC DFF, and the lower two are implemented as P-type and N-type latches, respectively.

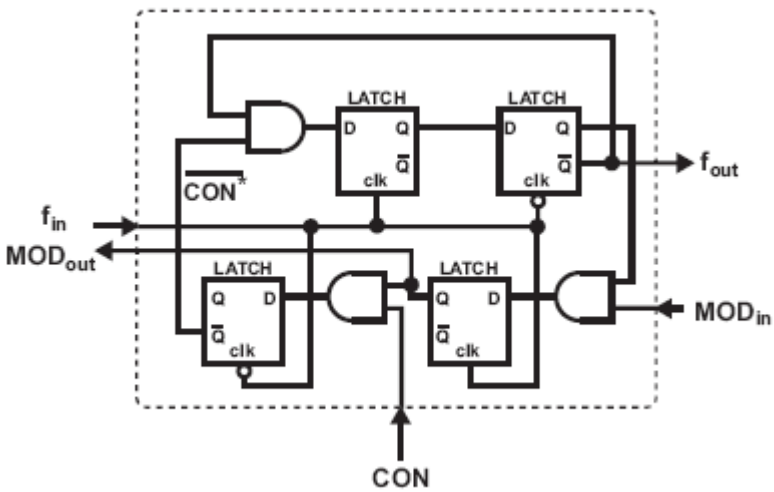


Figure 5.5 Schematic of the divide-by-two/three stage

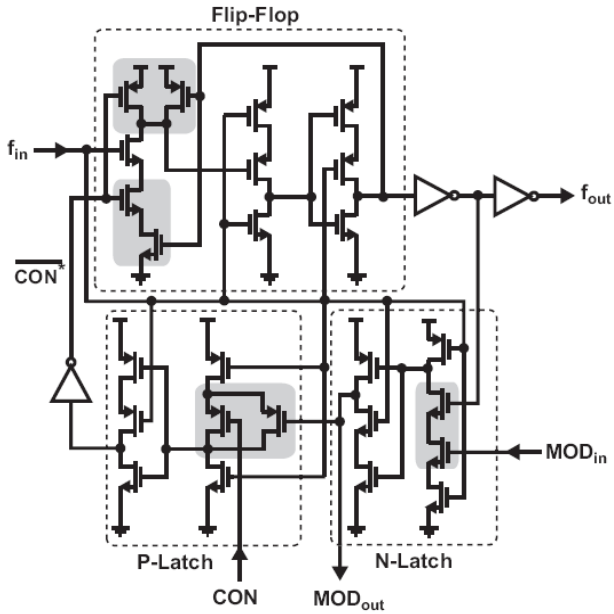


Figure.5.6 TSPC implementation of the divide-by-two/three stage.

CHAPTER 6

6 Behavioral Modeling and Simulation

In this chapter, we first analyze the models of the DPLL in z-domain and s-domain. After the models are built, the noise performance of the proposed DPLL will be presented. Finally, a short discussion on the loop dynamics is given.

6.1 Behavioral model of the type-II DPLL

6.1.1 z-domain model

The proposed DPLL is a discrete-time sampled system implemented with digital components connected with digital signals. Consequently, the z-domain representation is not only the most nature fit but it is also the most accurate with no necessity for those approximations that would result, for example, with an impulse response transformation due to the use of analog loop filter components.

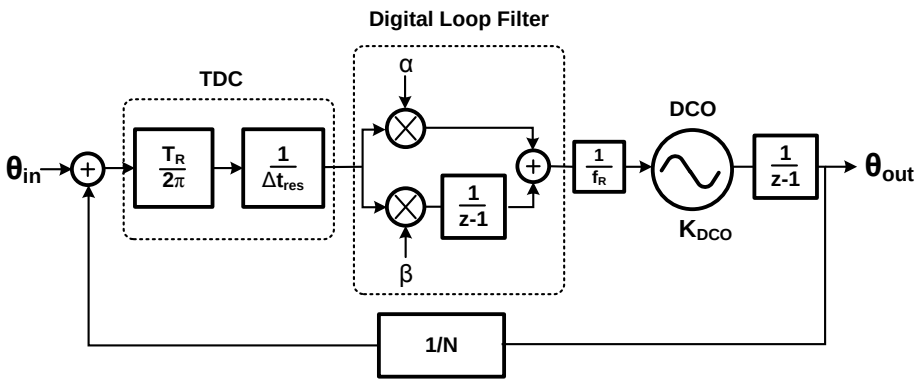


Figure 6.1 z-domain model of the DPLL.

A z-domain approximation for the second-order DPLL is shown in Fig. 6.1. The phase error is digitized by a time-to-digital converter with a

resolution of Δt_{res} . The transfer function of this operation can be approximated as

$$K_{TDC}(z) = \frac{T_R}{2\pi} \cdot \frac{1}{\Delta t_{res}} \tag{6.1}$$

The transfer function of digital loop filter is

$$H(z) = \alpha + \beta \cdot \frac{1}{z-1} \tag{6.2}$$

The z-domain DCO model is presented in Fig.6.1. The sampled or z-domain representation of the accumulation, as opposed to the more commonly used s-domain, implies that the accumulated timing deviation is defined only at the end of the DCO clock cycles with each rising clock edge.

6.1.2 s-domain model

The z-operator is defined as $z = e^{j\theta}$, where $\theta = \omega t_0$. $\omega = 2\pi f$ is the angular frequency and t_0 is the sampling period. In our case, $t_0 = 1/f_R$, which leads to $z = e^{j\omega / f_R}$. For small values of ω in comparison with the sampling rate, we can make the following approximation:

$$z = e^{j\theta} \approx 1 + j\theta = 1 + \frac{j\omega}{f_R} = 1 + \frac{s}{f_R} \tag{6.3}$$

Then we convert the z-domain to s-domain, as shown in Figure 6.2.

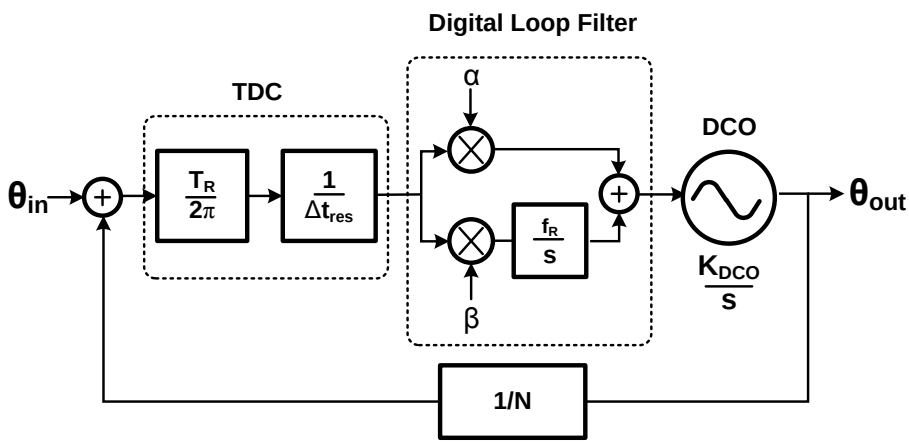


Figure 6.2 s-domain model of the DPLL.

The transfer function of digital loop filter in s-domain is

$$H(s) = \alpha + \beta \cdot \frac{f_R}{s} \tag{6.4}$$

The s-domain DCO model is presented in Fig.6.2.

$$K_{DCO}(s) = \frac{K_{DCO}}{s} \tag{6.5}$$

The open-loop transfer function of DPLL is

$$\begin{aligned} H_{OL}(s) &= K_{TDC}(s) \cdot H(s) \cdot K_{DCO}(s) \\ &= \frac{T_R}{2\pi} \cdot \frac{1}{\Delta t_{res}} (\alpha + \beta \cdot \frac{f_R}{s}) \cdot \frac{K_{DCO}}{s} \end{aligned} \tag{6.6}$$

The closed-loop transfer function is

$$\begin{aligned} H_{CL}(s) &= \frac{K_{TDC}(s) \cdot H(s) \cdot K_{DCO}(s)}{1 + K_{TDC}(s) \cdot H(s) \cdot K_{DCO}(s) / N} \\ &= \frac{\frac{T_R}{2\pi} \cdot \frac{1}{\Delta t_{res}} (\alpha + \beta \cdot \frac{f_R}{s}) \cdot \frac{K_{DCO}}{s}}{1 + \frac{T_R}{2\pi} \cdot \frac{1}{\Delta t_{res}} (\alpha + \beta \cdot \frac{f_R}{s}) \cdot \frac{K_{DCO}}{s} / N} \end{aligned} \tag{6.7}$$

6.1.3 PLL Stability Analysis

For a frequency synthesizer, where a simple first or second-order loop filter could be employed, loop stability has not been an issue since it is easy to maintain it with reasonably intuitive values of loop gain factors. A type I DPLL is unconditionally stable whena , $\alpha<1$. A type II DPLL is stable and exhibits acceptable peaking when the damping factor ξ > 0.707. Conventional s-domain control loop theory tools are used below to carry it out.

The DPLL open-loop transfer function follows Eq. 6.6. Figure 6.3 shows the magnitude and phase of the open-loop transfer function for the default DPLL loop settings: $\alpha=2^{-2}$, $\beta=2^{-11}$, $K_{TDC}=20ns/1.25ps/2\pi$, $K_{DCO}=2\pi \times 10kHz/LSB$, $N=100$. The stability analysis results in the following numbers:

1. Open-loop 0-dB point=65kHz
2. Open-loop -180^o point=0^o
3. Phase margin=76.6^o
4. Gain margin= infinite
5. Closed-loop gain at 500kHz (normalized to 0dB) =-22dB

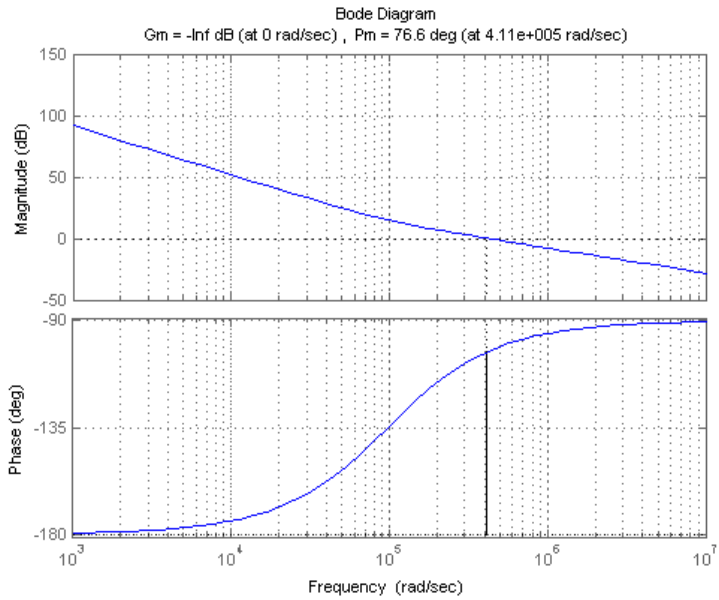


Figure 6.3 Open-loop transfer function with default loop settings.

The closed-loop transfer function is Eq.6.7. Figure 6.4 shows the magnitude and phase of the closed-loop transfer function for the default DPLL loop settings

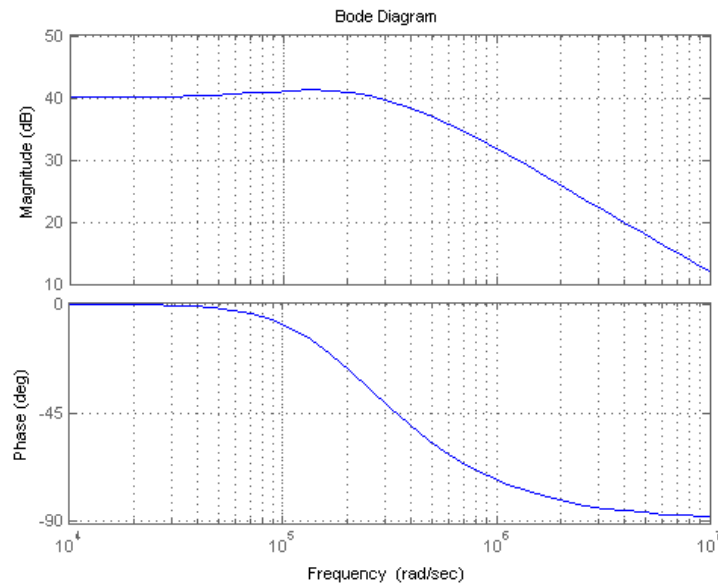


Figure 6.4 Reference closed-loop transfer function with default loop settings.

The step response of the closed-loop is shown in Figure 6.5. It is the approximation of the setting time. It is about 50us.

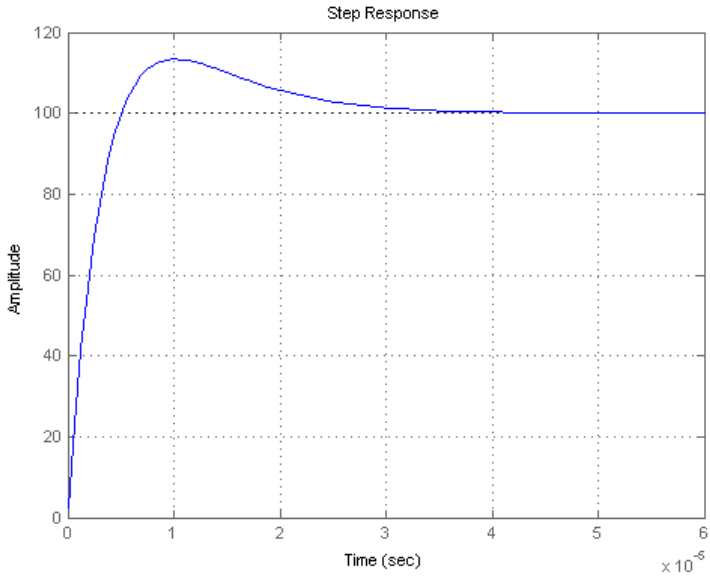


Figure 6.5 Step response of default loop settings.

6.2 PLL Noise Performance Analysis

6.2.1 Noise Transfer Functions

A DPLL linear model, including phase noise sources, is shown in Fig.6.6. $\Phi_{n,R}$ is the phase noise of the reference input that is external to the DPLL. Its transfer function is expressed by Eq.6.7. Internal to the system, there are only three places that the noise could be injected. Due to its digital nature, the rest of the system is completely immune from time or amplitude-domain perturbations.

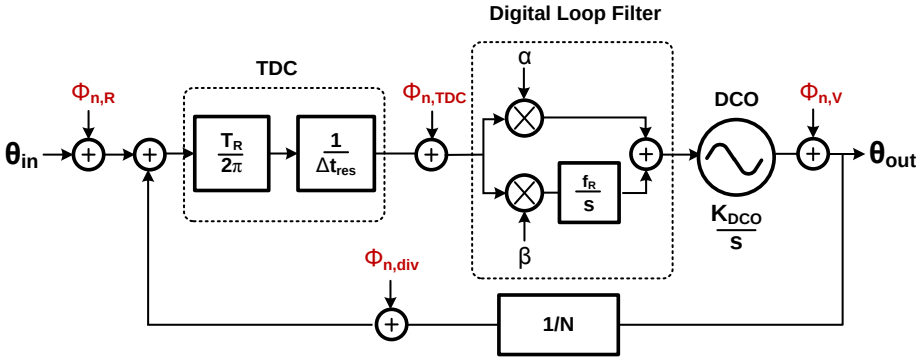


Figure 6.6 Linear s-domain model with noise sources added.

The first internal noise source $\Phi_{n,V}$, is the oscillator itself. It undergoes high-pass filtering by the loop. Its closed-loop transfer function is

$$H_{CL,V}(s) = \frac{1}{1 + H_{OL}(s)/N} \tag{6.8}$$

The second internal noise source $\Phi_{n,TDC}$ is the TDC operation of calculating ε. Even though the TDC is a digital circuit, the FREF and CKV inputs are continuous in the time domain. The TDC error has several components: quantization, linearity, and randomness due to thermal effects. The TDC quantization noise is governed by Eq.3.7. It should be noted that the rest of the phase-detection mechanism is digital in nature and does not contribute noise. The closed-loop transfer function of the TDC noise can be expressed as

$$H_{CL,TDC}(s) = \frac{H_{OL}(s)/K_{TDC}}{1 + H_{OL}(s)/N} \tag{6.9}$$

The third noise source $\Phi_{n,div}$ comes from the divider. Its closed-loop transfer function is the same with the phase noise of the reference input in Eq.3.7. Comparing to the other two noise source, the divider noise is much lower that it is intentionally not included.

6.2.2 Noise Source

As we mentioned in chapter 4, the single-sided power spectral density at the output is Eq. 4.12, as follows.

$$L\ \Delta f\ = \frac{1}{12}\left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \frac{1}{f_R} \tag{6.10}$$

In this case, for $\Delta f = 1MHz$, $\Delta f_{res} = 300Hz$, $f_R = 50MHz$, $L\ \Delta f$ = -158dBc/Hz. This value is much lower than the nature phase noise of oscillator. Therefore, the phase noise is not included in the noise calculation.

The nature phase noise of DCO is as illustrated in Fig.6.7. The phase noise of DCO at 5GHz carrier frequency is -125 and -151dBc/Hz at 1MHz and 20MHz offset, respectively.

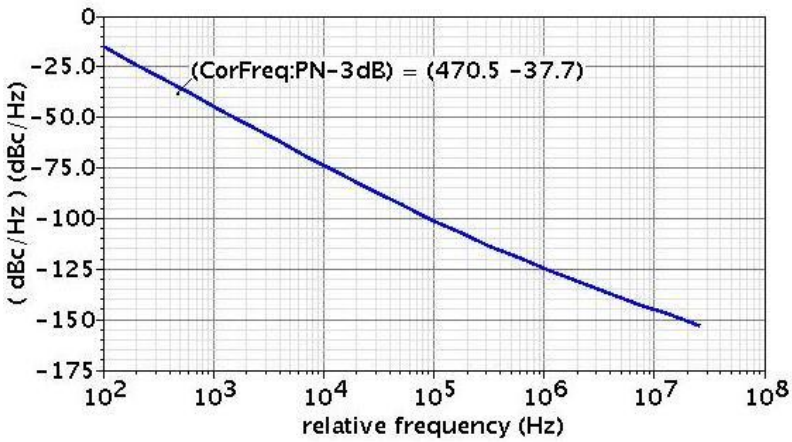


Figure 6.7 Phase noise performance of DCO

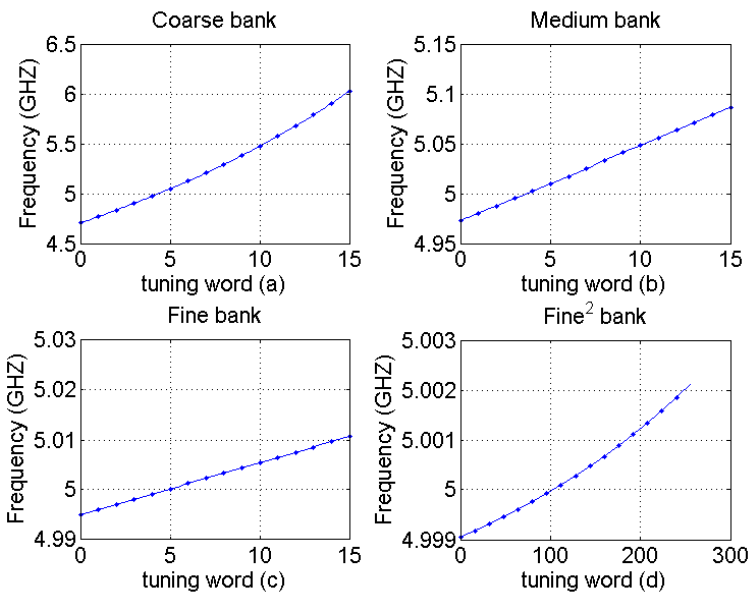


Fig.6.8 Simulated DCO gain curve of four banks. (a) coarse bank (b) medium bank (c) fine bank (d) fine^2 bank (integral bits)

For each bank simulation, the others were kept unchanged. The average coarse, medium, fine and fine^2 frequency steps are 70MHz, 7MHz, 1MHz and 10kHz, respectively. In particular, since one varactor in fine^2 bank is connected to a 5-bit DAC, the finest frequency resolution is approximate 300Hz (10kHz/32).

The TDC Noise contribution, within the loop bandwidth, at the DPLL RF output is

$$S_{TDC} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{res}}{T_{DCO}}\right)^2 \frac{1}{f_{REF}} \tag{6.11}$$

where Δt_{delay} denotes the delay time of a buffer cell, T_{DCO} the period of RF output, and f_{REF} is the frequency of reference clock. For example, Δt_{res} =1.25ps, T_{DCO} =1/5GHz, f_{REF} =50MHz, we obtain S_{TDC}= -116dBc/Hz

6.2.3 Phase Noise Performance of DPLL

As shown in Fig.6.9, the noise performance of DPLL was obtained by using Matlab. The loop bandwidth is designed 100kHz and the estimated noise performance of the DPLL at 5GHz is -110, -111, -124 dBc/Hz at 10kHz, 100kHz and 1MHz offset, respectively.

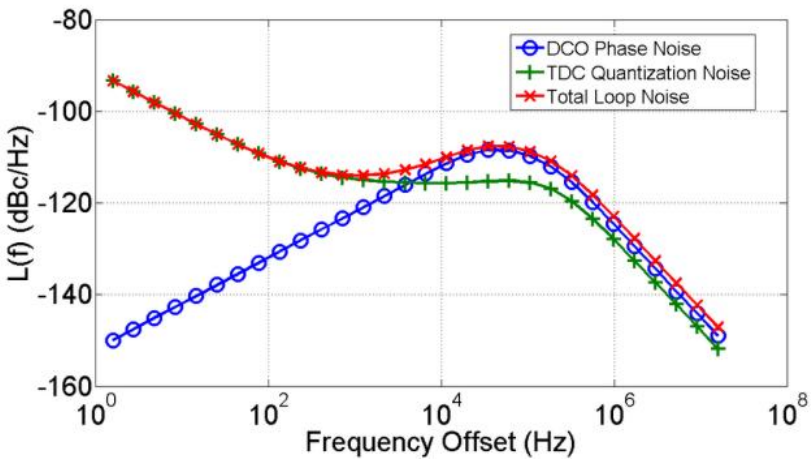


Figure 6.9 Phase noise performance of DPLL

6.3 PLL Transient Simulation

Fig.6.10 illustrates the frequency control word (FCW) during the phase locking. The loop characteristic moves from type-I to type-II when the fine^2 tuning bank is activated. When the loop is locked, the control word switches among four numbers, which generates the average value of the FCW. Fractional tracking bits of fine^2 bank do not contribute significantly to the locking process, so for clarity are not included.

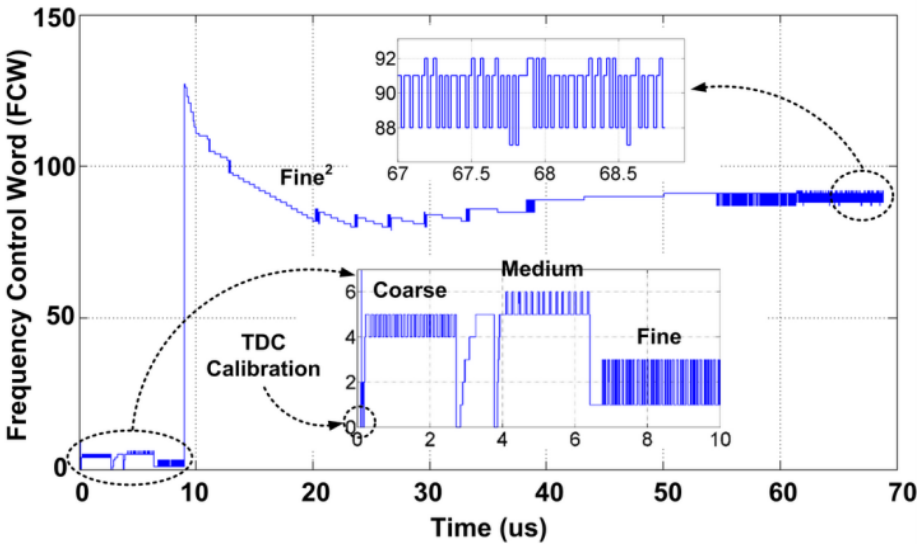


Fig.6.10 Simulated Frequency Control Word during locking

6.4 Performance Summary

TABLE 6.1. PEFORMANCE SUMMARY

Architecture	divider-assisted DPLL	
Output Frequency	4.7GHz-6GHz	
Reference Frequency	50MHz	
Phase Noise@5GHz	-125dBc/Hz@1MHz	
	-151dBc/Hz@20MHz	
Feature Size	90-nm CMOS	
Power Supply	1.2V	
Current Consumptions	Total	14mA
	TDC+Unwrapping	5mA
	DCO	7.5mA
	Divider+ Digital Circuits	1.5mA

CHAPTER 7

7 Conclusions

The scope of the thesis work has been to implement a digital PLL for the RF application.

A multi-delay coarse-fine high resolution TDC based CMOS DPLL is proposed and implemented. The TDC has a coarse delay line with different delay cells, which releases the requirement for a large number of delay cells. A coarse-fine TDC based on time amplifier (TA) is introduced to increase the time resolution which lowers the in-band noise of PLLs. As such, the combination of multi-delay and coarse-fine architectures achieves both the large detection range and high time resolution.

A Digitally Controlled Oscillator (DCO) based on capacitive degeneration in LC-Tank is also implemented. The DCO moves part of the tuning bank from the tank to the sources of the switching pair, exploiting an intrinsic shrinking effect that reduces the frequency resolution. A control mechanism for bank selection is then added to make the DPLL work automatically.

Circuit implementation and simulation results of the DPLL are illustrated. The multi-delay coarse-fine TDC achieves large detection-range and high resolution of 1.25ps. The DCO with the finest frequency step 300Hz is implemented for good phase noise performance. The DPLL is realized in 90nm CMOS process and consumes 14mA from a 1.2V supply.

CHAPTER 8

8 Future Work

8.1 Fractional-N Divider

For classical analog fractional-N synthesizers, it is common to use a divider structure due to its low power and compact layout. As shown in figure 8.1, application of this structure to a digital fractional-N synthesizer is straightforward in principle.

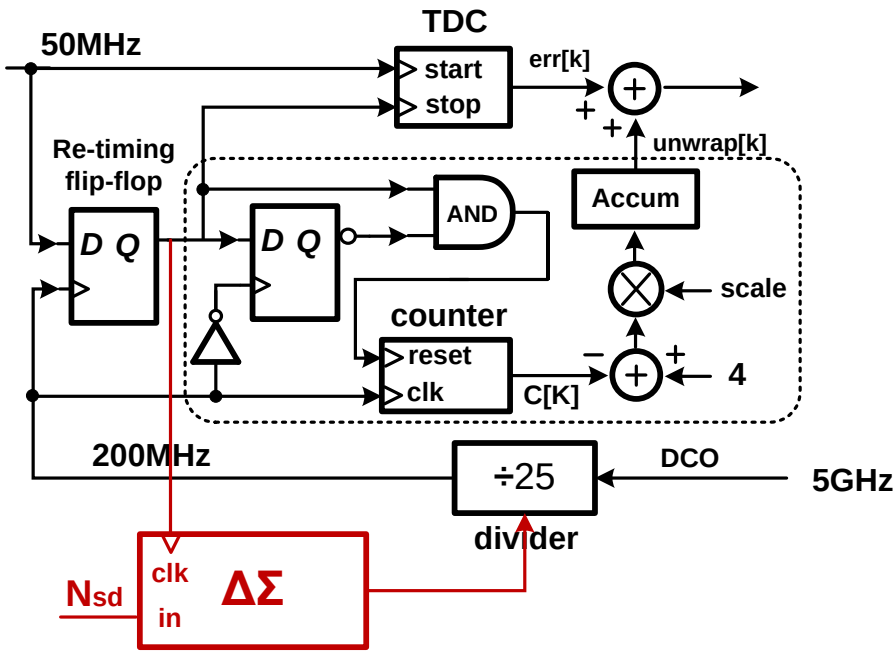


Figure 8.1 Fractional-N divider structure

8.2 High Order DPLL

The proportional and integral paths are configured in parallel to create a so-called proportional-integral (PI) control structure. The PI structure is proceeded by the IIR filter, whose purpose is to further improve the transition band rejection of the DPLL filtering characteristics.

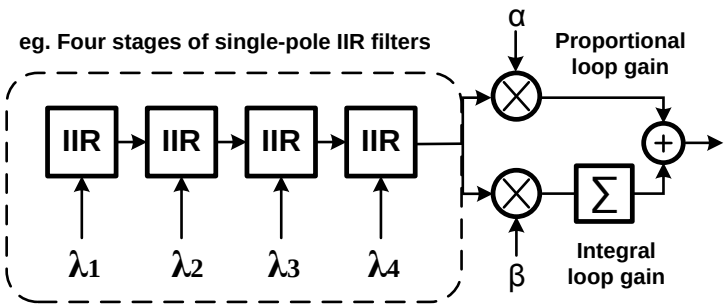


Figure 8.2 High order digital loop filter

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List of Tables

List of Acronyms

RF	Radio Frequency
CMOS	Complementary Metal Oxide Semiconductor
IC	Integrated Circuit
TDC	Time to Digital Converter
CTDC	Coarse Time to Digital Converter
FTDC	Fine Time to Digital Converter
DLF	Digital Loop Filter
DCO	Digital Controlled Oscillator
DFF	D Flip-Flop
VCO	Voltage Controlled Oscillator
DPLL	Digital Phase-Locked Loop
PLL	Digital Phase-Locked Loop
OTW	Oscillation Tuning Word
FCW	Frequency Controlled Word
PFD	Phase/Frequency Detector
LPF	Low Pass Filter
MUX	Multiplexer
DPLL	Digital Phase-Locked Loop
TA	Time Amplifier
MSB	Most Significant Bit
LSB	Less Significant Bit

Paper I

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A 0.13µm CMOS ΔΣ PLL FM Transmitter

Ying Wu, Xiaodong Liu, Dawei Ye, Vijay Viswam, Lin Zhu, Ping Lu, Dejan Radjen, Henrik Sjöland
Department of Electrical and Information Technology, Lund University, Sweden
Email: {mas09ywu, mas09xl2, mas09yda, mas09vv1, mas09zli}@student.lu.se
{ Ping.Lu, dejan.radjen, henrik.sjoland}@eit.lth.se

***Abstract* — A short range FM transmitter is presented. It uses an architecture where the output frequency of a phase locked loop (PLL) is modulated by varying the division number of the feedback divider, using the 1-bit output of a ΔΣ ADC. The measured total harmonic distortion (THD) plus noise is less than 1% at 75 kHz deviation. The transmitter is fully integrated in a 0.13µm CMOS process and the core area is 0.24 mm^2. The current consumption is 4.4mA from a 1.2V supply.**

I. Introduction

The use of wireless products is rapidly increasing and so is the functionality of the devices. For this to be successful the functionality must increase without increasing the size or cost of the devices, calling for increased integration. One function that is desired is a short range FM transmitter, enabling a mobile phone to receive streamed music over the cellular network, and then to send it to the car FM radio. Since a few years it is allowed to use short range FM transmitters in Europe with up to -43dBm effective radiated output power.

The target is therefore to find an FM transmitter architecture supporting small chip area and a high level of integration, that is a minimum number of external components, and demonstrate the performance by implementing an integrated circuit. Three different architectures for realizing frequency modulation are illustrated in Fig.1. The modulation signal can be (a) multiplied by a local oscillator (LO) frequency using a mixer, (b) fed to the control input of a voltage controlled oscillator (VCO), or (c) fed to the feedback divider of a PLL [1].

Architecture (a) is direct conversion one, and although not shown explicitly in the figure, quadrature mixers are required. However, using frequency modulation, very large phase deviations are associated with strong low frequency modulation signals, and such signals are common in music. A digital approach is probably needed to handle the large phase deviations in a robust way, requiring digital circuitry, two DACs (I and Q), two low pass filters, together with mixers. In case of an analog input signal also an ADC is needed. All this add up to a significant cost in implementation. Architecture (b) is referred to as direct modulation of a VCO. This technique allows a significant reduction in components. No mixers are needed since the VCO performs the frequency modulation. However, the loop must be very slow not to interfere with the transmission. Two problems arise; the capacitors of the loop filter get very large and must be realized off-chip, reducing the level of integration, and the start-up of the circuit also becomes slow. Finally,

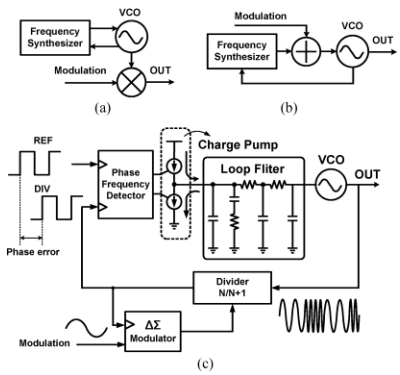

Fig.1 Frequency modulation architectures (a) Mixer based. (b) Direct modulation of VCO. (c) ΔΣ PLL based

architecture (c) can be viewed as indirect modulation of the VCO through appropriate control of a frequency synthesizer that sets the VCO frequency. The transmitter can be realized by only two building blocks; a frequency synthesizer and a ΔΣ modulator, and a low power solution can thereby be achieved. The bandwidth of the PLL can be wider in this architecture, and the loop filter can therefore be realized on-chip, resulting in a high level of integration.

This paper presents a ΔΣ PLL short range FM transmitter. The architecture illustrated in Fig.1 (c) consists of a one-bit ΔΣ modulator and an integer-N PLL. The PLL synthesizer is directly modulated by varying the division number of the feedback divider with the output of a 1-bit ΔΣ modulator. The modulated ΔΣ synthesizer has the advantage of adding little complexity to the PLL, as the ΔΣ modulator can be efficiently implemented in single bit. Thanks to the relative low complexity the modulated synthesizer is attractive from a power consumption point of view.

The paper is organized as follows; section II describes the proposed ΔΣ PLL transmitter architecture, section III and IV detail the circuit implementation, section V presents the measured results, and finally conclusions are drawn in Section VI.

II. Transmitter Architecture

The ΔΣ PLL is a popular approach to fractional-N frequency synthesis, which enables fast dynamics to be achieved by the PLL by allowing a high reference

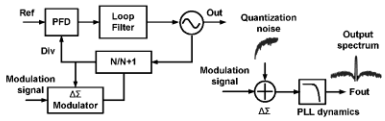

Fig.2 Quantization noise suppression

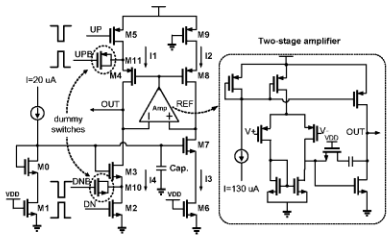

Fig.3 The architecture of charge pump

frequency. High resolution is achieved by allowing non-integer division numbers to be realized through dithering. It leads to a simple synthesizer structure and is referred to as a fractional-N synthesizer with noise shaping [2]. Using this approach, it is straightforward to realize a transmitter that performs frequency modulation in a continuous manner by direct modulation of the synthesizer.

As shown in Fig.1 (c), a typical ΔΣ PLL transmitter consists of a Phase/Frequency Detector (PFD), a Charge-Pump (CP), a Low-pass Loop Filter (LPF), a voltage-controlled oscillator (VCO), a frequency divider, and a ΔΣ modulator clocked by the divider output. The modulation signal from baseband is lead to the single-bit ΔΣ modulator, the output of which controls the instantaneous division number of the PLL. The variation of the division number causes the output frequency to be modulated according to the input signal. As shown in Fig.2, although ΔΣ modulator adds quantization noise that is shaped to high frequencies, the PLL acts as a low-pass filter that passes the information signal but attenuates the ΔΣ quantization noise. Therefore, the primary limitation is that the bandwidth of the PLL must be narrow enough that the quantization noise from ΔΣ modulator is sufficiently attenuated, but sufficiently high to allow for the desired modulation to pass.

III. CHARGE PUMP PLL

The charge pump PLL is the key building block in ΔΣ PLL FM transmitter. As shown in Fig.1 (c), the PFD compares the positive-going edges of the reference signal to those from the divider and causes the charge pump to drive the loop filter with current pulses whose widths are proportional to the phase difference between the two signals. The pulses are low-pass filtered by the loop filter and the resulting waveform drives the VCO. The charge pump noise is low-pass filtered by the PLL dynamics, whereas VCO noise is high-pass filtered. Therefore, while

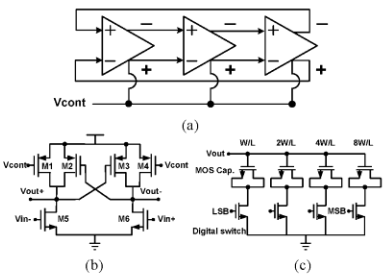

Fig.4 The structure of VCO; (a) topology of the ring oscillator, (b) delay cell, (c) tuning bank

raising the PLL bandwidth has the benefit of suppressing the VCO noise at low frequency offset, it also carries the penalty of increasing the influence of charge pump noise. Low noise for the PLL therefore requires both low noise charge pump and VCO.

A. Charge Pump

The current mismatch of the charge pump in the PLL generates a phase offset which increase spurs in the PLL output signals. To minimize the phase offset, one should reduce the on-time of the charge pump and the current mismatch. Some on-time, however, is necessary to eliminate the PFD dead-zone. Therefore we have to reduce the current mismatch as much as possible. Fig. 3 illustrates the structure of the charge pump, which can produce nearly perfect current matching characteristics by using an error amplifier. The amplifier makes the voltage at the node REF of the current mirror (M6~M9) follow the voltage at node OUT of the charge pump (M2~M5). For M5=M9, M4=M8, M3=M7, M2=M6, if the *DN* and *UP* signals are high, then *I4=I3=I2*, if the *DN* and *UP* signals are low, then *I3=I2=I1*. Therefore, we can make the sinking current *I4* equal to the sourcing current *I1*. In addition, the dummy transistor M11 and M10 are added to reduce the effects of charge injection and clock feedthrough. The error amplifier is implemented as a two-stage amplifier with a gain of 60dB.

B. Three-stage Ring Oscillator

The three-stage voltage-controlled differential ring oscillator used in this architecture is shown in Fig.4 (a). The ring oscillator was chosen for its high level of integration, and it lends itself well to implementation of oscillators at frequencies in the FM band (about 100MHz). Fig.4 (b) depicts the proposed delay cell of the ring oscillator. M5 and M6 are used for the input transistors coupling with the output of other stages. M2 and M3 are connected as a latch to provide the equivalent negative resistances ($-1/g_{m2,3}$) to guarantee the oscillation. In addition, M1 and M4 work in the triode region and are regarded as two tunable resistors controlled by the voltage V_{cont} from the loop filter. The size of M1 and M4 determines the VCO gain, K_V (Hz/V). Noise on the control voltage V_{cont} will be converted to phase noise by the gain

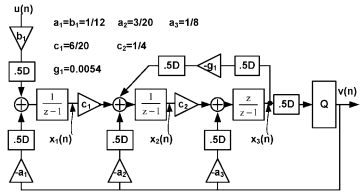

Fig.5 Signal flow graph of the ΔΣ Modulator

of the VCO. A small value of K_V therefore has the benefit of less phase noise, but reduces the tuning range of the VCO. To break up this trade-off, the switchable capacitor array shown in Fig.4 (c) was added to widen the tuning range while keeping a small K_V for good phase noise performance [3]. The switchable capacitors can be arranged in a binary weighted array, so the tuning can be performed by a digital control word.

C. Fourth Order Loop Filter

The forth order loop filter shown in Fig.1 (c) is used to filter out spurs and noise caused by the PLL and the ΔΣ modulator. When a third-order ΔΣ modulator is used, a fourth order loop filter is recommended. Careful design is required to avoid the stability problems in the feedback loop. In this design, the bandwidth of PLL is 150kHz.

IV. ΔΣ MODULATOR DESIGN

The ΔΣ modulator is implemented using cascaded integrators with distributed feedback (CIFB) architecture. It is a third-order discrete time loop filter which consists of three switched-capacitor integrators and a single-bit quantizer. A clock generator is also included to generate the two non-overlapping clock phases, from the reference single phase clock.

A. Modulator Overview

Fig. 5 shows the signal flow graph (SFG) of the third-order CIFB loop filter. The delay elements referred to as "D" in the graph are used to achieve a correct timing. To achieve a measured signal to noise ratio (SNR) of ~50dB at -25dBFS input, the oversampling ratio (OSR) is chosen to be 64, which ensures thermal noise is dominant. The coefficients *(a, g, b, c)* in the SFG are determined by using Schreier's ΔΣ toolbox [4]. Proper scaling is necessary to avoid saturating the integrators. The noise transfer function (NTF) and signal transfer function (STF) from this loop filter are

$$NTF = \frac{(z-1)(z^2-2z+1.001)}{(z-0.6692)(z^2-1.53z+0.6637)} \quad (1)$$

$$STF = \frac{0.044084}{(z-0.6692)(z^2-1.53z+0.6637)} \quad (2)$$

B. Switched-Capacitor Integrator

In order to generate stable capacitance ratios, which are equal to the coefficients (*a, g, b, c*), the stray-insensitive

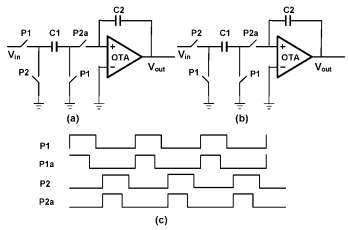

Fig.6 (a) Non-inverting switched-capacitor integrator, (b) inverting switched-capacitor integrator, (c) two-phase non-overlapping clock signals

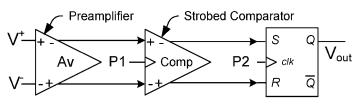

Fig.7 Single bit quantizer

switched-capacitor integrator is used as shown in Fig.6. Fig.6 (a) is a non-inverting type and the transfer function is

$$V_{out}(z) = \frac{C_1}{C_2} \cdot \frac{1}{z-1} \cdot V_{in}(z) \quad (3)$$

which results a unit delay. Fig. 6 (b) is an inverting type and the transfer function is

$$V_{out}(z) = -\frac{C_1}{C_2} \cdot \frac{z^{1/2}}{z-1} \cdot V_{in}(z) \quad (4)$$

which results a half unit delay. The switching clock is controlled by the two-phase non-overlapping signals shown in Fig. 6 (c) and distributed according to the SFG in Fig. 5 to get the desired delay.

C. Single-bit Quantizer

The single-bit quantizer is shown in Fig. 7. It consists of a preamplifier, a strobed comparator and an SR flip-flop. Since the quantizer only has two output levels and it is preceded by the loop filter with third order noise shaping function, the tolerance to non-idealities is high, which relaxes the design requirements of the comparator. The SR flip-flop is shifts the output stream from the comparator by half a clock cycle.

V. MEASUREMENT RESULTS

The FM transmitter was implemented in a 0.13μm CMOS process, and the chip microphotograph is shown in Fig.8. The total active area is 0.24 mm^2 (excluding pads), of which the ΔΣ modulator and PLL occupy about 0.1 mm^2 and 0.14 mm^2 respectively.

Fig.9 depicts the ΔΣ Modulator's output spectrum comparison between the ideal system simulation in Matlab and real measurement. A -25dBFS at 6.1kHz sine signal is used as input while the sampling frequency for testing is

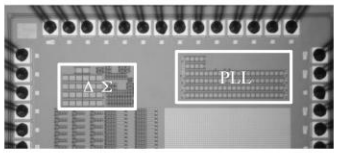

Fig.8 Die photo of implemented 0.13-µm transmitter

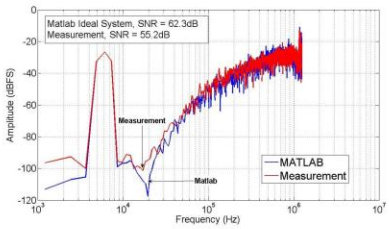

Fig.9 The spectrum of ΔΣ modulator output signal

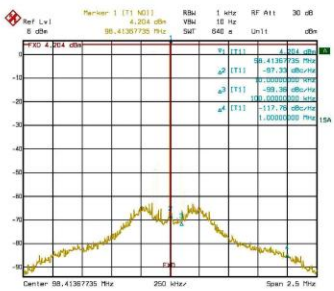

Fig.10 The measured phase noise of PLL

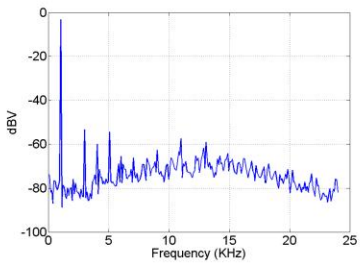

Fig.11 Spectrum of the demodulated signal

2.5MHz. The noise shaping function is verified through the matched spectrums. The difference in the noise level at low frequency is mainly due to the thermal noise in real circuit.

TABLE I. PERFORMANCE SUMMARY

Architecture	ΔΣ PLL transmitter	
Process	0.13µm	
Output Range	(79.2~112.8) MHz	
Reference Frequency	2.4 MHz	
THD and Noise	0.1% (Minimum)	
	< 1% (@75kHz)	
Area (excluding pads)	0.24 mm^2	
Power Supply	1.2V	
Current consumption	Total	4.4mA
	ΔΣ Modulator	0.3mA
	PLL	2.6mA
	Buffers	1.5mA

The phase noise was measured using a Rohde&Schwarz FSEB spectrum analyzer. As shown in Fig.10, the phase noise at 98.4MHz carrier frequency is -97, -99 and -117dBc/Hz at 10kHz, 100kHz and 1MHz offset, respectively.

Fig.11 illustrates the spectrum of the demodulated signal. An HP 8901B modulation analyzer was used to demodulate the FM output of the transmitter. The demodulated signal was fed to an Audio Precision System-2 that measured THD plus noise and the spectrum. The measured THD plus noise was less than 1% at the maximum frequency deviation 75kHz.

VI. CONCLUSION

This paper presents a ΔΣ PLL FM transmitter for short range applications. The modulation signal from baseband is lead to a single-bit ΔΣ modulator, output of which controls the division number of the PLL feedback divider. With this approach, it is straightforward to realize a fully integrated FM transmitter with high performance.

A circuit was implemented in a 0.13µm CMOS process by students in the course IC-project and verification at Lund University. The circuit was fabricated and measured, showing less than 1% THD plus noise of a demodulated RF signal with a frequency deviation of 75kHz, consuming 4.4mA from a 1.2V supply.

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Paper II

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A Digital PLL with a Multi-Delay Coarse-Fine TDC

Ying Wu, Ping Lu, Pietro Andreani
Department of Electrical and Information Technology, Lund University, Sweden
Email: mas09ywu@student.lu.se, {Ping.Lu, Pietro.Andreani}@eit.lth.se

***Abstract*—A 5GHz digital frequency synthesizer achieving a low noise for wireless RF application is presented. This architecture uses a multi-delay coarse-fine Time-to-Digital Converter (TDC) to achieve both the large detection range and fine resolution. A Digitally Controlled Oscillator (DCO) based on capacitive degeneration in LC-Tank is also implemented. The DCO achieves frequency quantization step of 300 Hz without any dithering. Simulated phase noise at 5 GHz carrier frequency is -125 and -151 dBc/Hz at 1 MHz and 20 MHz offset, respectively. The Digital phase-locked loop (DPLL) is realized in 90nm CMOS process and consumes 14mA from a 1.2V supply.**

I. INTRODUCTION

Digital phase-locked loops have recently emerged as a viable alternative to traditional analog PLL. The migration of PLL towards to digital architectures with a comparable and even better performance will be made possible by the deep-submicron CMOS process.

Currently, there are two main types of DPLL architectures which are used for high performance frequency synthesis: counter-assisted digital PLL (CDPLL) and divider-assisted digital PLL (DDPLL) [1, 2]. As we noted, in CDPLL, the TDC uses the very high frequency clock directly from DCO to quantize the phase error, resulting in high power consumption. In addition, the period normalization of output from TDC leads high complexity of the circuits. On the contrary, in the DDPLL, as shown in Fig.1, the TDC is specifically employed to measure edge time difference between the reference clock and the complementary DCO clock after divider, which is much larger than the DCO period. Therefore, it reduces the power consumption and simplifies the TDC design.

In this work, a multi-delay coarse-fine high resolution TDC based CMOS DPLL is proposed and implemented. The TDC has a coarse delay line with different delay cells [3]. In classical TDC [1], the delay cells should be matched to be as equal as possible. However, as we noted, only a number of delay cells will be used when the loop is in the locked state. The rest part of delay cells are used only at acquisition and will thus not affect the phase noise performance. Therefore, the multi-delay structure releases the requirement for a large number of delay cells which should cover the whole period of reference clock. This reduces the power consumption and saves the chip area. The highest time resolution of the coarse delay line is a single buffer delay (two inverters), approximate 20ps in 90nm CMOS process. In order to increase the time resolution which dominates the in-band noise of PLLs, a coarse-fine TDC based on time amplifier (TA) is introduced [4]. The TAs are utilized to amplify the time residue with a high gain in order to resolve the time interval better than a single buffer delay. As such, the combination of multi-delay and coarse-fine architectures

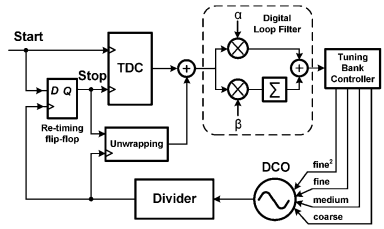

Fig.1 Block Diagram of proposed DPLL

achieves both the large detection range and high time resolution.

The DCO is the replacement of the VCO in analog PLLs. The frequency tuning of the DCO presented in [1] is accomplished by means of a quantized capacitance of the LC tank. Due to the natural discrete tuning of DCO, the quantization noise is inevitable, which will degrade the total noise performance. A reduced frequency step reduces the quantization noise. In [1], the required frequency resolution is achieved by frequency dithering using a sigma-delta modulator but, as occurs in any sigma-delta data converter, the quantization noise is moved to higher frequencies. However, the DCO here is to move part of the tuning bank from the tank to the sources of the switching pair, exploiting an intrinsic shrinking effect [5]. A control mechanism for bank selection is then added to make the DPLL work automatically.

An overview of the paper is as follows. Section II describes the proposed DPLL architecture. Section III details the circuit implementation. Section IV gives the simulated results. Conclusions are drawn in Section V.

II. LOOP ARCHITECTUE

Fig. 1 shows the block diagram of the proposed DPLL. The key components of the proposed structure are a multi-delay coarse-fine high resolution TDC, a retiming flip-flop, unwrapping circuit which eliminates the phase wrapping at TDC output, digital loop filter, the asynchronous divider with a low-power implementation and the DCO achieving both the large tuning range and the fine frequency resolution.

The TDC measures the phase error between the two inputs *Start* and *Stop*. Since a TDC cannot handle a negative phase error directly, the retiming flip-flop is needed to make *Start* always lead *Stop*. In addition, the retiming flip-flop is clocked at four times the reference frequency. As shown in Fig.2 the maximum time span seen by the TDC is 1/4 the reference period rather than the full reference period. In the case the phase error exceeds the detection-range, the "phase wrapping" will occurs, that is, the TDC overestimates or underestimates the phase

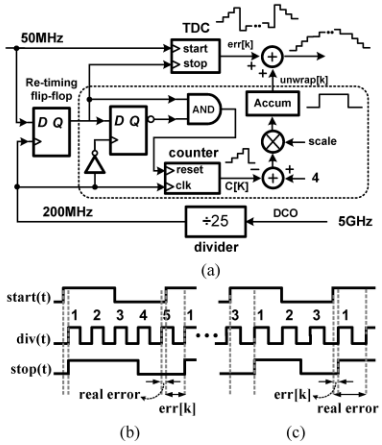

Fig.2 Phase unwrapping function

error *err[k]*, as shown in Fig.2(b) and Fig.2(c). Therefore, the idea is to switch in an offset *unwrap[k]* to eliminate the negative effect of the phase wrapping [2]. The unwrapping function in this prototype is implemented in Fig.2(a). The counter output is leveraged to indicate whether phase wrapping occurs. Its output compares with four, and their difference is scaled and accumulated to generate *unwrap[k],* which provides the offset value to the TDC output. The scale factor is a digital word corresponding to the full range of TDC. Once the PLL is locked, no phase wrapping occurs, *c[k]* is four and nothing is accumulated.

The TDC output with the unwrapping function drives the digital loop filter. To support type-II loop, the DLF consists of a proportional path and an integration path. The DLF can be easily configured to type-I or type-II PLL by disabling or enabling the integration path. In order to further speed up the setting time, the loop is to start with the ultra-wide acquisition bandwidth and to progressively narrow it down while traversing through finer DCO tuning banks. At the end of setting, the PLL switches its characteristic from type-I to type-II in order to filter out the high frequency noise and ensure almost zero phase error between reference and feedback clock.

The tuning bank controller is a digital interface of DCO which switches capacitances in and out of the LC-resonator [3]. It operates as follows: at initialization, the loop uses the coarse tuning bank and then, when the coarse control word becomes sufficiently stable, moving only inside a small range, a judging mechanism decides to lock the tuning word to an average value in that stable state. The control is then switched to the next control bank. As shown in Fig.1, the four tuning banks, coarse, medium, fine and fine^2 are sequentially activated during the frequency locking. The fractional parts of fine^2 bank have the smallest elementary capacitance which determines the DCO resolution in the locked state.

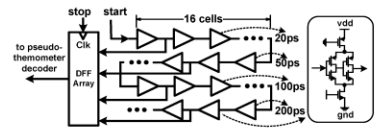

Fig.3 Multi-delay architecture of TDC

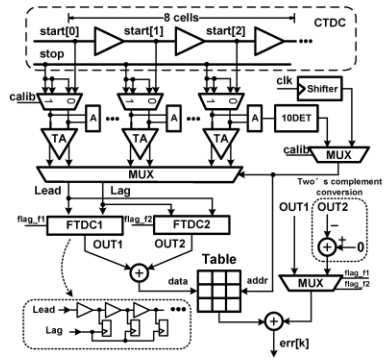

Fig.4 Coarse-fine architecture of TDC

III. CIRCUIT DETAILS

A. Multi-delay coarse-fine TDC

In traditional TDC, the delay cells are matched as equal as possible. However, when the PLL is in the locked state, the loop is configured to type-II, which means that only a small part of the buffers are activated in maintaining the feedback. Therefore, a TDC with different delay-time cells is implemented, as shown in Fig.3. The complete delay chain has been divided into four segments. The first segment has the shortest delay-time cells, eight of which are used for the time amplification for the fine TDC (FTDC). The other three segments use current-starved inverters to increase the delay time and reduce the power consumption.

The coarse-fine architecture resolves intervals less than a buffer delay by amplifying the time residue. The TAs used in this design have a high gain (=16 to use a 4-bit fine TDC) and a linear range large enough to cover the shortest delay (T_d = 20ps) of one stage in the coarse line. As shown in Fig.4, the time difference between the edge of each buffer, *start[k],* and the edge of *stop*, creates every possible time residue. While the arbiters (A) determine which of the residues is the critical one, and then the detector (DET) identifies the critical amplified residue to be sent to the FTDC for the fine conversion. The FTDC consists of one buffer chain which is similar to the traditional TDC [1]. The time resolution of FTDC is equal to the shortest delay cells in coarse line, about 20ps. Therefore, the final resolution of the TDC achieves 1.25ps (20ps/16). The Fig.5(a) details the circuit of TA, the gain of which is express as

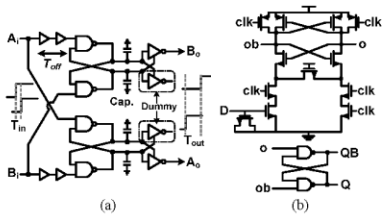

Fig.5 Architecture of (a) TA, (b) small setup-time flip-flop

$$A_T = \frac{2C}{g_m T_{off}} \quad (1)$$

Where the g_m is the transconductance of a NAND gate in metastability and C is the capacitance at its output. The T_{off} is the time offset that can control both the gain and linear range [4]. The flip-flop in Fig.5(b) has the small setup time which means the amount of time the data signal should be held steady before the clock event.

As can be seen in the typical operational amplifier, the device mismatch in a TA shifts the zero crossing of the gain curve, which appears as a TA offset. This offset can be corrected by calibration in the following way. The *Calib* switches the multiplexer (MUX) to feed though the same *stop* signal to both inputs of the TA, which creates zero input, and thus the amplified offset is quantized by the FTDC and stored in the look-up table, and then the value in the table will correct the output of the FTDC during normal operation. Since the offset value can be positive or negative and also large enough to drive the FTDC into over-range, double FTDCs with opposite direction are introduced and the number of stages is doubled (4+1 bits). In particular, the outputs of two FTDCs are always expressed as absolute value. Therefore, the output from FTDC2 should be converted to two's complement. This offset calibration process is sequentially performed during the startup by shifting the control pulse signal to select each TAs.

B. Digitally-Controlled Oscillator

The Fig.6 illustrates the architecture of DCO, which consists of LC oscillator core and four tuning banks. Three 4-bit banks (named coarse, medium and fine tuning banks) are located in the LC-tank. However, the fine^2 bank, in particular, moves from the tank to the source of the switching pair of the LC oscillator. As reported in [5], the capacitive degrading mechanism produces an equivalent scaled down replica of the fine^2 tuning bank in parallel to the LC-tank. The effect of C on the DCO frequency tuning characteristic can be estimated by the admittance Y in Fig.6. For $g_m \ll 2\omega_{LO}C$ the admittance can be approximated as:

$$Y = -\frac{g_m}{2} - j\omega_{LO}C \cdot \left(\frac{g_m}{2\omega_{LO}C}\right)^2 \quad (2)$$

Where the real part is the classical negative conductance that compensate the tank losses, while the imaginary part is equal to the capacitor C shrunk by a factor $g_m^2/(2\omega_{LO}C)^2$. The MOS conductance g_m is averaged over one period of the oscillation frequency. The value of g_m required to sustain the oscillation can correspond to a shrinking factor that makes the value of C excessively large. To solve the problem, a second cross-coupled transistors pair is added in parallel to M3-M4. The M1-M2 provides an extra degree of freedom to choose the shrinking factor. The M1 and M2 are biased to operate in Class-C resulting in reducing the phase noise and lowering the current necessary for a given shrinking factor [5]. To further improve the phase noise performance, the noise filtering technique with an inductor in the tail current source is also used.

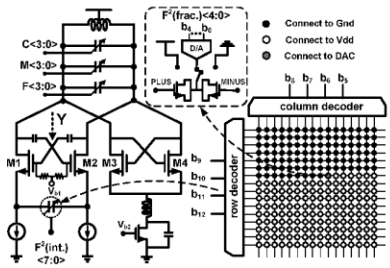

Fig.6 Complete DCO scheme with four tuning banks

The integral and fractional bits of fine^2 bank are realized as depicted in Fig.6. The 8 most significant bits (MSB) are used to control a matrix of 16×16 varactors. All elements except one are connected either to voltage supply or ground, generating a thermometric filling of the matrix. The remaining one varactor is connected to the output of a 5-bit digital-to-analog converter (DAC). It provides 32 additional voltage levels which realized as the fractional part of fine^2 bank, generating the finest resolution of DCO.

C. Digital Loop Filter and Tuning Bank Controller

A type-II PLL is used in this work for its zero phase difference characteristic, which allows use of the multi-delay coarse-fine TDC. In the digital loop filter, this is accomplished by summing a proportional phase error (scaled by $\alpha=2^{-n}$) and an accumulated phase error (scaled by $\beta=2^{-(n+1)}$). The scaling factors are chosen as 1/2 to the power of n, where n is an integer. In order to speed up the setting time, the loop is to start from type-I corresponding to fast loop dynamics. The α value is changed several times during the frequency locking with an initial $\alpha=2^{-1}$, then $\alpha=2^{-2}$, $\alpha=2^{-3}$ and final $\alpha=2^{-2}$ values for coarse, medium ,fine, and fine^2, respectively. The final value of α is chosen to be the best phase noise performance. The integral loop factor β is activated after the fine bank is settled. It switches the PLL characteristic from type-I to type-II in order to effectively improve the phase noise.

The tuning bank controller makes the PLL work automatically when multiple frequency tuning banks are adopted in DCO. The details of the circuit have been reported in [3].

IV. Simulation Results

The DPLL is implemented in a 90-nm CMOS process. The simulated DCO gain curves are shown in Fig.7. For

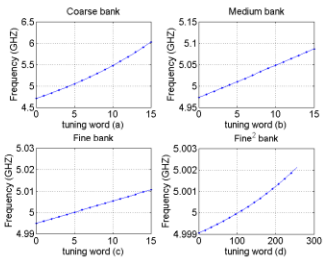

Fig.7 Simulated DCO gain curve of four banks. (a) coarse bank (b) medium bank (c) fine bank (d) fine^2 bank (integral bits)

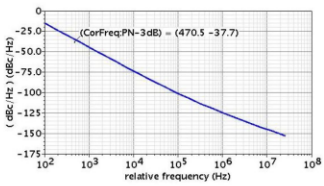

Fig.8 Phase noise performance of DCO

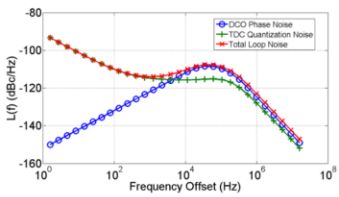

Fig.9 Simulated output phase noise of synthesizer

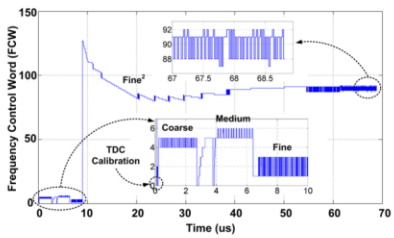

Fig.10 Simulated Frequency Control Word during locking

each bank simulation, the others were kept unchanged. The average coarse, medium, fine and fine^2 frequency steps are 70MHz, 7MHz, 1MHz and 10kHz, respectively. In particular, since one varactor in fine^2 bank is connected to a 5-bit DAC, the finest frequency resolution is approximate 300Hz (10kHz/32).

As shown in Fig.8, the phase noise of DCO at 5GHz carrier frequency is -125 and -151dBc/Hz at 1MHz and 20MHz offset, respectively.

TABLE I. PEFORMANCE SUMMARY

Architecture	divider-assisted DPLL	
Output Frequency	4.7GHz-6GHz	
Reference Frequency	50MHz	
Phase Noise@5GHz	-125dBc/Hz@1MHz -151dBc/Hz@20MHz	
Feature Size	90-nm CMOS	
Power Supply	1.2V	
Current Consumptions	Total	14mA
	TDC+Unwrapping	5mA
	DCO	7.5mA
	Divider+ Digital Circuits	1.5mA

The TDC Noise contribution, within the loop bandwidth, at the DPLL RF output is [1]

$$S_{TDC} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{delay}}{T_{DCO}}\right)^2 \frac{1}{f_{REF}} \qquad (3)$$

where Δt_{delay} denotes the delay time of a buffer cell, T_{DCO} the period of RF output, and f_{REF} is the frequency of reference clock. As shown in Fig.9, the noise performance of DPLL was obtained by using *Cppsim System Simulator* [2]. The loop bandwidth is designed 100kHz and the estimated noise performance of the DPLL at 5GHz is -110, -111, -124 dBc/Hz at 10kHZ, 100kHz and 1MHz offset, respectively.

Fig.10 illustrates the frequency control word (FCW) during the phase locking. The loop characteristic moves from type-I to type-II when the fine^2 tuning bank is activated. When the loop is locked, the control word switches among four numbers, which generates the average value of the FCW. Fractional tracking bits of fine^2 bank do not contribute significantly to the locking process, so for clarity are not included.

V. CONCLUSIONS

This paper presents system design, circuit implementation and simulation results of a divider-assisted DPLL. The multi-delay coarse-fine TDC achieves large detection-range and high resolution of 1.25ps. The DCO with the finest frequency step 300Hz is implemented for good phase noise performance. The DPLL is realized in 90nm CMOS process and consumes 14mA from a 1.2V supply.

VI. REFERENCES

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