DESIGN OF A SUCCESSIVE APPROXIMATION (SAR) ADC IN 65 nm TECHNOLOGY

SUBMITTED BY

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ABSTRACT:

In the current technical era, the technology advancement leads most of the applications demanding for a reduction in the whole size of the system in terms of its space occupied in any device. Mobile applications are one of the apt scenarios for this category. Apart from the size reductions due to the technology advancement, it also calls in for the reduction in the power consumption.

The Data Converters section, besides being very power hungry, it is also usually extremely power hungry in comparison with the other blocks of any architecture and that's why low power has also become a tough requirement in most of the systems. The total power consumption of the system being maintained in a low figure has almost become a mandatory specification in many applications.

The SAR Analog to Digital Converter architecture is chosen in this master thesis project, as it is one of the very successful moderate resolution achievable converter system present among all the data converter architectures. The schematic model of the entire system is implemented in Cadence system in order to fulfill the technical requirements of the project.

The SAR architecture is implemented in ST Microelectronics 65 nm technology and the power supply used is 1.2 volts. A differential configuration of the whole system is thoroughly studied and an equivalent single ended system is also studied, implemented and measured in this project. The differential architecture is studied in this project to learn the merits behind the differential architecture, which basically avoid the linearity and offset errors raised in the single ended architecture. The resolution for which the system is designed is 10 bits. The reference voltage maintained here is 600mV, which is half of the full-scale value.

ACKNOWLEDGEMENT:

I sincerely would like to thank Mr.Dejan Radjen for his timely help and assistance, my project supervisor Professor Mr. Pietro Andreani and my project coordinator Professor Mr. Peter Nilsson for giving away this opportunity of carrying out my master thesis work under their supervision.

I would like to dedicate this work to my friends Valentina, Ibrahim, Mark, Shyam, Rohit and also to all of my corridor friends. Last but definitely not the least, a life size thanks to my mother for being the sole reason for what I am today. Thanks Amma.

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CHAPTER I

1.INTRODUCTION:

In the fastest changing electronics world, the grip which Analog electronics has always had, can never be changed or manipulated in any kind of applications right from old trivial designs to high end designs. In-spite of the Herculean development in Digital electronics, the status of Analog electronics still remains proud enough as the real world always operates on Analog concepts.

As all the real quantities are analog in nature, in any kind of applications there should be some means to convert those analog quantities into digital logic levels to process the signals according to the applications' accuracy requirements. So the referred critical job of converting from Analog levels to Digital levels is generally carried out with the help of Data Converters.

The two obvious types of Data converters are Analog to Digital (ADC) and Digital to Analog (DAC) converters. In this thesis work, the type ADC is chosen to evaluate the merits and demerits with respect to its expected specifications. There again comes a major classification in types of ADCs namely the Nyquist type ADCs and Oversampled ADCs mostly differentiated by the sampling frequency specified.

In all the portable applications, the main concerned issue would be the withstanding capacity of the battery power, which directly reflects to the power dissipation capability of all the circuits present in that system. As the technology develops/advances, the Digital world does as well, equally in terms of its circuits' performance but the real bottleneck has been posed on Analog side of the application as low voltage analog powered systems demand some tough compromises in

the circuit to maintain the same or improved performance levels as before.

As normally any data converter circuits possess both analog and digital circuits in its system, the technological constraints like operating frequency, supply voltage levels, voltage swing limits, power consumption do speak a lot in terms of its difficulties in implementing the system in par to the advancement in technology.

1.1 THESIS ORGANIZATION:

This master thesis report is basically divided into four different sections. In the first division, the general theory about Data Converters, important types of Data Converter architectures, the reason for analyzing SAR converters for this masters project, necessary performance parameters to be considered during Data Converters designing and general applications of Data Converters in the electronic market.

In the second division, the schematic level of both single ended and differential architectures of 10-bit SAR ADC is implemented through the help of Cadence simulation tool and through the VerilogA language.

In the third division the simulation details, the plots corresponding to those simulations and also the measurement of performance parameters of all the possible static and dynamic characteristics are presented.

In the fourth division, the result and conclusion about the SAR performance is explained with the possible improvements that can be proposed for the possible improvements in the master project proposed in this report. The final appendix part composes of the Matlab code used for the measurement of performance parameters and also the verilogA code of the SAR Logic block used in the system.

CHAPTER II

2.THEORY OF OPERATION:

2.1 DATA CONVERTERS:

In general, Data Converters (here ADC) constitutes an important block in any kind of applications where the continuous amplitude, continuous time real world analog signals are transformed into discrete time, quantized amplitude digital signals as an end product.

An entire ADC system can be divided into four main sections namely

- Anti_Aliasing Filter
- Sampling
- Quantisation
- Coding

The operation of an ADC is highly non-linear as the sampling and quantization process is inherently a non-linear operation. The operating frequency (sampling frequency) decides the design and specifications of the anti_aliasing filter. Based on the sampling frequency, the ADCs can be broadly classified into two major categories namely

- Nyquist Rate ADCs
- Oversampled ADCs

2.2 NYQUIST RATE ADCS:

When the referred ADC's sampling frequency is minimum twice the signal frequency as per the Nyquist's Sampling theorem, then those ADCs are termed as Nyquist Rate ADCs. There are various different types of Nyquist rate ADCs present in the Data Converters market out of which the very familiar and famous ones are mentioned with suitable explanation of its operation.

The converters, which can be thought of very successful, are

- Flash ADC
- Interpolating ADC
- R-2R and C-2C ADC
- Pipeline ADC
- SAR ADC

2.2.1 FLASH ADC:

Flash ADC referred also as Direct Conversion ADC is one of the familiar types of ADC for its fast operation. It comprises a linear voltage ladder with different reference voltage nodes created by resistors. The input voltage signal is compared with the respective voltage node from the voltage reference ladder with the help of a comparator, which are there each at every reference node point and the output of the comparator is allowed to enter the digital logic circuitry to produce the necessary output in the respective format.

Pros: Extremely fast Conversion time

Con: Number of comparators (2^n-1) increases as the resolution (n) increases and hence the noise and power consumption.

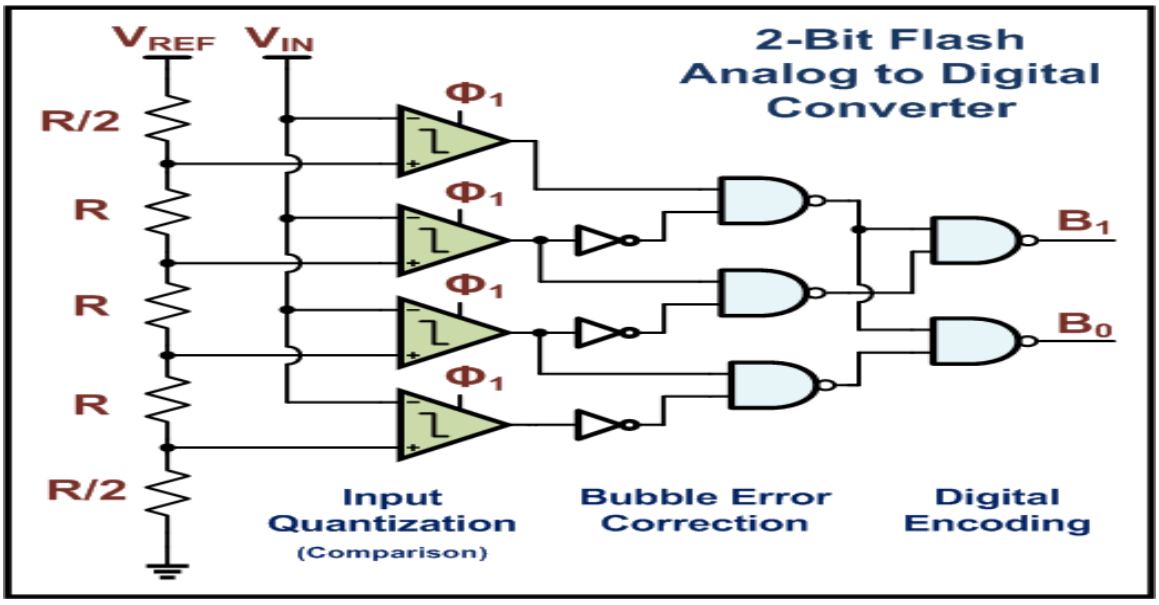


Figure 2.1: 2-bit Flash AD *(Ref: Wikipedia)*

2.2.2 INTERPOLATING ADC:

This type of ADC converts an unknown input voltage into a definite digital value through the help of an integrator and a known reference voltage source. The basic operation is as follows. An unknown input voltage level is applied to the inverting input of an integrator and allowed to ramp up for a certain predetermined run-up time. Once the run-up time is reached, then a known level of reference voltage of opposite polarity to the input voltage is now applied to the inverting output of the integrator. The time it takes to ramp down the integrator response is noted down and it's called as run-down time. So an unknown voltage level can thus be computed as a function of reference voltage, run-up and run-down time.

Pros: Highly Accurate

Con: Extremely slow (6 samples per second) and thus not suitable for audio and signal processing applications. Used in digital voltmeters.

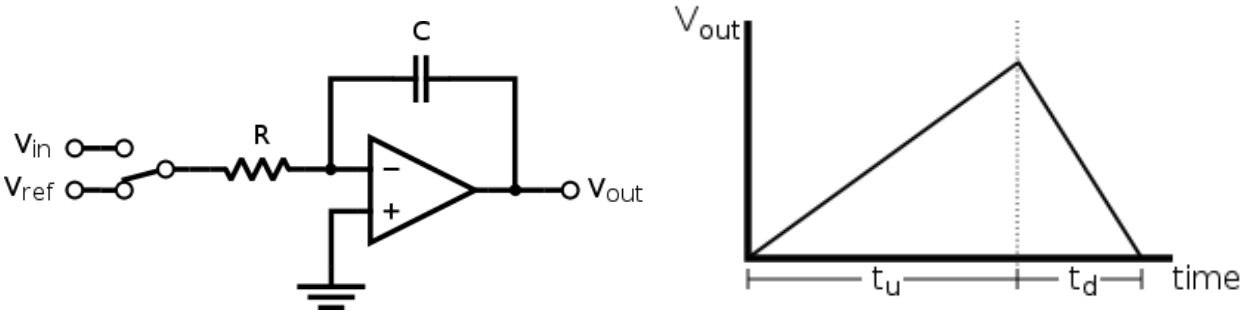


Figure 2.2: Integrating ADC and its output waveform (*Ref*: *Wikipedia*)

2.2.3 PIPELINE ADC:

This type of ADC, which is also known as Sub ranging ADC is very notorious for its high-resolution achievement and better throughput. As the lower sampling rate applications are dominated by SAR converters Integrating ADCs and Delta-Sigma Converters and the higher sampling rate applications are dominated by Flash Converters, the pipeline ADC can be considered to be in the middle range which compromises in a good way with most of the technical specifications of the Data converters in general such as SNR, SNDR, Resolution, Quantization noise etc.

The operation of this converter is as follows with respect to the figure presented below. It consists of four identical stages in which the conversion takes place successively. The input analog voltage is allowed to pass through a sample-and-hold circuit to make a discrete time signal. It is also passed through a Flash ADC to convert the signal into 3-bit digital value. But this is called as the stage of coarse conversion, which concentrates mostly on the computation of MSBs. This 3-bit digital value is subtracted from the sample-and-hold value and the residue value is sent to the successive stages for further refinement of the signal for better accuracy. The output of the final stage is connected to a 4-bit flash converter where the LSBs are computed.

Pros: High throughput, better efficiency, moderate sampling rate

Con: Latency

2.3 OVERSAMPLED CONVERTERS

2.3.1 DELTA SIGMA ADCS:

This converter is one of the very famous and efficient types of ADCs present in the current market. This converter trades off sampling rate for high resolution. The oversampling ratio (OSR), which is defined as the ratio of the Nyquist frequency ($f_s/2$) and the signal frequency, decides the efficiency of the converter. The order of the converter depends on the application it is used for. Most of the time, second order is preferred as it has a good compromise between circuit complexity and better performance. The basic first order modulator is explained as follows.

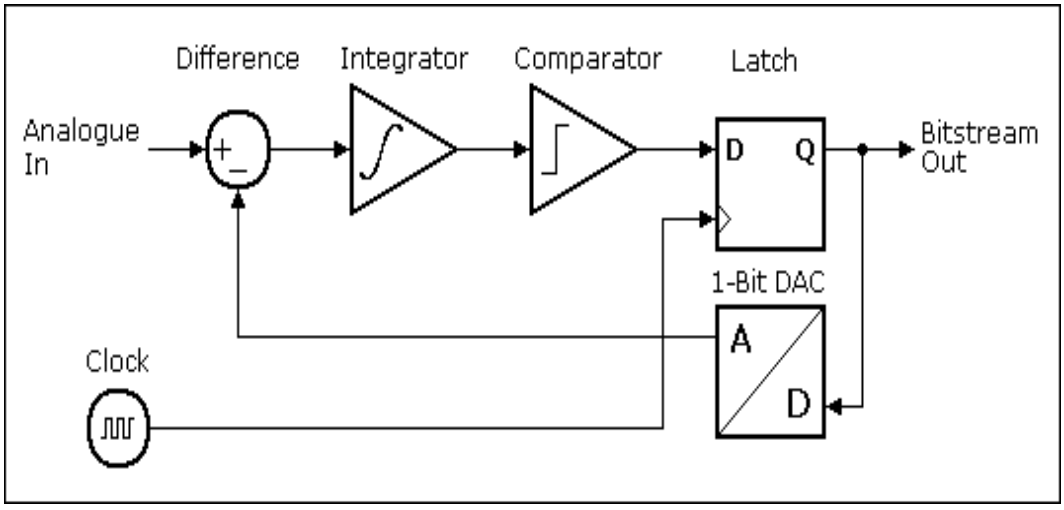


Figure 2.3: First order Delta Sigma Modulator (*Ref: http://www.beis.de*)

The difference block computes the error waveform, which comes as a result of the subtraction of the analog input signal and the output of the 1-bit bitstream passed through the DAC. Then it gets integrated and compared with the threshold reference level to give either a high level (1) or a low level (0) bitstream. The bitstream is usually higher than the data rate of the ADC. The averaging of the bitstream is done after the modulator section through digital processing to get the digital equivalent of the input analog signal. The SNR depends on the order of the modulator and also on the OSR ratio.

2.4. PERFORMANCE METRICS:

There are different performance metrics used in an ADC to explain its quality in many different ways. These performance metrics are broadly classified into two major divisions namely

- Static Characteristics
- Dynamic Characteristics

The category of Static Characteristics is again classified into four different types namely

- Differential Non Linearity (DNL)
- Integral Non Linearity (INL)
- Offset Error
- Missing Codes

The category of Dynamic Characteristics is compromised of four major performance parameters namely

- Signal to Noise Ratio (SNR)
- Signal to Noise and Distortion Ratio (SNDR)
- Spurious Free Dynamic Range (SFDR)
- Effective Number of Bits (ENOB)

2.4.1. STATIC CHARACTERISTICS:

Static Characteristics of an ADC explains the deviation of the transfer characteristics of an ADC from the ideal characteristics. As mentioned above, the four performance parameters DNL, INL, Missing codes and Offset error comprises in this category.

2.4.1.1 DIFFERENTIAL NON-LINEARITY (DNL):

Differential Non linearity is one of the important performance parameter in the static characteristics. It explains the difference in code width of one LSB level from the ideal width of one LSB level. If for example the code width for the code 10 is 0.25 LSB longer than the ideal width of it, which is 1LSB, then the DNL error is +0.25 LSB. In the same way, if the code width is 0.25 LSB shorter than the ideal code width, then the DNL error is -0.25 LSB. During the measurement of DNL and also INL, the offset error and the full-scale error are considered negligible. The positive DNL error can be computed from widest code and the negative DNL can be computed from the narrowest code.

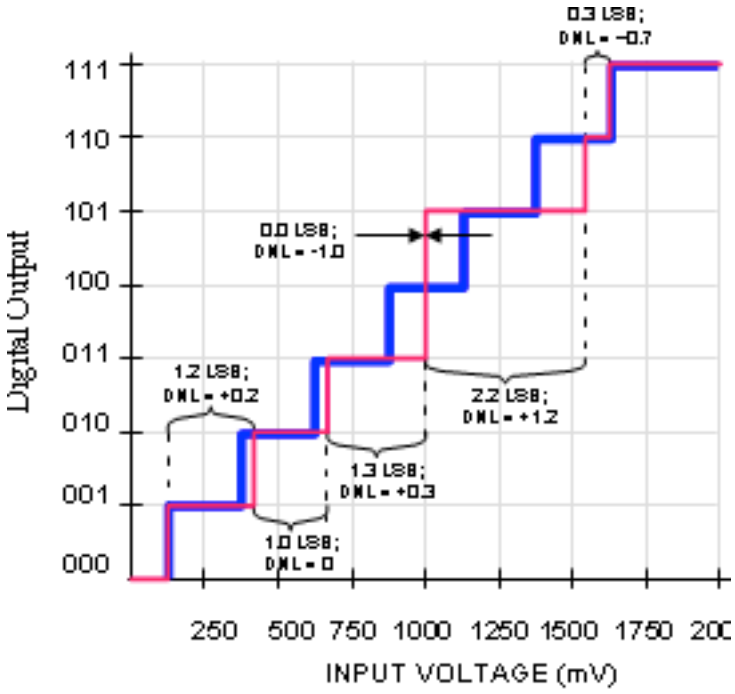


Figure 2.4: DNL Characteristics for a 3-bit converter (XX)

2.4.1.2 INTEGRAL NON-LINEARITY (INL):

Integral Non Linearity is again one important static performance parameter, which is a lot similar to DNL in terms of its measurement process. It explains the deviation from the ideal straight line shaped transfer characteristics. It actually explains the cumulative nature of the DNL property of the mentioned system. The size and distribution of DNL errors decide the nature of INL of the converter. The dotted line in the diagram represents the ideal characteristics whereas the bold line represents the actual characteristics.

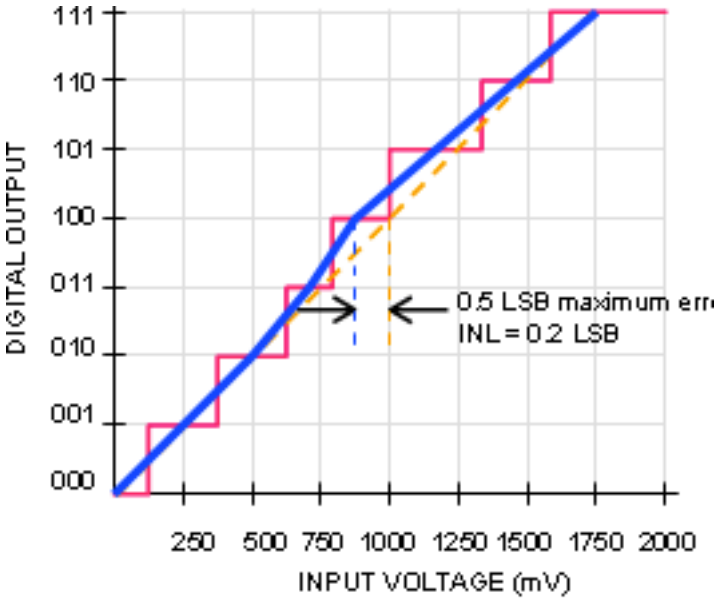


Figure 2.5: INL Characteristics for a 3-bit converter (XX)

2.4.1.3 OFFSET (ZERO) ERROR AND FULL SCALE ERROR:

Offset Error is the difference between the beginning of the first actual code transition point and the ideal code transition point present in the ideal characteristics. The full-scale error is the difference between the beginning of the actual last code transition point and the point where the last code transition point starts for an ideal ADC.

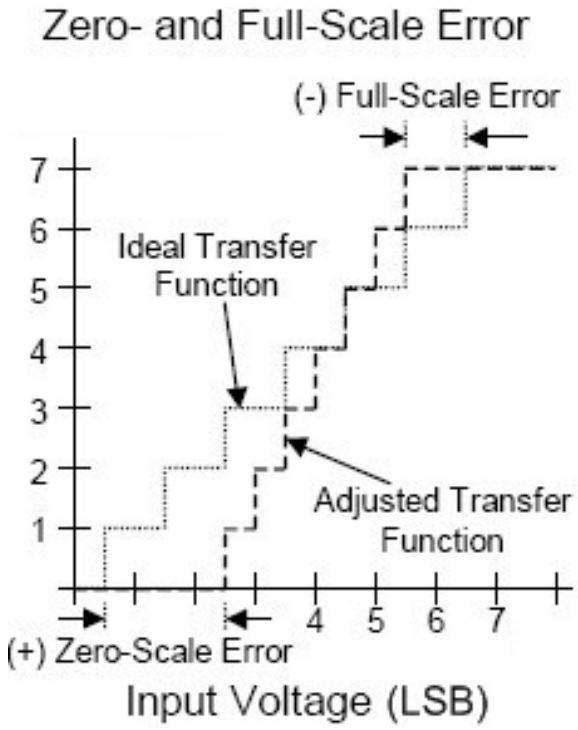


Figure 2.6: Zero/Full Scale Error for a 3-bit converter (XX)

2.4.1.4 MISSING CODES:

Missing Codes are the ones that are missing from the transfer characteristics of an ADC mainly either due to the masking of that specific code by the lower transition code or by the upper transition code. The code, which gets missed, gives out a DNL of -1 LSB. So if there is an appearance of -1 in the DNL graph, then that's a sign to prove in one way that there is a missing code in the system during the conversion process.

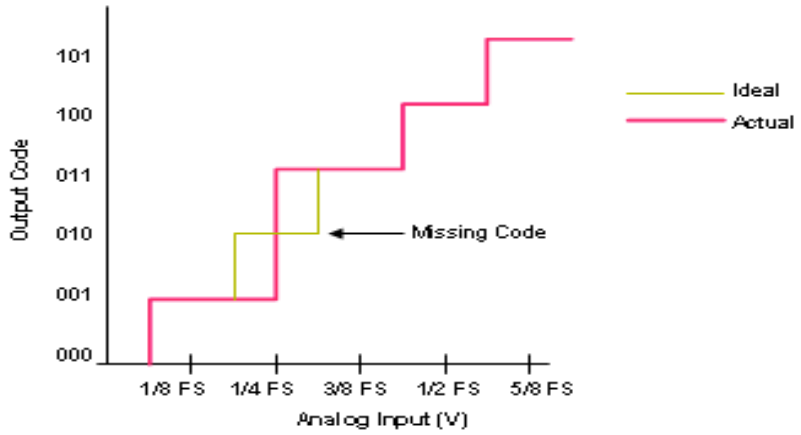


Figure 2.7: Missing codes plot for a 3-bit converter (XX)

2.4.2 DYNAMIC CHARACTERISTICS:

The Static Characteristics are tested by a DC input whereas the dynamic characteristics are measured by the response of the ADC for a sinusoidal input. It is used to compute the frequency response of the system. This analysis is used to know more information about noise and also about other high frequency effects. These performance metrics are exhibited by the parameters like SNR, SNDR, SINAD, SFDR and ENOB.

2.4.2.1 SIGNAL TO NOISE RATIO (SNR):

The SNR can be defined as the ratio of the power of the signal and total noise power generated by quantization process. Usually the signal, which is referred here, is a sinusoidal signal. This dynamic property accounts for the whole noise present in the entire Nyquist range. Its value depends on the magnitude of the input signal and it proportionately decreases with the reduction in the signal amplitude. The value of SNR is given by SNR = ((6.02*Resolution) + 1.76).

2.4.2.2 SIGNAL TO NOISE AND DISTORTION RATIO (SNDR):

SNDR can be defined as the root mean square of the power of the signal in the Nyquist range and the noise power due to quantization process and also due to the other noise sources (except dc noise) including the non-linear distortion sources.

2.4.2.3 SPURIOUS FREE DYNAMIC RANGE (SFDR):

SFDR can be defined as the ratio of the root mean square of the signal amplitude and the root mean square value of the highest spurious spectral component that could possibly present in the first Nyquist interval.

2.4.2.4 EFFECTIVE NUMBER OF BITS (ENOB):

The Effective Number of bits (ENOB) is a parameter, which stands out to show the accuracy of the ADC for a specific input signal given at a specific sampling rate. It can be computed by the following expression, which is as follows

$$\mathbf{ENOB} = \frac{\boldsymbol{SINAD}\ (\boldsymbol{dB}) - \mathbf{1.76}\ (\boldsymbol{dB})}{\mathbf{6.02}\ (\boldsymbol{dB/bit})}$$

2.5 SUCCESSIVE APPROXIMATION (SAR) CONVERTERS:

Among various advantages copyrighted to itself by its own architecture, the simple implementation is also a big plus for SAR converter. The whole system can be divided into four main subsystems namely

- Sample (Track) and Hold Circuit
- Digital to Analog (DAC) Converter
- Comparator
- SAR Logic Block

The main operation of the SAR works on Binary search algorithm. The operation is assumed to have a digital value equal to half of the full-scale value at the digital registers present in the SAR logic block. This condition leaves us with the logic 1 as MSB and rest of all the bits to be logic 0. The corresponding switches to this mentioned condition gets activated in the DAC block to have the necessary capacitors connected to the actual operation. This gives away the necessary voltage from the DAC block to the comparator input where this voltage level is compared with the input voltage.

If the input voltage is less than the DAC voltage level, then the comparator outputs a logic 0 and logic 1 if it's the other way around. This output value is stored in one of the SAR logic block's registers and the next comparison is

done in the comparator with the newly generated next DAC voltage level to get the correct digital level interpretation of the analog input voltage level. Usually the sampling frequency of the input signal is N (number of bits) times lesser than the clock frequency of the system clock as the internal clock has to be N times faster than the input clock to convert all the bits successfully. The capacitor stage in the DAC block have also got a dummy capacitor next to the LSB stage in order to make the total amount of capacitance to a power of 2 which makes the analysis better and sensible.

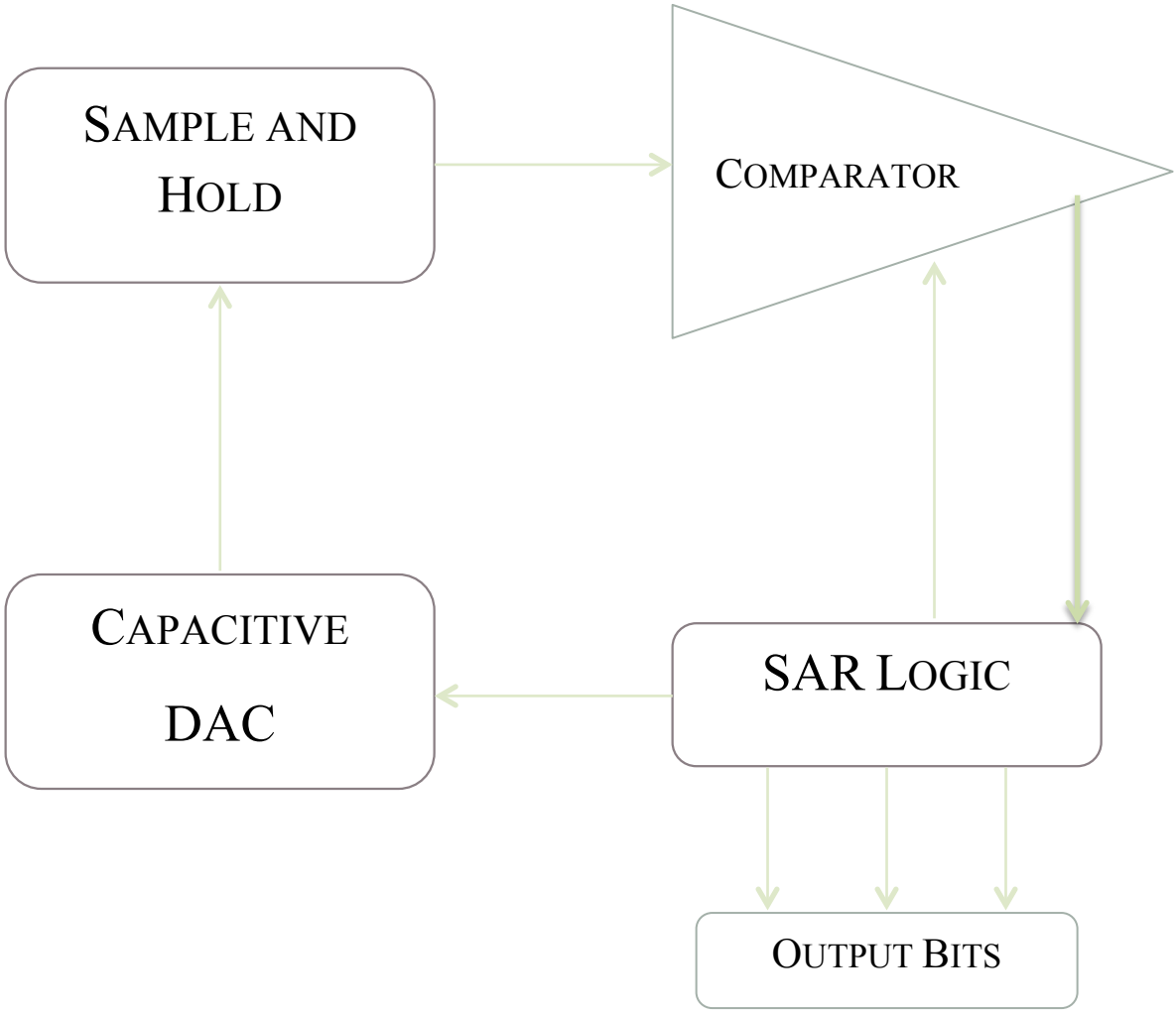


Figure 2.4: General block diagram of SAR ADC

2.6 WHY SAR AND NOT OTHER ARCHITECTURES?

SAR architecture has only one comparator block, which is relatively a low power-consuming block. It also reduces the power hungry requirement by not having an opamp block in its system and hence an appreciable power consumption factor can be achieved in comparison with other architectures.

The power dissipation capacity gets scaled with the sample rate associated with the system unlike Flash ADCs in which the power dissipation is independent of the sample rate. In this project, the signal frequency is maintained at 200 Hz and the sampling rate is around 2 KS/s. The frequency of the internal clock is maintained at the rate of 22 KHz.

CHAPTER III

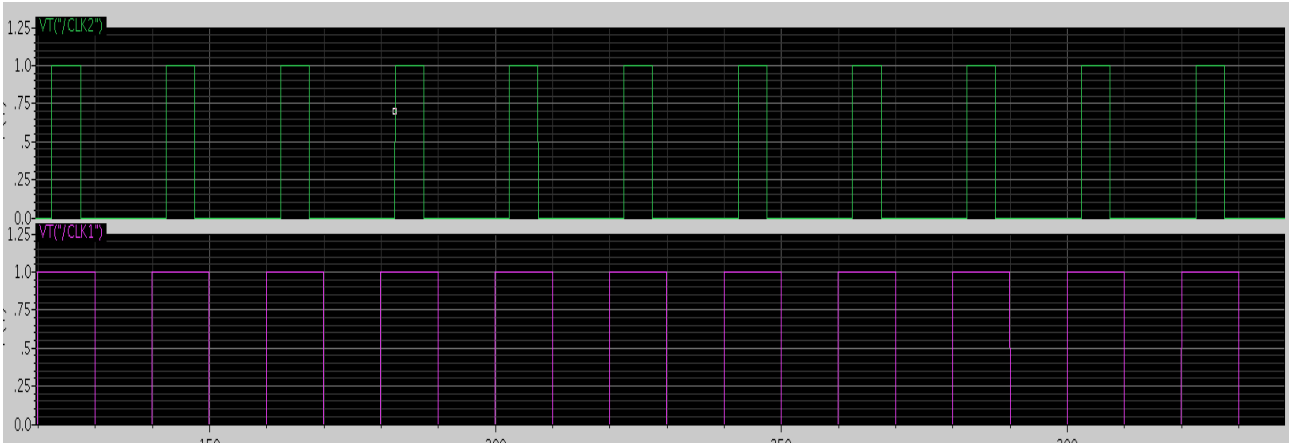
3.DESIGN AND IMPLEMENTATION:

3.1 COMPARATOR:

The function of a comparator is crucial, and often a limiting component in the design of high-speed data conversion systems due to its finite accuracy, comparison speed and power consumption [3]. The comparator part of the system is the analog part of the architecture. A fully differential comparator is employed here in order to have more benefits than the single ended architecture in terms of attaining better power supply rejection and immunity to common mode noise property. The comparator comprises mainly three sections namely

- Differential Input Stage
- CMOS latch (flip-flops)
- SR latch.

The main block diagram of the differential comparator is shown in the figure 3.2. It is composed of two input transistors M_1 and M_2. This input stage has a biasing stage composed of a current mirror M_{13} and M_3. The current mirror is designed to have the current ratio of 1:2 for M_{13} and M_3. The CMOS flip-flop section consists of both a N-channel flip-flop and a P-channel flip-flop. The transistors M_4 and M_5 form a N-channel flip-flop and the transistors M_6 and M_7 form a P-channel flip-flop. The transistor M_{12} is used as a resetting switch and the transistors M_{10} and M_{11} are used as pre-charging transistors, which helps recharging towards the positive supply voltage level. The transistors M_8 and M_9 are used for strobing (clocking), which can separate the N-channel flip-flop and P-channel flip-flop during the resetting phase and also partially during the first regeneration phase.



There are two non-overlapping clocks CLK1 (bottom one in the graph) and CLK2 (top one in the graph) used in the differential comparator. The nature of the clock waveforms is shown in Figure 3.1.

Figure 3.1: Comparator Clock waveforms

3.1.1 CIRCUIT OPERATION:

The operation of the comparator can be clearly divided into three different phases namely

- Resetting Phase
- First Regeneration Phase
- Final Regeneration Phase

During the Resetting phase, the clock CLK1 is high and it connects the N-channel flip-flop in a way that it gets reset (pre-charged) to the ground level. During this interval, the current flows through M_{12} and it leads to the resetting of the previous logic levels that are already present at the nodes M and N (source and drain of M_{12}). The CLK2 that is low at this moment gets connected to the pre-charging transistors and make the nodes P and Q to go to the positive supply voltage level, which is otherwise termed as resetting the P–channel flip-flops. So at this resetting stage, the N-channel flip-flops are in the ground level and the P-channel flip-flops are connected to the positive power supply Vdd level.

The First Regeneration phase occurs right between the time when CLK1 is about to get into the low logic level and the CLK2 getting into the high logic level. This phase is considered as necessary as the final regeneration phase because it

increases the regeneration speed. This stage also helps in reducing the offset voltage.

During the final regeneration phase, the CLK2 becomes high and hence the transistors M_8 and M_9 (strobing transistors) connect both the P-channel flip flop and N-channel flip flop and it regenerates the voltage difference between the nodes M&N and P&Q. The following SR latch stage is driven to full complementary digital output levels at the end of the regenerative mode and remains in the same state in the forthcoming resetting mode for the next level of comparison [3].

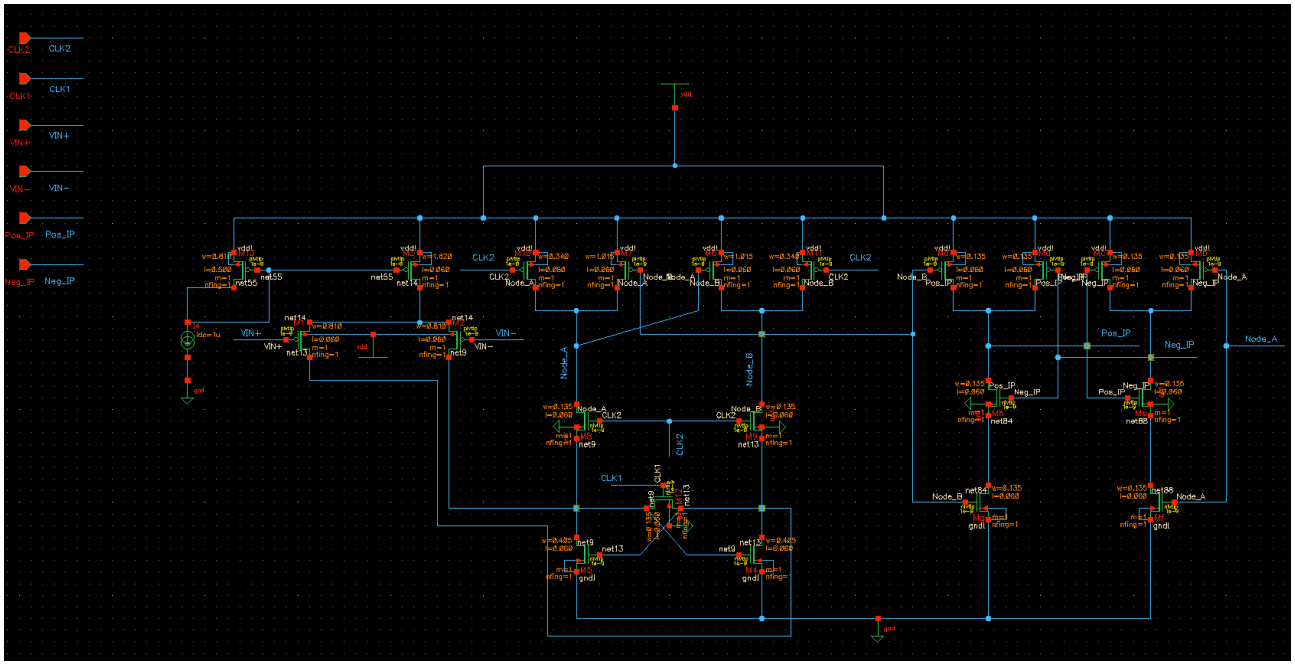


Figure 3.2: Fully Differential comparator

3.1.2 OFFSET VOLTAGE MEASURES:

In this comparator design, the differential comparator was given more importance on the comparison speed and hence any kind of offset cancellation measures were not exploited. The mentioned statement was made provable by careful dimensioning of the transistors in the circuit in such a way that the offset value would be quite negligible.

The total offset voltage of the comparator circuit is given by $V_{off} = V_{off1} + ((g_{m4}/g_{m1})(V_{off2})$. In this expression, the first term represents the offset value of the input transistor pair and the second term represents the offset value of the N-channel flip-flop. The second term is usually the smaller one as the N-channel flip flop are connected to zero voltage substrate bias. The condition of fulfilling a small value of time constant during the first regeneration phase is quite necessary, as it is just not increasing the regeneration speed but it also reduce the total input offset voltage. The condition is given by

$\tau = C_M/(g_{m4}-2g_{012})$, where

τ → Time constant of the first regeneration phase.

g_{m4} → Transconductance of M_4 or M_5

g_{012} → Output conductance of M_{12}.

C_M → Capacitance at the node M or N.

The dimensions followed in the comparator circuit are given below. From the specific conditions, the width of M_4 and M_5 can be chosen roughly as 1 um. M_1 and M_2 are twice the width of M_4. The width of M_{12} is found to be atleast bigger than 0.25 times M_4 and hence it's sized as almost 0.33 times M_4.The width of M_6 and M_7 are found to be 2.5 times M_4. The width of M_{10} and M_{11} would be 2.5 times the size of M_{12}. The size of M_3 would be twice the size of M_1 or M_2 and the size of M_{13} would be half size of M_3 as the current mirror follows a 1:2 ratio configuration.

The value of the time constant obtained is around 1.15 ns as the value of the capacitance at node M depends on the value of the parasitic capacitances of $M_{1,8,4}$ and the value is found to be 57.598 fF. The g_{m4} is found to be 50.08 uS for the biasing current of 3 uA.

3.2 DIFFERENTIAL COMPARATOR II

This comparator circuit can be mentioned as a structure, which is a combination of a latch only comparator; a buffer and a SR latch. There is also an isolation switch, which is connected to each input in order to reduce the kickback noise.

The operation of this circuit can be divided into two phases namely the reset mode and the regenerative mode. During the reset mode, the pre-charging operations carry out in the switches and make them to be at the highest voltage level in case of PMOS and to the lowest voltage level in NMOS. The isolation switches are switched on during the reset mode. During the regenerative phase, the isolation switches get switched off and the comparator does the comparison process during this phase. The SR latch present at the output stores the result during the next reset phase so that it will be possible to send the output of the comparator to the next stage. The circuit diagram of the mentioned comparator is given below. This comparator is chosen to implement in this project for its low power consumption during its operation. The detailed operation of the comparator is given below.

During the reset phase, the latch signal is low. The PMOS transistors M11, M12, M14, M16 gets pre-charged to Vdd and the NMOS transistor M19 gets pre-charged to the ground level. The output nodes get pre-charged to Vdd level during this reset phase. During the regenerative node, the latch signal gets high and the NMOS transistor M19 gets switched on and the current starts flowing through the differential pair. The transistors M13, M15, M17, M18 forms the cross coupled inverters during this phase. If the voltage at NMOS becomes lower than Vthn, then the corresponding NMOS gets turned off and allows Vdd to charge its output capacitance which results in a condition at the output of having Vdd level at one output node and zero voltage at the another output node.

This configuration is termed, as low power configuration as there is power consumption only during the regenerative phase as there is no power consumption during the reset phase and so the only time the comparator consumes power is the time when the Vdd voltage level charges the output capacitance.

3.2.1 ISOLATION SWITCHES:

The cross-coupled inverters present in the comparator introduce large voltage transients during regeneration phase. These voltage transients gets mixed with the input voltage levels in the comparator through the parasitic capacitance of the input pair. If the preceding stage of DAC has non-zero output impedance, then the input levels gets changed with the variations created by the cross-coupled inverters. This leads to an inaccurate operation of the comparator.

In order to avoid this situation, there is an isolation switch connected at the input node of the comparator. The input of the isolation switch is controlled by the inverse of the latch signal. During the regenerative phase, the isolation switch gets turned off so that the variations created by the cross-coupled inverters (i.e) kickback noise don't disturb the input stage.

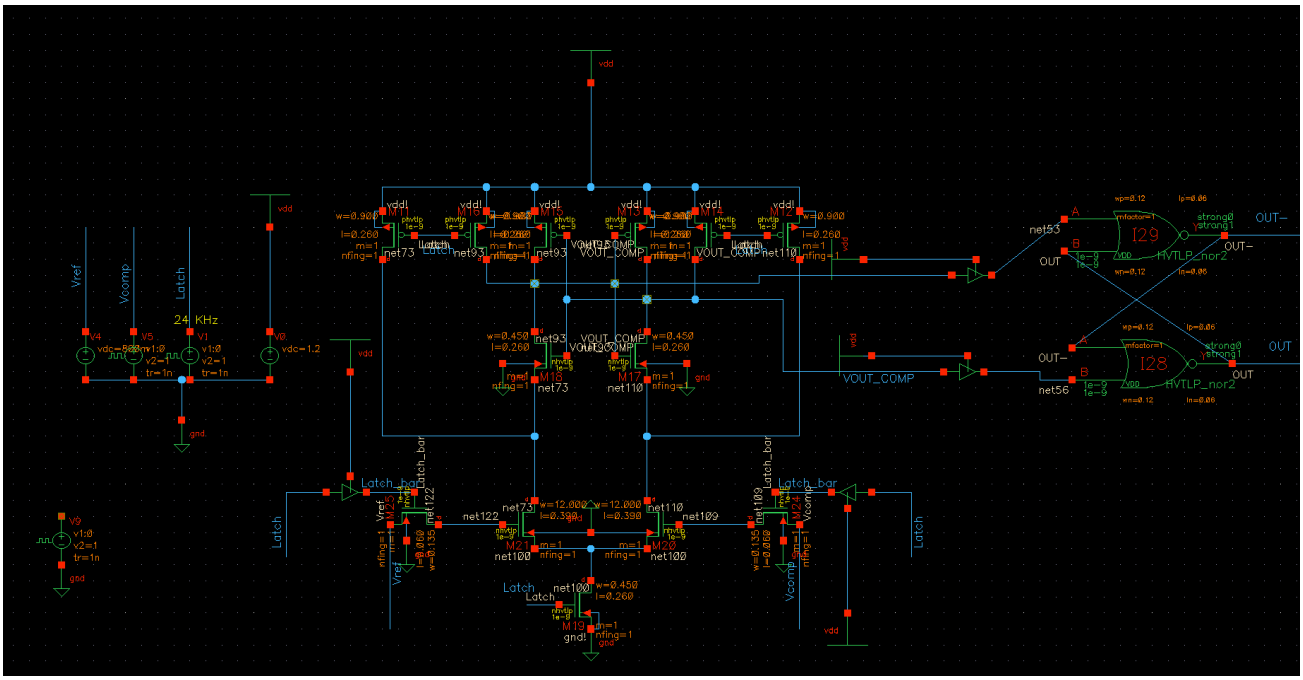


Figure 3.3: DIFFERENTIAL COMPARATOR-II

3.3. DIFFERENTIAL COMPARATOR III:

In this configuration of the dynamic comparator, the choice is made to analyze as it proves to give the lowest offset voltage and high output drive load capability.

This architecture of comparator consists of a regenerative latch, an SR latch and a couple of inverters. The inverters at the output are added to the circuit to maintain the rise time and fall time sharper, which leads to make the comparator being used at higher speeds. [XVIII]

In this configuration, the comparator's input stage and the output latch stage are separated from each other so that it could be able to work at a lower supply voltage and have a stable offset voltage. This configuration has two additional inverters apart from the general conventional architecture in order to strengthen the regenerative nodes so that the comparison speed is relatively much faster than the conventional one.

When the latch signal gets low, the PMOS transistors connected to the input stage gets turned on and it leads to the charging of the drain nodes to the supply voltage level which in turn leads to the activation of the PMOS transistors present at the regenerative latch leading to the operation of pre-charging the transistors to the supply voltage level. But at the same time, the NMOS transistors gets pre-charged to the ground level at the same time.

During the regenerative phase the decision of the comparator's result is made. In this mode, the latch signal gets high and the nodes, which got pre-charged to Vdd level during the reset phase gets discharged at the rate of the input voltages according to its input level. If the input voltage level to the PMOS at the input stage gets reduced below Vdd-Vthp, then the PMOS present between the input stage and the regenerative stage gets switched on and this leads to the turning on of the NMOS transistors at the regenerative latch which helps regenerating the input difference to the full scale voltage level.

The length of all the transistors incorporated in this architecture is maintained at 65 nm and width of the input PMOS pair is maintained at 1.2 um. The NMOS pair of the inverter placed between the input stage and the regenerative stage was maintained at the width of 5 um and PMOS is maintained at the width of 10 um.

The measurements were carried out in the comparator block and it appears to have the lowest offset voltage out of all the other comparator configurations employed in this project. The respective waveforms of the mentioned comparator are given in the next chapter. The propagation delay was found to be around 280 ps for this comparator.

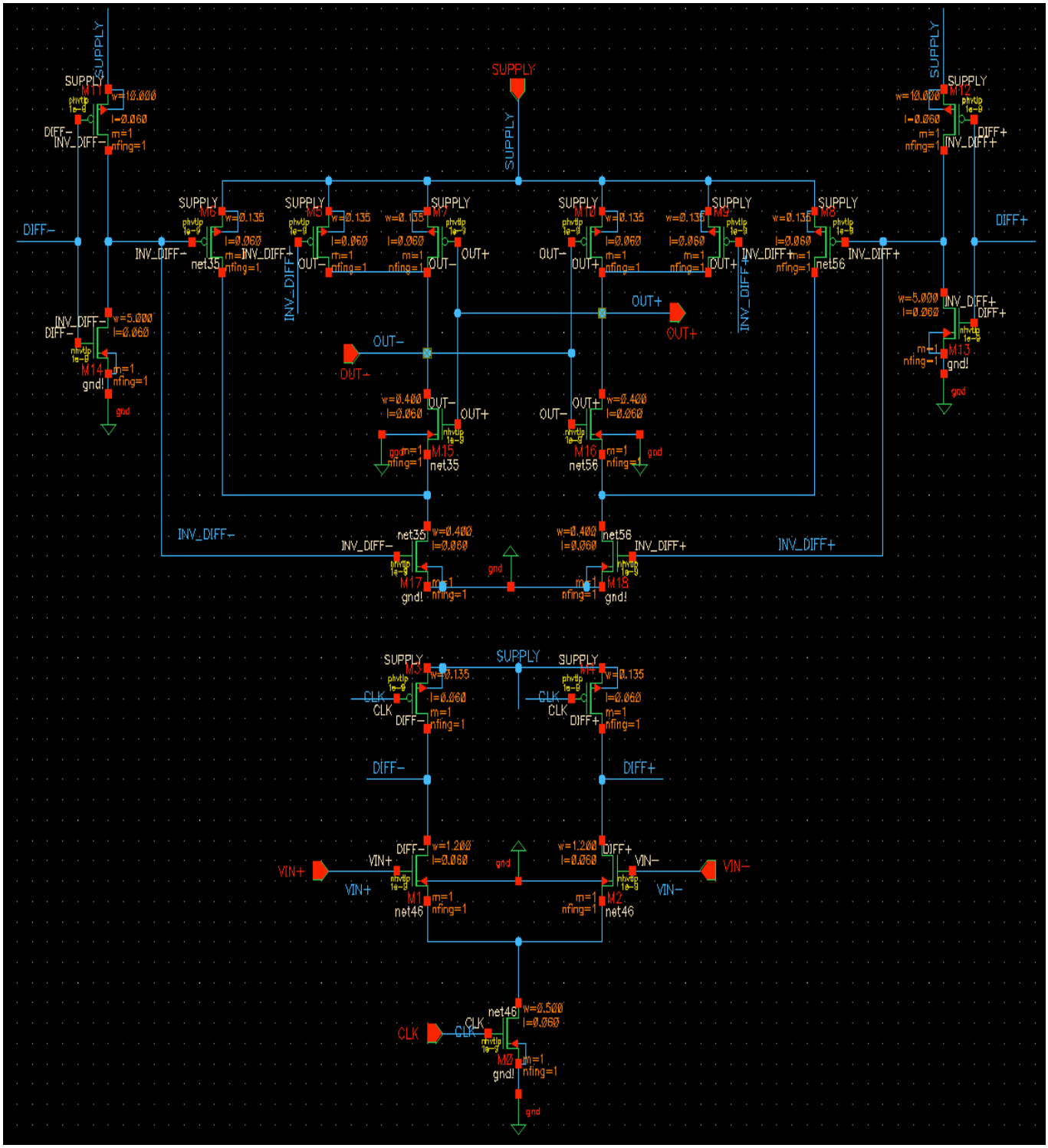


Figure 3.4 DIFFERENTIAL COMPARATOR III

3.4 DESIGN TRADE-OFFS:

The design trade-offs of the comparator usually comes with a couple of compromises. When dimensioning the transistors, it is advisable to use a lesser value for length if the time constants for both the resetting phase and the regenerative phase are expected to be small but the total current consumption and the offset voltage gets decreased by choosing the increased value for the length of the transistors.

3.5 BINARY WEIGHTED SWITCHED CAPACITIVE DAC

In a conventional SAR ADC, the DAC part of the entire system determines the linearity of the entire system and hence it is critical to design it with as minimal non-linearities as possible. The configuration of the DAC used here in this project is binary weighted switched capacitor array type, which is also called as Charge Scaling DAC. It is implemented in fully differential configuration. Since it is composed mostly of capacitors and the energy consumption is directly proportional to the value of the capacitors, most of the power consumed in the entire system is from this part of DAC. High resolution and accuracy can be achieved using capacitor array during data conversion [II].

The basic operation of the DAC can be divided into four basic sections namely

- Resetting state
- Sampling state
- Holding state
- Redistributing state

The resetting state can be roughly explained as the resetting of all the capacitors in the DAC so that there are no pre-stored charges present so that the conversion process would get more linear by avoiding many non-linearities in terms of wrong values in the capacitors. This step is accomplished by connecting all the capacitors to ground.

In the sampling mode, all the top plates of the capacitors gets connected to Vcm level which is Vdd/2 and all the bottom plates of the capacitors are connected to the input voltage level so that the corresponding value of the charge is present in each of the capacitor arms as the capacitors are arranged in the binary weighted fashion and hence the charge is quite distributed all over the arms and the charge expression is $Q= -2CV_{IN}$. In the next stage of holding state, the capacitors' top plates are disconnected from the Vcm connection and all the capacitors' bottom plates are disconnected from the input voltage level and connected to the ground. Since the charge (Q) is conserved in the capacitor, an equivalent negative amount of voltage is still present in the top plate of the capacitor.

In the next re-distribution state, the available charge (Q) mentioned earlier gets redistributed among different capacitors at different stages of the conversion cycle according to the computation of the respective MSBs of the whole digital output. The reference voltage is connected to the MSB stage of the capacitor array (the farthest one from the comparator's input) while all the rest of the capacitors are connected to the ground level. Since the connection of Vref to one capacitor arm and ground connection to all the other capacitor arms and as the capacitors are arranged in a binary weighted fashion, it eventually forms a perfect voltage divider ending up having Vref/2. So the voltage (V_{DAC}) present at the positive input of the comparator would be [Vcm–Vin + (Vref/2)].

Then the input voltage is compared with the resulted voltage of the negative input of the DAC and yields out a high level output if the positive input is greater than the negative input voltage or else it will yield a low level output at the output of the comparator. The operation continues in the same way for all the rest of the capacitor arms till the LSB capacitor arm. It is good to be mentioned here again that DAC part of the system works with the internal clock, which is (Resolution+1) times faster than the sampling clock frequency.

3.4.1 CIRCUIT STRUCTURE:

The circuit of the 10-bit DAC consists of ten branches of capacitors valued based on the binary weight of the position in which the capacitor is placed in the DAC array. There is a dummy capacitor presented in the right most end of the DAC array (nearest to the comparator input), which has the same value of the LSB capacitor in order to maintain the binary weight and prefect voltage division arrangement during the DAC operation.

There are two switches implemented for each capacitor arm one for the Input/reference voltage and the other for the ground level. One more valuable thing to be mentioned here is that the ground level in the differential DAC configuration is the common mode voltage level (Vcm = 0.6 V) and not the zero voltage level. Since the input voltage and the reference voltage are arranged in a way that it comes from the same source, it shares the same switch and gets connected to the system at the respective intervals.

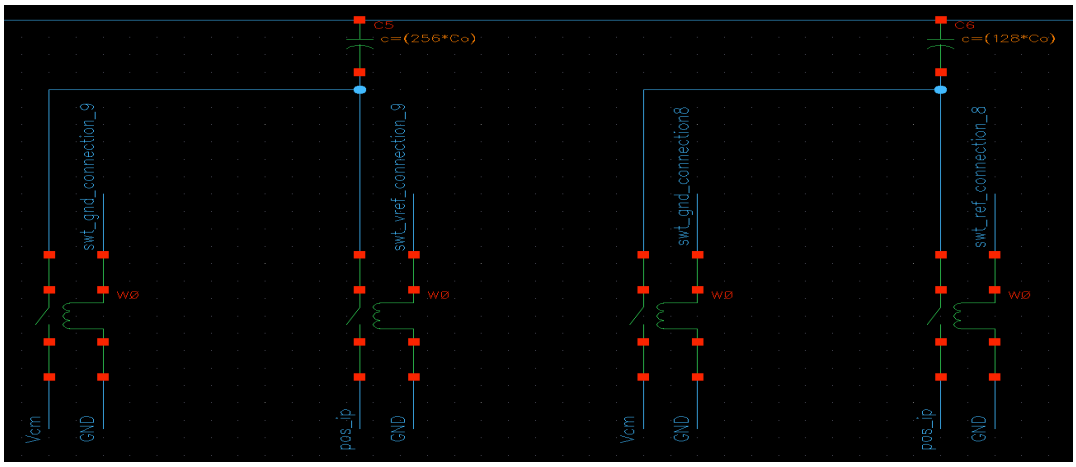


Figure 3.5: A small part of the differential DAC showing the detail of an individual switch structure for a capacitor.

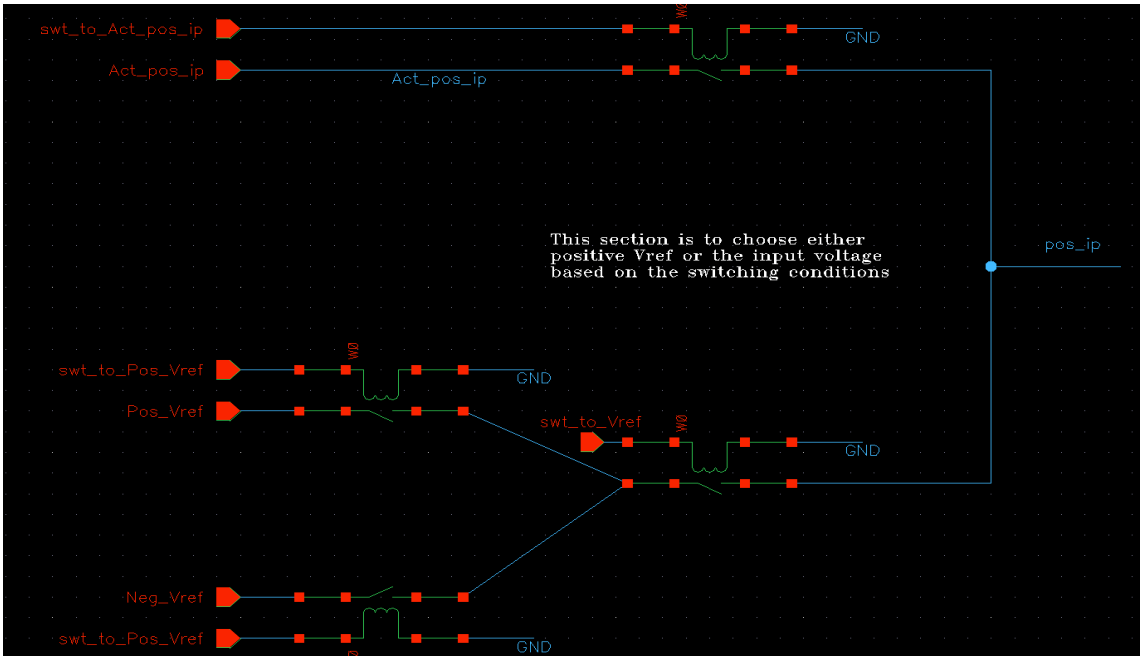


Fig 3.6: The part of the DAC where the input voltage signal and the reference voltage are produced at the right intervals

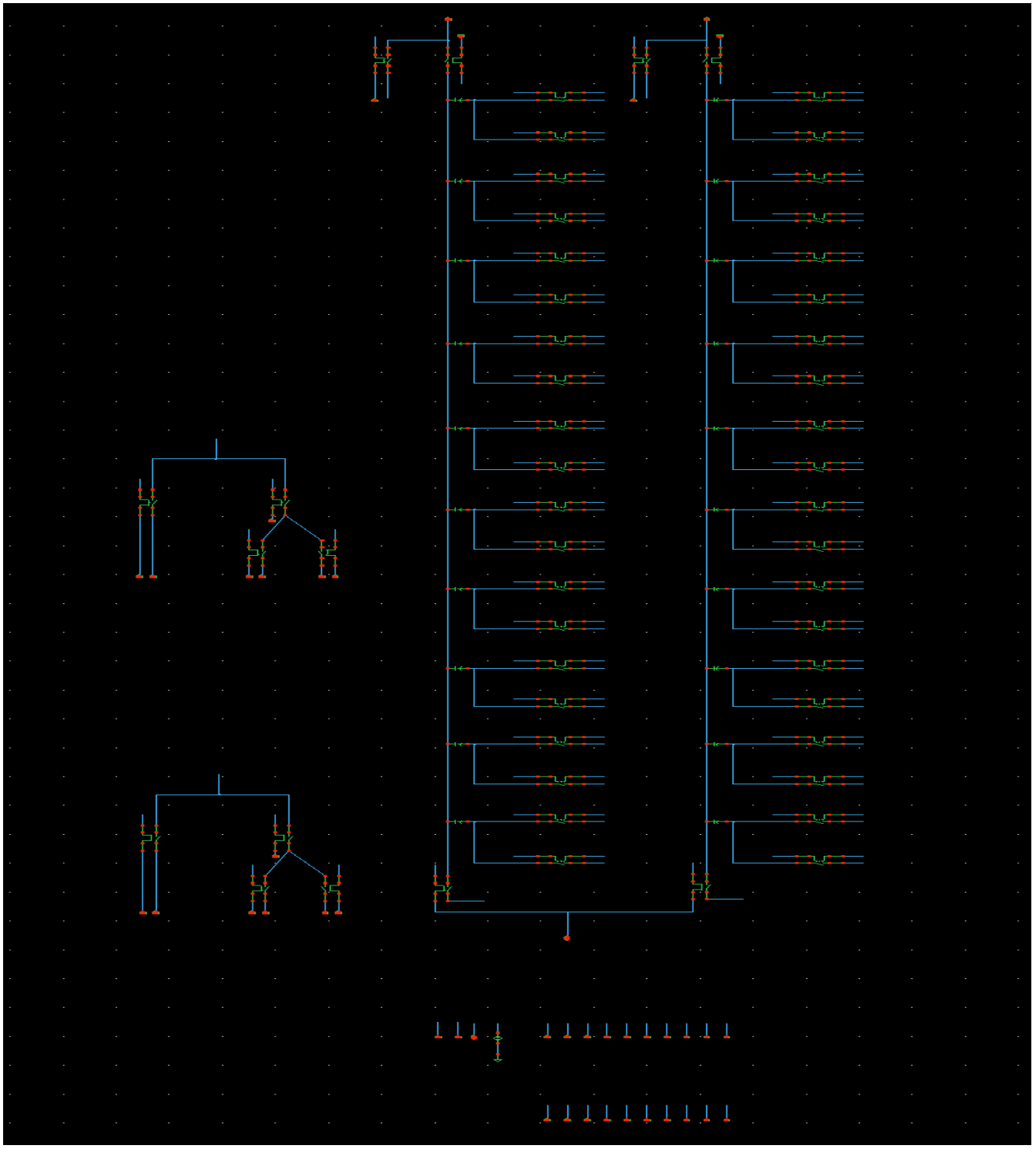


Figure 3.7: Complete structure of the Differential charge scaling DAC

3.5.2 SAMPLE MODE:

In this particular mode of operation, all the ten capacitors in the positive array are connected to the voltage level (in_Vp), which represents the positive input voltage level in this mode and all the ten capacitors in the negative DAC array are connected to the voltage level (in_Vn), which represents the negative input voltage level. In this particular mode, the sampling process is carried out and the value is stored in all the capacitors.

3.5.3 HOLD MODE:

In this mode, the capacitors both in the positive array and negative array are connected to the ground level in the differential configuration. Since the charge is conserved in a capacitor, the top plate of the capacitors would have the value of charge equivalent to Vcm–Vin in all the positive array capacitors and Vcm+Vin in all the negative array capacitors.

3.5.4. RE-DISTRIBUTION MODE:

In this mode, the voltage division operation happens among the capacitor arrays (both positive array and negative array) by connecting the MSB capacitor (512Co) to the reference voltage (in_Vp), which represents the half reference voltage level at this point of the operation. The same manner is followed in the negative array too by connecting the MSB capacitor (512Co) of the negative array to the reference voltage (in_Vn). This operation leads to the situation of having a voltage equivalent of [Vcm-Vin+(Vref/2)] at the comparator's positive inputs and a voltage equivalent of [Vcm+Vin -(Vref/2)] at the negative input port of the comparator.

The same operation is followed for the subsequent stages of the capacitors in the differential DAC array till the LSB capacitor is reached. The comparator gives out a high logic if the positive Vdac is greater than the negative Vdac level or a low level if the positive Vdac is smaller than the negative Vdac level. The high logic of 1.2 and the low level of 0 are maintained in the project.

3.5.5 CHOICE OF SWITCHES AND ITS IMPLEMENTATION:

In general, there are two ways to design a switch, which are either by designing by a single NMOS or a parallel connection of both NMOS and PMOS. The parallel connection of PMOS and NMOS is chosen due to its superior transconductance (g_m) parameter compared to the single NMOS configuration.

The switch that is used in the differential DAC block is a transmission gate switch configuration, which is a parallel combination of NMOS and PMOS with complementary inputs to each other. The total sampling rate of the system would be decided by the time constant of the whole setup of the total capacitor ($512C_o$) and the ON resistance of the sampling switch. Since the sampling rate of this system is decided as 2 KHz, the value (T_{clk} / 2 = 250 us) should be in such a way that it is much greater than the time constant ($R_{on}.C_{total}$) value in order to promise an accurate sampling process.

In order to achieve the required sampling rate, the ON resistance for the switch is analyzed for many different dimensions of NMOS and PMOS. The ON resistance can either be found by directly checking the transistor property or by calculating the parallel combination of (V_{dsPMOS}/I_{dsPMOS}) and (V_{dsNMOS}/I_{dsNMOS}. The value of the ON resistance for NMOS is found to be 386 ohms and 96 ohms for PMOS. It yields the time constant value of 2.365 ns (77* 512* 60fF), which is much lesser than the internal clock period rate of 45.5454 us. Hence an accurate sampling is perfectly possible in this system.

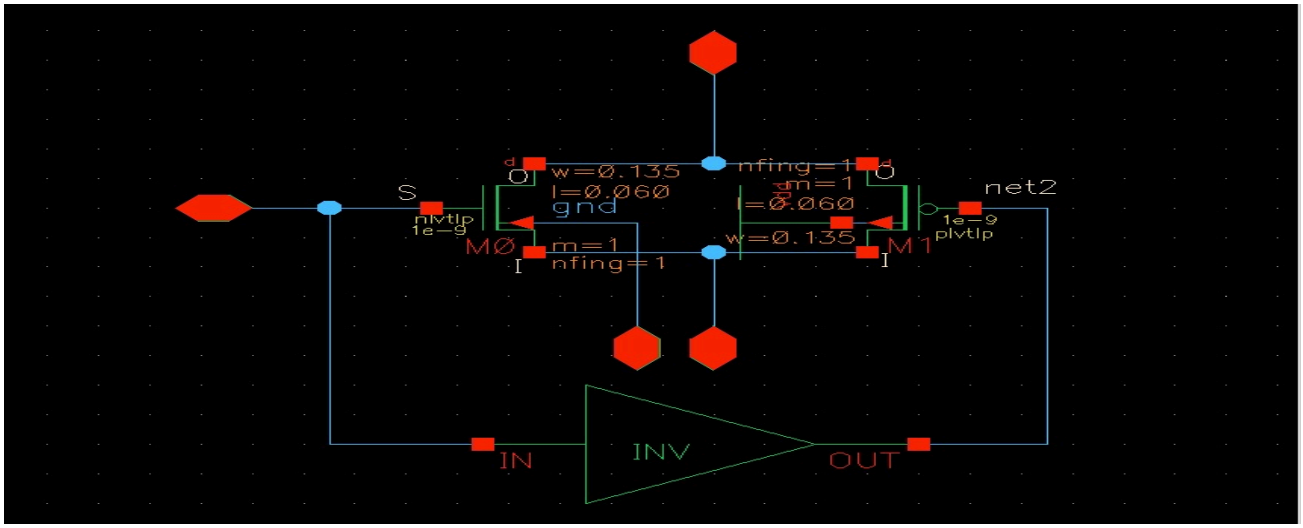


Figure 3.8: Schematic model of a switch

3.5.6 MERITS AND DE-MERITS

In the case of the binary weighted DAC implemented in the SAR architecture, the main benefits would definitely be the simplicity in its architecture and being quite efficient in performance. Since the parasitics associated with the capacitors are almost at the same level during the beginning of the conversion as during the end of the conversion, the non-linearity issues due to capacitors are minimized quite efficiently. Minimal number of switches in a relatively manner, can also be a big advantage of this DAC architecture when compared to the other configurations. The operation of the DAC is comparatively faster than the other configurations.

The demerits of the system could possibly be ending up having a slightly poor DNL (Differential Non-Linearity) and the monotonicity (Same output for the repetition of the same nature of the inputs) property could not be promised.

3.5.7 DESIGN TRADEOFFS:

In order to have less thermal noise (kT/C) noise, the unit capacitor (Co) value could be increased. The same logic goes true also for the less mismatch effect but the inverse logic goes true for Bandwidth as the bandwidth get increased by decreasing the size of the unit capacitor.

3.6 SAR LOGIC BLOCK

This block of the architecture could be better described as the BRAIN of the system as it is the most critical one in making the entire system to work in a proper way with regards to timing specifications. This block works in such a way that it stores the output digital value of the analog input equivalent value and also sends the switching signals to the DAC at the correct intervals in order to get the conversion done at the right time for the right level of values.

The whole block of the SAR logic is realized in VHDL and also in Verilog-A. The whole description of the block is explained here in terms of VHDL, as the processing approach is almost similar in both VHDL and in Verilog-A.

The entity of the SAR logic is composed of thirteen (*eleven in Verilog-A as clk_inverse port is not used there*) different ports. There are three different types of clocks used namely clk, clk_delayed and clk_inverse. The clk is the main internal clock used in the system and its rising edge can be used as a detector for every step of the conversion of each bit. The comparator's actual response would be available almost during the end of the falling edge of the clk and so it is logical to use the falling edge of the clk named clk_delayed as the detector for finding the correct proper response.

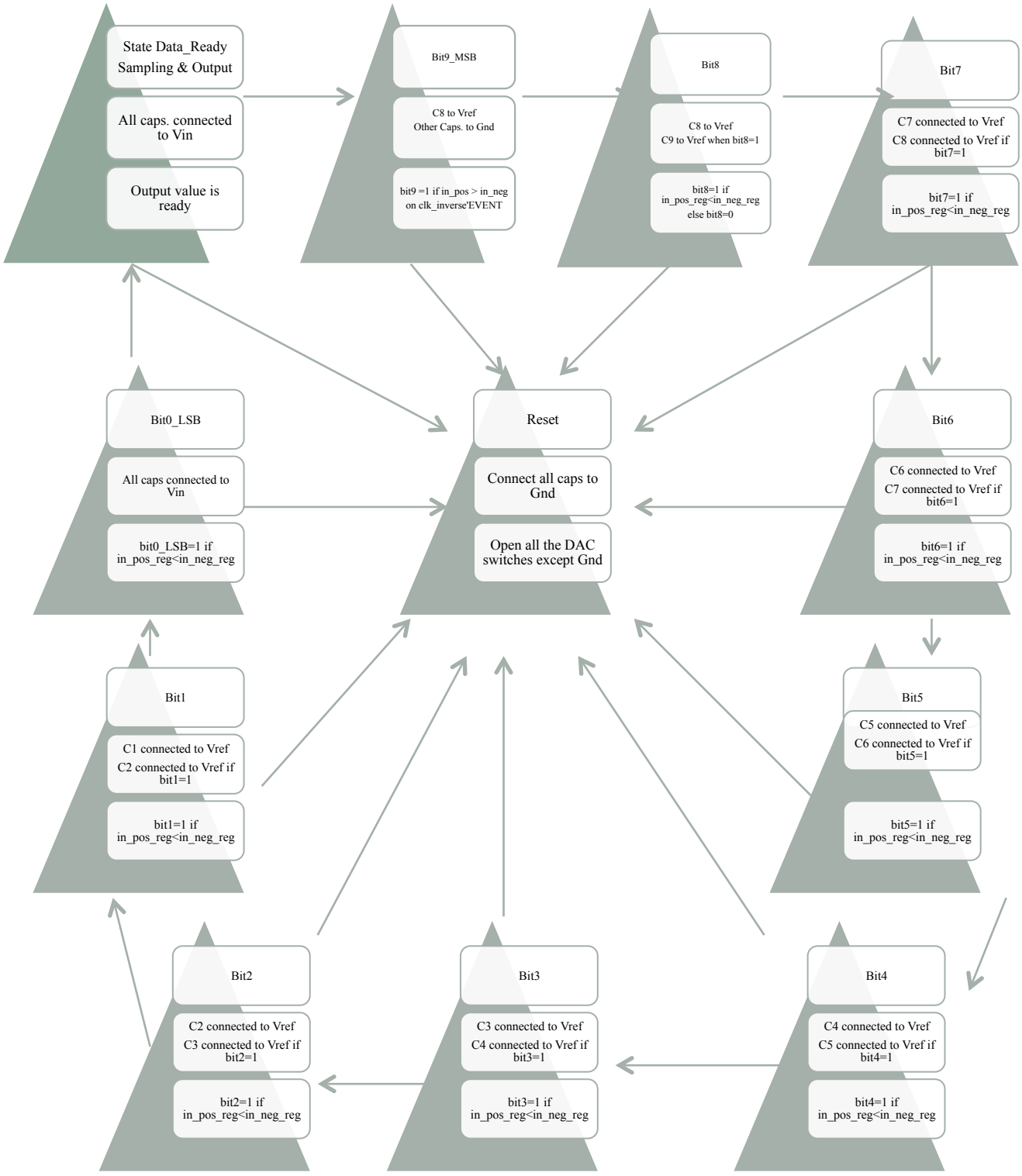
The port clk_delayed is used in the system in order to make sure the switches which are supposed to get switched off, gets switched off completely before the switches which are supposed to get switched on. This is done so that the linearity or any other performance parameters of the DAC gets maintained in the proper limits. The ports pos_ip and neg_ip are the differential outputs of the comparator, which are actually the inputs of the SAR logic block.

The reset is the reset signal, which is used to reset the entire operation when necessary. It is an active low signal. The conv_start_flag is an input port as well, which is again an active low signal. This indicates the onset of the conversion process. This signal is kept high during the sample mode during which the output bits are read from the registers of the SAR block. This signal is then made low to start with the next conversion.

The output ports namely swt_pp, swt_pn, swt_to_sampling_flag, swt_to_reference_flag are the switching signals which are used as flag signals in order to make the corresponding capacitors in the differential capacitive DAC array to get connected with the corresponding signals at the respective intervals. These signals are quite critical in terms of timings as it decides completely the promising performance of the DAC.

The output ports namely swt_gnd_connection and swt_vref_connection are the signals, which connect the capacitors to either to ground level (common mode level) or to the reference voltage level according to the other output flag signals which were mentioned in the previous paragraph. The output port named output_from_SAR yields out the actual digital equivalent output of the analog input level.

3.6.1 STATE DIAGRAM



3.6.2 PROCESS 1:

This process describes the condition to be maintained for the entire operation to have the right moment to do the sampling process as otherwise the system tends to convert some random value into its digital equivalent, which is quite irrelevant to the system. This is done through this process by introducing a temporary signal called *temp*, which is explained as follows:

temp <= clk and (not clk_delayed);

This temp signal is the result of the reason explained earlier that is related to the reason of the existence of the port clk_delayed. So the sampling is done only when the temp signal is not at logic 1 or else the respective ports are connected to the ground level.

3.6.3 PROCESS 2:

The second process is considered to be the critical block of setting the switching processes for the capacitors in the right intervals so that the actual operation is done in the DAC portion of the system. Since this process is responsible for the proper working of the DAC, the control signals are managed through case statements so that it is quite easy and logical to explain as how each stages of the DAC should be, during the operation. This block can also be called as the timing controller of the DAC block.

3.6.4 PROCESS 3

This process is basically plotted to set the correct bits in each of the flip-flops of the shift registers allocated to store the output bits. This is also formed by the same case statements used in the process 2. The bits of the shift register are set by the comparison of the comparator outputs. The conditions to check between the comparator outputs are clearly elaborated in the process.

3.6.5 VERILOG-A VERSION OF SAR LOGIC BLOCK:

The SAR block was modelled using Verilog-A language in this project, which almost follows the same procedure followed in the VHDL version of the same block. And hence the explanation is not given in this part of the report. There are quite a few differences in the implementation though in the verilogA mode. The variable temp is not used there and hence there is no clk_delayed clock port. There is also a separate switch given to the input connection to the capacitor arm and not like the sharing process, which was followed in VHDL version.

CHAPTER IV

4.1 SINGLE ENDED ARCHITECTURE:

An equivalent single ended architecture is also built for the 10 bits SAR ADC presented in this paper. The single ended architecture mostly shares the same blocks realized for the differential configuration but with some changes. This system also comprises three major blocks namely Comparator, Digital to Analog Converter (DAC) block and SAR Logic block. Each of the blocks is mentioned below with its implementation details.

4.2 COMPARATOR:

Out of the three different configurations of comparators designed for the differential configuration, the second one was chosen for the single ended architecture. The positive input of the comparator is the reference voltage and the negative input of the comparator is given from the DAC block. If the signal from the DAC block is bigger than the other input, then the comparator outputs a logic 1 and logic 0 if the other way is true. The level of comparison gets changed according to the bit level in the conversion cycle. For example, during the first clock cycle of the conversion cycle, the reference voltage is compared with the input voltage from the DAC, which is Vref-Vin+ (0.5Vref). If the DAC voltage is bigger, then the comparator gives out a logic 1 or logic 0 otherwise.

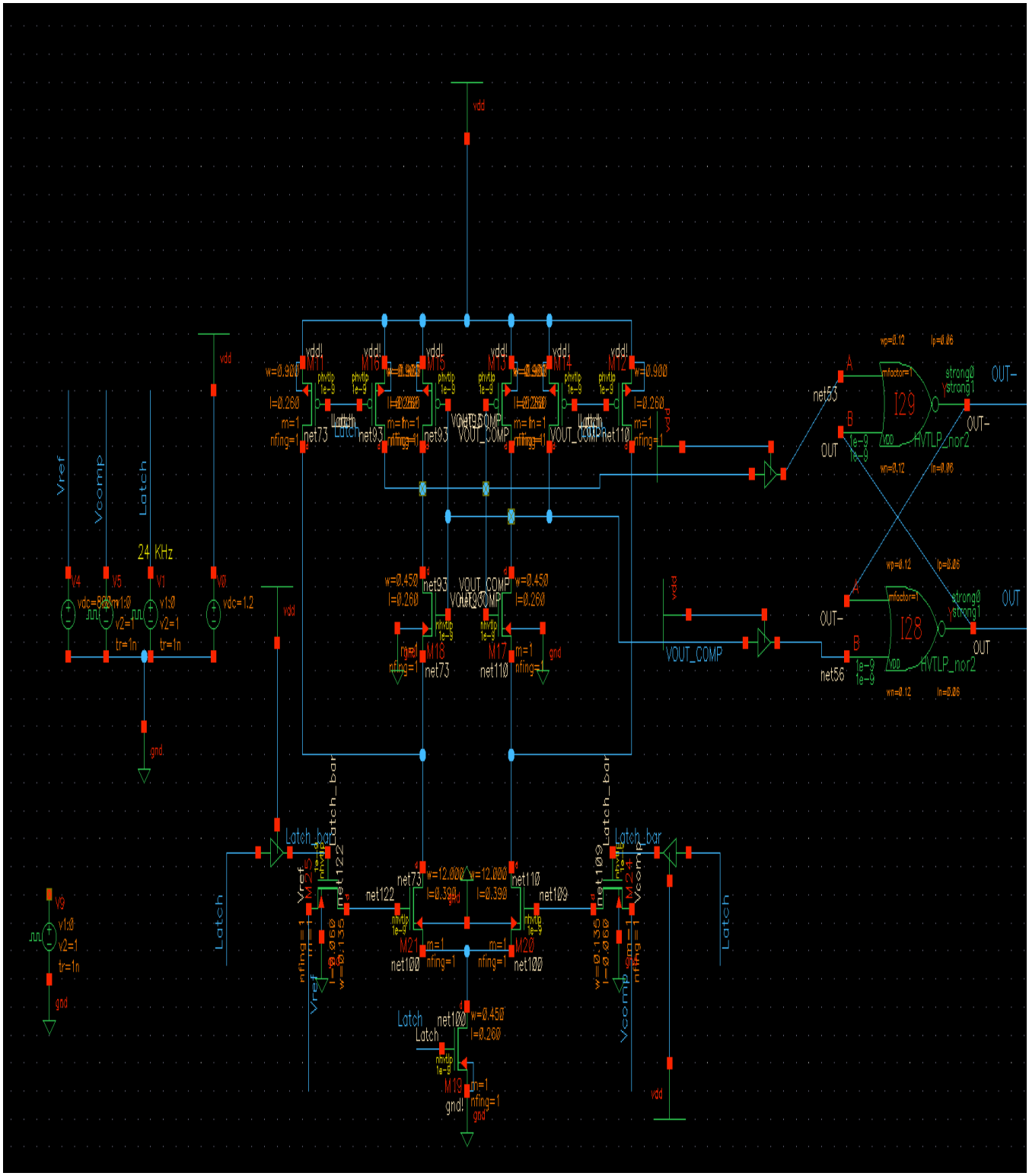


Figure 4.1 Comparator with buffer and a SR Latch

4.2 SAR LOGIC STRUCTURE:

The SAR logic structure for the single ended architecture is realized in VerilogA language. The code is attached in the appendix section of the project report. There are four 10 bits output ports used in the program one for the ground connection, one for the Vref connection, one for the Vin connection and one for the Output bits from the system.

The SAR logic gives out the control signals for the DAC block for each conversion cycle. The actual operation of the program was already explained in a detailed manner in the previous chapter. The modification done to the program was that there was a separate port introduced for the Vin output port to connect to the DAC system. In the differential version, the port for the signals input voltage and reference voltage was shared together with one switch.

4.3 DAC STRUCTURE:

The DAC structure consists of 10 capacitor arms and also one dummy capacitor arm, which accounts for the total capacitance to be the power of 2. Each switch structure comprises of three switches inside and in which one accounts for the connecting the input voltage, one for the reference voltage and one for the ground connection. The CMOS transmission gate model is used as a switch in the DAC system. The switch ON resistance is found to be 77 ohms. The schematic of this structure is presented below.

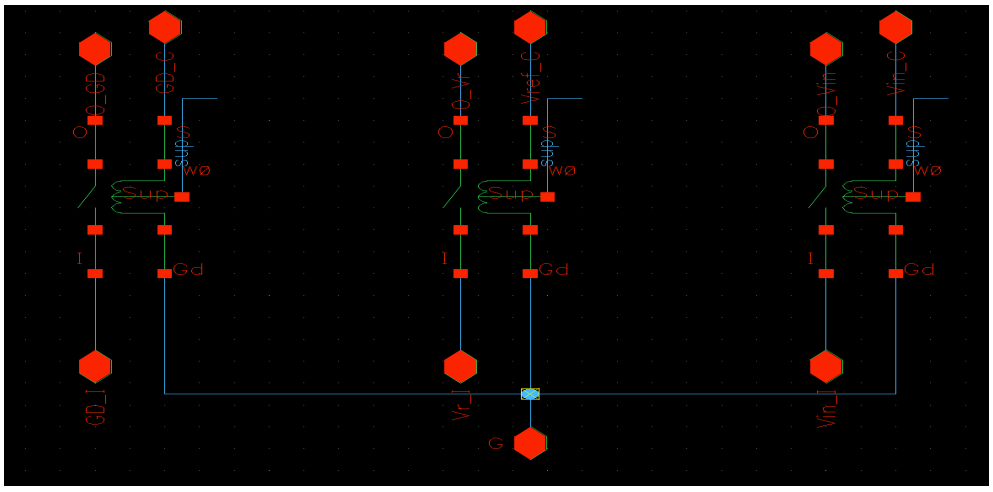


Figure 4.2 Switch Structure of the DAC block

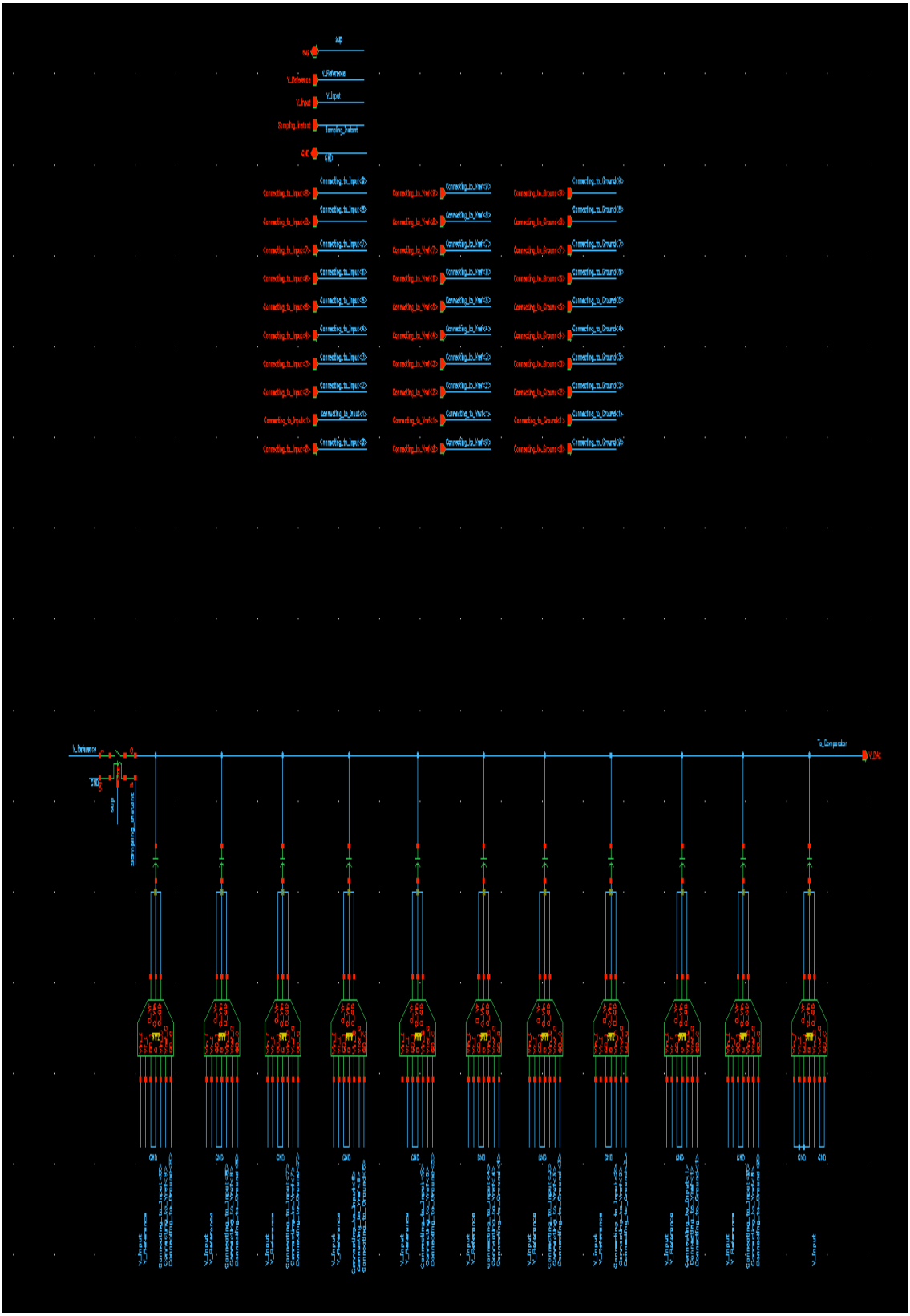


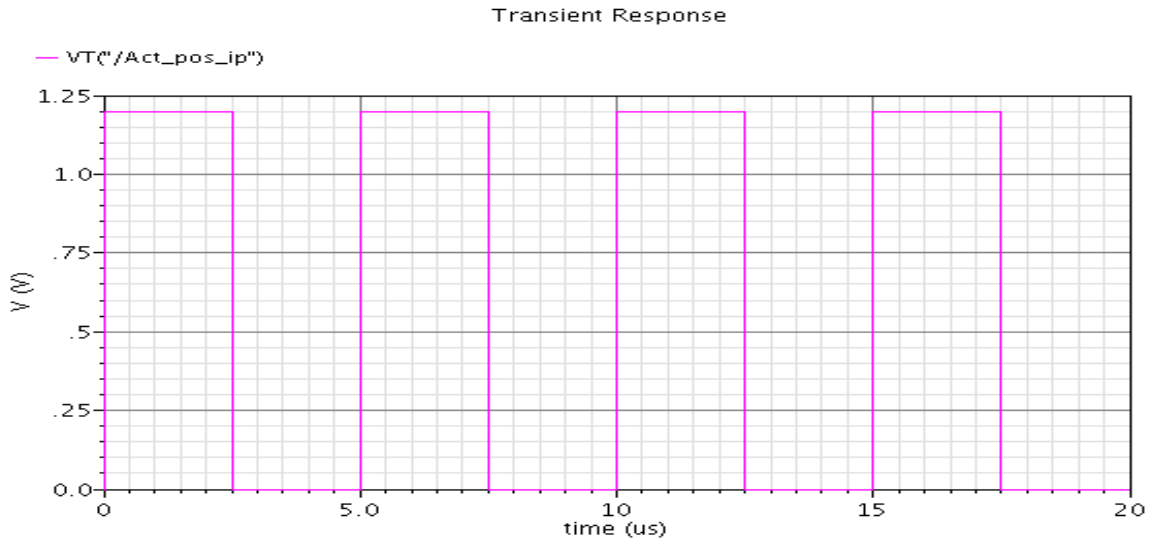
Figure 4.3 Entire DAC structure of the system

CHAPTER V

5.SIMULATION RESULTS AND MEASUREMENTS

5.1 COMPARATOR

The Differential Comparator was simulated with the circuit mentioned in the previous chapter. The comparator as explained earlier, has three blocks namely the differential input stage, two regenerative CMOS flip-flops and a SR latch. The transistors' aspect ratios are designed in a way such that the mobility property of PMOS was taken into consideration and the designing of the bias current was done based on the nature of the outputs for the small level voltages. The simulations were carried out for both the highest level of input voltage 1.2 volts and also for the lowest possible voltage level, which might be encountered in the architecture. The lowest voltage can be found by computing the ratio of the dynamic range and the resolution ($2.4/2^{10}$), which is around 2.343 mV. The waveforms are given below.



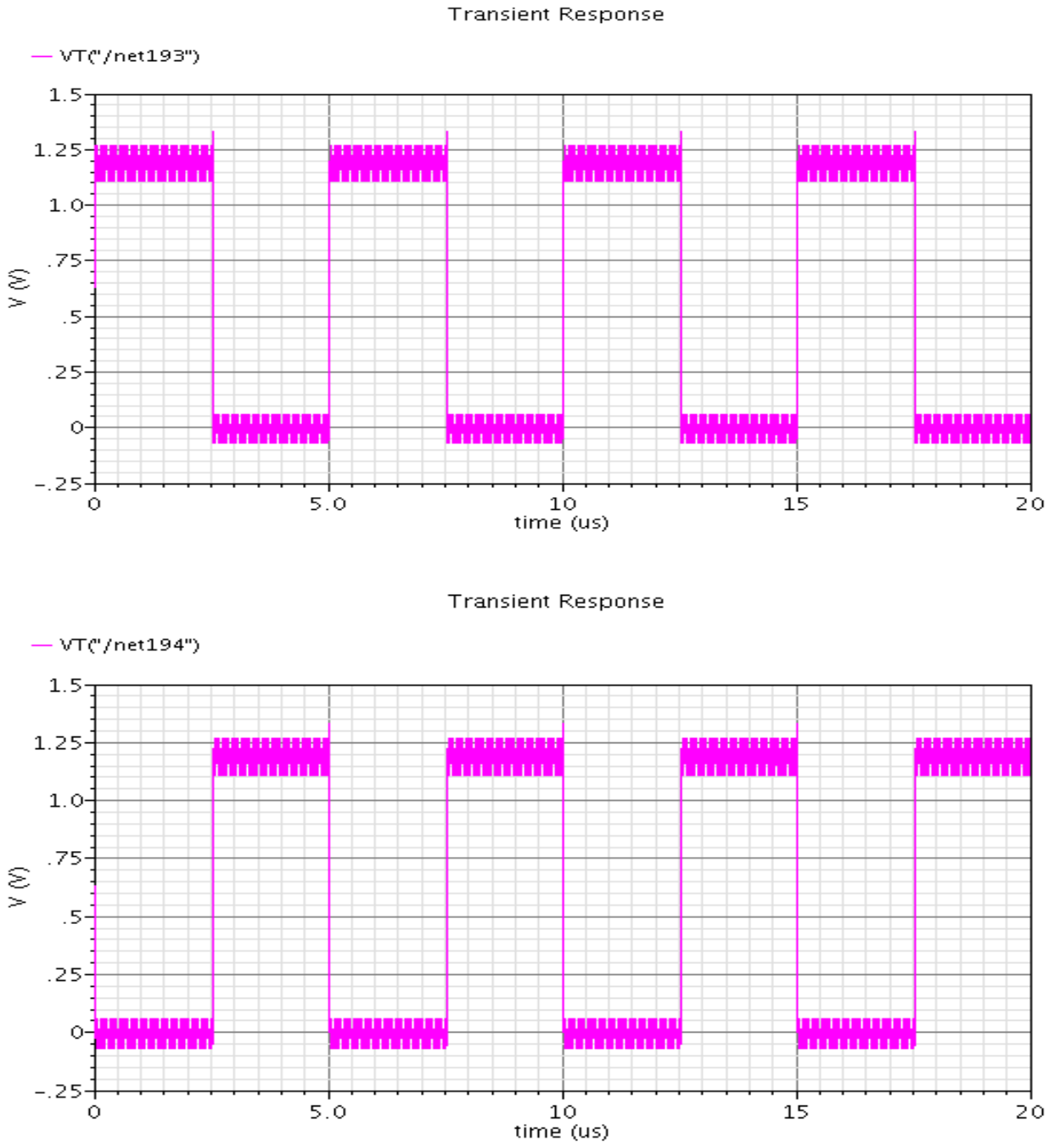


Figure 5.1: Input and Output waveforms for 1.2 V differential input levels.

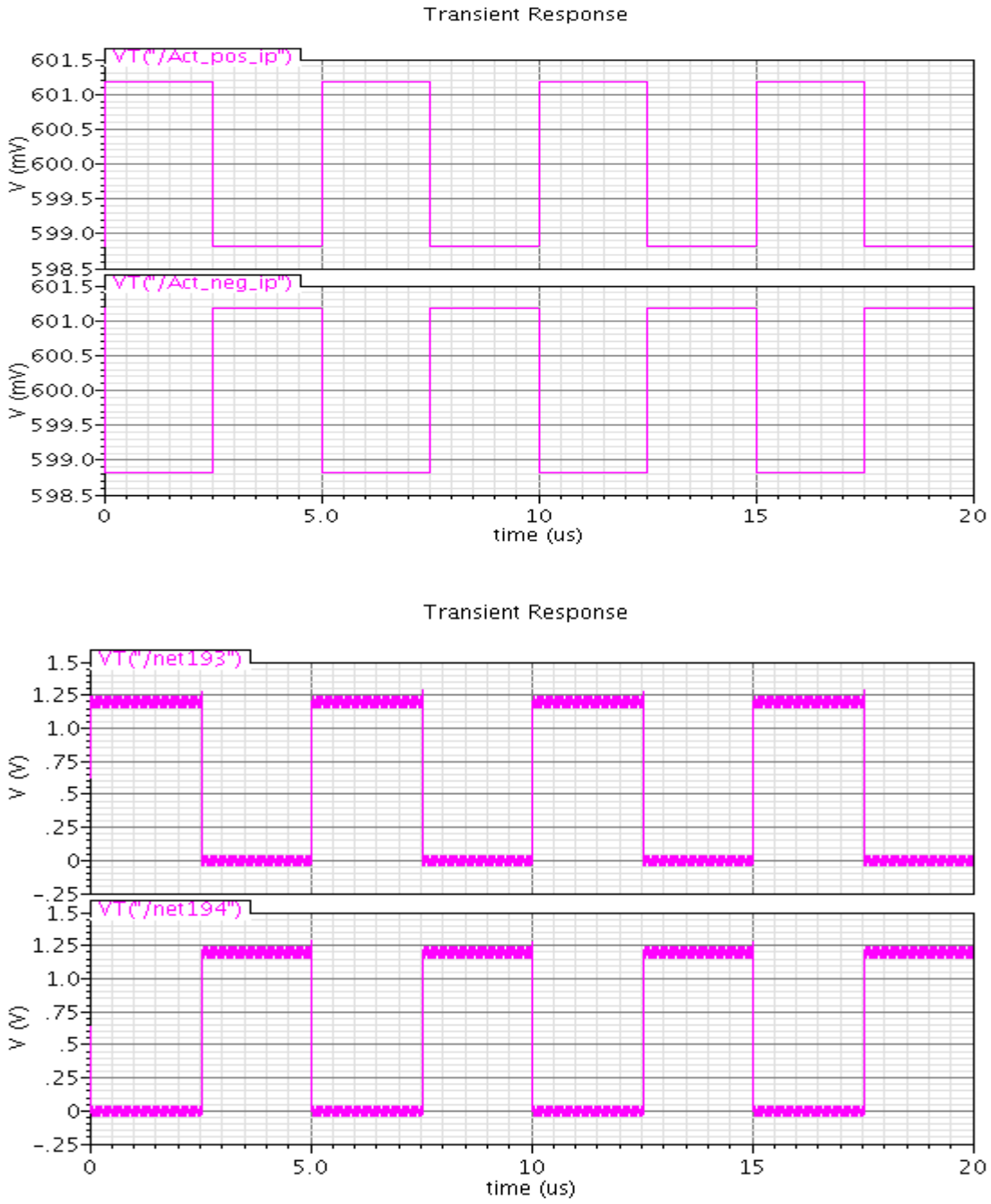


Figure 5.2: Input and Output waveforms for 2.3 mV differential input level

5.2 SAR LOGIC BLOCK SIMULATIONS:

The SAR logic block's simulation measurements were carried out with suitable input and different part of the SAR block's graphs will be presented below.

5.2.1 CURRENT STATE AND NEXT STATE:

These two variables are taken out as output ports temporarily from the main program to check with the proper execution of suitable voltage levels given to each case statements by connection of either the input voltage or the reference voltage at suitable intervals. There are totally 12 states including the state for collecting the output named MSB_samp_int, which does both collecting the output and also the sampling process. The state named reset_state_int performs the reset operation once the data is sent out after one cycle. The voltage level for all the states start from 1 V representing MSB_samp_int and goes till 11 V representing reset_state_int.

Both the current_state and next_state simulation graphs are presented below for reference. It shows the excursion of the process in every conversion cycle from the sampling process to LSB level.

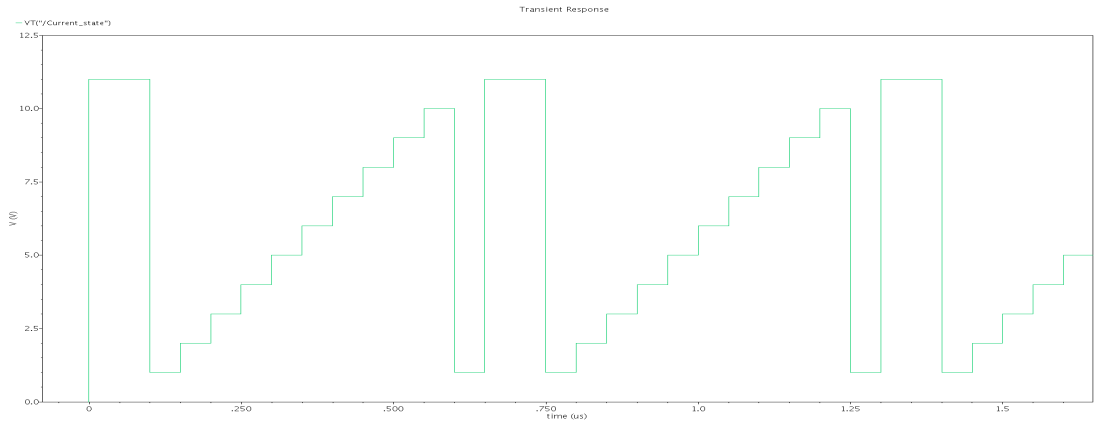


Figure 5.3: Current_State graph for one cycle of signal frequency

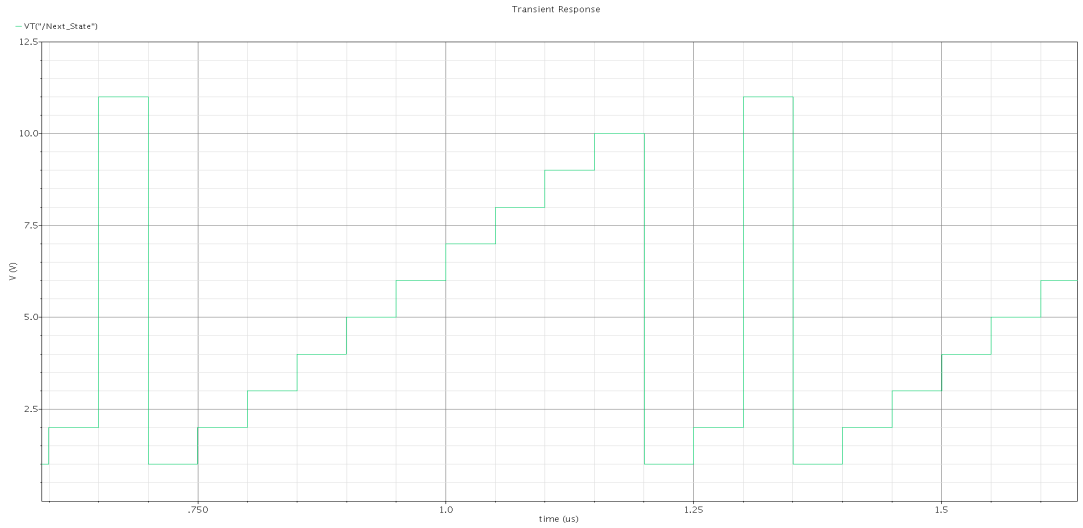


Figure 5.4: Next_State graph for one cycle of signal frequency

5.2.2 GROUND CONNECTIONS AND REF. VOLTAGE CONNECTIONS:

There are two other important variables used in the SAR block, which explains the flow of the process inside the SAR block. These variables are the timing control signals for the DAC block, which makes the DAC to get connected to the proper voltage levels by connecting the respective capacitor arm at proper intervals. In the below diagram, it is shown that all the capacitors' bottom plates are connected to ground level during the sampling phase and then getting disconnected from each capacitor arm one after one as the conversion cycle proceeds.

In the same way, the graph for reference voltage connections are all connected to the bottom plates during the sampling phase as they supply the input voltage during this interval and later it all gets connected to ground level during the Hold phase and then gradually starts to get connected to each capacitor arm starting from MSB, as the conversion cycle proceeds.

5.2.3 OTHER IMPORTANT PORTS' GRAPHS:

There are also other graphs presented below, which shows some of the important variable's excursions during the conversion cycle. The function of each variable was already explained in a detailed manner in the previous chapter and hence the reference can be made suitably.

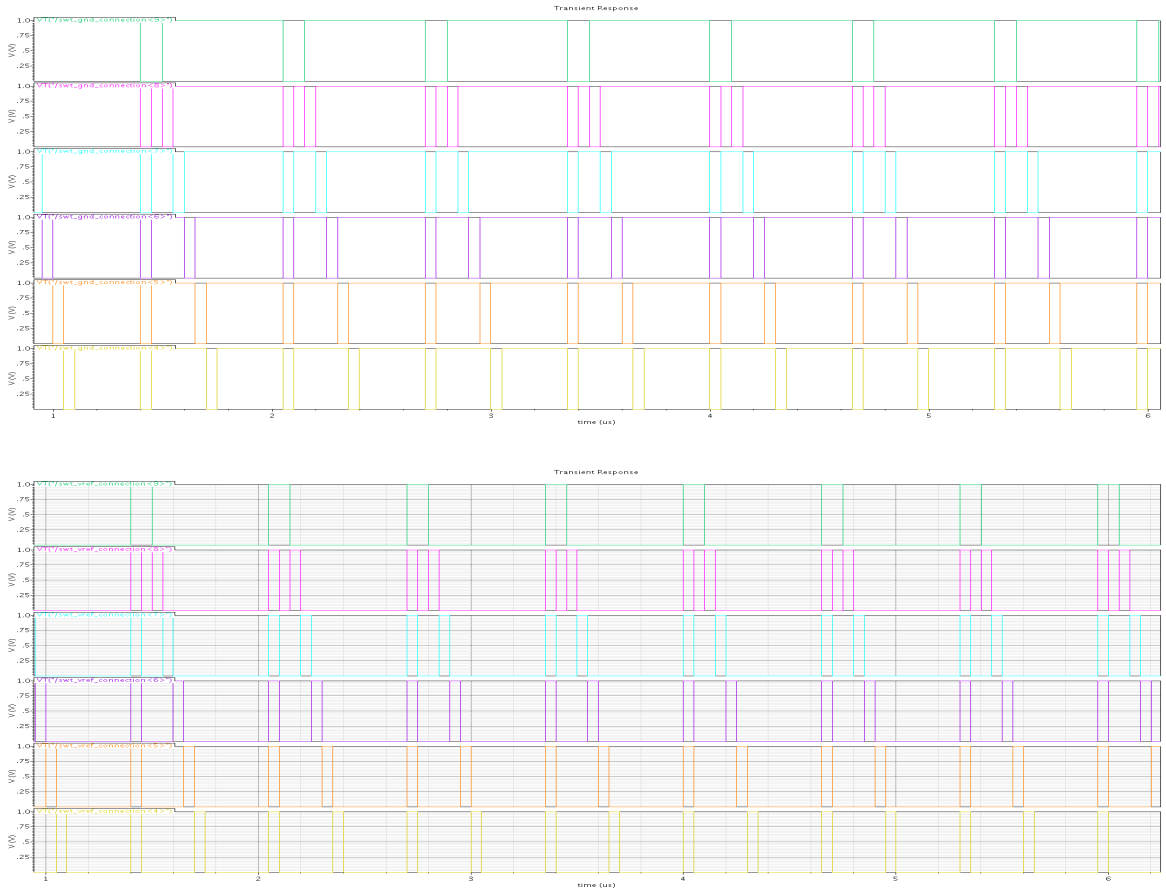


Figure 5.5 SwtgndConnection and SwtVrefConnection (bit9-bit5)

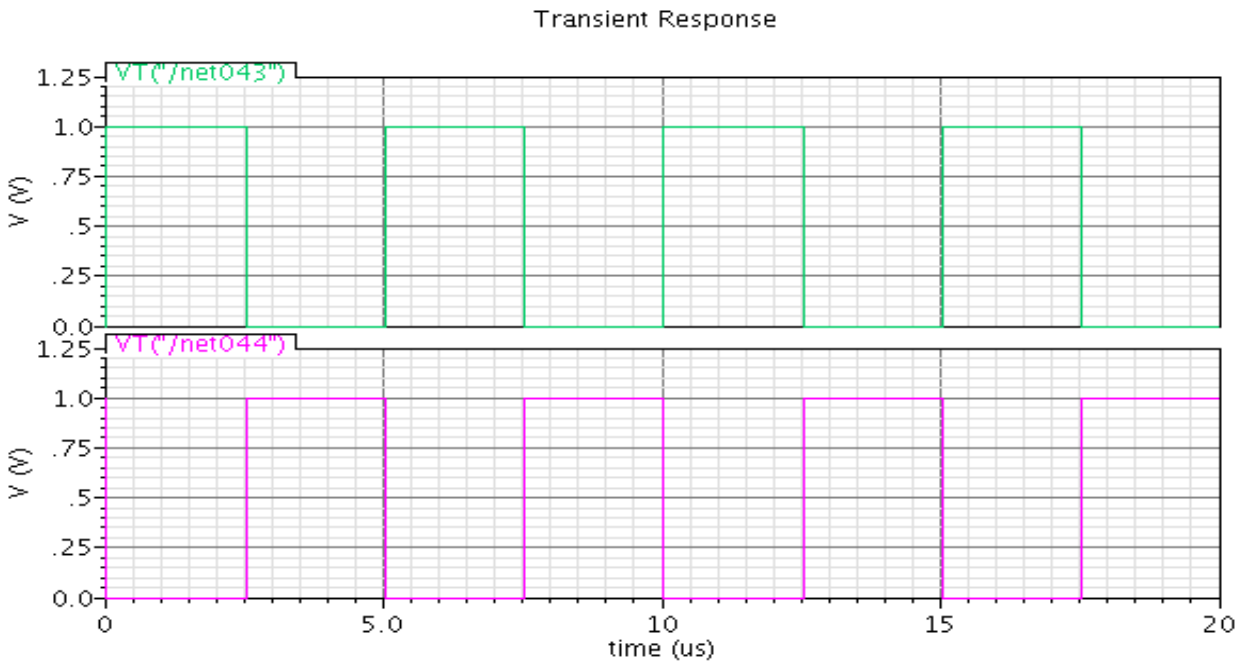


Figure 5.6 In_pos_reg (top) and In_neg_reg (bottom)

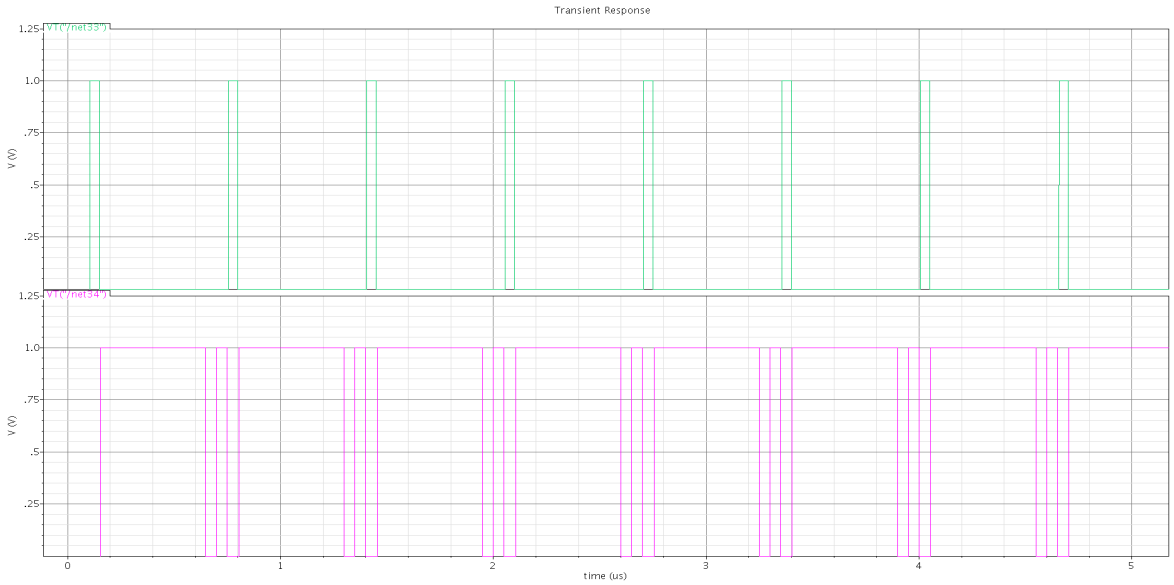


Figure 5.7 Swt_sampling_flag (top) and Swt_reference_flag (bottom)

5.2.4. VHDL SIMULATION TIMING CHART FOR HALF LEVEL:

The below simulation graph explains the waveform for all the variables used in the SAR logic block. The output shown is the result of the attainment of the half level value of the full-scale value which is 1000000000.

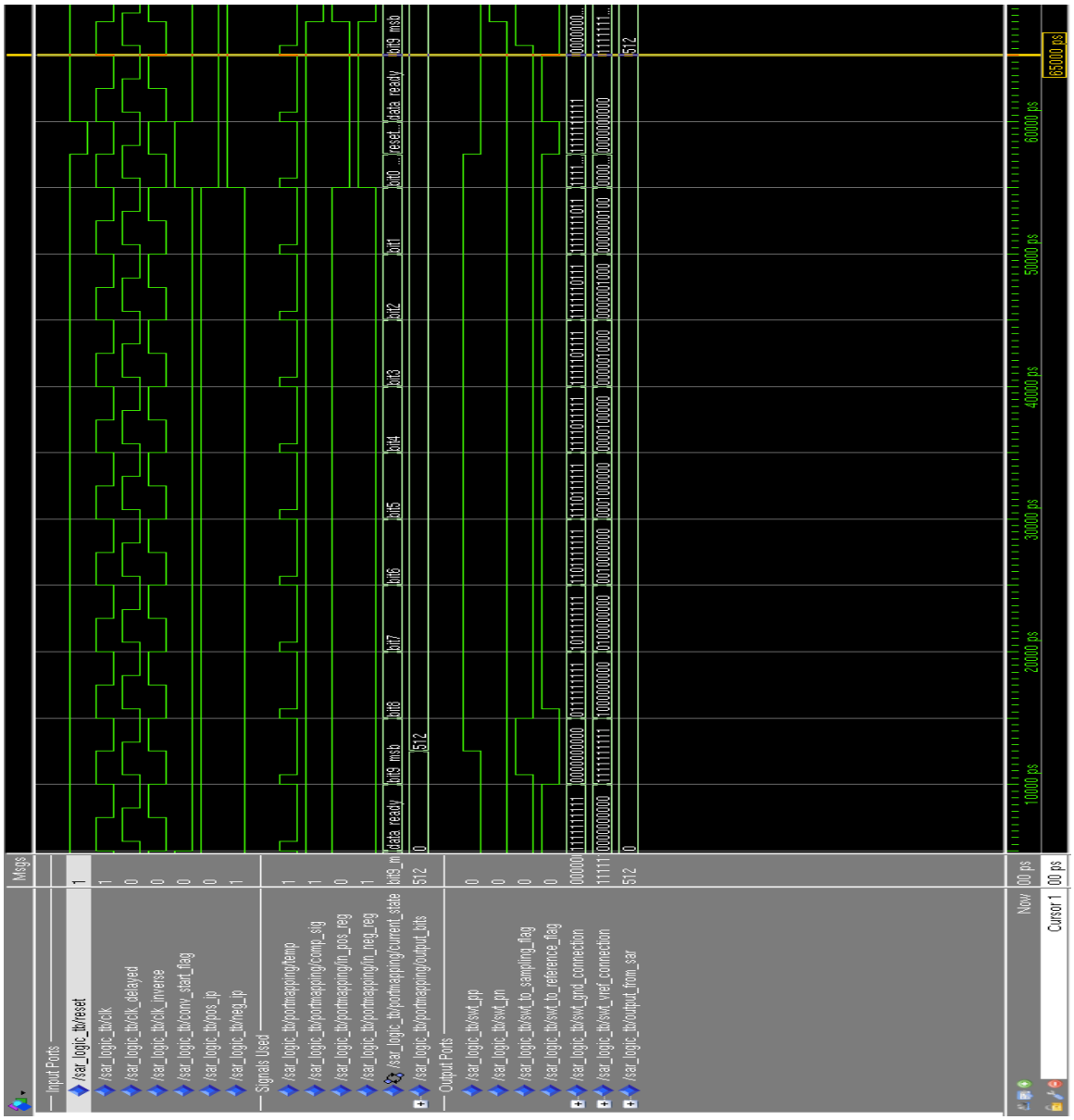


Fig 5.8: SAR Logic waveforms at half full-scale level (1000000000)

5.3 DAC SIMULATION MEASUREMENTS:

The DAC's operation is analyzed by applying a dc input to the whole system and checked its operation according to it during one conversion cycle, which comprises 11 clock cycles. The excursion of the signal starts from the attainment of the Vref/2, which is 500 mV here. Then the levels are approximated by each decision of the output bits in the SAR logic block. At the end of the conversion cycle, the result waveform attains the input level given, which is 1 V after 11 clock cycles. The respective waveform is shown in figure 5.9.

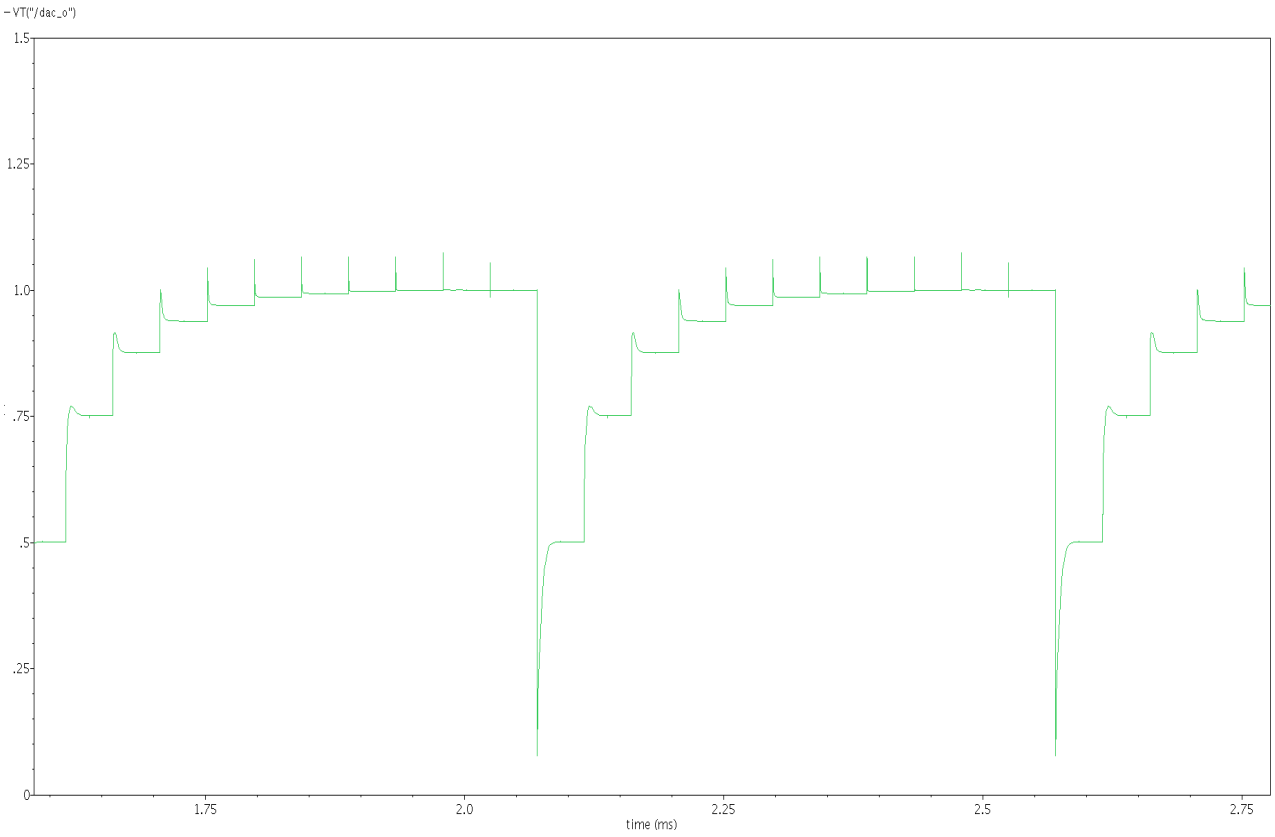


Figure. 5.9 : DAC output for a DC signal value of 1 V

The DAC block was also tested for an ac input level of 500 Hz, 100 mV at the input. The following figure 5.11 shows the output of the DAC for all the three-implemented comparators. The middle waveform belongs to the comparator finalized for the project. The waveform explains the output waveform of 500 mV centered at 500mV. The second (middle) waveform clearly shows the conversion of the input waveform by confirming the time cycle of the waveform, which is 10 milliseconds.

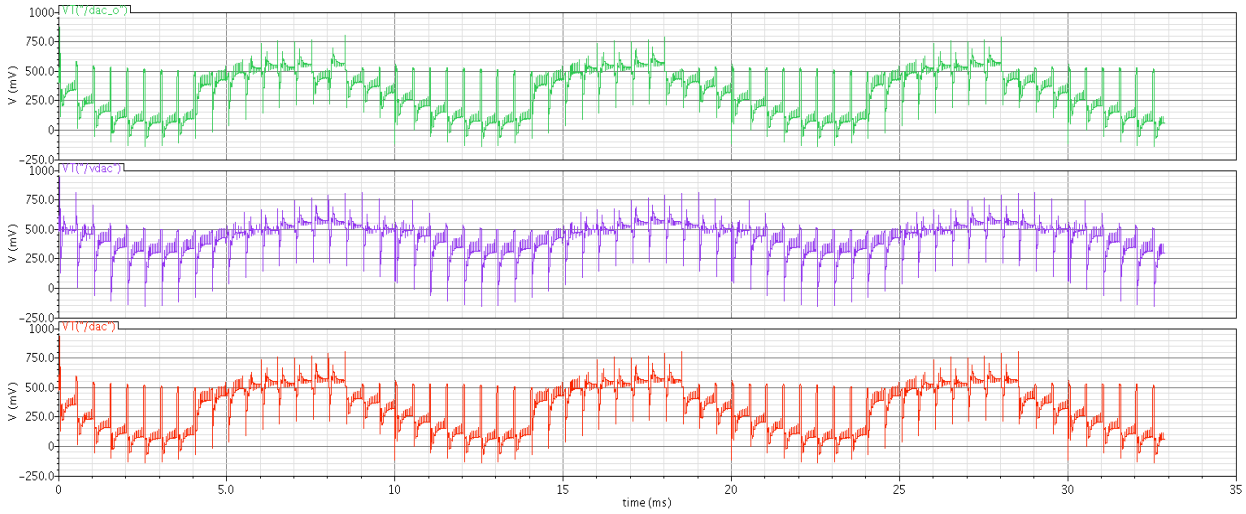


Fig 5.10: DAC response for a sinusoidal input of 100 Hz, 100 mV centered at 500 mV

the output of the DAC for all the three-implemented comparators. The middle waveform belongs to the comparator finalized for the project. The waveform explains the output waveform of 200 mV centered at 500mV. The second (middle) waveform clearly shows the conversion of the input waveform by confirming the time cycle of the input waveform.

5.4 OUTPUT SPECTRUM:

The output spectrum for the ac input signal and also for a ramp input signal is presented below. The given ac signal is a 50.78125 Hz amplitude of about 200mV that is centered on 400mV. The reference voltage is used is 600mV, which is half of the supply level used. The quantization steps are quite uniform and the signal frequency is selected so low so that it can be possible to plot all the possible output codes.

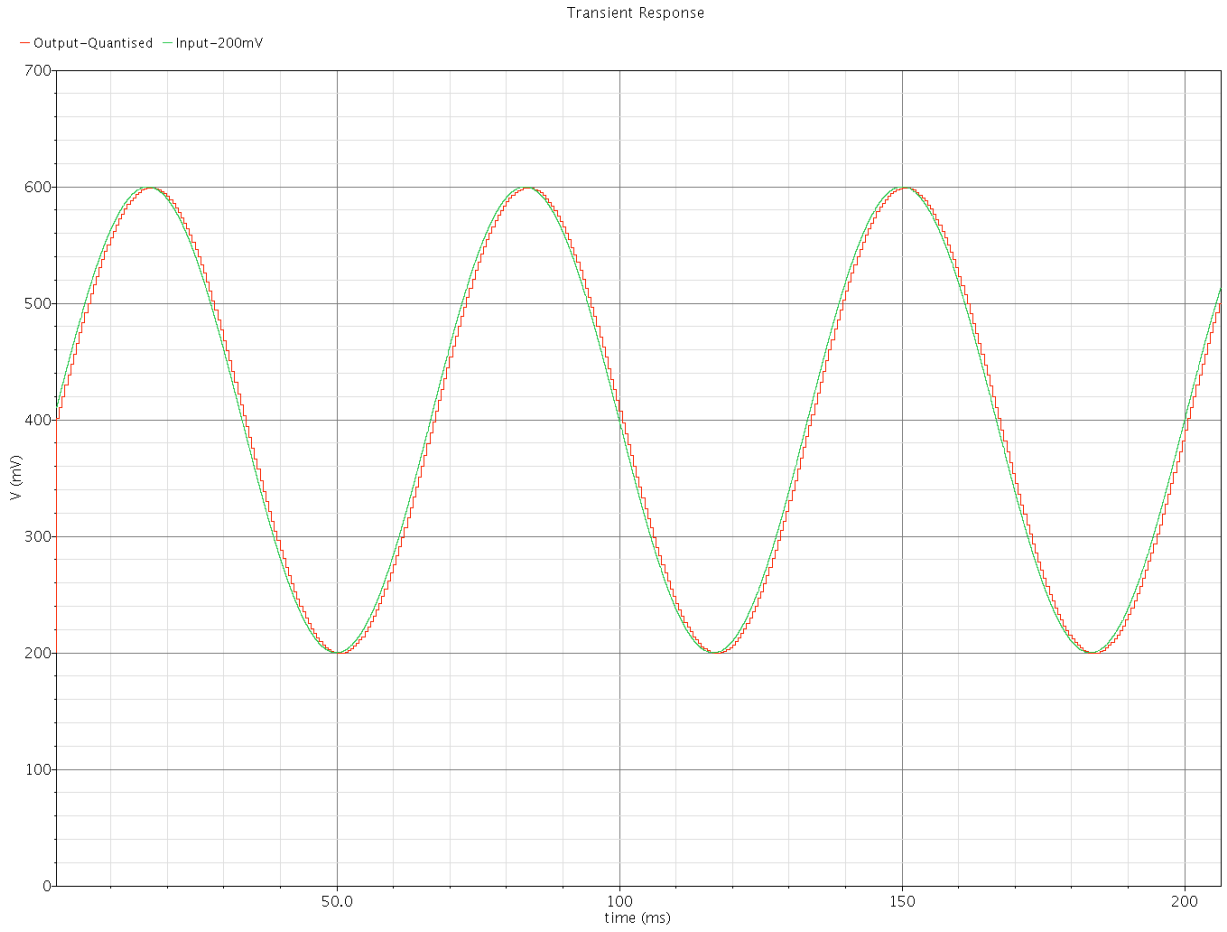


Figure 5.11 : Output Spectrum for a very low frequency AC signal

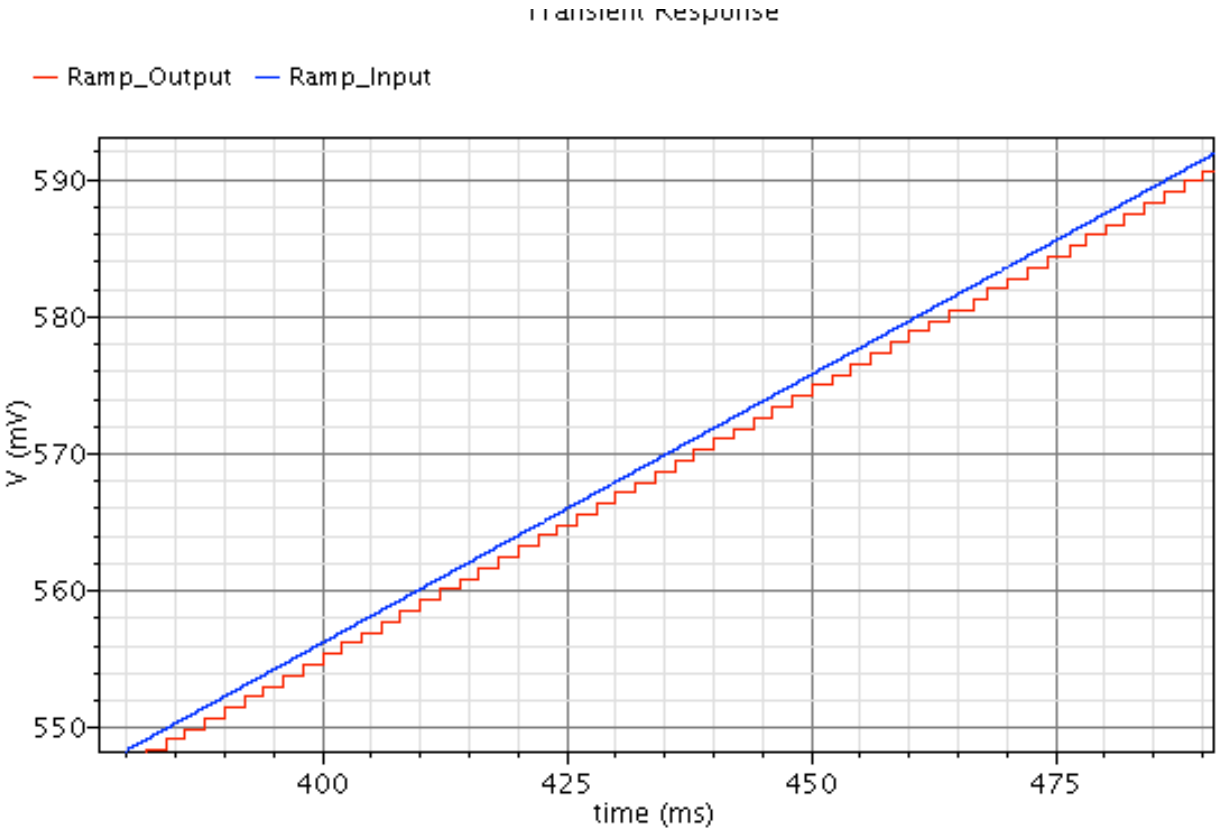


Figure 5.12 : Output Spectrum for a ramp input signal

5.5 FFT PLOT OF THE OUTPUT

The FFT analysis is done for the whole system in an efficient way by following the coherent sampling process. It poses a big issue of spectral leakage to the whole SNR figure of the system if the coherent sampling process is not followed. In coherent sampling process, the attention is paid to the coherence of the sampled waveform in the data record. There are some specific rules to be followed when it comes to coherent sampling. The number of cycles and the number of samples in a record should not have any common factors, which guarantees that the samples are uniformly distributed in phase from 0 to 2**π.**

This relationship can be explained mathematically as follows.

$$\text{Fin} = \frac{M*Fs}{N},$$

where Fin is Input frequency, M is a prime number which indicates the chosen number of periods of input signal for the computation of FFT, N is number of FFT points chosen and Fs is the sample frequency. The chosen M is 47, N is 2048 and Fs is 2 KHz so that the input frequency comes around 45.99 Hz. The simulation time is around 1.024 seconds.

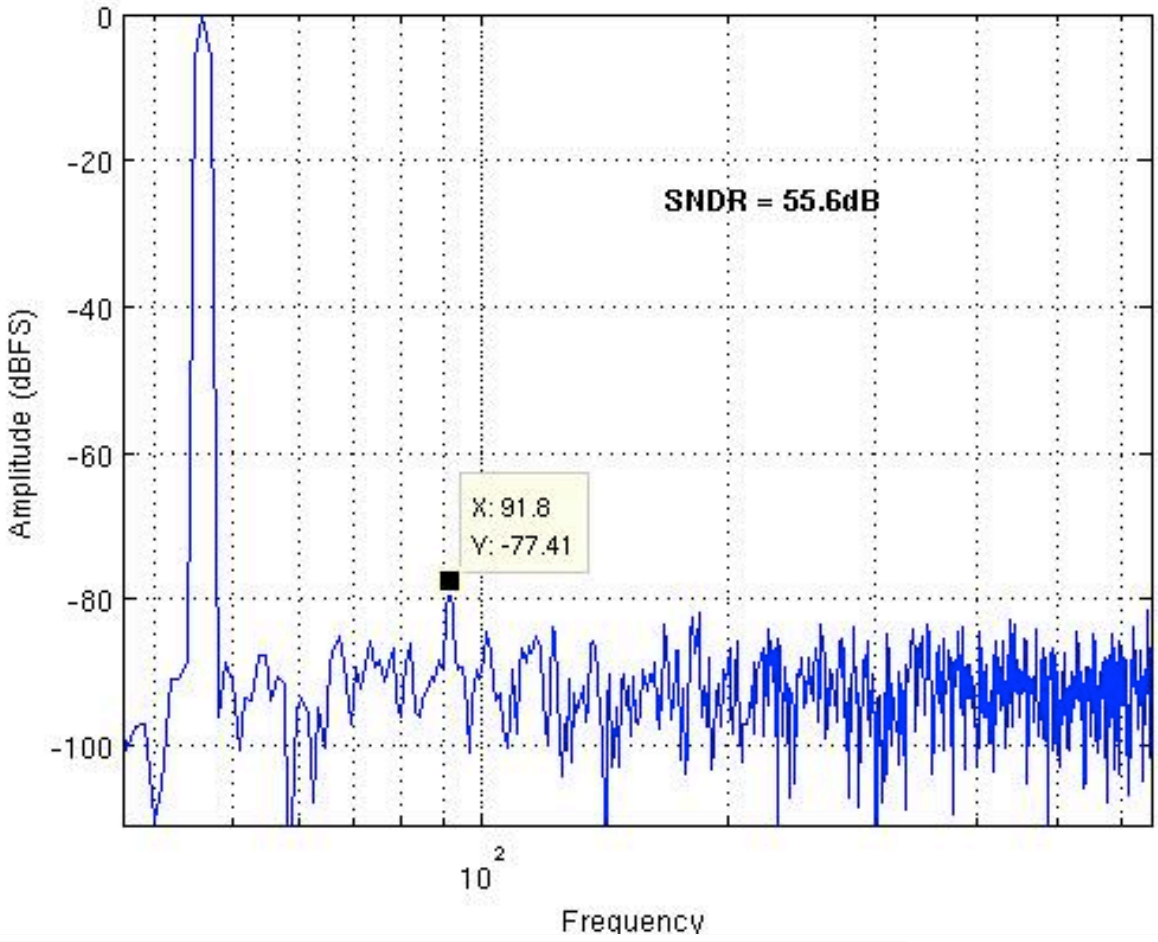


Figure 5.12. FFT plot of the whole system

5.6 SIGNAL TO NOISE AND DISTORTION RATIO (SNDR)

The computed SNDR is calculated to be 55.6 dB for the system.

5.7 SPURIOUS FREE DYNAMIC RANGE (SFDR)

The calculated SFDR is calculated from the FFT plot and it is found to be 77 dB for the entire system.

5.8 EFFECTIVE NUMBER OF BITS (ENOB)

The Effective Number of bits can be found out using the following formula and it is found to be 8.97 bits.

$$\textbf{ENOB} = \frac{\boldsymbol{SINAD}\ (\boldsymbol{dB}) - \mathbf{1.76}\ (\boldsymbol{dB})}{\mathbf{6.02}\ (\boldsymbol{dB/bit})} = \mathbf{8.97\ bits.}$$

6. CONCLUSION:

In this project, the fully differential architecture is completely studied and also the single ended architecture of the 2KS/s 10-bit SAR ADC is studied and simulated in the Cadence tool and found out the respective performance parameters. In order to minimize the power consumption by the system, the track and hold circuit is inherently implemented in the DAC circuit. Three different types of comparators are studied and the one with the low offset voltage capability is chosen to implement the comparator in the SAR system. The SAR logic is completely implemented in VerilogA language and the control signals to the DAC block are given accordingly.

The switch used in the DAC block is made of CMOS transmission gates due to its capability to maintain the constant ON resistance and also the negligible level of charge injection property. The supply voltage used here is 1.2 volts.

CHAPTER VII

REFERENCE

(I) A 0.92 mW 10 bit 50 MS/s SAR ADC in 0.13 um CMOS process-*Chun Cheng Liu, Soon Jyh Chang, Gaun Ying Huan, Yin Zy Lin.*

(II) A 10-bit 40 MS/s Successive Approximation Register A/D Converter. *Tzu Hen Hsu, Ying-Shun Chuang, Chun-Ping Huang.*

(III) A High-Speed CMOS Comparator with 8-bits resolution .*G.M.Yin, F.Op't Eynde and W.Sansen*

(IV) Verilog-A Language Reference Manual – Version 1.0

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(XIV) A High Speed CMOS comparator for use in an ADC – *Benjamin J.McCarroll, Charles G.Sodini and Hae Seung Lee.*

(XV) Data Converters- *Franco Maloberti Pavia University Italy.*

(XVI) Principle of Data Conversion System Design – *Behzad Razavi*.

(XVII) Study of Interleaved SAR ADC and Implementation of comparator for high definition video ADC in 65nm CMOS process-Sara Qazi

(XVIII) Design and Evaluation of an ultra low power Successive Approximation ADC- Dia Zhang

(XIX) Design of High Speed Analog to Digital converters using low Accuracy components- Timmy Sundström.

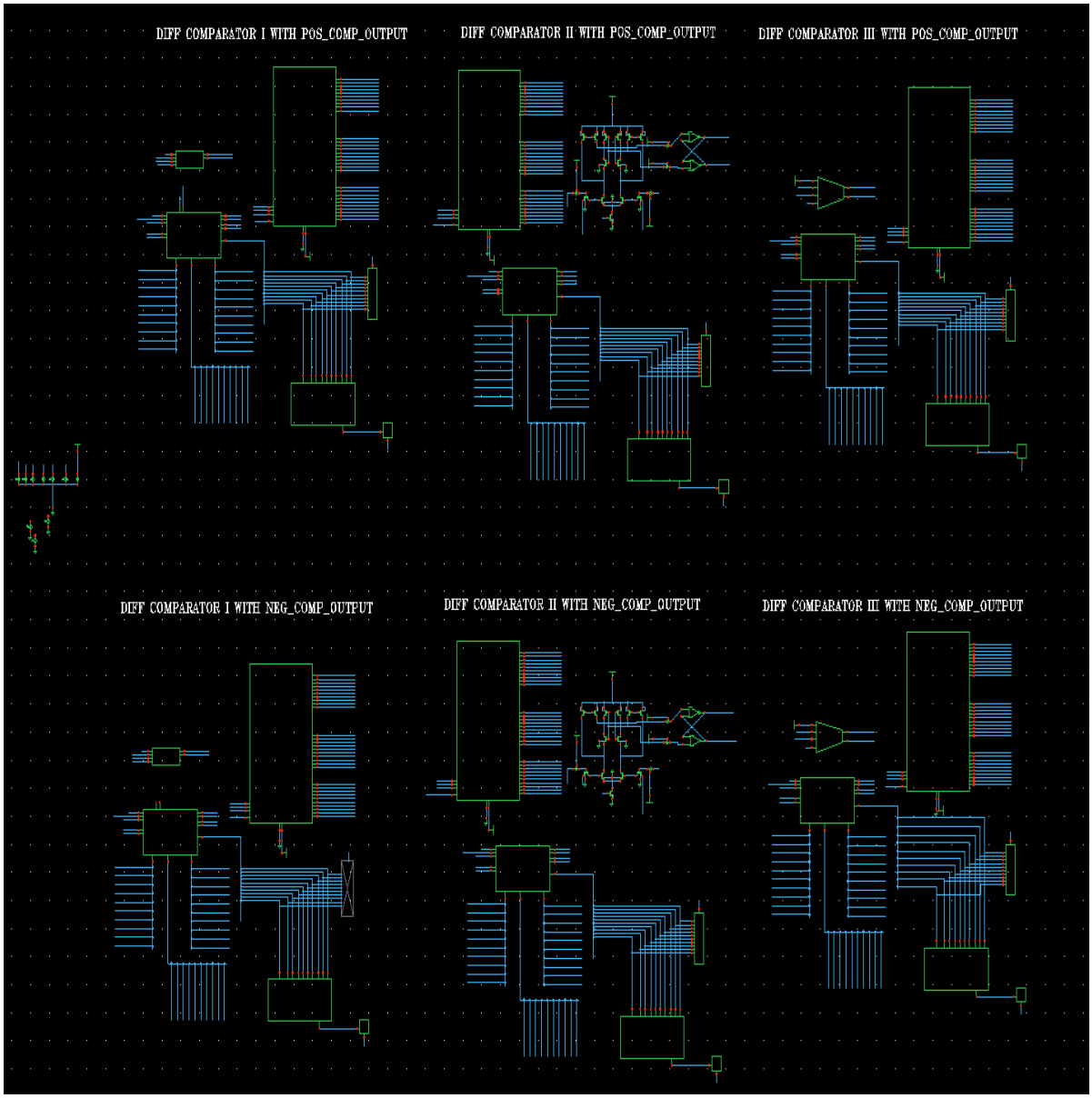
(XX) http://www.national.com/AU/design/courses/179/print.htm#01sum04.

(XXI) Offset voltage analysis of dynamic latched Comparator. By HeungJun Jeon and Yong Bin Kim.

CHAPTER VIII

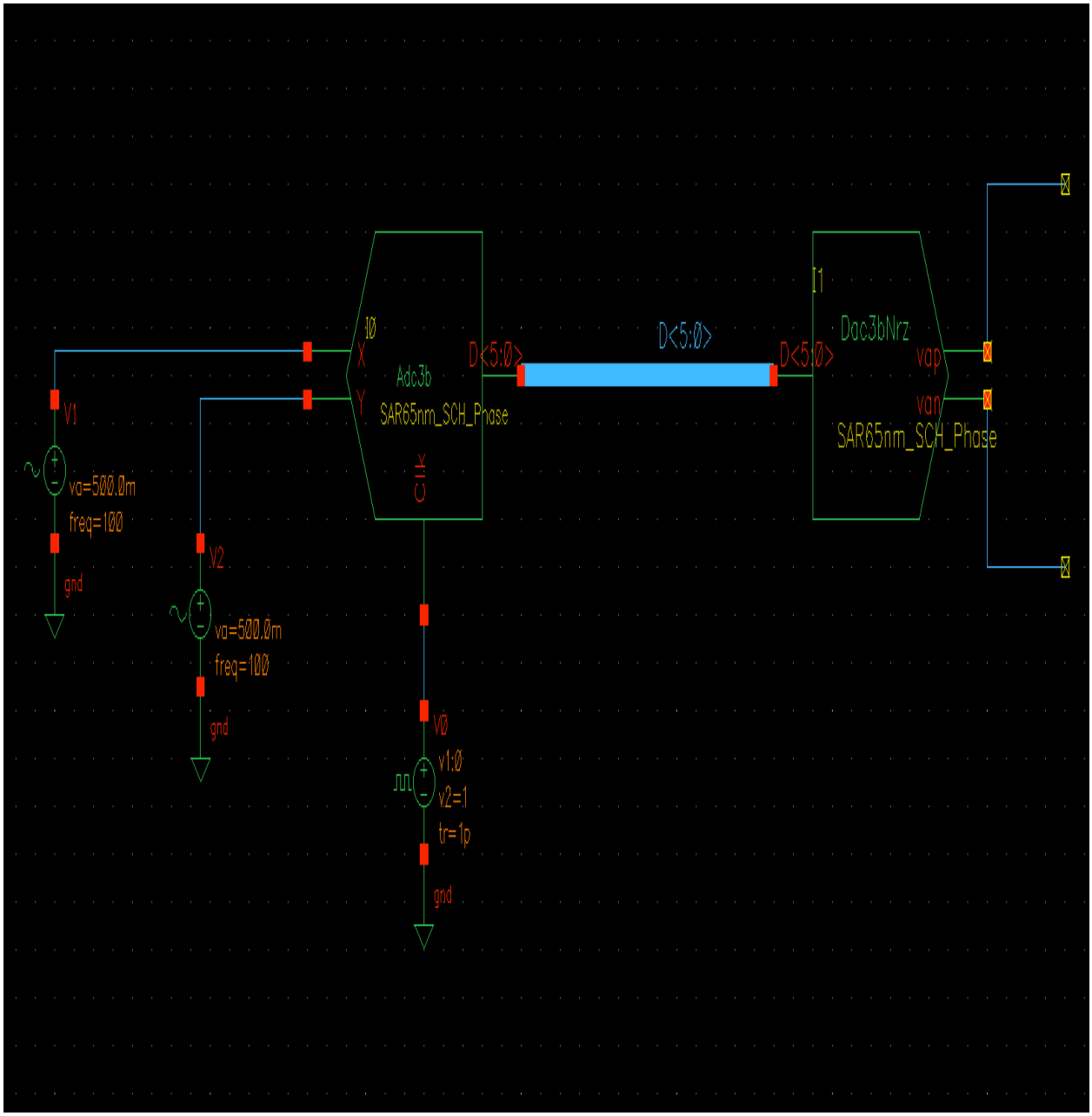
8.APPENDIX 8.1 APPENDIX II

8.1.1 TEST BENCH WITH THREE DIFFERENT COMPARATORS

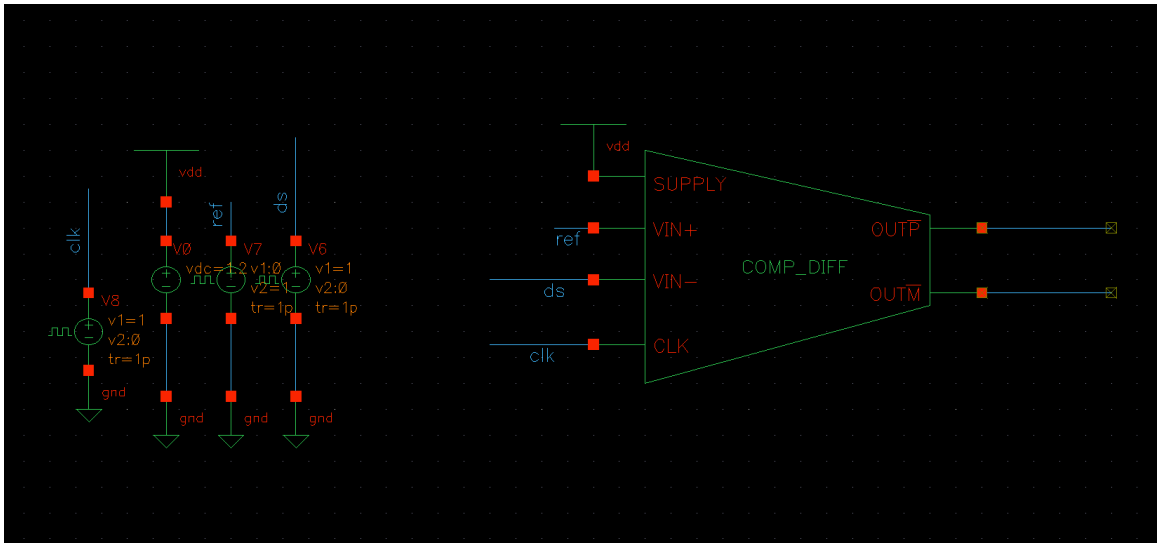


8.1.2 TEST BENCH FOR IDEAL 3-BIT DAC SETUP:

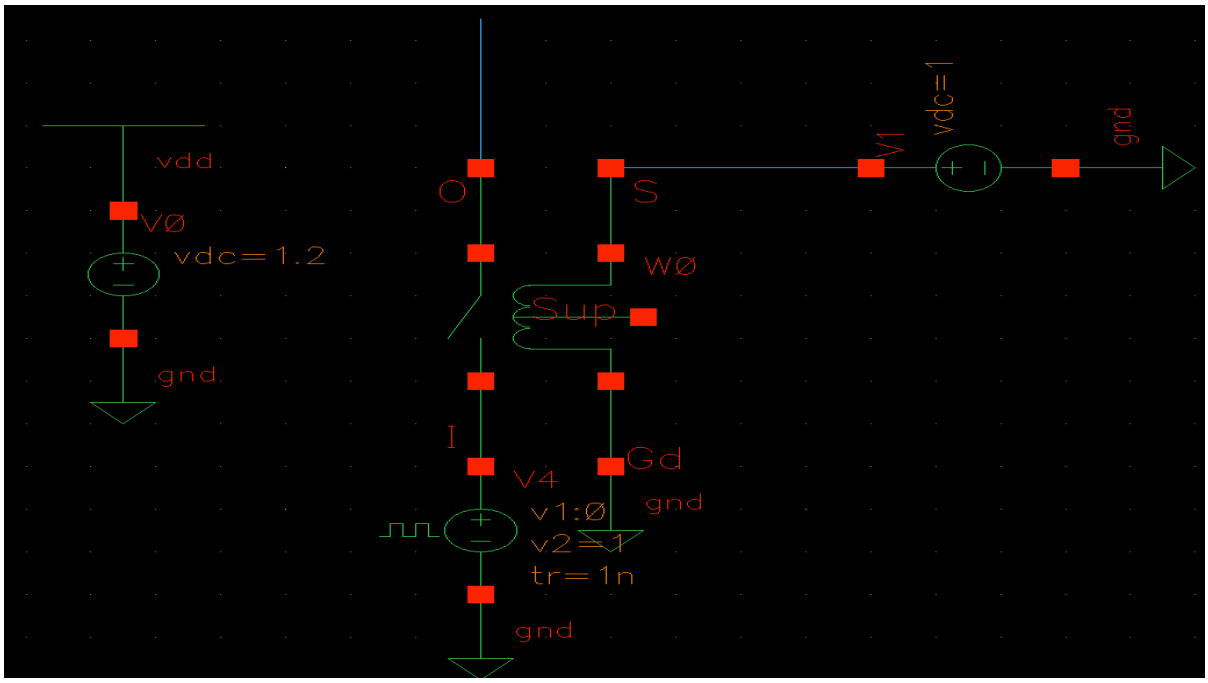
(MODIFIED LATER FOR 10-BITS)



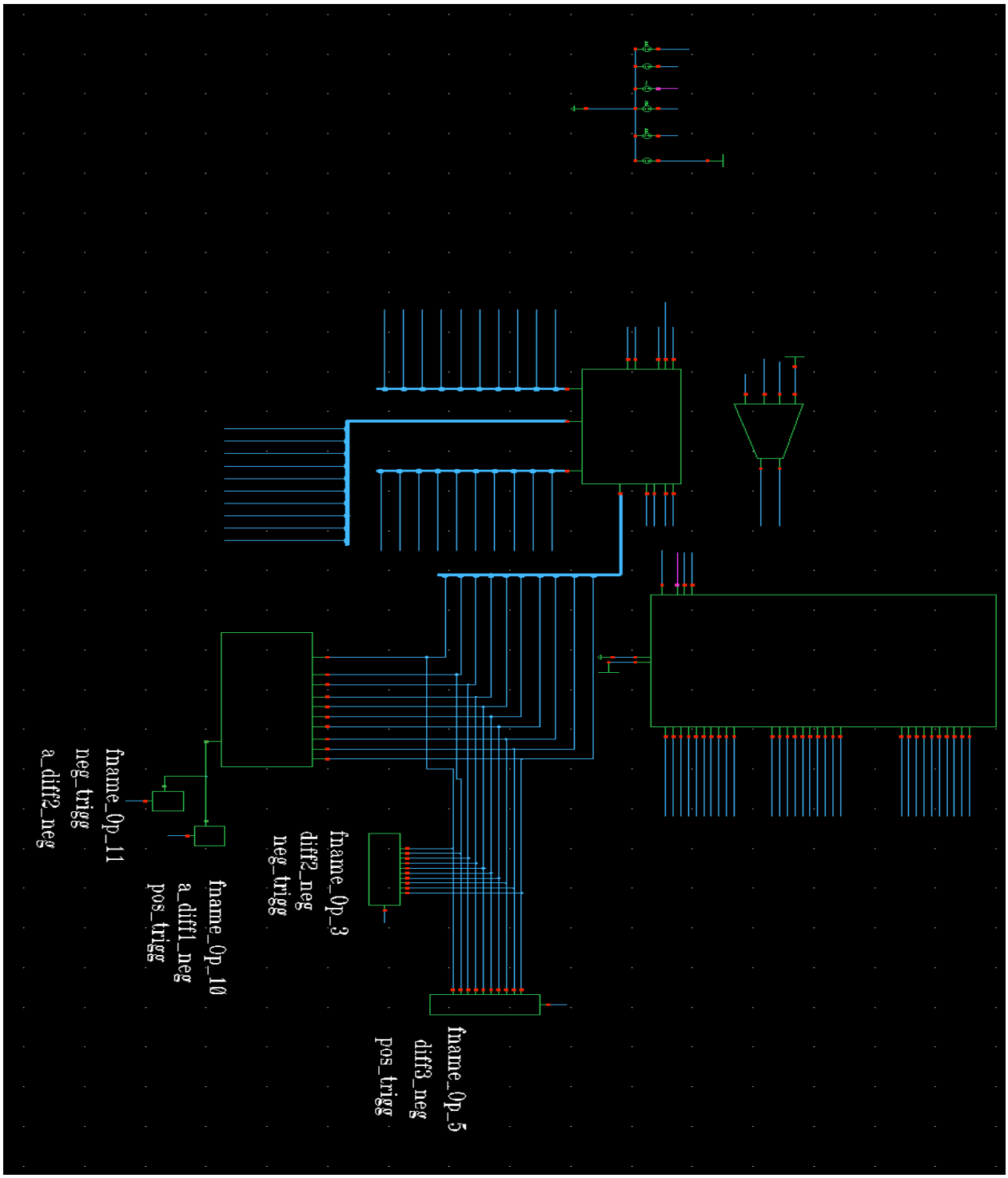
8.1.3 TEST BENCH OF THE CHOSEN COMPARATOR



8.1.4 TEST BENCH FOR SWITCH STRUCTURE:



8.1.5 TEST BENCH FOR THE ENTIRE SYSTEM



8.2 APPENDIX III

MATLAB SCRIPTS FOR PERFORMANCE METRICS:

8.2.1 FFT CALCULATION:

```
function [spec] = calcfft(data, window)
% Number of fft points
N = length(data);
ss = zeros(1,N/2);
if (nargin<2 | (window==2 | window==0)==0) %Hann window
   nsig = 1;
   w=hann1(N);
elseif (window==2)                %Hann2 window
   nsig=2;
   w=hann2(N);
elseif (window==0)                %rectangular window
   nsig=0;
   w=rectwin(N)';
end
% calculate the fft
s = fft(data .* w) / norm(w,1);
% accumulate the power, times 2 to obtain the single ended spectrum
ss = ss+2*abs(s(1:N/2)).^2;
% calculate the rms value, normalized to a Vref of +- 1
spec = sqrt(ss) *sqrt(1-(-1));
```

8.2.2 DYNAMIC PERFORMANCE METRICS

8.2.2.1 SNR, ENOB

```
function snr = calculateSNR(hwfft,f,nsig)
% snr = calculateSNR(hwfft,f,nsig=1) Estimate the signal-to-noise ratio,
% given the in-band bins of a (Hann-windowed) fft and
% the location of the input signal (f>0).
% For nsig=1, the input tone is contained in hwfft(f:f+2);
%  this range is appropriate for a Hann-windowed fft.
% Each increment in nsig adds a bin to either side.
% The SNR is expressed in dB.
if nargin<3
   nsig = 1;
end
signalBins = [f-nsig+1:f+nsig+1];
signalBins = signalBins(signalBins>0);
signalBins = signalBins(signalBins<=length(hwfft));
%s = norm(hwfft(signalBins));                    % *4/(N*sqrt(3)) for true rms value;
s = sum(hwfft(signalBins).*hwfft(signalBins));
noiseBins = 1:length(hwfft);
noiseBins(signalBins) = [];
%n = norm(hwfft(noiseBins));
n = sum(hwfft(noiseBins).*hwfft(noiseBins));
if n==0
   snr = Inf;
else
```

```
  %snr = dbv(s/n);
  snr = 10*log10(s/n);
end
N    = 1024;                  % Number of samples
Vref = 1;                     % Reference level
nper = 7;                     % Number of periods of the input signal (integer)
                              % that are going to be sampled
Fs = 2^11;                    % Sampling frequency 2 KHz
Fin = (nper * Fs / N);        % Input signal frequency (Fin = nper * Fs / N)
Ts = 1/Fs;                    % Sampling period
bw = Fs/2;                    % Signal bandwidth
Nbits = 10;
NintQ = 2^Nbits;              % Number of intervals in the quantizer,
wintype=1;     %wintype = 1 for hann1; = 2 for hann2; = 0 for rectangular
load('AFIDAC_diff1_neg.dat');
data     = AFIDAC_diff1_neg';
spec1 = calcfft(data,0);
f = Fin / Fs;                 % Normalized signal frequency
bw_bins = round(N * (bw / Fs));                    % Base-band frequency bins
spec1_inband = spec1(1 : bw_bins);
SNR = calculateSNR(spec1_inband,nper,wintype)
Rbit = (SNR - 1.76) / 6.02            % Equivalent resolution in bits
```