Master's Thesis

Validation Testing of Analog Certification Testing Equipment

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Abstract

The certification laboratory at Nokia Copenhagen ensures that the mobile phones developed by Nokia meets the requirements according to specific technology standards. The laboratory is focused on test concerning the communication between SIM/USIM-card and the mobile phone. This communication is monitored and measured by a probe supplied by an external manufacturer.

Once every year the probe is sent to the manufacturer for calibration. Interest has been shown to make testing of the measuring device easier and more reliable. These validation tests occur in between the calibrations and are done to ensure the accuracy of the testing.

The part of the certification testing procedure that will be the focus of this master thesis are the analogue tests according to the test case specifications found in the ETSI documentation. These tests concern, among other things, the voltage levels on the different contacts on the SIM/USIM-card, the rise- and fall time and cycle ratio of those signals.

The goal of this master thesis is to determine how these tests should be carried out in order to ensure the reliability of the probe while still keeping the test fast and easy to perform.

Abbreviations

APR	Analog Probe
ETSI	European Telecommunications Standards Institute
SIM	Subscriber Identity Module
USIM	Universal Subscriber Identity Module
VCC	Common-Collector Voltage
RST	Reset
CLK	Clock
I/O	Input/Output
SPU	Standard or Proprietary Use
AMB	Analog Measurement Board
COTS	Commercial Off The Shelf

Contents

1 Introduction

The certification laboratory at Nokia Danmark A/S has the objective to verify the compliance of newly developed mobile devices against relevant industry standards. This is essentially done by testing the mobile devices using test systems and simulators, one of these being a SIM/smart-card simulator which also acts as a measuring unit.

The digital measurements are analyzed in the computer but for the analog signals a test probe is being used. This probe needs to maintain a certain accuracy in order for the certification testing to be valid.

In order to determine if the probe is producing precise and valid results I need first to find out what the probe is measuring and how these measurements are performed. This is closely related to the certification requirements and which tests needs to be carried out for the phone to be certified. Another important figure is the tolerated inaccuracy of the probe, i.e when the certification will be invalid.

After establishing how and what the probe should be able to measure correctly, it's time to take a look at what kind of signals the probe should manage to generate. It is of high importance which tolerances there are for these generated signals.

Consideration is taken to the fact that this equipment is designed to be used at the testing laboratory at Nokia. Although there should be no problems regarding the validity of the test and test equipment derived if they were to be used at any other laboratory.

In short these are the questions I expect to be able to answer at the end of this thesis:

1) What kinds of signals does the probe measure and transmit, and which of these signals are of importance to ensure a valid certification?
2) How can we be assured that the probe performs valid certification measurements?
3) What requirements does that put on the equipment performing the validation testing?
4) How can we limit the need for calibration of the validation test equipment?

Since this paper discusses the testing of test equipment, to avoid too much confusion in regards to which testing equipment is being referred to, the test equipment acting as the device under test will be called "probe" and the tests and test equipment derived in this thesis will be called "validation test/ validation test equipment" or simply "test/test equipment".

2 Theoretical background

2.1 The Smart Card

For a mobile phone to be operational for other things than emergency calls, it needs a SIM (Subscriber Identity Module). This is realized through a smart card that is to be inserted into the mobile device. On the smart card is stored the IMSI number (International Mobile Subscriber Identity) which is used to identify the subscriber to the network. There can also be personal information stored on the smart card, such as phone numbers and pictures. The physical shape of the smart card, dimensions and location of the contacts, is defined by the standard given in ISO/IEC 7816. In figure 1 the layout of the card is shown. The contacts are specified as follows [2]:

- C1: VCC, supply power input
- C2: RST, reset signal input
- C3: CLK, clock signal input
- C5: GND, ground
- C6: SPU, standard or proprietary use
- C7: I/O, input/output for serial data

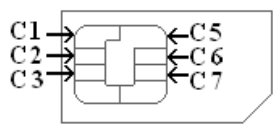

Figure 1: Smart card layout and pin numbering

The smart card can be operated at different voltages and there are four different classes defined for a mobile phone. The classes are named A, B, C and D and their operating voltages are 5 V, 3 V, 1.8 V and 1.2 V respectively. Two of these classes will not be included in this thesis, class A and class D, this is because 5 V technology is not used in Nokia mobile phones and the 1.2 V technology is not yet developed. The validation test procedure is of such sort, that it should not be necessary to change anything should class D be introduced, but if that need should arise; any updates or changes should be easily introduced.

2.2 The IT^3 Test System

The test system used in the Nokia certification laboratory is the IT^3 test system. It is supplied by Comprion and the two main parts of the test system is an IT^3-tower and an analog probe, see figure 2 below.

Figure 2: The IT^3-tower to the left and the analog probe to the right.

Figure 3: One of the four types of flex adapters used to connect the mobile phone to the test system.

The mobile phone connects to the analog probe via a flex adapter, shown in figure 3. This is an accessory supplied by Comprion with good and well-known characteristics, giving the test system a satisfying connection to the mobile phone. This means that the resistance and other parasitic introduced by the adapter will in no way affect the outcome of the testing of the mobile device. Via the flex adapter the IT^3 sends signals to the mobile phone, simulating a smart card, both logical as well as electrical.

Asides from simulating a smart card the IT^3 also performs testing on the connected mobile phone. The signals of the interface are measured and recorded and the communication can be displayed on electrical, protocol, transport and application layer.

This is done by using digital comparators, comparing the tested signal against adjustable values. When the state of such a comparator changes, a so called trigger event is activated and the state of every

trigger signal combined with a clock-cycle-counter-value (i.e. the total number of actual clock cycles) and a time stamp will be saved. During time measurements, additional information such as the results of rise- and fall time measurements, duty cycle and periodic time, is transmitted as well. In total the IT^3 works with approximately 100 active trigger signals simultaneously.

This data structure, the trigger status together with the time stamp, clock-cycle-counter and additional timing information is referred to as *traceline*, which is analyzed and visualized in the different layers with the help of analyzing programs. [5]

The basic construction and the data flow are shown adumbrated below [5]:

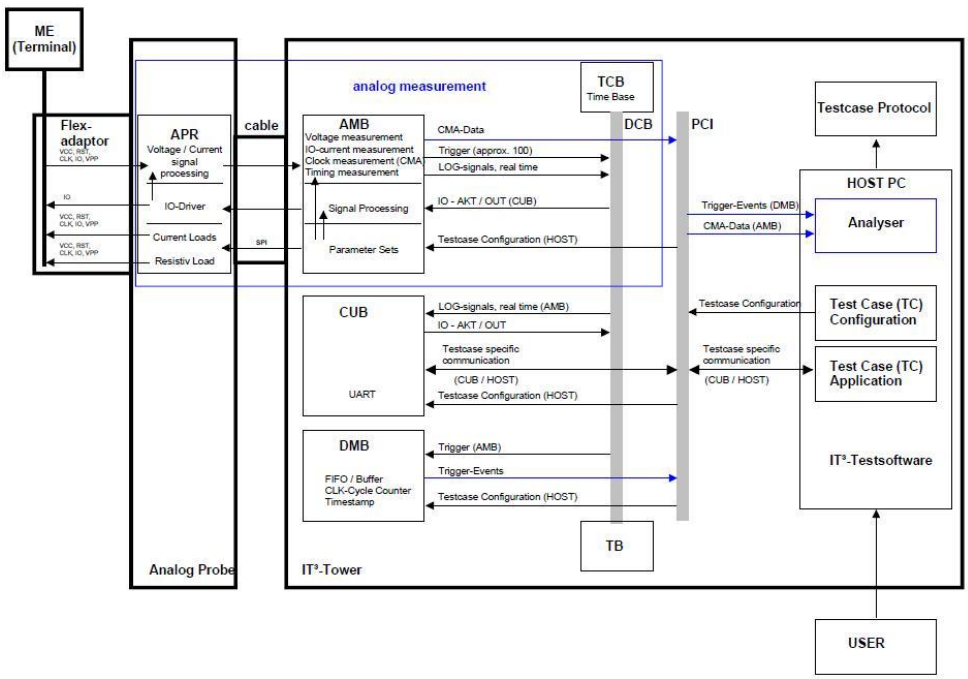

Figure 4: Block diagram and data flow

When performing measurements, the Analog Probe (APR) uses analog buffer amplifiers to buffer the signals and then sends them as differential signals to the Analog Measurement Board (AMB). Here the signals are digitized with a resolution of 50 MHz and 12 bit with the exception of the clock signal for which the time measurements must have a higher resolution and are digitized with a resolution of 1.25 ns. This can be compared with the resolution of the other channels which is 20 ns.

Test sequences and trigger levels are only fixed when using the IT^3 for certification purposes. For validation testing procedures custom test sequences are available where all trigger levels can be changed as well as which signals are to be measured.

2.2.1 Measurement uncertainties

For all parameters there are uncertainties for each of the contacts. These are determined by the manufacturer of the probe. These should be compared with the required precisions stated in the test specifications [4]. Both of these are presented in the table below. All the uncertainties are specified for the normal distribution with a k-value of 2. This k-value means that in 95.4 % of the cases the measured value lies within these uncertainties.

Contact	Parameter	Max. allowed unc.	Probe unc.	
C1 (VCC)	Voltage level	±50 mV	±8.6 mV	
C2 (RST)	Voltage level	±50 mV	±13 mV	
C3 (CLK)	Voltage level	±50 mV	±13 mV	
	Rise time	±5 ns	±2.1 ns	for a max. rise time of 50 ns and card class C (1.8V)
	Cycle ratio	±2.5 %	±0.97 %	for a max. frequency of 6MHz and card class C (1.8V)
	Frequency	±0.5 %	±0.65 %	for f = 5 MHz
			±0.13 %	for f = 1 MHz
			Period ±1.3 ns	This is what is given. The above percentages are calculated.
C7 (I/O)	Voltage level	±50 mV	±13 mV	
	Current level	None given	±38 µA	for a max. current of 2.000 mA
			±63 µA	for a max. current of 5.000 mA
	Rise time	±100 ns	±52 ns	for a max. rise time of 1 µs and card class C (1.8V)

Table 1: Uncertainties for measurements on the four contacts [6]

The uncertainties of the probe lie, in most of the cases, well beneath the maximum allowed uncertainties, with the exception of the frequency measurement for the clock. For frequencies higher than 3.846 MHz, the probe does not meet the requirements. At the moment this is not a problem for the test laboratory at Nokia as the phones produced at Nokia do not support a clock frequency higher than 3.8 MHz. The manufacturer is aware of this flaw and is working on a solution to better the accuracy of the probe and until it is implemented the test system rules in favor of the mobile phone if the frequency is close to or exceeds this upper limit.

The question on whether one should test the limits regarding the probe uncertainties, or if it is of higher importance to see when the probe fails to measure adequately for certification purposes, is raised. This is of course a question of the purpose with the validation testing. If it is to catch the probes first signs of drifting or to determine when the need for calibration is imminent. Measuring both of these cases might give the appropriate time frame to take proper actions, from the first sign of drifting to the risk of faulty certification.

2.3 The Certification Test Specifications

In order to make sure the smart card works properly together with the mobile phone a set of test sequences have been developed. A number of such test sequences exist, but the ones that are of interest for the purpose of this thesis are specified in ETSI 102.230 [3] and in order for the phone to be certified it has to meet these standards. The tests that are treated in this thesis are the electric characteristic tests, and to be more specific the ones making use of the probes internal analog analyzer. These test cases are numbered from 5.1.1 to 5.2.5 and are in total 15 main test cases, some of which have sub-sequences. For each test case the following is specified:

- Definition and applicability
- Conformance requirements

- Reference
- Test purpose
- Method of test
- Acceptance criteria

The test cases will be described in a general way below. For more specific information see reference [3].

There are in effect five different kinds of measurements of interest carried out. These are measurements of the voltage and current levels of the smart card contact, the rise-and fall time, the duty cycle and the frequency of the signal. The two latter ones are only carried out for the clock signal.

Table 1 states the nominal test conditions [3] and if not stated otherwise in the different test sequences these are the conditions that must be applied to the contacts of the smart card. The conditions are the same for 3 V and 1.8 V operational modes except for the conditions on C1, thus this contact has two values stated in table 2.

Contacts	Low level	High level	Max. capacitive load
C1 (VCC) (3V)	- - -	I = 7.5 mA	
C1 (VCC) (1.8V)	- - -	I = 5 mA	
C2 (RST)	I = -200 µA	I = 20 µA	30 pF
C3 (CLK)	I = -20 µA	I = 20 µA	30 pF
C5 (GND)	- - -	- - -	
C7 (I/O)			30 pF
Terminal input	I = 1 mA	I = 20 µA	
Terminal output	I = -1 mA	I = 20 µA	

Table 2: Nominal test condition on a 3 V and 1.8 V smart card

Currents going into the contacts are considered to be positive and outgoing currents are considered negative. All voltages are measured with respect to ground (GND).

2.3.1 Measurements on contact C1 (VCC)

The tests on this contact only concern the voltage level. The voltage level should for all test cases stay within a certain range. This range is specified by the operational mode (1.8 V or 3 V), and is given by

$$V_{CC} = V_{op} \pm 10\%$$

where V_{op} is the operational mode voltage. This should be true during both normal operation for currents up to 10 mA and for spikes in the current consumption induced by the simulator. These spikes can be both continuous and random and are of six different kinds, three random and three continuous [3]. These spikes can be found specified in Appendix B.

2.3.2 Measurement on contact C2 (RST)

As with the test concerning contact C1 this test only concerns the voltage levels applied to the contact. The range of the voltage is specified in [3] and is given by

$$-0.3\,V \leq V_L \leq 0.2 * V_{CC}$$

$$0.8 * V_{CC} \leq V_H \leq V_{CC} + 0.3\,V$$

V_L is the low level voltage and is valid for a current of -200 μA. V_H is the high level voltage, valid for a current of 20 μA. These currents are applied by the simulator. The value of V_{CC} is not the operational voltage of the mobile device, but the actual voltage applied to the smart card. This means that the limits are time dependent and are constantly changing during the test case. This is also true for the tests performed for contact C3 and C7 (CLK and I/O).

2.3.3 Measurements on contact C3 (CLK)

For this contact the voltage level, the rise- and fall time, clock cycle ratio and the frequency are being measured and should all be within the specified ranges. These ranges are given in table 3.

	Range
Voltage Low state (I = -20 μA) High state (I = 20 μA)	 $-0.3\ V \leq V \leq 0.2 * V_{CC}$ $0.7 * V_{CC} \leq V \leq V_{CC} + 0.3\ V$
Rise- and fall time	< 50 ns
Cycle ratio	40% - 60%
Frequency	1 MHz – 5 MHz

Table 3: Ranges specified for the contact C3

2.3.4 Measurements on contact C7 (I/O)

Three measurements are performed on this contact; the voltage level, the current level and the rise- and fall time. There are three different states with specified ranges for the contact. These states together with their ranges are given in table 4.

State	Range
Terminal receiving state A (low state)	$I \leq 1\ mA$ when V = 0 V
Terminal transmitting state A (low state)	$-0.3\ V \leq V \leq 0.2 * V_{CC}$ when I = 1 mA
Terminal transmitting or receiving state Z (high state)	$0.7 * V_{CC} \leq VV_{CC} + 0.3\ V$ when I = 20 μA
Rise and fall time (valid for all states)	≤ 1 μs

Table 4: Ranges specified for contact C7 in different states

2.4 Existing validation test equipment

The currently used validation testing of the probe consists of a so called “Golden Sample”, that is, a mobile phone with proven good characteristics, which undergoes the test procedures. If the test system gives a fail verdict for any of the test cases the conclusion can be drawn that the probe does not measure correctly.

This is not a satisfyingly good test procedure for a number of reasons. The first and most obvious one is that it only measures if the probe gives a false fail verdict. The probe may very well be measuring incorrectly even though the verdict for the Golden Sample is correct. Secondly, this method does not test if the probe gives a correct fail verdict and without it there is no guarantee that a pass verdict in fact is a true pass. This could make the certification somewhat unreliable. Furthermore this validation test does not test the limits for fail or pass verdicts, and it is most likely here that the probe will show the first signs of incorrect measurements. There is also good reasons to include test regarding the

maximum allowed mismeasurements for certification in the validation test procedure and with this existing method, no such tests are performed.

Without more proper means to verify that the probe is measuring correctly it is not an adequate way of verification. A better solution is needed.

2.5 Setting up the IT^3

There are a number of settings available for the IT^3 and the ones of interest will be discussed here. As mentioned earlier the IT^3 compares the signal from the test equipment with trigger thresholds. All of these thresholds for all contacts are adjustable.

There are four different classes in which the smart card can be operated. The IT^3 can simulate two classes in series. It is also possible to simulate in one single class. The first thing to address is how to configure these classes. The names of the classes are of no importance when constructing the validation tests as they can be changed according to will, thus they are merely notations to separate the classes.

Below figure 5 shows how the classes are defined when running certification tests. The limits used are the ones defined in the ETSI test specification.

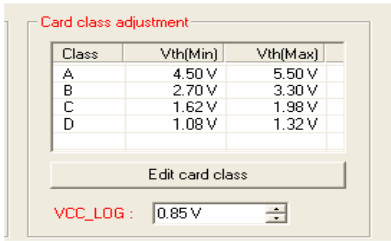

Figure 5: Default limits for the card classes

If simulation in two classes is chosen a set of parameters will be allocated to each voltage class, set 1 and set 2, see figure 6. The threshold for all other contacts will be programmable for the different classes separately. If only one class is chosen it will be allocated to set 1.

The voltage thresholds are for all signals except VCC of the type

$$Threshold = a * V_{CC} + b$$

There are also a high and low state for these signals and thus there are four thresholds; low min, low max, high min and high max. It is of utter importance that the following condition is fulfilled:

$$Low\ Min < Low\ Max < High\ Min < High\ Max$$

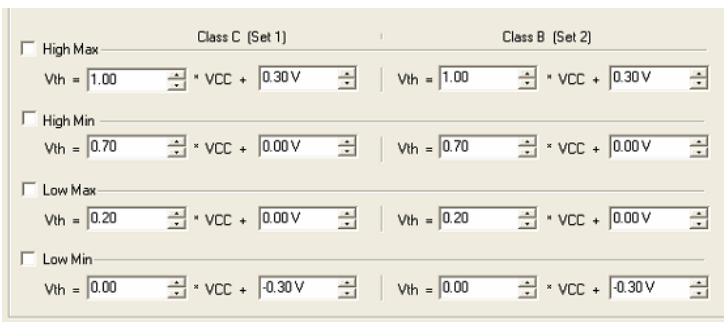

Figure 6: Setting the voltage threshold

The current threshold, only applicable for the contact C7 (I/O), has an adjustment range of 0.1 mA to 5 mA. Since this measurement only is performed when the in terminal receiving state (see table 4) the current measurement will not be enabled unless the voltage on contact C7 is below the Low Max threshold and two card clock cycles have elapsed. The measurement will stop as soon as the Low Max threshold is overshot.

Rise and fall time measurements are carried out for the CLK and I/O contact. The maximum rise and fall times can be set separately. It is also possible to choose between two types of measurement; one percentage dependent and one with adjustable V_{CC} dependent thresholds of the same type as the voltage thresholds described above. For the measurements of the rise and fall time on the CLK signal there is also a choice of setting the thresholds as a percentage of the clock cycle duration.

The duty cycle and frequency measurements on the CLK signal can be adjusted V_{CC} or percentage dependent, see figure 7.

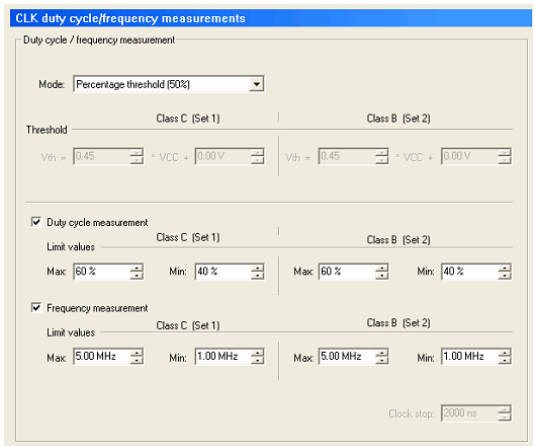

Figure 7: Setting up measurements on the CLK signal

For the voltage, current and rise/fall time measurements there is a programmable trigger time and hysteresis. As the system operates at a sampling rate of 50 MHz the minimum trigger time is 20 ns. This means that if the signal crosses the threshold for less than 20 ns it might not be detected. If the signal stays above or below the threshold for longer than 20 ns, a trigger event will occur. There may be a need for increased trigger times when measuring the voltage on C1 (VCC) during the stress of current spikes and thus the trigger time is adjustable in 20 ns steps.

The hysteresis helps in avoiding toggling of the trigger signal when the voltage or current is near the trigger value. The system resolution is 3 mV and the uncertainty of the probe is 8.6 mV. Therefore the default value of the hysteresis is 9 mV. Below is an illustration of how this symmetrical hysteresis works. When the hysteresis is set it applies to all thresholds of that channel.

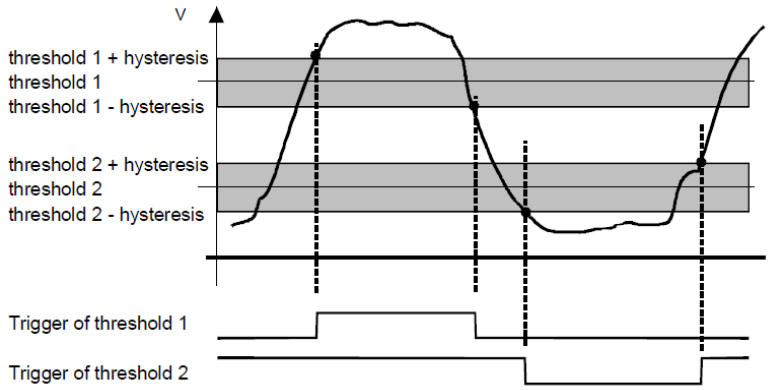

Figure 8: Hysteresis

When performing measurements on a signal that has a high and a low state, the signal overshoots the maximum voltage of the low state whenever the state is changed from low to high and in the same way undershoots the minimum voltage of the high state when going from high to low state. This is of course a correct behavior when changing states. In order to be able to detect when the voltage of the signal is too high or too low for a state a burst trigger can be activated. Whenever the voltage overshoots the maximum low voltage and then undershoots it without overshooting the minimum high voltage (that is, it does not change state) a burst trigger event will occur. The burst signal for the high state works in the same manner.

Generally the IT[3] does not engage testing of signals until the test object, for example the mobile phone, is started. This is controlled with a signal called VCC_VALID or MEAS_VALID. This signal will become 1 when the voltage on C1 (VCC) rises above $V_{th(min)}$ of the chosen class and resets to 0 when the voltage drops below the $V_{th(max)}$ of the subordinate class. For class D which does not have a subordinate class this voltage is set by the VCC_LOG value. As long as the measurement valid signal is 0 no measuring will occur. There is a way to override this criteria, see figure 9 below.

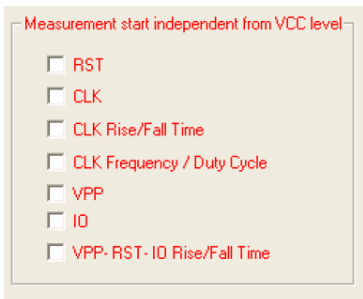

Figure 9: Starting measurements independent from VCC level

This means that all trigger signals are activated at the start of the test case. In this case it is important to configure the thresholds as V_{CC} independent otherwise they might overlap. If this mode is chosen, designing the validation test equipment might become a little easier, but requiring this signal to be valid gives an easily achievable control of when to start the measurements.

In addition to performing all the above measurements, the probe can also charge all of the contacts on the smart card with load. There are two different kinds of loads of interest, the resistive loads and the current loads. The resistive loads are set by permanent resistors and cannot be changed, only activated. The current loads on the other hand can be changed very freely. Starting with the DC-current load on VCC this can be adjusted from 0 to 100 mA. There is another current that can be applied to the VCC

contact and this is the pulse generator. Here it is possible to choose between random or continuous spikes, the pause duration of the continuous can be set and the minimum and maximum pause duration of the random spikes is also changeable. Additionally the maximum current and duration of the spike can be set as well as the rise and fall time or the slew rate. See figure 10 below.

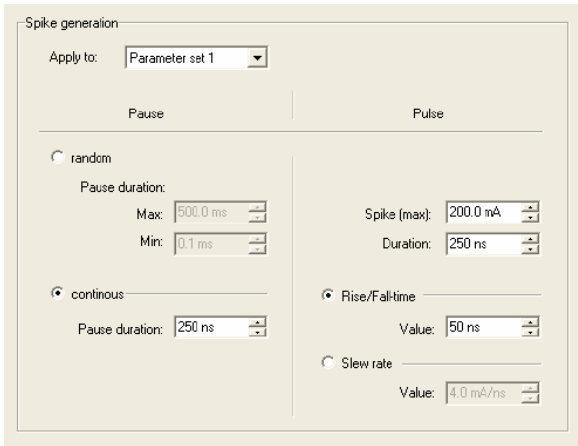

Figure 10: Spike generator settings

Where the thresholds for the voltage measurements are set it is also possible to activate that specific trigger by checking the box next to the trigger name, see figure 6. It is only an activated trigger that will produce a trigger event. That is, if the trigger is not activated it is of no importance what the trigger is set to for the verdict of the test case. In the case of current loads it is important to activate the triggers, as they in many cases determine what kind of current load is applied to that contact.

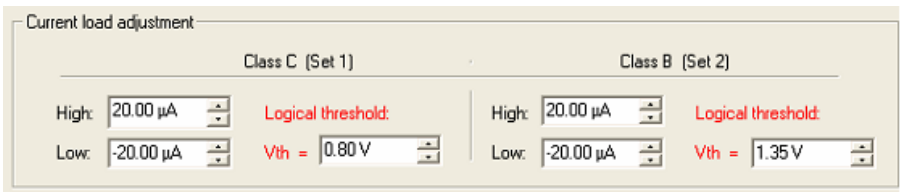

Figure 11: Setting the current loads

The logical threshold determines which of the current loads that should be applied to that contact. The threshold should lie central between the Low Max and High Min values.

3 Experimental methods

In order to determine whether or not the probe is measuring correctly a computer controlled device was considered. This device should replace the mobile phone during the test sequences. By using this kind of equipment settings can be done in order to see if the probe is behaving as expected. Boundary value analysis was used to derive the input data to the tests. These are on the boundary between equivalence classes, and within these classes the probes behavior is assumed to be consistent. The levels are then to be set just above or below the acceptance criteria, thus knowing what verdict to expect from the test system. In order to test the five probe measurements there must be adjustable levels for all of them. The accuracy must be sufficient for the application and lay well within these to avoid an extensive need for calibration of the test equipment. Another important characteristic of the

equipment is the settling time. This is critical for the signals simulating the clock and I/O, where a too long settling time might result in an unwanted fail-verdict, implying that the probe is measuring incorrectly when in fact it is the test equipment that is slow.

A block schedule of the apparatus is depicted below in figure 13.

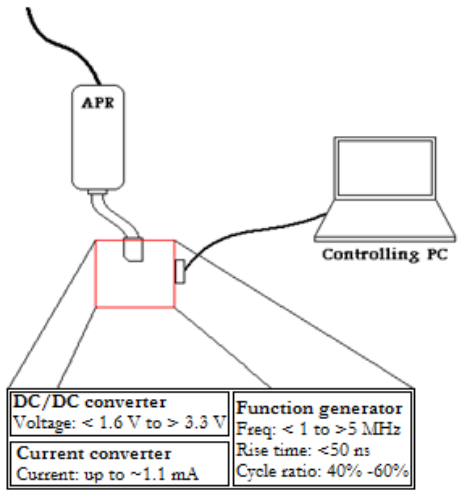

Figure 13: Block schedule of first solution suggestion.

In order to verify that the probe in fact carries out the measurements correctly a number of tests must be carried out. These tests must then be carried out for all five of the different kinds of measurements performed by the probe.

3.1 Verification measurements

As mentioned earlier, for each of the signals emitted from the mobile equipment to the smart card there are ranges wherein the signal must lie to get a pass verdict. As these limits can be changed and the test procedures can be customized when not performing certification testing these specific limits are of lesser importance. They are, although, interesting in that way that they show what kind of parameter values the probe is expected to measure correctly.

The main idea is to set a trigger value in the IT^3 test system and then increase the parameter-under-test stepwise past this value and monitor the output result from the IT^3 in order to see if the output verdict changes within the acceptable interval with respect to the uncertainties introduced by the probe and the maximum uncertainties allowed for certification. As there are a separate A/D converter for each of the contacts, verification tests for all four contacts that are tested in the certification must be carried out.

These are the tests that are required to test if the probe is measuring correctly but in the test specifications there are also a number of voltages but mostly currents and impedances that are to be supplied to the contacts via the probe during the test procedures. Is there a need to confirm that these applied parameters are correct, i.e make sure that the probe is *performing* the tests correctly (in contrast to the above discussion whether the probe is *measuring* correctly)? There is relevance to these kinds of tests; if the test system in fact is not sending out the correct current spikes for measuring the smart card supply voltage during various power consumption scenarios it would not be a sufficient test for certification purposes. It is also here that the probe most often fails.

Due to the nature of these current spikes and the amount of work hours needed to integrate this into the test system, this is decided to be outside of the scope for this thesis. Although it is recommended that this is looked into by some other instance. There are some currents and resistive loads that can be

easily measured and the integration of this and a suggestion on how to use this measuring part of the validation test equipment to roughly measure the current spikes will be discussed.

When designing the different scenarios performed by the test equipment there are a number of things that must be taken into consideration. None of the values sent by the validation equipment should lie within the given uncertainties for that contact and operation class. There should also be at least one of the fail-scenarios that lie outside the required precisions for certification purposes. As there will be only one parameter tested at a time, the same signal source can be used for each of the contacts. Though if the IT^3 setting "Measurement start independent from VCC level" is not chosen, there must be a valid VCC voltage on contact C1 in order for the IT^3 to start performing the test, meaning there must be at least two sources. Of course, one of them can be a stable voltage source that has a fixed out voltage that just lies within the specified voltages for the card class chosen. It is nevertheless recommended to set all the voltage levels to be independent from the VCC voltage to avoid unnecessary errors derived from the small drifting that may occur in this voltage source. This source can of course be skipped all together if the choice is made to not depend on the VCC level to start the testing.

3.1.1 Voltage testing

Voltage testing will be performed for all of the four contacts and the procedure will be the same for all of them, the difference lies in the uncertainties specified for the contacts. The various uncertainties were discussed in section 2.2.1. These uncertainties are given as fixed voltage values and are valid for the whole allowed voltage range and are thus percentile the largest for the lower voltages. It might also be that the error in measurement is larger for the higher voltages. It can then be reasonable to test the probe at two voltage levels, one at each of the extremes of the voltage range. Below in figure 14 is a sketch showing how the stepping of the signal could look.

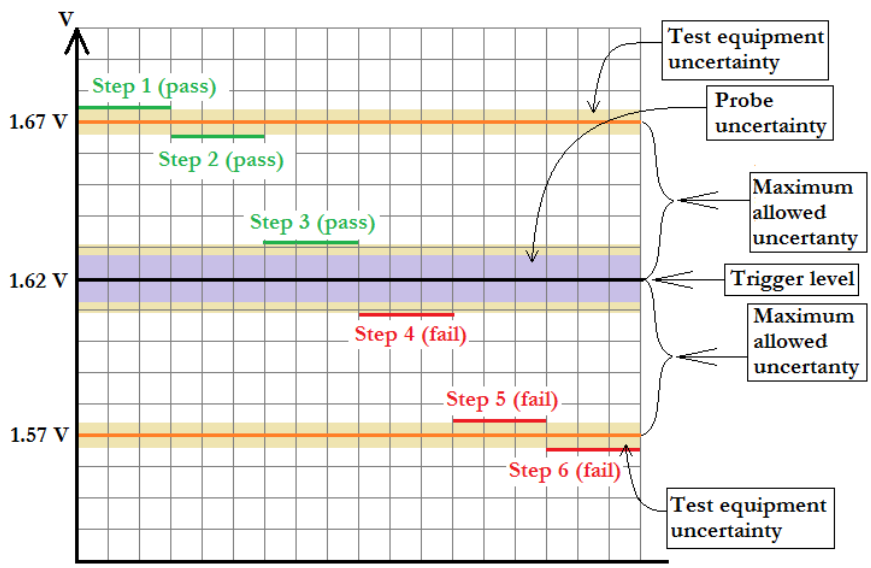

Figure 14: Suggested steps to be performed during validation testing

The three lower steps should then produce the opposite verdict of the three higher steps. In the figure above the trigger level is the lower trigger level, and so the three lower steps should produce a fail

verdict and the three higher should produce a pass. If the trigger level had been the higher level the three higher steps should be a fail and the three lower should produce a pass.

This gives both a good indication of the probes first signs of incorrect measurement and at which point the probe no longer is sufficient for certification testing.

The steps are calculated using the following equation:

$$Step\ 1 = V_{th} + (U_R + U_T)$$
$$Step\ 2 = V_{th} + (U_R - U_T)$$
$$Step\ 3 = V_{th} + (U_P + U_T)$$
$$Step\ 4 = V_{th} - (U_P + U_T)$$
$$Step\ 5 = V_{th} - (U_R - U_T)$$
$$Step\ 6 = V_{th} - (U_R + U_T)$$

Where V_{th} is the threshold voltage, U_R is the maximum allowed uncertainty, U_T is the validation test equipment uncertainty and U_P is the probe uncertainty.

The example depicted in figure 14:

On contact C1 (VCC) the voltage for the 1.8 V operational mode should lie within 1.62 V to 1.98 V to pass certification. If the trigger level then is set to 1.62 V, which is the lowest trigger level for the VCC measurements, the first three steps above should render a pass and the three latter should render a fail. The uncertainties for the probe is +/- 8.6 mV and the maximum allowed uncertainty is +/- 50 mV the sequences could look like this if the uncertainty of the test equipment is 3.1 mV (National Instruments NI PXI 6221, appendix D):

Pass 1 ; 2 ; 3 1.62 V + (50 mV + 3.1 mV) ; 1.62 V + (50 mV – 3.1 mV) ; 1.62 V + (8.6 mV+3.1mV)

Fail 1 ; 2 ; 3 1.62 V – (8.6 mV+3.1mV); 1.62 V – (50 mV – 3.1 mV) ; 1.62 V – (50 mV + 3.1 mV)

If the verdicts are as expected the probe is measuring correctly and there is no need for calibration. If step 3 or step 4 is faulty this is a sign that the probe is starting to drift but it is still valid for certification. The same is true for the step 2 and step 5, but now there is a great need for calibration of the probe. If the any of the two extreme steps, step 1 or step 6, is incorrect the probe can no longer be used for certification and must immediately be sent to the manufacturer for calibration.

Below is compiled the low and high level voltages (that is, the highest and lowest voltages allowed for certification, according to the test specifications) together with the uncertainty for the different contacts. The maximum allowed uncertainty is 50 mV for all voltage measurements and the uncertainty of the validation test equipment is considered to be 3.1 mV for all contacts.

Contact	Low level	High level	Probe uncertainty
C1(VCC)	1.62 V	3.3 V	8.6 mV
C2(RST)	0 V	3.6 V	13 mV
C3(CLK)	0 V	3.6 V	13 mV
C7(I/O)	0 V	3.6 V	13 mV

Table 5: Extreme voltage levels and uncertainties for the four contacts

The high level of the three latter contacts are given by the equation

$$V_{high} = V_{CC} + 0.3\ V$$

which is in accordance to the acceptance criteria during certification testing discussed above. The highest value VCC can obtain without rising above its highest allowed value is 3.3 V. Thus the highest allowed voltage for the high state for these three contacts is 3.6 V.

As mentioned earlier the test sequences used for verification can be altered to suite the purpose, these tests should not be designed to test the extreme limits of the probe. The interesting signal range is the one that a mobile phone might lie within.

The same concept is then applied to the higher voltage trigger level and to the other contacts, resulting in a test structure that looks like this:

Contact	Voltage level	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6
C1 (VCC)	Low	1.674 V	1.667 V	1.632 V	1.608 V	1.574 V	1.566 V
	High	3.354 V	3.347 V	3.312 V	3.246 V	3.254 V	3.288 V
C2 (RST)	Low	54 mV	46 mV	17 mV	-17 mV	-46 mV	-54 mV
	High	3.654 V	3.647 V	3.617 V	3.546 V	3.554 V	3.583 V
C3 (CLK)	Low	54 mV	46 mV	17 mV	-17 mV	-46 mV	-54 mV
	High	3.654 V	3.647 V	3.617 V	3.546 V	3.554 V	3.583 V
C7 (I/O)	Low	54 mV	46 mV	17 mV	-17 mV	-46 mV	-54 mV
	High	3.654 V	3.647 V	3.617 V	3.546 V	3.554 V	3.583 V

Table 6: Suggested voltages for validation testing the voltage measurements of the probe

3.1.2 Rise time testing

This kind of testing is necessary for two of the contacts, C3 (CLK) and C7 (I/O). There is only one limit for the rise time measurements, the rise time cannot be too short, and this limit is the same for all operational modes, so only one test sequence per contact is necessary. Below the limits and uncertainties are repeated.

Contact	Max. allowed rise/fall time	Probe uncertainty	Max. allowed uncertainty
C3 (CLK)	50 ns	2.1 ns	5 ns
C7 (I/O)	1 µs	52 ns	100 ns

Table 7: Limits and uncertainties for rise time measurements

The uncertainty for the validation test equipment is assumed to be negligible. This assumption is not likely to be wrong, of course depending on which equipment is used. The reference equipment for this testing, NI PXI-5402, not the one used to approximate the uncertainty for the voltage testing, has a resolution of 14 bits and a maximum voltage range sensitivity of 41 mV, and as the voltage levels and frequency of the signal is of no importance to these tests and the signal to be constructed is periodical, the equipment performs with a good enough precision for the uncertainty of it to be neglected. The model used for the voltage testing sequence above is thus not applicable and the second step is merely taken as the median of the first and last step. The second step is not skipped as it still serves as an indicator when calibration is needed, but certification needs are still fulfilled.

Contact	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6
C3 (CLK)	55.0 ns	53.6 ns	52.1 ns	47.9 ns	46.5 ns	45.0 ns
C7 (I/O)	1.100 µs	1.076 µs	1.052 µs	0.948 µs	0.924 µs	0.900 µs

Table 8: Suggested rise times for validation tests

3.1.3 Cycle ratio and frequency testing

It is only for the clock signal; contact C3 that the cycle ratio and frequency measurements are carried out.

The specification require that the ratio lies between 40 % and 60 %, the probe uncertainty is 0.97 % and the maximum allowed uncertainty is 2.5 %. As for the rise time measurements the uncertainty of the test equipment is neglected and the same way to determine the second step is used. Then the test procedure would look as follows:

Contact	Level	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6
C3 (CLK)	Low	42.5 %	41.8 %	41.0 %	39.0 %	38.2 %	37.5 %
	High	62.5 %	61.8 %	61%	59%	58.2 %	57.5 %

Table 9: Suggested cycle ratios for validation test

For the frequency measurements it is a little different. As discussed earlier the probe does not have well enough accuracy for certification when the frequency lies over 3.86 MHz and the maximum allowed frequency is 5 MHz. This will be solved by focusing the high frequency measurements on the maximum frequency for Nokia mobile phones which is 3.8 MHz. Below the compiled information needed is shown.

Contact	Level	Frequency	Probe uncertainty	Maximum allowed uncertainty
C3 (CLK)	Low	1 MHz	1.3 ns (0.13 %)	0.5 %
	High	3.8MHz	1.3 ns (0.494 %)	0.5 %

Table 10: Maximum and minimum frequencies with their respective uncertainties

If the uncertainty of the test equipment is assumed to be negligible and the second step is again taken as the median of the extreme values this is the test structure that arises:

Contact	Level	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6
C3 (CLK)	Low	1.0050 MHz	1.0032 MHz	1.0013 MHz	0.9987 MHz	0.9968 MHz	0.9950 MHz
	High	3.7812 MHz	3.7811 MHz	3.7810 MHz	3.8190 MHz	3.8189 MHz	3.8188 MHz

Table 11: Suggested frequencies for validation testing of the probe

All of these timing measurements require a high precision on the test equipment. All of the uncertainties have been assumed to be negligible. This means that a lot of effort must be put into realizing these parts of the test equipment.

3.1.4 Current testing

As it cannot be found any maximum uncertainty requirements for the current testing on the I/O contact, this part of the validation test equipment will be considered to be redundant. This is fortified by the fact that there is no other contact where the current is being measured.

3.2 Measuring the signals from the probe

During all of the certification tests the probe should send some kind of signals to the device under test. The nominal test conditions are stated in table 1. For the main part these tests to assure that the probe in fact is sending the correct signals are quite straight forward, the current and resistive loads are more or less static.

3.2.1 Resistive loads

In the software of the IT^3 the loads are easily adjusted. If choosing to load the contacts resistively the following resistors will be connected permanently to the contacts [5]:

Contact:	VCC	RST	CLK	VPP	I/O
Resistance connected to VCC	No	No	No	No	No
Resistance connected to GND	10 kΩ	50 kΩ	50 kΩ	50 kΩ	50 kΩ
Tolerance: ±2 % (k=2)					

Table 12: Resistive loads

3.2.2 Current loads

There are three different kinds of current loads. First, the contact C1 (VCC) has two kinds of loads, one DC load and one current load from the spike generator and secondly the rest of the contacts have level dependent current loads. The various current spikes and the level dependent currents are stated in section 2.3. See table 13 below for the DC part [5].

VCC DC current load		
Range	1 – 100 mA	(resolution ca 25 µA/bit)
Accuracy	± 100 µA	For currents ≤ 45 mA
	± 250 µA	For currents ≤ 100 mA

Table 13: DC current loads

There are no maximum allowed uncertainties to be found for any of the DC currents or for the level dependent current loads, so these will not be tested as a part of the validation test procedure. For the current spikes these maximum allowed uncertainties are defined and looks as follows:

Continuous spikes		
		Maximum allowed uncertainty
Current load amplitude	0 mA - 20 mA	1 mA
Additional current offset	0 mA – 5 mA	1 mA
Random spikes		
		Maximum allowed uncertainty
Current load amplitude	50 mA – 200 mA	1 mA
Additional current offset	0 mA – 5 mA	0.1 mA

Table 14: Uncertainties allowed for current spike generator

The spikes are applied to the contact C1 (VCC) during the entire test case as long as the tested device is turned on. The criteria for this are that the clock of the device must be running and RST should be 1. The random pause duration of the latter part of the generated spikes is produced by a 13 bit shift register with feedback, giving a maximum of 8192 random value. The step size though is 0.1 ms, that is, the number of variations is mostly dependent on the range of the pulse variation.

A simplified approach to this part of the validation test could be to measure the maximum and minimum currents transmitted by the probe. The maximum current would give an assessment of the spikes generated and the minimum current would give an assessment of the additional current offset applied. This would of course not be a complete validation test, but it would give an indication of the condition of this part of the probe and should not be so intricate to realize.

4 Results

It is concluded that there are a number of validation tests that needs to be carried out in order to ensure that the functionality of the probe is adequate and these have been discussed in the previous section. In this section the configuration of the test equipment during the testing will be formed, i.e. which signals and loads that must be applied to the contacts of the SIMflex and how the settings of the IT^3 should be. All this will be structured as the actual test sequences needed to perform the validation test. The detailed programming of the test sequences can be found in Appendix C whilst here the idea behind the tests will be discussed.

The general test procedure will look like this:

- → Program IT^3
- → Program validation test equipment
- → Start validation test equipment
- → Start test sequence at IT^3
- → Stepwise change the output from the validation test equipment
- → Stop test sequence at IT^3
- → Stop validation test equipment
- → Compare actual results with expected results

The programming of the IT^3 will of course be done prior to test execution and saved as different test sequences.

4.1 Validation testing of the voltage measurement

During certification testing voltage measurements are carried out for all four contacts and when performing the validation test the voltage measurement equipment for the four contacts needs to be tested. Thus four different test sequences should be programmed and saved on the IT[3].

4.1.1 Programming for contact C1 (VCC)

The first contact to be tested is C1 (VCC). The programming for this contact is fairly simple. The class being used in this text is class D, although, as mentioned earlier, any of the available classes could be used. When taking all classes available for the mobile devices developed at Nokia into consideration, the voltage for this contact can lie between 1.62 V and 3.3 V. The thresholds $V_{th(min)}$ and $V_{th(max)}$ will be set to 1.62V and 3.3 V respectively. The value for V_{CC_log} needs to be set to a value lower than 1.574 V and is here chosen to be set to 1 V. The hysteresis will be kept at the default and minimum 9 mV to assure that the system obtains its highest sensitivity. As the changes in voltage will be done stepwise and then kept stable for a relatively long time, there is no need to set the trigger time to a higher value than 20 ms but there is also no problem in setting it to a higher value if so is desirable. If the validation test equipment shows signs of a toggling before settling to a fixed value then a higher trigger time could be helpful to avoid memory overflow.

4.1.2 Programming for contact C2 (RST), C3 (CLK) and C7 (I/O)

These three contacts will have pretty much equal test set ups. This is because they all have four programmable threshold levels; Low Min, Low Max, High Min and High Max. Additionally all three contacts have the same maximum and minimum level voltages, the same uncertainty in measurement and so they all possess the exact same voltages for all the twelve steps in the validation test sequence, see section 3.1.1 for details on the sequence.

The class used in this text will still be class D, thus all the thresholds set here are done for class D. For the voltage measurements on these contacts there are four thresholds that need to be set. The levels are designed to be V_{CC} independent thus not relying on the V_{CC} signal to be stable. The High Min and Low Max value should be set to a value that is lower than the minimum voltage used for the high level measurements and higher than the maximum voltage used for the low level measurements respectively. In this case the High Min should be lower than 3.546 V and is thus chosen to be set to 3.3 V and the Low Max level should be higher than 54 mV and the value chosen is 0.5 V. The two remaining levels are Low Min and High Max and it is those that should be used to set the limits for pass and fail. The Low min level will thus be set to 0 V and the High max is set to 3.6 V, in accordance to section 3.1.1.

Since there will be no measurements carried out on the current loads sent out by the probe these will be set to 0 A and the logical threshold is set to a value somewhere between the high and low level, it is here chosen to 1.8 V. Alternatively, if possible, the current load on the contacts is to be disabled altogether.

All that needs to be done now is activating the correct triggers. This is done by checking the boxes next to the Low min and High max threshold levels for the corresponding contact the test is intended for. If only one voltage source is to be in use the box corresponding to the specific contact under “Measurement start independent from VCC level” needs to be checked. For the contact C3 (CLK) there are three boxes here and only the one named “CLK” should be checked.

4.1.3 Validation test procedure

For each test sequence on the IT[3] there is to be programmed a corresponding sequence on the controlling device connected to the validation test equipment. This sequence will instruct the validation test equipment to stepwise change the output voltage with predefined time intervals. This will produce a structure that looks as follows:

→ Set the voltage to Step 1, low level

→ Timestamp #1: Start test case

→ Timestamp #2: Set the voltage to Step 2, low level

→ Timestamp #3: Set the voltage to Step 3, low level

→ Timestamp #4: Set the voltage to Step 4, low level

→ Timestamp #5: Set the voltage to Step 5, low level

→ Timestamp #6: Set the voltage to Step 6, low level

→ Timestamp #7: Set the voltage to Step 1, high level

→ Timestamp #8: Set the voltage to Step 2, high level

→ Timestamp #9: Set the voltage to Step 3, high level

→ Timestamp #10: Set the voltage to Step 4, high level

→ Timestamp #11: Set the voltage to Step 5, high level

→ Timestamp #12: Set the voltage to 6, high level

→ Timestamp #13: End test case

→ Turn off validation test equipment

→ Compare result output

The output from the IT[3] measurement system is to be compared with the expected output, depicted below on a time line, figure 15.

Expected:

Figure 15: Expected output from IT[3]

If there is a discrepancy in the result when compared to the expected, where this discrepancy lies determines what action, if any, must be taken.

- Between timestamp 3-4, 4-5, 9-10 or 10-11 → Signals the start of a drift. The probe is still good for certification and no immediate action is needed
- Between timestamp 2-3, 5-6, 8-9 or 11-12 → The probe is still good for certification but calibration is needed.
- Between timestamp 1-2, 6-8 or 12-13 → If the probe measures incorrectly here it cannot be used for certification any longer and the need for calibration is imminent.

4.2 Validation testing of the rise and fall time measurements

Validation testing of the rise and fall time are carried out for two of the contacts during certification testing, namely C3 (CLK) and C7 (I/O). As discussed in section 3.1.2, there is only an upper limit for the rise and fall time and thus fewer steps during the validation test sequence are needed.

Choosing the thresholds to be percentage dependant means that fixed thresholds will be calculated from the max low and min high levels for that specific contact. This means that when for this test the rise time will be measured from when the signal rises above 0.78 V until it rises above 3.02 V and vice versa for the fall time. However the signal behaves outside of this range is of no importance to the test verdict.

4.2.1 Validation test procedure

The test procedure will be the same for both contacts.

→ Set the waveform generator to produce a signal with a rise and/or fall time to Step 1

→ Timestamp #1: Start test case

→ Timestamp #2: Change the rise and/or fall time to pass Step 2

→ Timestamp #3: Change the rise and/or fall time to pass Step 3

→ Timestamp #4: Change the rise and/or fall time to fail Step 4

→ Timestamp #5: Change the rise and/or fall time to fail Step 5

→ Timestamp #6: Change the rise and/or fall time to fail Step 6

→ Timestamp #7: End test case

→ Turn off validation test equipment

→ Compare result output

The expected output is similar to the one expected during the voltage measurements, see figure 16. As for the voltage measurements there are different actions needed depending on where the probe is measuring incorrectly.

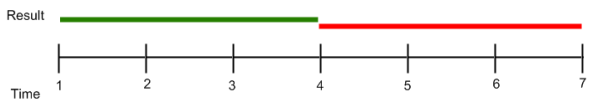

Figure 16: Expected output from rise/fall time measurement test

The actions needed are specified in equivalence to the ones from the voltage measurement tests.

If the discrepancy lies:

- Between timestamp 3-4 or 4-5 → Signals the start of a drift. The probe is still good for certification and no immediate action is needed
- Between timestamp 2-3 or 5-6 → The probe is still good for certification but calibration is needed.
- Between timestamp 1-2 or 6-7 → If the probe measures incorrectly here it cannot be used for certification any longer and the need for calibration is imminent.

4.3 Validation testing of the frequency and duty cycle measurements

The only contact concerning the frequency and duty cycle measurements is C3 (CLK). The IT^3 can measure the frequency by using the voltage levels max low and min high for the C3 contact. By taking the median value of these two it constructs a threshold used for measuring the frequency. It does this by measuring the time between two rising edges crossing this threshold and then inverting this period time to obtain the frequency, see figure 17.

In figure 17 it is also shown how the IT^3 calculates the duty cycle of the CLK signal, by measuring the time between a rising and a falling edge crossing the previously calculated threshold and dividing that time with the period time (between two rising edges).

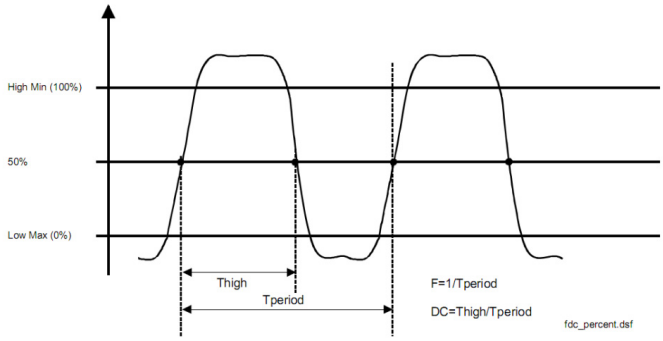

Figure 17: Frequency and duty cycle measurements of the CLK signal

4.3.1 Validation test procedure

For both the frequency and the duty cycle measurement tests the procedure will be the same. It is also the equivalent procedure as for the voltage measurement tests:

- → Set the frequency/duty cycle to Step 1, low level
- → Timestamp #1: Start test case
- → Timestamp #2: Set the frequency/duty cycle to Step 2, low level
- → Timestamp #3: Set the frequency/duty cycle to Step 3, low level
- → Timestamp #4: Set the frequency/duty cycle to Step 4, low level
- → Timestamp #5: Set the frequency/duty cycle to Step 5, low level
- → Timestamp #6: Set the frequency/duty cycle to Step 6, low level
- → Timestamp #7: Set the frequency/duty cycle to Step 1, high level
- → Timestamp #8: Set the frequency/duty cycle to Step 2, high level
- → Timestamp #9: Set the frequency/duty cycle to Step 3, high level
- → Timestamp #10: Set the frequency/duty cycle to Step 4, high level
- → Timestamp #11: Set the frequency/duty cycle to Step 5, high level
- → Timestamp #12: Set the frequency/duty cycle to Step 6, high level
- → Timestamp #13: End test case
- → Turn off validation test equipment
- → Compare result output

The output from the IT^3 measurement system is to be compared with the expected output, see figure 15. The interpretation of the difference between the expected and actual result is exactly the same as for the voltage measurement tests and can be found adjacent to figure 15.

4.4 Measuring the current spike generator

This part of the probe is likely to be the first to show signs of drifting, as the measurement part is more sustainable. Thus it is important to test this part.

There are four different types of accuracies that can be tested for the current loads on the C1 (VCC) contact. The spike generator is supposed to be able to generate two different types of spikes,

continuous and random, and it should at the same time be able to generate a DC current offset. For both types of current spikes there are maximum uncertainties defined, for the spikes as well as for the current offset, see section 3.2.2. For the continuous current spikes during certification testing the current amplitude, that is the spike amplitude plus the offset current, is always 12 mA. The random current spikes can have total amplitude of 30 mA or 60 mA and the current offset for both types of current spikes is either 0 mA or 3 mA. See Appendix B for details of the applied current spikes.

To be able to carry out these tests three signals must be transmitted from the validation test equipment, namely a valid clock signal, a valid VCC signal and the reset signal must be high. If these three signals are not present, the spike generator will not be running. The IT^3 assures that this is the case by using three triggers associated to the three signals, these are VCC_VALID, RST_LOG and CLOCK_STOP. When VCC_VALID and RST_LOG is 1 and CLOCK_STOP is 0, the spike generator will be activated. This means that the voltage limits for the VCC and RST signals must be specified in the IT^3 and for the CLK signal there must be a Threshold and a Clock stop time set, see figure 20.

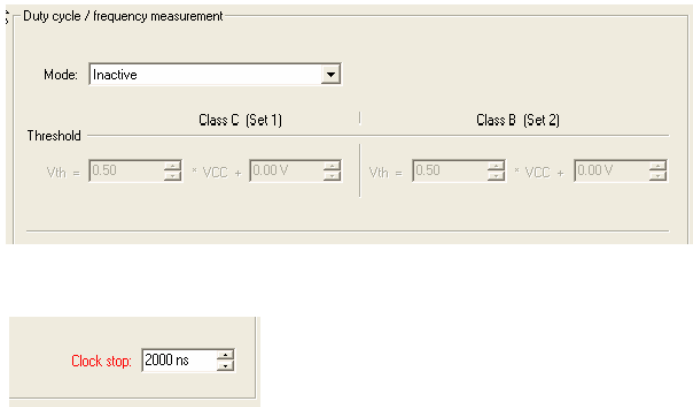

Figure 20: Top: Threshold setting. Bottom: Clock stop setting. Both are used for generation of the CLOCK_STOP signal

As seen in the figure above, the duty cycle and frequency measurements are not activated, and that should also be the case when testing the spike generator. The threshold defined for these measurements are still the threshold used for generating the CLOCK_STOP trigger signal. Whenever the CLK signal rises above this threshold, the CLOCK_STOP is set to low (clock is running) and at the same time a timer is started and if there is no further positive edge crossing the threshold within the specified clock stop time, the trigger signal CLOCK_STOP turns high, indicating that the clock is not running, the spike generator is disabled and all current loads are switched to their idle current settings [5].

4.4.1 Validation test procedure

When all the settings are done to enable the current spike generator to run during the test case it is time to consider the spike generator settings. There will be five different scenarios tested; these are compiled in table 15 below. These are the same spikes that are applied during certification tests.

Test scenario	Type of spikes	Spike amplitude	Offset current
1	Continuous	12 mA	0 mA
2	Continuous	9 mA	3 mA
3	Random	60 mA	0 mA
4	Random	30 mA	0 mA
5	Random	57 mA	3 mA

Table 15: The five different test scenarios for the current spike generator testing

For each of the five validation tests the current generated by the IT^3 will be measured by the validation test equipment and the current will be analyzed by the controlling software, which will produce a failing or passing verdict.

When measuring the current there are two states to take into consideration, the low state in the pause duration and the high state, which is when the spike is being applied. This introduces some complications as the current will rise above the maximum allowed low current and it will fall below the minimum allowed high current when changing from one state to the other, see figure 18.

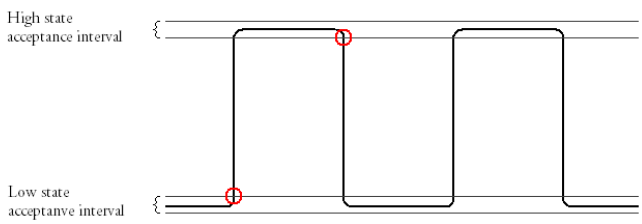

Figure 18: Current falls outside acceptance interval whenever a change of states occurs

One way to avoid this being falsely interpreted as a faulty current sent out by the IT^3 is by applying the following state chart, figure 19:

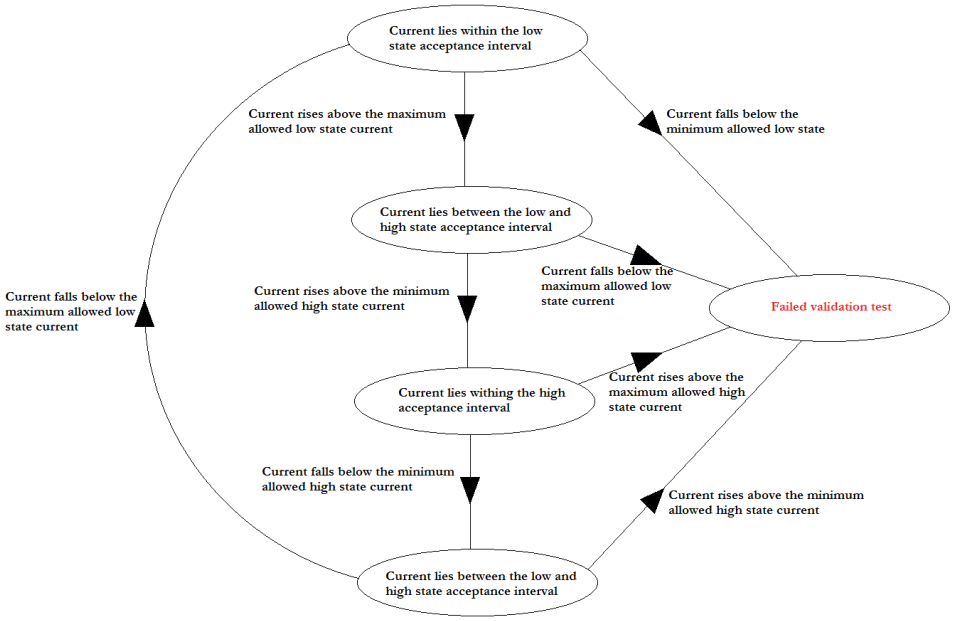

Figure 19: State chart applicable on the current measurements

That is, if the current is in the low state and rises above the maximum limit of the low state and then falls beneath the maximum allowed low state current without first rising to the high state, a fail is generated. In the same way if the current is in the high state and falls below the minimum allowed high state current it might just be on its way to change state, so if the current falls below the maximum allowed current for the low state there is no fail generated, but if it rises above the minimum allowed high state current instead, a fail is generated. The same principle is used in the IT^3, called burst detection [5].

Consideration must also be taken to the accuracy of the current measurement device chosen to be implemented. To void this uncertainty being able to cause false measurements I would recommend including a hysteresis slightly higher than the measurement uncertainty of the device.

In the case of selecting the simplified and less thorough solution by just measuring the maximum and minimum current transmitted, two scenarios should be adequate. A suggested set up of these two would be:

Test scenario	Type of spikes	Spike amplitude	Offset current
1	Continuous	0 mA	5 mA
2	Random	60 mA	0 mA

Table 16: The two test scenarios suggested for the simplified validation test solution

In the first scenario the offset current is primarily measured and in the second scenario both the spike generator and the current offset is measured. The validation test would fail if the minimum and maximum current measured is not between 4 mA and 6 mA for scenario 1 and it would also fail if the minimum current is not between -0.1 mA and +0.1 mA and the maximum current is not between 59 mA and 61 mA for scenario 2. As in the other validations tests, it might of course be of interest to give an indication if the probe is starting to drift; in that case a warning could be generated if the measured current is off by 0.5 mA.

5 Discussion

During the process of writing this thesis I have studied the test specifications [3] and identified the relevant measurements the probe performs as well as which emitted signals that are of interest to verify. With these signals in mind I then studied the system specifications [2] to determine for which signals there are accuracies specified and what the accuracies are required, for both the measurements performed by the probe and the generated signals. To design a validation test procedure that verified the validity of the certification performed at the laboratory at Nokia I combined my findings from the previously mentioned studies with the characteristics of the mobile devices produced by Nokia. This concluded in what I have described in section 3. Below are the compiled findings of these studies

Contact	Parameter	Measured/ Generated	Range	Required accuracy
C1 (VCC)	Voltage	M	1.62 V – 3.3 V	±50 mV
	Current	G	0 mA – 60 mA	±0.1 / ±1 mA
C2 (RST)	Voltage	M	0 V – 3.6 V	±50 mV
C3 (CLK)	Voltage	M	0 V – 3.6 V	±50 mV
	Rise/Fall time	M	< 50 ns	±5ns
	Cycle ratio	M	40 % - 60 %	±2.5 %
	Frequency	M	1 MHz – 3.8 MHz	±0.5 %
C7 (I/O)	Voltage	M	0 V – 3.6 V	±50 mV
	Rise/Fall time	M	< 1 µs	±100 ns

Table 16: Relevant parameters and their respective range and allowed accuracies

The next step was then to understand the IT^3 test system [5] and the possibilities there are to design customized test sequences and also what limitations there are. My findings of these studies (see section 2.2 and section 2.5) together with which tests were necessary resulted in the spine of what later evolved into the different test sequences I have described in section 4. But before these test sequences could become reality the uncertainty of the probe and the IT^3 system had to be identified. Even during the best circumstances, a newly calibrated probe suffers from some measurement uncertainty and this need to be taken into consideration when constructing the test sequences. These uncertainties are well known by Comprion and they can be found in table 1, section 2.2.1.

Now I needed some idea of what kind of uncertainties would be introduced by the validation test equipment, so the next challenge was to determine what demands my findings put on the validation test equipment that was going to be used in the verification testing, and thus finding out what kind of uncertainties this kind of equipment might inherit. A discussion was then started with Jaako Kerula from National Instruments and the outcome was a proposal using their equipment. This might not be the equipment that eventually will be put to use for this task, but it gave me an idea of what I might expect performance wise from this kind of equipment. In Appendix D the specifications for NI PXI-6221 are stated. An additional search of components from other manufacturers gave the approximately the same conclusion, at least regarding the accuracy for the voltage generator. This was not the tricky part, though. Finding an arbitrary function generator with good enough characteristics without ending up with a over the top sophisticated piece of equipment was. Apart from the frequency also the rise and/or fall time must be adjustable as well as the duty cycle. Generators that were able to do the two latter often lacked the frequency range needed.

The suggested solution from National Instruments would also solve the current measurement part of the test equipment. The input voltage range is -10 V to 10 V and the measurement accuracy is 3100 µV. Converting this to be applicable on the current measurement, taking the current range of the spikes, 0 – 60 mA, the accuracy would be approximately 20 µA. It also has a high sampling rate of 250 kS/s and a 16 bit resolution, thus providing adequate measurement capability for performing the validation measurements of the current spikes on contact C1.

For all of the performed tests during the validation test noise is a major factor. For the validation test to be as reliable as possible the reduction of noise must be high. This means proper shielding of the probe and the validation test equipment during testing.

If the choice is made not to use the equipment from NI but rather construct custom validation test equipment costs could be cut substantially but a lot of work has to be put in the construction of such equipment. It should not be hard to find fitting voltage generators, with good enough characteristics at a reasonable cost, the main problems are to find a function generator and a current measurement device that are good enough. By choosing two function generators, one that has the requested frequency range and one that has the possibility to set duty cycle and rise and/or fall time, rather than one that has the capability of both, could be a good way to get around a big part of this problem. One cost cutting solution for the latter generator is to find a generator that is able to generate triangle and/or saw tooth signals. By setting the trigger levels and the output amplitude and offset, the requested rise time and duty cycle can be obtained, see figure 20 and 21 for graphical representations.

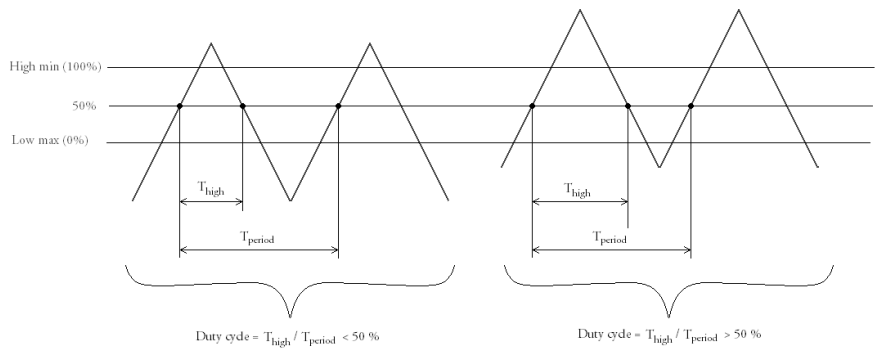

Figure 20: Obtaining adjustable duty cycle through changing offset of a triangle wave

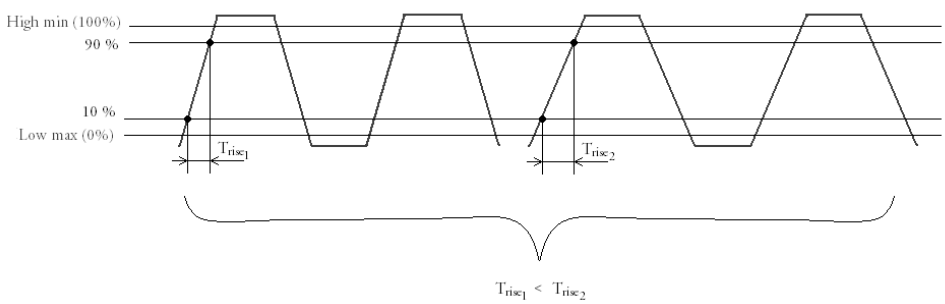

Figure 21: Obtaining adjustable rise (and fall) time through changing amplitude of triangle wave

The triangle wave used for the setting the rise and fall time in figure 21 has been clipped so that there is no risk of exceeding the input voltage range of the probe. The same can of course be done to the triangle wave used to obtain the desired duty cycle, although I do not think it to be necessary.

For the current measuring part it is my suggestion to, at least as a first step, choose the simplified solution. This would significantly lower the cost of the equipment and make testing faster and easier to realize.

There is still the need to ensure that the validation test equipment in its turn is still reliable. It is my suggestion that this it done just after the probe has returned from calibration at the manufacturers. At this time all the validation tests should pass, and if there are any errors these should be addressed and investigated. This might mean that the validation test equipment needs to be calibrated and the cost and ease of this is of course dependent upon which solution you choose. A COTS solution might provide these kinds of calibrations, whereas manually constructed equipment might be easier to calibrate in house if needed.

Regardless of which solution is selected to be implemented, the confidence in the certification testing equipment will be highly improved and the testing even more reliable.

6 References

[1] *An Introduction to GSM*, Siegmund M. Redl, Matthias K. Weber, Malcolm W. Oliphant

[2] *ISO/IEC 7816-3, third edition*

[3] *ETSI TS 102 230 V5.7.0*

[4] *3GPP TS 51.010-1 V7.11.0 2008-09 annex A5.4.2.1 Default measurement / setting uncertainties*

[5] *Understanding the IT³ – document provided by Comprion and can be found in Appendix A.*

[6] *IT³ Analog Simulator - Specification of measurement uncertainties*

7 Appendix

7.1 Appendix B

Current spikes applied to contact VCC during test

1) continuous spikes:
   - current amplitude 12 mA;
   - current offset 0 mA;
   - duration 100 ns;
   - pause 100 ns.
2) continuous spikes:
   - current amplitude 12 mA;
   - current offset 0 mA;
   - duration 400 ns;
   - pause 400 ns.
3) continuous spikes:
   - current amplitude 9 mA;
   - current offset 3 mA;
   - (i.e. maximum amplitude = 3 mA + 9 mA = 12 mA);
   - duration 150 ns;
   - pause 300 ns.
4) random spikes:
   - current amplitude 60 mA;
   - current offset 0 mA;
   - duration 200 ns;
   - pause between 0.1 ms and 500 ms, randomly varied.
5) random spikes:
   - current amplitude 30 mA;
   - current offset 0 mA;
   - duration 400 ns;
   - pause between 0.1 ms and 500 ms, randomly varied.
6) random spikes:
   - current amplitude 57 mA;
   - current offset 3 mA;
   - (i.e. maximum amplitude = 3 mA + 57 mA = 60 mA);
   - duration 200 ns;
   - pause between 0.1 ms and 500 ms, randomly varied.

For each test case, only one type of spikes is applied. The spike duration is specified to be measured at 50 % of the spike amplitude.

7.2 Appendix C

Voltage test C1 (VCC)

→ Choose class D

→ Set Vth(min) to 1.62 V

→ Set Vth(max) to 3.3 V

→ Set Vcc_Log to 1 V

→ Set the voltage source connected to the C1 contact on the test equipment to 1.566 V (fail step 3)

→ Timestamp #1: Start test case

→ Timestamp #2: Set voltage to 1.574 V (fail)

→ Timestamp #3: Set voltage to 1.608 V (fail)

→ Timestamp #4: Set voltage to 1.632 V (pass)

→ Timestamp #5: Set voltage to 1.667 V (pass)

→ Timestamp #6: Set voltage to 1.674 V (pass)

→ Timestamp #7: Set voltage to 3.246 V (pass)

→ Timestamp #8: Set voltage to 3.254 V (pass)

→ Timestamp #9: Set voltage to 3.288 V (pass)

→ Timestamp #10: Set voltage to 3.312 V (fail)

→ Timestamp #11: Set voltage to 3.347 V (fail)

→ Timestamp #12: Set voltage to 3.354 V (fail)

→ Timestamp #13: End test case

→ Turn off test equipment

→ Compare result output

Voltage test C2 (RST)

→ Choose class D

→ Set Vth(min) to 1.62 V

→ Set Vth(max) to 3.3 V

→ Set Vcc_Log to 1 V

→ For the Class D RST-signal thresholds set:

- High max to 0*Vcc + 3.6 V
- High min to 0*Vcc + 3.3 V
- Low max to 0*Vcc + 0.5 V
- Low min to 0*Vcc + 0 V
- Current load adjustment:
  - High and low value to 0 A
  - Logical threshold Vth to 1.8 V

→ Check the boxes for High max and Low min, thus activating them

→ Check the box for starting testing on the RST contact independent from Vcc level

→ Set the voltage source connected to the C2 contact on the test equipment to -54 mV (fail step 3)

→ Timestamp #1: Start test case

→ Timestamp #2: Set voltage to -46 mV (fail)

→ Timestamp #3: Set voltage to -17 mV (fail)

→ Timestamp #4: Set voltage to 17 mV (pass)

→ Timestamp #5: Set voltage to 46 mV (pass)

→ Timestamp #6: Set voltage to 54 mV (pass)

→ Timestamp #7: Set voltage to 3.546 V (pass)

→ Timestamp #8: Set voltage to 3.554 V (pass)

→ Timestamp #9: Set voltage to 3.583 V (pass)

→ Timestamp #10: Set voltage to 3.617 V (fail)

→ Timestamp #11: Set voltage to 3.647 V (fail)

→ Timestamp #12: Set voltage to 3.654 V (fail)

→ Timestamp #13: End test case

→ Turn off test equipment

→ Compare result output

Voltage test C3 (CLK)

→ Choose class D

→ Set Vth(min) to 1.62 V

→ Set Vth(max) to 3.3 V

→ Set Vcc_Log to 1 V

→ For the Class D CLK-signal thresholds set:

- High max to 0*Vcc + 3.6 V
- High min to 0*Vcc + 3.3 V
- Low max to 0*Vcc + 0.5 V
- Low min to 0*Vcc + 0 V
- Current load adjustment:
  - High and low value to 0 A
  - Logical threshold Vth to 1.8 V

→ Check the boxes for High max and Low min, thus activating them

→ Check the box for starting testing on the CLK contact independent from Vcc level

→ Set the voltage source connected to the C3 contact on the test equipment to -54 mV (fail step 3)

→ Timestamp #1: Start test case

→ Timestamp #2: Set voltage to -46 mV (fail)

→ Timestamp #3: Set voltage to -17 mV (fail)

→ Timestamp #4: Set voltage to 17 mV (pass)

→ Timestamp #5: Set voltage to 46 mV (pass)

→ Timestamp #6: Set voltage to 54 mV (pass)

→ Timestamp #7: Set voltage to 3.546 V (pass)

→ Timestamp #8: Set voltage to 3.554 V (pass)

→ Timestamp #9: Set voltage to 3.583 V (pass)

→ Timestamp #10: Set voltage to 3.617 V (fail)

→ Timestamp #11: Set voltage to 3.647 V (fail)

→ Timestamp #12: Set voltage to 3.654 V (fail)

→ Timestamp #13: End test case

→ Turn off test equipment

→ Compare result output

Voltage test C7 (I/O)

→ Choose class D

→ Set Vth(min) to 1.62 V

→ Set Vth(max) to 3.3 V

→ Set Vcc_Log to 1 V

→ For the Class D I/O-signal thresholds set:

- High max to 0*Vcc + 3.6 V
- High min to 0*Vcc + 3.3 V
- Low max to 0*Vcc + 0.5 V
- Low min to 0*Vcc + 0 V
- Current load adjustment:
  - High and low value to 0 A
  - Logical threshold Vth to 1.8 V

→ Check the boxes for High max and Low min, thus activating them

→ Check the box for starting testing on the I/O contact independent from Vcc level

→ Set the voltage source connected to the C7 contact on the test equipment to -54 mV (fail step 3)

→ Timestamp #1: Start test case

→ Timestamp #2: Set voltage to -46 mV (fail)

→ Timestamp #3: Set voltage to -17 mV (fail)

→ Timestamp #4: Set voltage to 17 mV (pass)

→ Timestamp #5: Set voltage to 46 mV (pass)

→ Timestamp #6: Set voltage to 54 mV (pass)

→ Timestamp #7: Set voltage to 3.546 V (pass)

→ Timestamp #8: Set voltage to 3.554 V (pass)

→ Timestamp #9: Set voltage to 3.583 V (pass)

→ Timestamp #10: Set voltage to 3.617 V (fail)

→ Timestamp #11: Set voltage to 3.647 V (fail)

→ Timestamp #12: Set voltage to 3.654 V (fail)

→ Timestamp #13: End test case

→ Turn off test equipment

→ Compare result output

Rise/Fall time test C3 (CLK)

→ Choose class D

→ Set Vth(min) to 1.62 V

→ Set Vth(max) to 3.3 V

→ Set Vcc_Log to 1 V

→ For the Class D CLK-signal thresholds set:

- High max to 0*Vcc + 3.6 V
- High min to 0*Vcc + 3.3 V
- Low max to 0*Vcc + 0.5 V
- Low min to 0*Vcc + 0 V
- Current load adjustment:
  - High and low value to 0 A
  - Logical threshold Vth to 1.8 V

→ Set maximum rise/fall time value for the CLK signal to 50 ns

→ Set the thresholds to be percentage dependant

→ Check the boxes for maximum rise/fall time values, thus activating that trigger

→ Check the box for starting testing CLK rise/fall time independent from Vcc level

→ Set the waveform generator to produce a signal with a rise and/or fall time of 45 ns (pass)

→ Timestamp #1: Start test case

→ Timestamp #2: Change the rise and/or fall time to 46.5 ns (pass)

→ Timestamp #3: Change the rise and/or fall time to 47.9 ns (pass)

→ Timestamp #4: Change the rise and/or fall time to 52.1 ns (fail)

→ Timestamp #5: Change the rise and/or fall time to 53.6 ns (fail)

→ Timestamp #6: Change the rise and/or fall time to 55.0 ns (fail)

→ Timestamp #7: End test case

→ Turn off test equipment

→ Compare result output

Rise/Fall time test C7 (I/O)

→ Choose class D

→ Set Vth(min) to 1.62 V

→ Set Vth(max) to 3.3 V

→ Set Vcc_Log to 1 V

→ For the Class D I/O-signal thresholds set:

- High max to 0*Vcc + 3.6 V
- High min to 0*Vcc + 3.3 V

- Low max to 0*Vcc + 0.5 V
- Low min to 0*Vcc + 0 V
- Current load adjustment:
    - High and low value to 0 A
    - Logical threshold Vth to 1.8 V

→ Set maximum rise/fall time value for the I/O signal to 1000 ns (1 µs)
→ Set the thresholds to be percentage dependant
→ Check the boxes for maximum rise/fall time values, thus activating that trigger
→ Check the box for starting testing I/O rise/fall time independent from Vcc level
→ Set the waveform generator to produce a signal with a rise and/or fall time of 0.900 µs (pass)
→ Timestamp #1: Start test case
→ Timestamp #2: Change the rise and/or fall time to 0.924 µs (pass)
→ Timestamp #3: Change the rise and/or fall time to 0.948 µs (pass)
→ Timestamp #4: Change the rise and/or fall time to 1.052 µs (fail)
→ Timestamp #5: Change the rise and/or fall time to 1.076 µs (fail)
→ Timestamp #6: Change the rise and/or fall time to 1.100 µs (fail)
→ Timestamp #7: End test case
→ Turn off test equipment
→ Compare result output

Frequency test C3 (CLK)

→ Choose class D
→ Set Vth(min) to 1.62 V
→ Set Vth(max) to 3.3 V
→ Set Vcc_Log to 1 V
→ For the Class D CLK-signal thresholds set:
    - High max to 0*Vcc + 3.6 V
    - High min to 0*Vcc + 3.3 V
    - Low max to 0*Vcc + 0.5 V
    - Low min to 0*Vcc + 0 V
    - Current load adjustment:
        - High and low value to 0 A
        - Logical threshold Vth to 1.8 V
→ Choose the percentage threshold mode
→ Set minimum frequency to 1.00 MHz and maximum frequency to 3.8 MHz
→ Check the box for frequency measurement to activate that trigger
→ Check the box for starting testing CLK frequency/duty cycle independent from Vcc level
→ Set the waveform generator to produce a signal with a frequency of 0.9950 MHz (fail)
→ Timestamp #1: Start test case

→ Timestamp #2: Set the frequency to 0.9968 MHz (fail)
→ Timestamp #3: Set the frequency to 0.9987 MHz (fail)
→ Timestamp #4: Set the frequency to 1.0013 MHz (pass)
→ Timestamp #5: Set the frequency to 1.0032 MHz (pass)
→ Timestamp #6: Set the frequency to 1.0050 MHz (pass)
→ Timestamp #7: Set the frequency to 3.7810 MHz (pass)
→ Timestamp #8: Set the frequency to 3.7811 MHz (pass)
→ Timestamp #9: Set the frequency to 3.7812 MHz (pass)
→ Timestamp #10: Set the frequency to 3.8188 MHz (fail)
→ Timestamp #11: Set the frequency to 3.8189 MHz (fail)
→ Timestamp #12: Set the frequency to 3.8190 MHz (fail)
→ Timestamp #13: End test case
→ Turn off test equipment
→ Compare result output

Duty cycle test C3 (CLK)

→ Choose class D
→ Set Vth(min) to 1.62 V
→ Set Vth(max) to 3.3 V
→ Set Vcc_Log to 1 V
→ For the Class D CLK-signal thresholds set:
    - High max to 0*Vcc + 3.6 V
    - High min to 0*Vcc + 3.3 V
    - Low max to 0*Vcc + 0.5 V
    - Low min to 0*Vcc + 0 V
    - Current load adjustment:
        - High and low value to 0 A
        - Logical threshold Vth to 1.8 V
→ Choose the percentage threshold mode
→ Set minimum duty cycle to 1.00 MHz and maximum duty cycle to 5.00 MHz
→ Check the box for duty cycle measurement, activating that trigger
→ Check the box for starting testing CLK frequency/duty cycle independent from Vcc level
→ Set the waveform generator to produce a signal with a duty cycle of 37.5 % (fail)
→ Timestamp #1: Start test case
→ Timestamp #2: Set the duty cycle to 38.2 % (fail)
→ Timestamp #3: Set the duty cycle to 39.0 % (fail)
→ Timestamp #4: Set the duty cycle to 41.0 % (pass)
→ Timestamp #5: Set the duty cycle to 41.8 % (pass)
→ Timestamp #6: Set the duty cycle to 42.5 % (pass)
→ Timestamp #7: Set the duty cycle to 57.5 % (pass)

→ Timestamp #8: Set the duty cycle to 58.2 % (pass)

→ Timestamp #9: Set the duty cycle to 59 % (pass)

→ Timestamp #10: Set the duty cycle to 61 % (fail)

→ Timestamp #11: Set the duty cycle to 61.8 % (fail)

→ Timestamp #12: Set the duty cycle to 62.5 % (fail)

→ Timestamp #13: End test case

→ Turn off test equipment

→ Compare result output

Testing the current spikes

→ Choose class D

→ Set Vth(min) to 1.62 V

→ Set Vth(max) to 3.3 V

→ Set Vcc_Log to 1 V

→ For the Class D CLK-signal thresholds set:

- High max to 0*Vcc + 3.6 V
- High min to 0*Vcc + 3.3 V
- Low max to 0*Vcc + 0.5 V
- Low min to 0*Vcc + 0 V
- Current load adjustment:
  - High and low value to 0 A
  - Logical threshold Vth to 1.8 V

→ For the Class D RST-signal thresholds set:

1) High max to 0*Vcc + 3.6 V
2) High min to 0*Vcc + 3.3 V
3) Low max to 0*Vcc + 0.5 V
4) Low min to 0*Vcc + 0 V
5) Current load adjustment:
   - High and low value to 0 A
   - Logical threshold Vth to 1.8 V

→ In the duty cycle/frequency measurement settings for class D, set the threshold to 0*Vcc + 1.8 V

→ Set Clock stop to 5000ns (clock must run higher than 200 khz)

→ Set up the current spike generator for class D with one of the following test scenarios:

1) DC: 0 mA

   Choose continuous spikes

   Pause duration: 250 ms

   Pulse (max): 12 mA

   Duration: 250 ms

   Rise/Fall-time: 50 ns

2) DC: 3 mA

   Choose continuous spikes

   Pause duration: 250 ms

   Pulse (max): 9 mA

   Duration: 250 ms

   Rise/Fall-time: 50 ns

3) DC: 0 mA

   Choose random spikes

   Pause duration, max: 250 ms, min: 0.1 ms

   Pulse (max): 30 mA

   Duration: 250 ms

   Rise/Fall-time: 50 ns

4) DC: 0 mA

   Choose random spikes

   Pause duration, max: 250 ms, min: 0.1 ms

   Pulse (max): 60 mA

   Duration: 250 ms

   Rise/Fall-time: 50 ns

5) DC: 3 mA

   Choose random spikes

   Pause duration, max: 250 ms, min: 0.1 ms

   Pulse (max): 57 mA

   Duration: 250 ms

   Rise/Fall-time: 50 ns

→ Set the voltage source connected to the C2 contact on the test equipment to 3.45 V (high)

→ Set the waveform generator to produce a clock signal with a frequency of 2 MHz and an amplitude of (3.45 – 1.8) V and an offset of 1.8 V

→ Set the voltage source connected to the C1 contact on the test equipment to 2.46 V

→ Start test case

→ Run for a few seconds

→ Stop test case

→ The result will be generated by the controlling software

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