

A Linear, Wide-band, Low-Power Receiver for Narrowband- Internet of Things (NB-IoT)

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MASTER'S THESIS

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Abstract

Advancement of technology with the aid of new application, wireless communication has grown rapidly in the past two decades. Recently, in the wireless communication industry, Narrowband- Internet of Things (NB-IoT) is being discussed by everyone, as the most important emerging technology of the day. Being a wireless technology, owing to the exodus of devices to be connected, with due consideration to the data transfer requirements, and spectrum allowances, the 3rd Generation Partnership Project (3GPP) have standardized the technology with a list of specifications. In this thesis, a comprehensive study is conducted to find the most promising receiver front end architectures for an NB-IoT User Equipment (UE) which is highly integrable, has the least DC power consumption at its best performance and has the least price per unit.

For NB-IoT, the 3GPP standard mandates the requirement of a receiver front end to be capable of tuning to signals within the frequency range 450MHz to 2200MHz, thus necessitating it to wide-band reception with better selectivity. By emphasizing upon the reduction of price per device demands, comparing the characteristic trade-offs of the various architectures, analysis of the typical receiver's non-ideal factors and considering the specifications and requirements, an inductor-less, external Surface Acoustic Wave (SAW) filter-less Direct Conversion Receiver (DCR) has been chosen as the potential candidate.

The study reveals that the Frequency Translational Noise Canceling (FTNC) receiver front end and gain switching receiver front end stand as the most promising receiver topologies. The former, with its two modes of operation, saves DC power, displays a decent linearity performance and a relaxed trade-off between noise figure and linearity; while the latter has the advantage of variable gain control at RF which supports lower DC power consumption in the presence of large wanted signal without compromising largely on noise figure. The simulated DC power consumption for each of the architectures have a maximum of 40mW at their best performance with DSB noise figure \approx 2dB, impedance matching <-15 dB, <-70 dBm spurious emission from LO divider circuits, and 3rd order harmonic rejection >40 dB. The study is conducted in 40nm CMOS technology.

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Popular Science Summary

Internet of Things (IoT) is a network constituted by uniquely identifiable material objects or devices equipped with some kind of physical sensing system. IoT standard enables the objects, otherwise called things, for sensing, which subsequently inter-operate and communicate with other objects for data and information exchange through an existing physical network infrastructure. Therefore, IoT promotes a seamless connection between the smart devices, which scatter everywhere around us, and the physical world to ensure full automation that eventually improves human lifestyle. Some examples of IoT-enabled material devices include heart monitoring implants, automobiles with embedded sensors, firefighter devices, smart thermostat systems, and Wireless Fidelity (Wi-Fi) enabled washer/dryers, to name a few. As the platform of IoT is expanding, the number of IoT-enabled applications is also rapidly growing, which also results in large scale growth of smart devices. This swift increase in the number of sensing things generates diverse data and storage at much faster rate becomes essential [1].

The ambitious nature of such a technology demands a robust system to transfer the acquired data wirelessly to the backbone network. The problem has been addressed with the Narrow-band Internet of Things (NB-IoT) standard in the 3rd Generation Partnership Project (3GPP) Long Term Evolution (LTE) Release 13 which standardizes the technology for providing wide area connectivity for massive Machine-type communications (MTC) for IoT. NB-IoT is a cellular radio access technology that provides Low-power wide-area (LPWA) IoT connectivity in licensed spectrum, unlike short-range technologies in unlicensed spectrum, including Bluetooth, ZigBee, and so on, and unlike LPWA technologies including Sig-Fox, Long Range Wide Area Network (LoRaWAN), and so on. The 3GPP design targets for Release 13 were those typical for MTC: long device battery life, low device complexity to ensure low cost, support for massive numbers of devices, and coverage enhancements to be able to reach devices in basements and other challenging locations [2].

NB-IoT significantly improves the power/energy requirements of user devices, system capacity and spectrum efficiency, especially in deep coverage. The need

for reducing the cost for these remotely stationed peer devices also demands a reduction in their operation cost. This is possible if the overall power consumption of the devices could be limited to a minimum operating value, maximizing the overall time of its operation with a one charge battery pack. This reflects a low power operation with a substantial need to reduce the power of the radio module of these devices. All this should be done without compromising on the performance of the circuits, while following the 3GPP defined specifications. Consequently, the development of highly linear, wide-band, low power wireless receiver is required to cater to the flexibility, cost and use case scenarios of such a system in a real world.

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List of Acronyms

3GPP	3 rd Generation Partnership Project
A/D	Analog-to-digital
AC	Alternating Current
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AM	Amplitude modulated
BB	Base-Band
BPF	Band pass filter
CM	Common Mode
CMFB	Common Mode Feedback
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CP1dB	1dB Compression point
CSF	Channel-select-filter
DC	Direct Current
DCR	Direct Conversion Receiver
DM	Difference Mode
FTNC	Frequency Translational Noise Canceling
GBW	Gain Bandwidth Product

HB	Harmonic Balance
HBAC	Harmonic Balance AC
HBNOISE	Harmonic Balance Noise
HBSP	Harmonic Balance S-parameter
HRM	Harmonic Rejection Mixer
I	In-phase
IB	In-Band
IF	Intermediate frequency
IIP2	Input referred 2 nd order intercept point
IIP3	Input referred 3 rd order intercept point
IM3	3 rd order inter-modulation
IoT	Internet of Things
IP2	2 nd order intercept point
IP3	3 rd order intercept point
LNA	Low Noise Amplifier
LNTA	Low Noise Transconductance Amplifier
LO	Local Oscillator
LoRaWAN	Long Range Wide Area Network
LPWA	Low-power wide-area
LTE	Long Term Evolution
MTC	Machine-type communications
NB-IoT	Narrowband- Internet of Things
NC-LNA	Noise Canceling- Low Noise Amplifier
NC-LNTA	Noise Canceling- Low Noise Transconductance Amplifier
NF	Noise Figure
OB	Out-Band
OP-amp	Operational Amplifier
PAC	Periodic AC
PNOISE	Periodic Noise
PSP	Periodic S-parameter

PSS	Periodic Steady State
PSTB	Periodic Stability
PXF	Periodic Transfer Function
Q	Quadrature-phase
QPAC	Quasi-Periodic AC
QPSP	Quasi-Periodic S-parameter
QPSS	Quasi-Periodic Steady State
QPXF	Quasi-Periodic Transfer Function
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RX	Receiver
S11	Input reflection coefficient
SAW	Surface Acoustic Wave
SDR	Software-defined radio
SNR	Signal-to-noise-ratio
STB	Stability
TIA	Trans-Impedance Amplifier
TRAN	Transient
TT	Typical-Typical
UE	User Equipment
VCO	Voltage Controlled Oscillator
Wi-Fi	Wireless Fidelity
x-coupled	Cross-coupled
XF	Transfer Function

Introduction

Communication and exchange of information has always been an important part of modern day human life. Wireless communication has become the modern day normality because of its reliability and operational efficiency. This has given birth to different forms of technology ranging from a simple wireless pager to the high data traffic bearing mobile communications. Internet of Things (IoT) is the latest emerging concept in this domain where an ambitious amount of physical day to day articles are provided with sensors and small processors, and a wireless interface to talk to others. The wireless communication techniques used in such devices are standardized as User Equipment (UE) category NB1 in the 3rd Generation Partnership Project (3GPP) Long Term Evolution (LTE) release 13 with a list of specifications in order to enhance its operating life, reduce power consumption and thereby the cost.

IoT idea has got boosted up in the recent years. With IoT, everything in the human environment from the kitchen appliances to the industrial equipment could be equipped with sensors and processors that can exchange data and help in the maintenance and coordination of tasks. For this, it requires transmitters that are powerful enough to broadcast to devices that are tens of meters away and are energy efficient enough to last for months or even years. Similarly, the receivers equipped in these devices should be capable to give a good performance while maintaining low power consumption.

1.1 Motivation

Narrow-band Complementary Metal Oxide Semiconductor (CMOS) receiver front-ends invariably make use of external RF filtering to meet the stringent blocking conditions. But these external filters are bulky and expensive, obstructs front end flexibility, increases the handset form factor, bill of materials and cost [11]. Since RF filters are almost always fixed, multiple filters are required to cover the large number of frequency bands serviced by a modern wireless device.

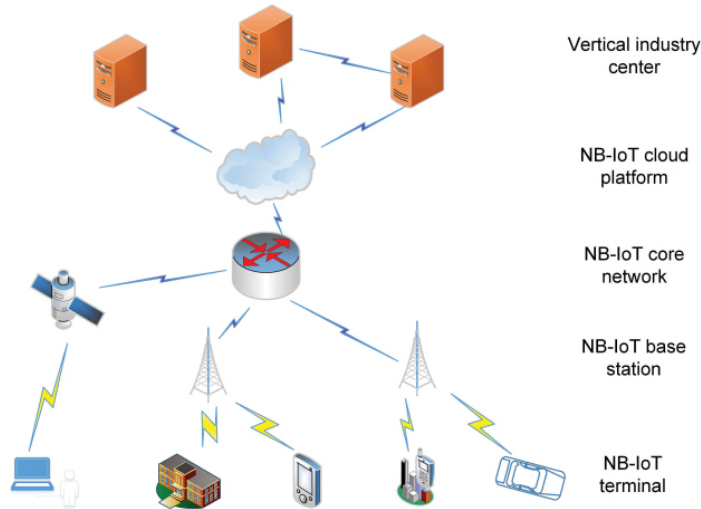


Figure 1.1: A general diagram showing the NB-IoT networking [3]

In the spirit of miniaturization and cost minimization, removal of external RF filter could be considered. Additionally, integrating multi-band front ends into single wide-band front ends which is tunable over spectrum of interest, can be beneficial as it enables to have a lesser pin count, simple package design and faster design times [4].

A Direct Conversion Receiver (DCR) on the other hand, have a principal advantage of eliminating the Intermediate frequency (IF) filter and making the design entirely integrable [12]. By eliminating any IF stages and directly converting the signal to effectively a zero-IF frequency, the image problems associated with super-heterodyne architectures could be ignored.

Thus, in this work, the focus is mainly maintained on wide-band DCRs. These Surface Acoustic Wave (SAW)-less receivers should conform to the specification of NB-IoT in the 3GPP LTE release 13.

1.2 Scope

The scope of this thesis is to design and simulate most preferred types of architectures which would be suitable to the problem specifications defined for the thesis. The architectures are supposedly to focus on the important parameters of RF receivers front ends such as high linearity over a wide bandwidth, decent gain for sensitivity and low operating DC power.

The discussion is the comparison of the methods and techniques used to address the problem arising from the SAW-less operation, simulation of two most promis-

ing architectures, after comparative study of different architectures used in the prior art. However, the layout design which certainly could throw more light into the performance and the operating capabilities of the selected architectures is not covered as a part of this work due to shortage in available time. A set of much complicated architectures are also identified, but not studied in this thesis, are categorized under the future work.

The design thus developed have been evaluated using rigorous simulations. The thesis mainly focus on design of a filter-less low power wide-band receiver front-end comprising of an inductor-less LNA complemented by a suitable mixer and Base-Band (BB) amplifiers, compatible with the NB-IoT specification. Its also involves enhancing its key parameters like linearity, noise performance, power efficiency for an optimum NF, conversion gain and lower inter-modulation distortion. Main parameter of interest here is to manage a blocker level of -15dBm while maintain decent sensitivity, with the minimum achievable inter-modulation distortion, especially the 3rd harmonic.

1.3 Thesis Organization

In this thesis, a number of receiver (RX) architectures have been studied, comparisons are obtained and finally two of the most promising ones are selected to study further with design of blocks and circuit level simulations for the RX architectures. This forms the detailed discussion in this report. Chapter 1 discusses the problem in general and sets the theme of the thesis. The rest of the report is organized as follows. Chapter 2 defines the design specifications and the targets to be achieved during the project. The comparative studies which classifies the RX architectures conducted as a part of the thesis forms the Chapter 3. The explanation of each design and implementation, and simulation results of blocks in each of the individual designs is presented and analyzed in Chapter 4. Chapter 5 gives the summary of all the results of this work. The final chapters 6 and 7 puts forward the conclusions of the thesis study and the future work that could be done further to improve this work.

Design requirements

A multi-standard RF front-end wide-band receiver should achieve not only wide bandwidth to support wide-band operation, but also high linearity to minimize sensitivity degradation due to In-Band (IB) inter-modulation and cross modulation distortion due to co-existence of strong interference signals. Linearity requirements are more stringent in multi-standard RF front-end receivers since, OB interference signals fall into operation RF bandwidth, requiring higher linearity as they cannot be filtered out any longer for multi-standard applications by an off-chip band selection filter.

Due to the lack of off-chip RF filtering, wide-band receiver front-ends have to handle interference signals that are much larger than those in conventional narrow-band receivers [13]. These receivers have no selectivity and amplifies both the wanted signal and any blockers present. Given the voltage amplification required to achieve a competitive noise figure and the low supply voltages used in modern CMOS processes, a 0dBm blocker will cause the LNA to clip. This will increase noise and distortion in the receiver [4].

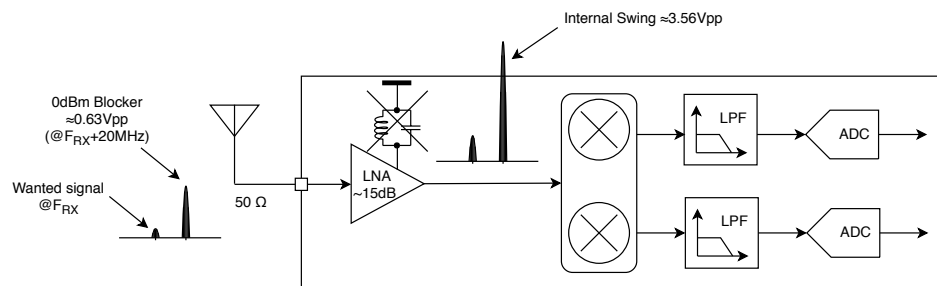


Figure 2.1: Effect of OB blocker [4]

Removal of the external SAW filter is very challenging as strong OB blockers could cause desensitization of the receiver through two major mechanisms: gain

compression and reciprocal mixing [14]. Besides nonlinearity, the front-end can produce IB distortion due to Harmonic Mixing.

Following are some of the key terms related to specifications of receiver front-ends.

DCR: A DCR directly demodulates an RF modulated carrier to BB frequencies, where the signal can be directly detected and the conveyed information can be recovered. The reduced component count that results by eliminating IF stages provides an attractive solution.

It translates the band of interest directly to zero frequency and employs low-pass filtering to suppress nearby interferers.

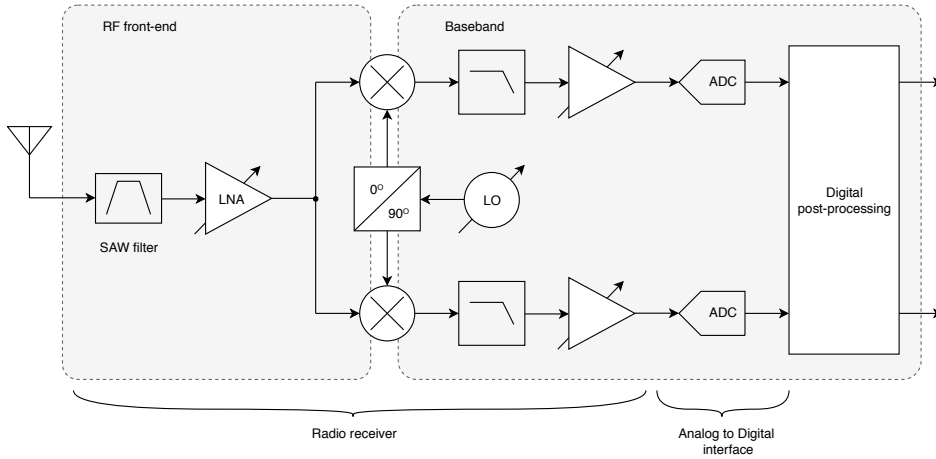


Figure 2.2: Conventional DCR

Selectivity: Selectivity of a receiver means how well a receiver performs in the presence of other unwanted co-channel and adjacent channel interfering signals. It is the measure of how strong signals can be, that interfere with the received signals.

Usually these unwanted signals could be difficult to be eliminated, as without filters, the inter-modulation products can fall upon the wanted signal. But, if the power levels of these signals are down with respect to the wanted signal, the receiver will function efficiently and, if the power levels of these interfering signals are comparable to the desired signals, the receiver starts misbehaving.

Sensitivity: Receiver sensitivity is the lowest power level at which the receiver can detect an RF signal and demodulate data. Sensitivity is determined by the Noise Figure (NF) of the receiver, the required signal-to-noise-ratio (SNR_{min}) needed to demodulate the information and the bandwidth (B) of the signal [10]. Greater the sensitivity, larger can be the range of distance between the transmitter and receiver antennas, assuming line-of-sight conditions. Sensitivity in dBm is given by

$$P_{sens} = -174 + NF + SNR_{min} + 10 \log_{10} (B) \quad (2.1)$$

Desensitization: The process of reducing the sensitivity of the radio receiver is known as desensitization. In other words, it refers to reduction in ability of receiver to accept the wanted signal in the presence of strong OB interfering signal in comparison to when the interfering signal was absent. Usually, receiver desensitization specification refers to ability of the receiver to withstand very strong OB undesired interfering signals which are about 100MHz away from the wanted or desired signal. When strong undesired signal is present, it will increase load on the design and hence, there would not be enough power budget to accommodate the weaker desired signals. But when the undesired signal is absent, weaker signals will receive full measure of the power budget.

LO Leakage: The key disadvantage of passive mixer-first receivers is the LO leakage. In the conventional receivers, LNA generally act as an isolator between RF input to the LO whereas, with absence of gain stage at the input, LO leakage can trigger several issues. As spurious emission levels are crucial and requirements need to be met as prescribed by the standard and regulations, the LO leakage is a mixer first receivers can be on the limit of what is tolerated from the spurious emissions point of view [10]. Also, signal leakage paths can occur in the receiver. LO energy can leak through the mixer to the antenna input and can get reflected back into the mixer. This can cause self-mix and create DC offset signal. The offset may be large enough to overload the BB amplifiers, cause reduction in the resolution of Analog to Digital Converter (ADC) and prevent reception of the wanted signal.

IIP2: It is a measure of 2nd order non-linearity and helps to quantify the receiver's susceptibility to single and two tone interfering signals. Considering the worst case of an Amplitude modulated (AM) input, modeling of AM signal is done by choosing two closely spaced signals with frequency f_1 and f_2 . These signals are applied to the input of the receiver, due to 2nd order non-linearity in receivers, corresponding distortion will be present at the output. This distortion generates 2nd order inter-modulation (IM2) at frequency $|f_1 - f_2|$, which will be at a BB frequency. The effects are less pronounced in LNA working at a high frequency and the low frequency distortion can be filtered out by placing a capacitor between the LNA and the mixer. Challenges to distinguish between the wanted information and IM2 can be observed following LNA, since both signals are present at the output BB frequencies, causing degradation in sensitivity and Signal-to-noise-ratio (SNR) [10].

A measure for 2nd order linearity is called an IIP2 can be calculated as

$$IM2|_{dBm} = 2P_{blocker}|_{dBm} - IIP2|_{dBm} \quad (2.2)$$

where the power of the two blockers ($P_{blocker}$) has been assumed equal for simplicity.

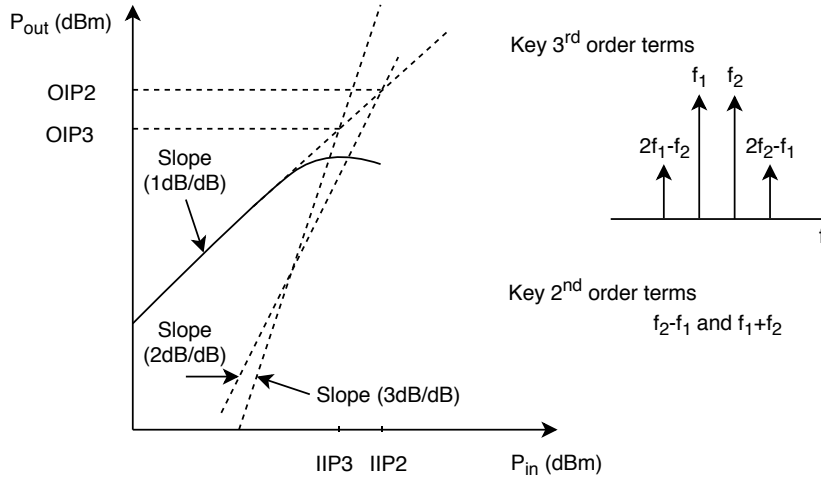


Figure 2.3: Non Linearity: IP2, IP3 [5]

IIP3: It generally occurs when a wanted signal is located, at a frequency f_1 and a blocker signals at frequency f_2 . This blocker will reach the input and generate 3rd order inter-modulation (IM3) at frequency $2f_1-f_2$, i.e. at the IB frequency as the wanted signal. The scenario is recreated when two blocker tones inter-modulate and the IM3 product appears again on top of the wanted signal. This is shown in the Figure 2.4. In this case, the RF spectrum will have the two blockers which have a frequency offset between themselves, which is exactly the offset made by one of them with the wanted frequency signal, at any three suitable frequencies in the RF bandwidth. These scenarios severely deteriorate the SNR. A measure for 3rd order linearity is called an IIP3 can be calculated [15] as

$$IM3|_{dBm} = 3P_{blocker}|_{dBm} - 2IIP3|_{dBm} \quad (2.3)$$

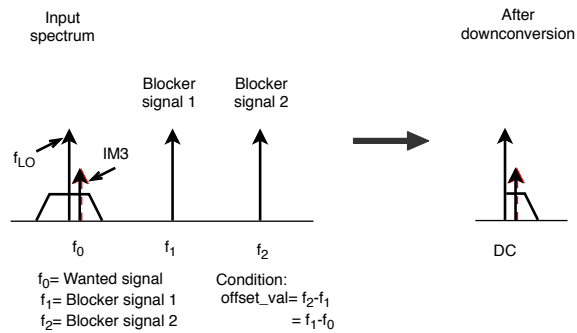


Figure 2.4: Scenario for IM3 products appearing on top of wanted signal due to inter-modulation between 2 blocker tones.

where the power of the two blockers ($P_{blocker}$) have been assumed equal for simplicity.

Gain Compression: Gain compression occurs when the input power of an amplifier is increased to a level that reduces the gain of the amplifier and causes a nonlinear increase in output power. The amplifier has a linear region of operation where gain is constant, and independent of power level. The gain in this region is commonly referred to as "small-signal gain". As the input power increases, the amplifier gain appears to decrease, and the amplifier goes into compression. The most common measurement of amplifier compression is the 1-dB compression point (Figure 2.5). This is defined as the input power which results in a 1-dB decrease in amplifier gain (relative to the amplifier's small-signal gain) [10].

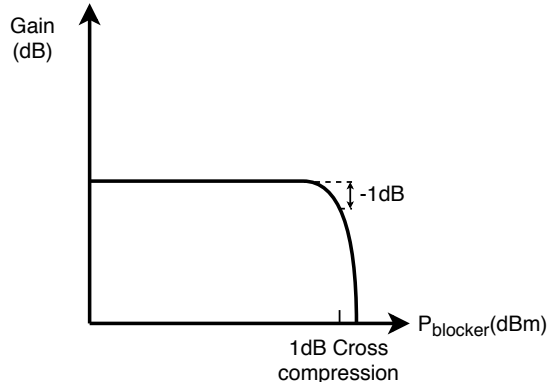


Figure 2.5: Gain Compression Plot

Cross Modulation: Cross modulation are seen in radio receivers at instances where the modulations schemes used have an amplitude component. Cross modulation is the amount of amplitude modulation due to non-linearities in the receiver chain which is transferred from an unwanted signal at OB frequency or LO leakage emissions, to the required one being received. These strong signal may cause part of the receiver to become non-linear and transfers the varying amplitude over to other signals. As it is a 3rd order effect, a receiver with a good 3rd order intercept point should also exhibit good cross modulation performance [10].

$$P_{crossmod} = C_{factor} + 2P_{fmod} + P_{f1} - 2IIP3 \quad (2.4)$$

Where $P_{crossmod}$ is resulting power of the cross modulation, P_{fmod} is the power of an amplitude modulated blocker at frequency f_{mod} , P_{f1} is the power of blocker signal at frequency f_1 and C_{factor} depends on modulation of blocker [10] [16].

Reciprocal Mixing: Reciprocal mixing results from the phase noise performance of the local oscillators within the radio receiver. For receivers operating in the presence of local strong signals, the reciprocal mixing performance of the over-

all receiver is important. This manifests phase noise requirements onto the LO synthesizers used within the receiver.

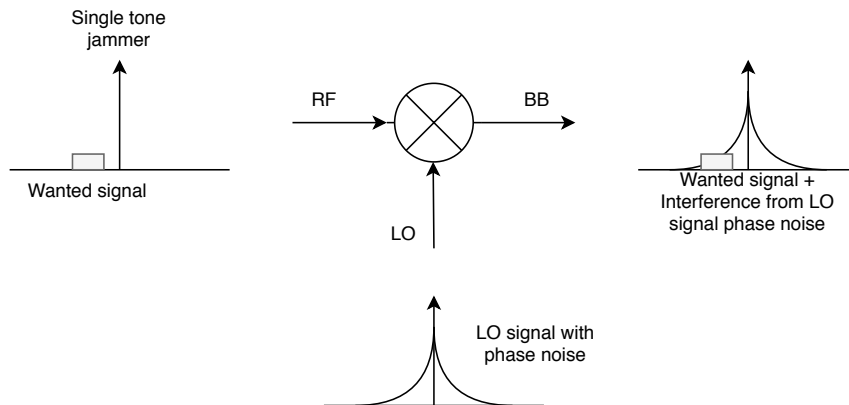


Figure 2.6: Reciprocal Mixing [6]

Harmonic Mixing: Harmonic mixing is from LO signals which are square wave signals controlling the mixer. Interference of odd harmonic will be converted into baseband. All the higher order harmonics which are a major issue can be rejected by using Harmonic Rejection Mixer (HRM).

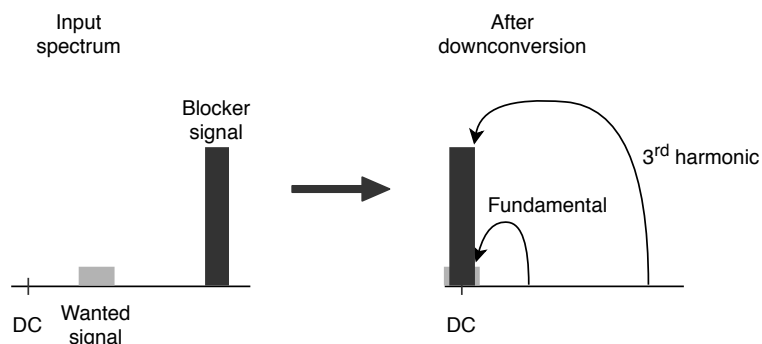


Figure 2.7: Harmonic Mixing [7]

2.1 Front end specifications

In NB-IoT, the 3GPP standard mandates the requirement of a receiver to be capable of tuning the signals within the frequency range 450MHz to 2200MHz, thus necessitating it to have wide-band reception with good selectivity. In this standard, the OB requirements are deliberately relaxed to allow SAW-less operation. It also demands to design a linear receiver with high dynamic range LNA.

Although, the RF front end has to follow the specifications mandated by 3GPP as a necessary requirement, additionally, a few more requirements have been defined for the master thesis work considering the practicalities and power constraint achievements. The requirements have been defined in such a way that the design can form a bench mark for other receiver architectures.

The receiver front-end comprising of RF components such as LNA and HRM, BB components such TIA and harmonic recombination circuit have been considered for design in this work. Design of dividers needed to produce the phase shifted LO signals are also considered.

The front end specifications defined for the thesis are as follows:

Parameter	Value
Process technology	40nm CMOS
Supply Voltage [V]	1.2
RX power [mW]	<20
RF Frequency range [MHz]	450 - 2200
BB Bandwidth (I/Q) [kHz]	100
Temperature range [°C]	-40 - 125
Noise Figure [dB]	3 typ. or less
Gain [dB]	60 \pm 10
OB Blocker Tolerance [dBm]	-15 max. @ 100 MHz offset
Third order harmonic rejection [dB]	>60
S11 [dB]	<-10
IB IIP3 [dBm]	>-20
OB IIP3 [dBm]	> 0
IB IIP2 [dBm]	>50
LO leakage [dBm]	<-57
Circuit type	Single ended LNA and passive mixer
Topology	Inductor-less and DCR

Table 2.1: Front end target specifications

Background

CMOS scaling is beneficial for wide bandwidth, but not for linearity because of more short-channel effects and lowered supply voltage sets tighter constraints for handling large interference. The linearity challenge in scaling CMOS is especially problematic for OB interference, which can be much stronger than IB interference. In a wide-band receiver, OB interference can generate IB distortion via non linearity or harmonic mixing, as described in Chapter 2. In recent years, many wide-band receivers have come up, partly enabled by the CMOS process advancement [17].

In traditional multi-standard receivers, multiple dedicated receivers were used in parallel, each for one band. It was effective from product development fronts having advantage of quick time to market and low risk. However, this approach significantly increased system size and cost for every band that is added, for both on-chip and off-chip components. It is becoming increasingly impractical to follow this approach as there are already a large number of radio communication standards, while new ones like LoRa, NB-IoT etc. are continuously being developed [17].

Relevant characteristics of a wide-band receiver include the input matching, gain, and NF versus frequency. A key enabling block is a wide-band LNA, which is usually the first block of a receiver chip and therefore can largely affect the input matching, gain, and NF of the whole receiver.

For a wide-band LNA, to simultaneously achieve good impedance matching, e.g. $|S_{11}| < -10\text{dB}$, and low noise, e.g. $\text{NF} < 3\text{dB}$, is challenging. Besides, another bottleneck of wide-band operation may come from the interface between LNA and mixer where the capacitive loading from mixer can limit the bandwidth of LNA [17].

To counter the extra-ordinary challenge due to OB interference and need of wide-band operation in the absence of pre-filtering, there are different innovative designs reported in literatures as discussed in the following section.

3.1 Prior art

Extensive efforts have been made in recent years to improve the performance of front-end receivers to mitigate co-existent issues. This is evident from the variety of approaches reported in the various literatures, which, as shown in this section, range from re-discovered concepts to novel receivers architectures.

Before going into depth of approaches used in different literatures to overcome the issues stated, more insights about basic functionality of these receivers with respect to different modes in which receivers are operated and topologies considered are given.

3.1.1 Voltage versus Current mode

Receivers are operated in two modes namely, Voltage Mode and Current Mode.

In voltage mode, the LNA drives the mixer as a voltage source developing a voltage gain at RF. On the contrary, in current mode approach, the LNA inject an RF current into the low input impedance of the mixer and no RF voltage gain is developed. In other words, in voltage mode, mixers are terminated by high impedance and in current mode, mixers are terminated with a low impedance. Since conventionally the LNA is assumed as a voltage source, in current mode operation it is called Low Noise Transconductance Amplifier (LNTA).

In both modes mixers are very similar where the input signal is multiplied with the LO. The input and the output of the mixer are alternatively connected and disconnected, resulting in a multiplication by a square-wave, with a period equal to $1/f_{LO}$. Only the first harmonic of the square wave is used to down-convert the signal obtaining a conversion gain (S_{21}) equal to $2/\pi$ [15]. When mixers operate in triode region they are called passive mixers and when in saturation region they are called active mixers. Since the passive mixers have excellent wide-band linearity, low flicker noise and no power consumption, passive mixers are preferred in modern low power designs. This however comes at the cost of conversion gain and need of full rail LO signal [18].

3.1.2 LNA first versus Mixer first

Depending on topologies used for design receivers, they can be classified in two ways:

1. LNA first.
2. Mixer first.

LNA first receivers are the traditional radio receivers, where the first stage is an LNA, whose main function is to provide enough gain to overcome the noise of

subsequent stages [19]. To make receivers blocker tolerant some researchers used the approach of avoiding the use of LNA and starting the receiver chain at the mixer, known as Mixer First receivers. These architecture prevents the amplification at the input which eliminates the amplification of blockers, as the antenna gets directly connected to the down conversion mixers. These Mixer First architectures can incorporate matching basically with the help of N-path filtering technique [20] or providing a positive feedback as in [21], obtaining an exceptionally linear receiver [4]. Due to absence of a gain stage in mixer first architectures, they tend to be more noisy compared to a LNA first architectures.

3.1.3 State-of-the-Art Wide-band RX

To avoid the need of SAW filter a variety of LNA first architectures [9,22–27] and mixer first architectures [4,21,28–31] have been proposed.

As basic N-path filtering technique is inadequate to meet the stringent OB blocker rejection demands, all the implementation discussed in this work, except [22], uses current mode of operation to minimize voltage gain at RF frequencies while, [22] uses low-pass reconfigurable differential sampling capacitor in the baseband. Unlike others [31], [21,22] are Software-defined radio (SDR) based receivers. Implementation in [31] incorporates tunable resistor, capacitor in the BB amplifiers to obtain tunable input match and tunable-Q Band pass filter (BPF) and 8-phase harmonic rejection mixer to reject 3rd and 5th order non-linearities. With better handling of OB interference and improved NF a current-mode passive mixer first architecture was proposed in [21]. Input matching at LO was established by introducing frequency translational positive feedback from BB to RF input, with tunable feedback resistance in the path. The gain and cut-off frequency of the TIA are also controlled digitally. These blocker tolerant designs are enabled with great programmability, possesses high linearity and wide-band matching at the expense of high NF and power consumption.

Different from traditional mixer first receivers and N-path filters, implementation in [30] employs Cross-coupled (x-coupled) passive switch-RC down-conversion mixer providing improvement in linearity and compression. The mixer switches are connected to the antenna through matching resistors offering wide-band input matching. In [25], active feedback frequency translational loop is introduced to provide better RF selectivity by using high pass filter along the feedback path. Though these designs achieves high linearity performance, they compromise on power and NF.

Implementation in [9,24] uses $\Delta\Sigma$ - based Analog-to-digital (A/D)- converting Channel-select-filter (CSF), where [9] uses highly linear gain switching Noise Canceling- Low Noise Transconductance Amplifier (NC-LNTA) to provide wide-band matching whereas [24] uses positive feedback as in [21] to attain impedance matching. The architecture is based on direct down-conversion $\Delta\Sigma$ feedback that is directly up-converted to RF nodes through N-path filtering technique. Though these digitally intensive architectures support blocker tolerance, achieves com-

petitive noise performance with $\approx 2\text{dB}$ higher NF and same linearity performance with respect to design considered in this work, for this work designing a complete $\Delta\Sigma$ -based receivers was chosen out-of-scope due to its complexity and time availability. Use of resonant load and design for narrow-band operation, implementation in [23] was chosen to be inadequate for our work.

Wide-band, blocker tolerant, SAW-less DCR front-end with harmonic rejection mixer are proposed in [26, 27]. Implementation in [26] uses a 8-phase HRM and operates in three modes, whereas [9] uses 6-phase HRM to achieve required harmonic rejection. These implementations shows good harmonic rejection performance, decent NF and high enough linearity, power consumption was on a high side in [26].

FTNC based receivers were proposed in [4, 28] which provides relaxed performance trade-offs between noise, OB linearity and wide-band operation.

A Zero-power receiver front end consisting of transformer in place of active LNAs and passive mixers complemented by noninvasive filtering which is a method that applies filtering to only interferers without invading the signal have been demonstrated in [32]. This power efficiency came at the expense of noise figure, narrow bandwidth and linearity.

3.2 Summary on Techniques adopted to make receivers Robust

3.2.1 N-Path Filtering

N-path Filtering : The N-path filter essentially performs down-conversion of RF signal, filters with a low-pass response and up-converts again to RF. This technique helps to realize RF transfer function with a precise center frequency and can offer high quality factor (Q-factor) with the aid of frequency translation. The 3dB bandwidth of the filter is estimated [20] as

$$f_{-3dB} = \frac{1}{\pi NRC} \quad (3.1)$$

Sometimes they are also called as Transferred Impedance Filter.

3.2.2 Noise Cancellation

Noise Cancellation: The noise canceling technique alleviates the trade-off between blocker tolerance and NF [4]. This technique dissociates noise and input impedance so that broadband resistive matching is realized [33]. In this technique two fully correlated Common Mode (CM) noise voltages cancel by taking

differential output. It includes two amplifier stages in parallel where one stage (main path) offers matching and an other stage (auxiliary path) provides gain. The two fully correlated noise contributions originating from the same matching device via two paths get canceled at the output. The wanted signal is injected out of phase with respect to noise of the matching device, so signal contributions are added, while noise is canceled.

To achieve $NF < 3dB$, several variants of noise canceling RX are proposed which make use of Noise Canceling- Low Noise Amplifier (NC-LNA) or NC-LNTA. In NC-LNA based architectures voltages at the output with suitable voltage gain is provided at RF are added to cancel noise. Whereas in NC-LNTA based architectures as in [9] and [34], the addition of signals from two path are done in current domain. These can have high linearity and good blocker handling capacities, especially when this is combined with high-linearity current mixers and frequency translated filtering [33].

Frequency Translational Noise Canceling (FTNC): Although noise canceling in RF with voltage gain have many attractive properties, there are also challenges, especially if we need to handle strong blockers. To avoid this, voltage gain at RF is moved to BB. The voltage to current (V-I) conversion takes place at RF, followed by a down conversion mixer and then current is converted to voltage in baseband where noise gets canceled. As noise canceling occurs after frequency translation it was named as FTNC [4]. As the gain is now realized in BB instead of RF, load capacitance that would otherwise limit the RF bandwidth of the current to voltage (I-V) conversion is no longer a problem. As filtering reduces the amplitude of blockers, we can then allow for much more BB gain without clipping. Large capacitance is needed across input of TIA to suppress OB blockers. In DCR, we can use simple low-pass filtering for anti-aliasing, and relax ADC dynamic range and sampling rate requirements.

3.2.3 Blocker Tolerance

Blocker Tolerance: A wide-band design amplifies both wanted signal and a very strong OB signal. This causes the sensitivity to reduce as the front-end amplifiers run into compression. This situation often arises when a receiver and transmitter are run from the same site and the transmitter signal is exceedingly strong. When this occurs it has the effect of suppressing all the other signals trying to pass through the amplifier, giving the effect of a reduction in gain. As in NB-IoT applications there will be situation when radio transmitter will be operating in the close vicinity to a receiver, if the radio receiver is blocked by the neighboring transmitter then it can seriously degrade the performance of the overall radio communications system. For e.g. when a user is using a mobile at a close vicinity of IoT system, strong signals received by mobile can corrupt the wanted IoT signals.

To tolerate the blockers i.e. to avoid receivers getting compressed, many blocker tolerant receivers are developed using different techniques. These receivers have

some common features like they employ passive mixers and they suppress voltage gain at blocker frequencies. Deployment of current mode passive mixers forces, voltage swing at the output of LNTA to be low as receiver works in current-mode and hence blocker does not experience voltage amplification causing gain compression significantly reduced. Also, due to the limited loop gain of the TIA its input impedance increases with frequencies, increasing the voltage swing at the input [27]. By inserting a shunt capacitor at the TIA input OB blockers are attenuated before the TIA as the impedance seen by the LNTA and mixer will be low also for high offset frequencies [21]. Generation of LO signals with low phase noise also reduces effect of blockers [4].

3.2.4 Harmonic Rejection

Harmonic Rejection: Mixers are generally controlled by square waves to maximize linearity and removing the interference at even harmonics of LO signal. Mixers under hard switching minimize the NF and nonlinearity but implying that the blockers at odd LO frequencies (such as 3rd, 5th...) will also be down-converted to the BB corrupting the desired signal. A key consideration in the design of broadband receivers is the spurious response of the down-conversion mixers, where LO harmonics can lead to down-conversion of unfiltered interferer to BB, along with the desired signal, thus degrading the signal-to-noise ratio.

Recent broadband receivers utilize a HRM to reject LO harmonics within the down-conversion mixer and prevent interferer from being down-converted to BB. Depending on the configuration of the HRM, it is possible to choose the harmonics that are rejected. In the ideal case, this rejection can be infinitely large. In practice however, the achievable level of rejection of LO harmonics is limited by phase mismatch in the multiphase clocks and gain mismatch in the sinusoidal gain coefficients [7].

Harmonic Rejection Mixer (HRM): This type of mixer allows for the significant reduction or removal of close-in harmonics of the effective down-conversion LO. The Harmonic suppression is achieved through the use of multiphase clocks along with sinusoidal gain coefficients within the mixer, which synthesizes an effective down-conversion LO which is a much better approximation to a sinusoidal LO waveform, compared to a simple square-wave [7].

The first HRM which was used within transmitter was proposed by Weldon in [8]. This implementation was based on Gilbert cell active mixers. The mixer input is operated on by three path, each with a clock frequency f_{lo} and relative phase shift and gain corresponding to a sampled sinusoid. In this implementation three square waves LO with 50% duty cycles at relative phase shifts of -45° : 0° : 45° and scaling the 2nd LO by $\sqrt{2}$ reject the 3rd and 5th harmonics when the three paths are summed at BB as shown in Figure 3.1.

In an another implementation a passive HRM was proposed by Molnar in [35] which alleviates the problem related to RF device mismatch as in [8] and increase

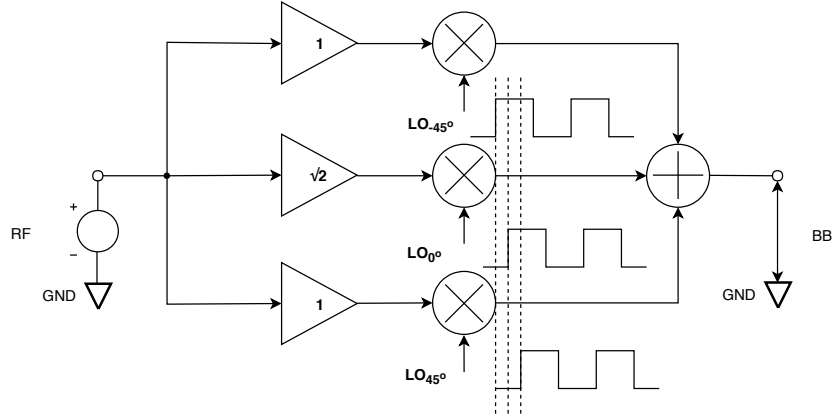


Figure 3.1: Traditional HRM by Weldon in [7,8]

linearity by applying all gain ratios for harmonic rejection after down-conversion i.e. in BB. The switches of this implementation are turned on in succession by eight, phase split, 12.5% duty-cycle LO signals at the IF frequency. As in [8] the same eight gains are applied individually to each paths to provide Harmonic rejection.

Rejection of fifth and higher order harmonic was not considered in this work and we decided to go HRM with 6 phases proposed by A. Nejedel in [27]. Using this technique power consumption is reduced and simplifies the LO divider circuit. In [35] and [27] the mixer is terminated by a TIA, enabling the operation in current mode. Following the TIA the gain ratios are implemented by a combination network where signal from TIA are combined by using proper resistor ratios at the the input of the summation circuitry. OP-amp provides the virtual ground for summing the current produced by each path and harmonics are rejected at the input.

3.3 Classification of RX architectures

The prior art in the domain of RX architectures have been employing several different techniques for achieving the specified requirements. However, there are a range of similarities among the architectures, for which a method of classification must be identified. Classifying architectures helps to study them more precisely leading to a potential solution for the problem defined in this thesis. The entire set of wide-band receivers can be classified generally as Mixer first and LNA first architectures, but this would not be giving a deeper insight into the properties of the receivers. Another way of classification is identification of the mode in which LNA is operated i.e. Voltage mode or Current mode and the conditions in which mixers down-convert the RF signal into the BB signal.

Architecturally the wide-band receivers are classified as:

1. Current mode Mixer first Receivers.
2. Voltage mode LNA first Receivers.
3. Current mode LNA first Receivers.

Table 3.1 summarizes the different topologies studied in this thesis as part of the Literature Survey which was conducted with respect to the architecture classification we have adapted and techniques adopted to make receivers robust.

	Architecture				Technique		
	Voltage Mode	Current Mode	LNA First	Mixer First	Noise-Canceling	Harmonic Rejection	Blocker Tolerant
JSSC'12 [4]		✓		✓	✓	✓	✓
RFIC'15 [21]		✓		✓		✓	✓
JSSC'10 [31]		✓		✓		✓	✓
JSSC'11 [22]	✓		✓			✓	
RFIC'16 [30]		✓		✓			✓
JSCC'13 [23]		✓	✓			✓	✓
JSSC'12 [25]		✓	✓		✓		
JSCC'15 [32]		✓	✓*				
NORCAS'16 [24]		✓	✓				✓
JSSC'15 [9]		✓	✓		✓		
ESSCIRC'13 [27]		✓	✓			✓	✓
RFIC'15 [28]		✓	✓		✓	✓	✓
TCAS-II'13 [26]		✓	✓			✓	✓

* Transformer is used as the LNA

Table 3.1: Summary of different topologies

In summary, most of the published literature about wide band receivers use a zero-IF architecture for high-level integration and adopt a passive mixer for low

1/f noise. Larger mixer switches helps to operate in current mode as ON resistance will be lower. Careful sizing of the mixer switches are to be accounted, as large switches require more driving power from LO dividers. Phase noise of LO circuits should be carefully monitored to achieve high tolerance to blockers. Also, voltage gain at blocker frequencies should be avoided to aid blocker tolerance. Square wave LO signals controlling the mixer helps to maximize linearity, gain, noise performance whilst also removing interference at even harmonics of the LO.

Different techniques like active feedback in [25], FTNC in [4] and [28], mixer first topology as in [31] are adopted to mitigate issues arising due to removal of SAW filters and achieve a wide-band matching. To make RX power efficient, [4] and [9] have adopted approaches like, turning off auxiliary path in the absence of blocker and gain switching in LNTA providing variable gain offers competitive power consumption without compromising on NF. To achieve good 3rd order harmonic rejection traditional 4-phase LO circuitry can be replaced with 6-phase LO circuits.

Design methodology

From the extensive survey of literature in RX, a large number of receiver architectures are found to be promising, but considering the scope of the thesis and its objectives, two of them are selected on the basis of their promising factor towards the goal of the thesis and their performance comparisons. The selected architectures being: a single ended Frequency Translational Noise Canceling RX [4] and a gain switching LNTA based RX [10].

The study upon their designs have revealed that these architectures have incorporated methods of noise canceling, gain switching, blocker tolerance and power saving into importance. As a result, both of them are considered for design and simulation further to bring about a detailed comparison among them and to find out how much they adhere to the requirements defined in the thesis.

In this chapter we shall discuss in detail the design methodology of each of the type of receivers separately.

4.1 Frequency Translational Noise Canceling RX (FTNC-RX)

The FTNC RX, described in [4] is a wide-band blocker tolerant and noise canceling DCR with two down-conversion paths. This corresponds to the main path and the auxiliary path where the former gives matching with the antenna and the latter helps to achieve noise cancellation in the presence of a strong OB blocker. The main path is basically a passive mixer first front-end which down-converts the RF current to baseband instead of converting the current measurement to a voltage at RF. A BB amplifier configured as TIA then converts any current in the receive band to voltage. The auxiliary path provides the voltage measurement using the transconductance stage in which an inverter LNTA converts the RF node voltage to current, which is then down converted by another passive mixer. The down-converted IB current is later converted to voltage by a second TIA. The

baseband outputs from both of the paths are then combined into In-phase (I) and Quadrature-phase (Q) components using operational amplifiers based weighting and recombination stage. In [4] the architecture is been presented as both single ended and fully differential topologies with respect to the antenna interfacing, since the latter require a balun and hence not considered in the thesis because of the expected insertion loss which will degrade the NF further.

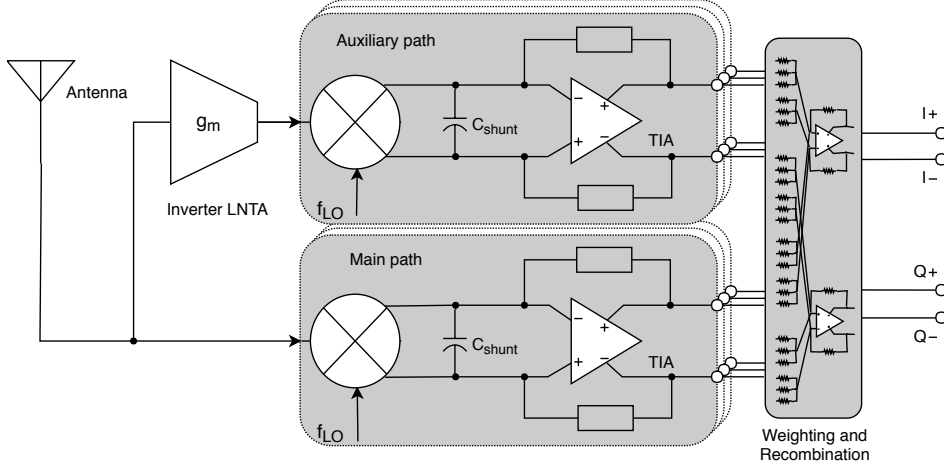


Figure 4.1: Block diagram of FTNC RX architecture

Impedance matching to the input port is achieved by the impedance looking into the main path similar to a mixer-first receiver, which is directly contributed by the mixer switch resistance and the up-converted measure of BB TIA input impedance (Z_{BB}). The low frequency noise in the BB of the main path is up-converted by the passive mixer to RF and appear at the input node. It will then enter the auxiliary path and appear as common mode at the output. As a result, under the perfect matched condition to the antenna port $R_S = Z_{in}$, noise in the receiver is optimally canceled by setting shown in Equation (4.1).

$$G_{MAIN} = G_{AUX} G_M R_S \quad (4.1)$$

where G_{MAIN} , G_{AUX} are respectively the baseband gains of the main and auxiliary paths and G_M is the auxiliary path transconductance. When the equation gets satisfied, the noise from the transconductance stage emerges as the only major noise contributor.

The input impedance of the main path which is the input impedance of the RX Z_{in} seen by antenna port at RF is given by Equation (4.2),

$$Z_{in}\{\omega_{LO} + \Delta\omega\} \approx R_{sw} + \frac{1}{M} \text{sinc}^2\left(\frac{\pi}{M}\right) Z_{BB}\{\Delta\omega\} \quad (4.2)$$

where R_{sw} is on-resistance of the M mixer switches driven by non-overlapping clocks and $(Z_{BB}(\Delta\omega))$ is BB impedance.

A large capacitor is connected at the output of the mixer to shunt the OB blockers. It provides a current sink at the large offset frequencies. In the BB, the TIAs convert the frequency translated current signal to voltage for subsequent processing. A pole is added in each of the TIAs which sets the BB bandwidth of the receiver. An operational amplifier configured as an inverting summing amplifier is connected in this path to perform the harmonic rejection operations. The summing amplifier works with the same set of equations used in [27] to reject the third order harmonics of LO frequency. The I and Q components of the BB signal are extracted and are made available to the ADC for digitization. As expected, in order to cancel the noise, signal components from the main and the auxiliary paths are subtracted at the summing amplifier which ensures noise cancellation and signal addition.

4.2 Gain switching LNTA based RX

Unlike FTNC RX topology mentioned in the previous section which is a mixer first architecture, a Gain-switching LNTA based RX is discussed in this section. This topology operates in current mode, which helps us to mitigate issues described in chapter 2. This topology uses inductor-less NC-LNTA implementation proposed in [9].

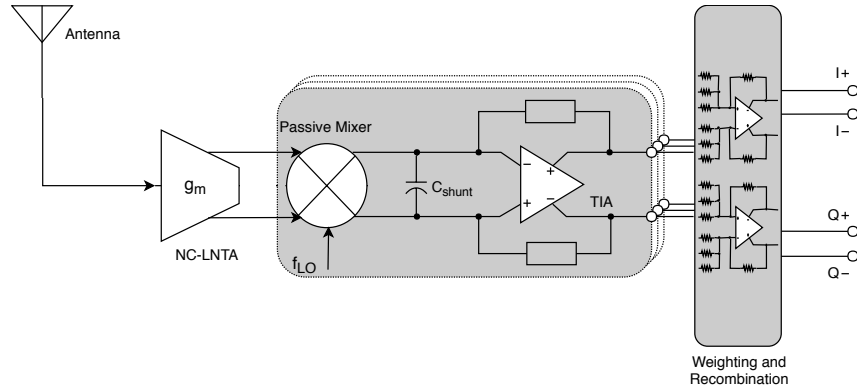


Figure 4.2: Block diagram of Gain Switching LNTA based RX architecture

Primary advantage of this LNTA is that input is single ended which helps us to avoid balun and hence the insertion loss associated with it. Wide-band NC-LNTA is based on a shunt-shunt feedback helps us to relax the trade-off between NF and wide-band matching in the input stage. To maintain a high second order linearity in presence of mismatches in the double-balanced passive mixers, the design of the LNTA is optimized for balanced outputs. The NC-LNTA operates in two gain

reduction modes (-3 dB and -6 dB) which is obtained by disabling some of the g_{mp} and g_{mn} stages and hence the name gain switching. The Gain switching together with noise canceling technique provides good trade-off for noise performance with respect to power consumption.

Use of differential mixer inherently cancels second order non-linearities due to its symmetry. Due to its differential structure noise and distortion arising from the LO divider is canceled. To operate in current mode large switches are used in the design. In the BB, a TIA using two stage OP-amp is adopted to support current mode operation. It boosts and converts the current-mode signal into voltage mode which will be recombined to reject third order harmonics using a harmonic recombination network. With the aid of feedback impedance in the TIA, low-pass response helps to filter out unwanted signal and retains the wanted information signal which will be then provided to ADC for further processing. A shunt pole is introduced at the input of the TIA to make RX insensitive to OB interfering blocker signals. Input resistors of summing amplifier used in harmonic recombination network are carefully scaled to achieve better third order harmonic rejection.

As LNTA is used to interface with the antenna, issues related to spurious emissions from LO can be mitigated.

4.3 Implementation and Circuit design

The complete receiver is built from the basic building blocks as discussed before. The circuit level discussions are presented in this section for each of the individual blocks which encompasses the design and block level simulations for each block.

4.3.1 Low Noise Transconductance Amplifier (LNTA)

As discussed earlier, in a typical receiver, the key task of an LNTA is to provide substantial small signal gain with low noise to suppress the noise of the mixer and baseband stages. Additionally, due to the absence of SAW filter, for wide-band RF input LNTA, linearity becomes highly necessary. The input stage linearity improvement should be solely focused upon having sufficiently high dynamic range to handle the large OB blocker and to avoid severe desensitization of the desired signal [36]. Having kept these in mind, different architectures are selected- starting with a single inverter transconductance stage, to a cascoded stage LNTA and finally to a gain switching LNTA with inbuilt noise canceling mechanism. The designs of these are discussed in detail below.

Although LNTAs are designed to give an optimal transconductance to meet the current mode operations of the RX circuit, the DC power consumption plays an important role in setting this value which is a major trade off along with linearity

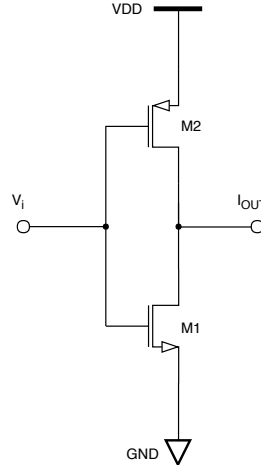
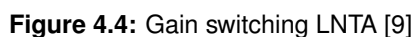


Figure 4.3: Inverter LNTA used in FTNC [4]

and noise specifications. An LNTA based on a simple inverter circuit as shown in Fig. 4.3 with the use of non-minimum length (from 40nm to 60nm) devices have been used in FTNC topology to boost the output impedance. Having minimum-length devices degrades the NF by a few tenths of a dB [4]. The transconductance of this class-AB LNTA have been set to 110mS, a higher value, which helped to linearize the working of the connected passive mixer into a better current mode for better noise performance. It is a high input impedance amplifier with a wide band characteristic and possesses good linearity. This topology is used in the FTNC-RX where the input impedance of auxiliary path should be very high and thus is very suitable for the architecture.

Another implementation of LNTA is discussed in [9] uses the LNTA architecture based on shunt-shunt feedback as shown in the Fig 4.4. The first stage of the LNTA is a voltage amplifier (A_m) which also gives a good wide-band impedance matching, and an optimal gain from fine tuning the feedback resistor (R_f). Its output is then fed to a bank of transconductances, g_{mp} which perform the voltage to current conversion for the LNTA operation, having an output in phase with the input signal. A second bank of transconductances, g_{mn} are connected directly to the RF, produces an output current which is in phase opposition to the input signal. The combined effect of the two banks of trans-conductances help to achieve single ended to differential signal conversion, while performing noise cancellation of the noise produced by transistors in voltage amplifier A_m stage.

The noise generated by the transistors of A_m stage is amplified by transconductance g_{mp} which reaches its output node O_p . The same noise source is also found at the RF input attenuated by the factor $1 + R_f/R_s$ (where R_s is the impedance of the RF antenna port which is assumed to be 50Ω in this work) and gets amplified by the transconductance g_{mn} and reaches its output node O_n . For optimal noise canceling the following equation has to be satisfied,



while perfectly balanced signals at output nodes O_p and O_n requires,

where A_v is the voltage gain of A_m stage.

Also, optimal input matching is demanded by the relation,

Since, all these three equations cannot be satisfied at the same time, a trade-off is been made between optimal noise cancellation, input matching and balanced outputs. A balanced output also helps to preserve the high 2nd order linearity in the presence of mismatches. In order to reduce noise contribution of R_f , to obtain additional gain at the matching stage along with a good compromise between the other two factors, R_f has been chosen with 330Ω as the optimal value for input matching.

During the simulations conducted while designing the circuit, the A_v was set to 5.7, with g_{mn} and g_{mp} having 196mS and 34mS respectively, satisfying the equation (4.4).

4.3.2 Passive Mixer

The ideal mixer has to multiply the incoming RF signal with the complex LO frequency which frequency shifts the wanted signal to DC. As explained before, the passive mixer because of its advantage of enhanced linearity with lower power consumption is employed in this work along with the technique of N-path filtering. A six phase mixer is used in this work for its ability to aid the linearity enhancement with respect to the third order harmonic distortions.

The passive mixers are configured single ended or differential as shown in the Figure 4.5. The single ended has an area advantage but at the cost of the amount of LO phase noise leakage and leakage through intrinsic capacitance due to large size mixer switches which is not optimally canceled. The differential mixer on the other hand needs to have a balanced differential LNTA output at its input for an LNTA first architecture or a balun in case of the mixer first architecture, of which the latter is ruled out because that would incorporate to the overall noise figure from its insertion loss. Thus a fully differential mixer was considered for gain-switching LNTA based RX, but the single ended variant for the FTNC RX.

Generally, since we need a very low ON-resistance from the mixers for current mode operation, the switch resistances were chosen in the order of 10 to 40 Ω . The sizes of these CMOS switches will be exceedingly large if operated under a very low overdrive voltage and hence, their overdrives were increased to 1.732V using on chip bootstrapping circuit with values of resistor equal to 20k Ω and capacitor equal to 5pF to get a nominal balance between the switch size and the overdrive voltage. This was also required by the fact that the DC voltage appearing at the drain or source of the transistors were same as the common mode setting voltage of the adjacent sitting TIA, which was set to ≈ 600 mV. This ensures that close to zero DC current follow through mixers avoiding need to decoupling capacitors at the input. The switch sizes ranged from 70.8 μ m to 9.44 μ m for getting a resistance of 10 Ω to 40 Ω .

In the mixer first path of the FTNC-RX, the sizes of the mixer switches are crucial, as they would be involved in providing the input impedance matching of the circuit according to the equation 4.2. Initially, after iterative analysis the R_{SW} and up-converted Z_{BB} values are chosen as 10 Ω and 40 Ω respectively, and vice versa, where the former performed very well with respect to linearity when the path by itself was considered alone. Subsequently, when the auxiliary path is introduced, the combination of 20 Ω , 30 Ω was considered as it improved the key parameters including noise cancellation and without compromising the linearity. However, in the auxiliary path, although input matching is not required, the R_{SW} is chosen as 20 Ω , for simplicity as degradation of performance is not observed

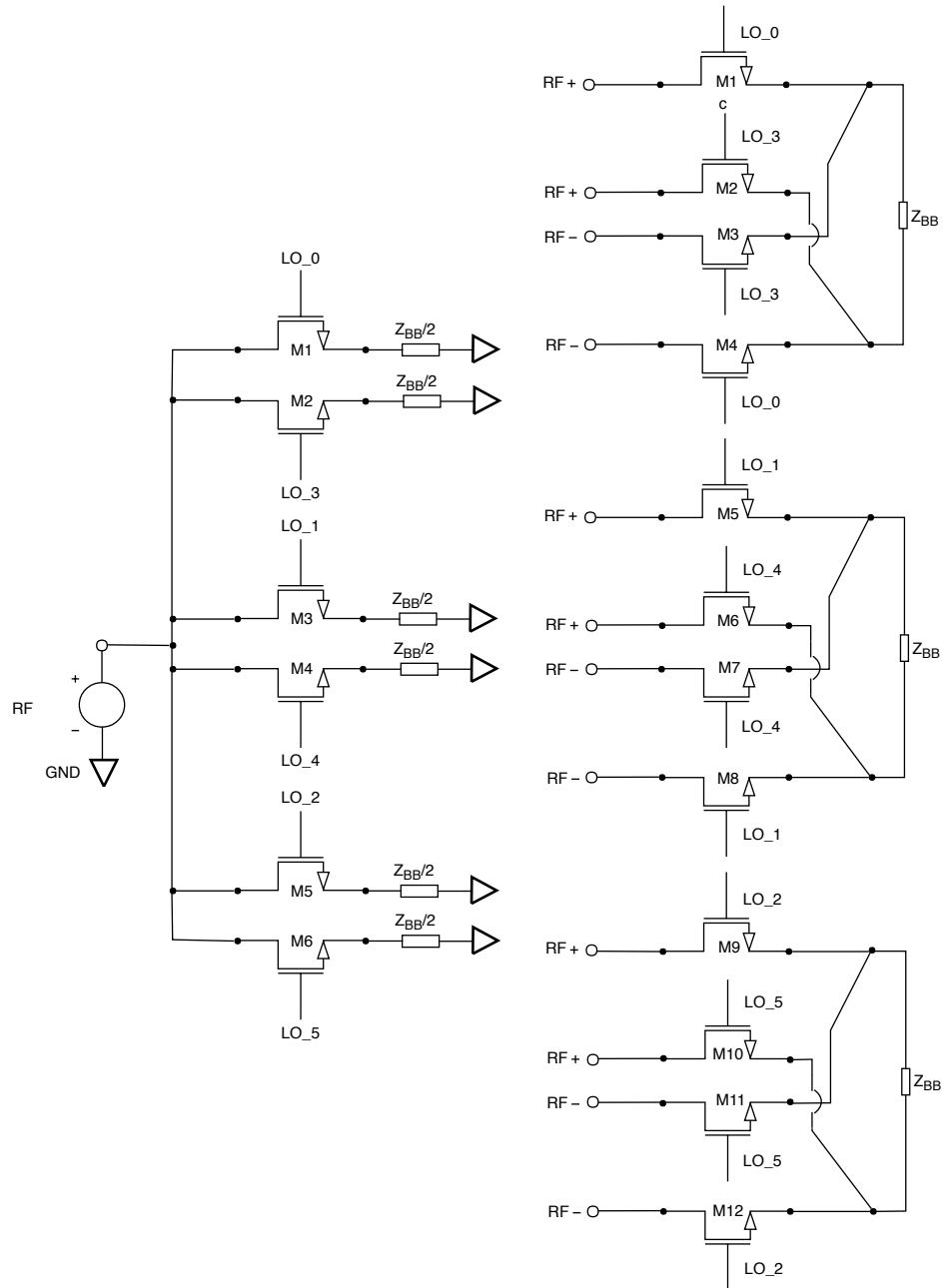


Figure 4.5: Block diagram of mixer single ended and differential

together with blocker tolerance of -15dBm and while a very low up-converted Z_{BB} is chosen to ensure, current mode operation.

Whereas, in LNTA based architecture, differential passive mixers coupled with N-path technique is used with values of R_{SW} to be equal to 5Ω and the corresponding width of mixer to be equal to $118\mu m$ to aid current mode operation.

4.3.3 LO pulse generation circuitry

The LO circuit is very critical in the design of the receiver. Important parameters such as LO leakage, Noise Figure, overall DC power consumption has direct dependence on the construction of the LO circuitry. Starting with the area perspective, if the Voltage Controlled Oscillator (VCO) is used at twice or thrice the wanted frequency helps to reduce the size of inductors on-chip. This also comes with the hidden benefit that the LO leakage problems are reduced [10]. This suggests that an LO divider circuit is essential for receiver operation. Other benefits are related to the circuit construction topologies.

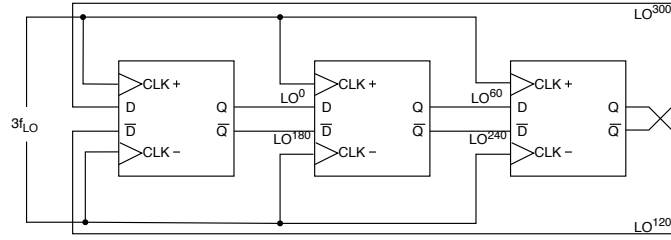


Figure 4.6: LO divider block diagram

In this thesis, the design of VCO is not considered, but however, the design of the divider circuitry is considered in order to ensure that the receiver operation is simulated correctly. The basic block of the divider circuit is a latch. In [4], a 6-phase LO divider in voltage mode operation using D-flip flops which are clocked

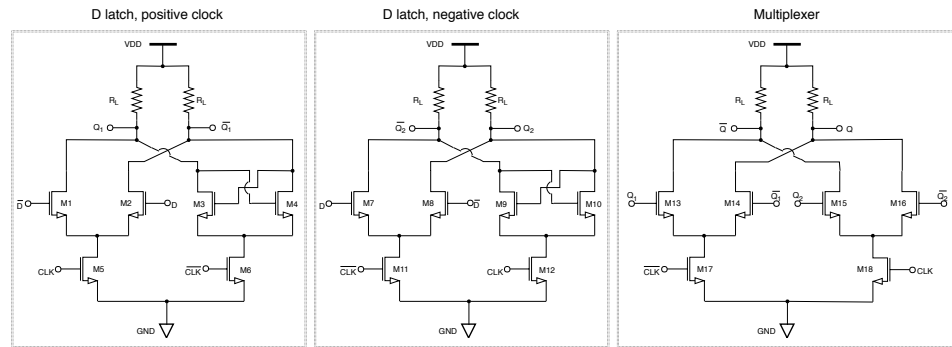


Figure 4.7: Elements of the CML latch in the LO divider circuit [10]

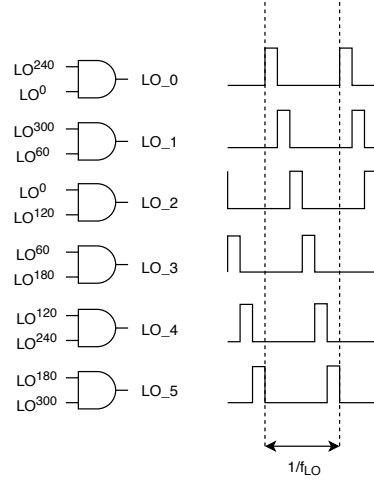


Figure 4.8: LO divider transient block diagram

modifications of latches is proposed. A CML based latch presented in [10] was selected for design in this thesis because of its high frequency performance and reliability. A frequency division of factor 3 is required in the generation of 6-phase LO and the divider uses three dual edge triggered latches, each of which has two sub-latches, where one is positive edge triggered while the other is negative. A multiplexer is then used to select either latch for the corresponding clock edge. The latches in the divider circuit are connected as shown in the Figure 4.6. Transistor level circuit diagram is as shown in the Figure 4.7.

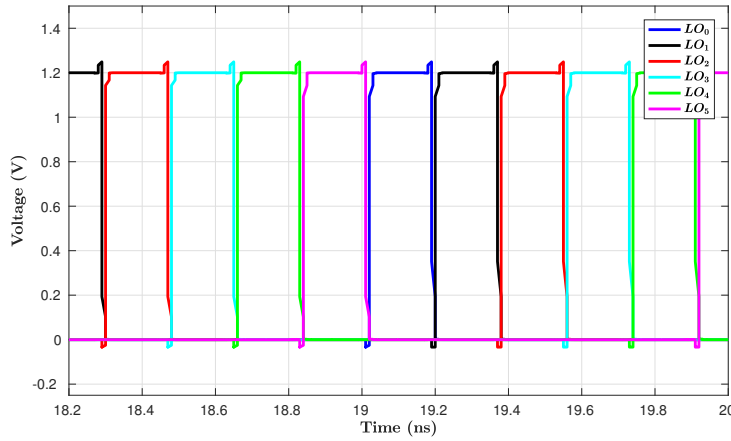


Figure 4.9: Simulated LO divider transient curves

A duty cycle of 16.67% is required for the selected 6-path mixer, and hence after the divider circuitry, a logic circuit based on AND gates is in place as shown in

the Figure 4.8 and the simulated transients is as shown in the Figure 4.9. The mixer switches being reasonably large in size, having to drive them using a large current, a set of buffers are also connected.

Very low phase noise with value equal to -142dB at 100kHz is achieved. The simulated phase noise curve is as shown in the Figure 4.10.

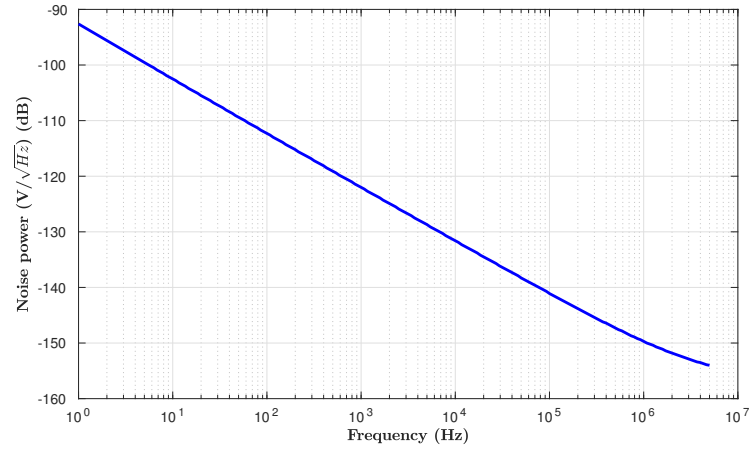


Figure 4.10: Simulated LO divider phase noise curve

Power consumption is found to be equal to 1.387mW at 440MHz which rises to 2.581mW when operated at 2.2GHz.

4.3.4 Base-Band Amplifiers

The OP-amp is the key building block in the BB. For reducing the power consumption without compromising NF and also to give a rail to rail output voltage swing with limited distortions, class AB designs have been explored. The designs from [4, 10] have been used as precursors. The OP-amps are configured fully differential with a local CMFB circuit to set the DC common mode voltage level at the output to 600mV. This ensures the maximum dynamic range for the BB signal through the receiver with a voltage swing of -1.2V to 1.2V at the power supply voltage of 1.2V.

The Figure 4.11 shows a single stage OP-amp whose design is inherited from [4]. Its structure resembles much more like a single stage difference amplifier, with an active resistor load circuit which forms the CMFB circuit of the OP-amp shown in Figure 4.12. The design could achieve a Gain Bandwidth Product (GBW) of 688.635MHz with a DC gain of 43.53dB shown in Figure 4.13. The input transistor sizes had to be increased to mitigate the noise problems. This had an impact on both the input stage operating point DC current and the associated CMFB circuit, whose sizes had to be increased in order to increase its loop gain to fix the output

CM voltage without error. Minimizing the power was given emphasis while adhering to the targets to be achieved. Hence the individual power consumption of the OP-amp was limited to 3.34mW.

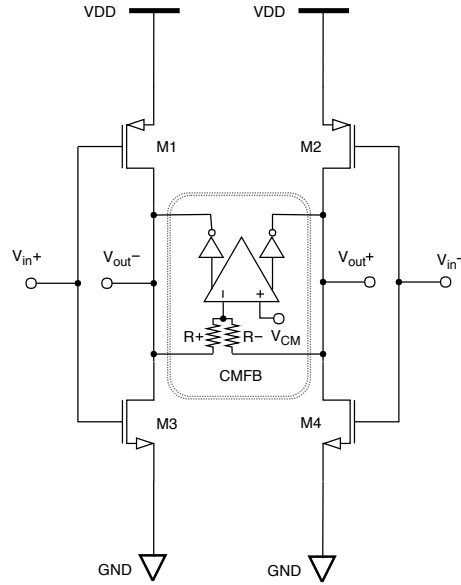


Figure 4.11: One stage operational amplifier [4]

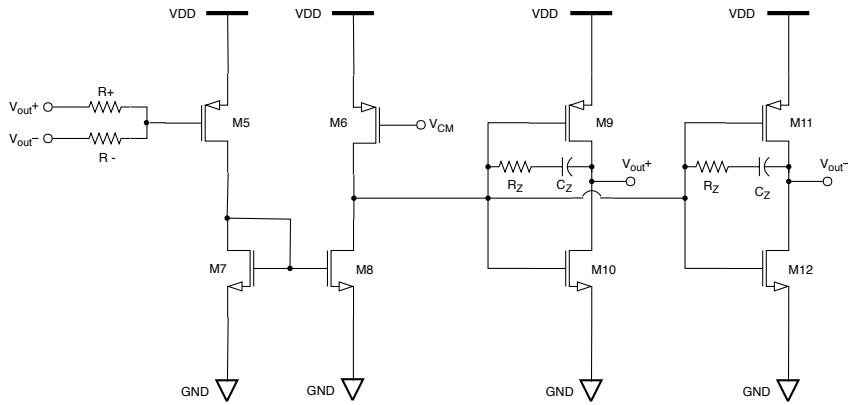


Figure 4.12: One stage operational amplifier CMFB circuit [4]

The OP-amp discussed above was limited to the fact that it could not provide a lower input impedance to the TIA, because its open loop gain is low which is the most important requirement of the current mode operation in LNTA first architectures. This is discussed in detail in the later sections. Due to this reason, a two stage OP-amp originally used in [10] is explored.

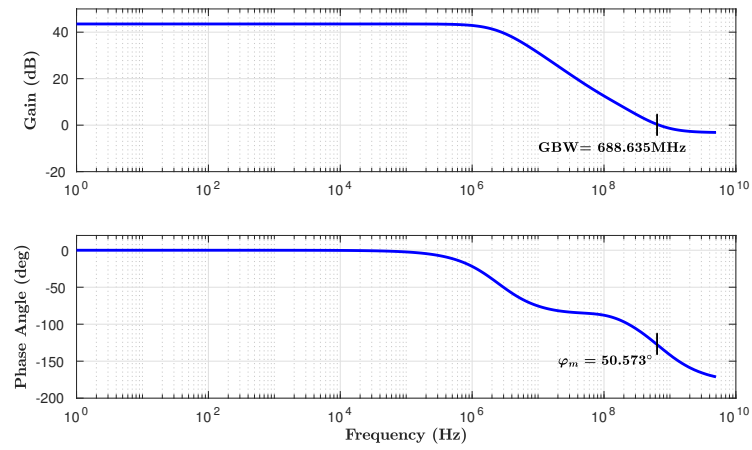


Figure 4.13: One stage OP-amp open loop Gain and Phase

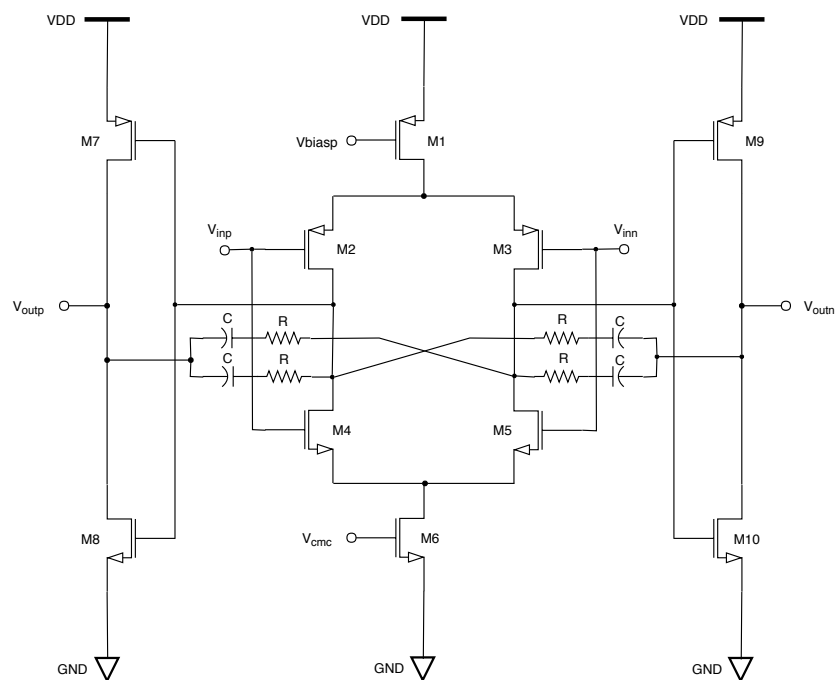


Figure 4.14: Two stage operational amplifier [9]



Figure 10 consists of two vertically stacked plots sharing a common x-axis representing Frequency (Hz) on a logarithmic scale from 10^0 to 10^{10} .

The top plot shows Gain (dB) on the y-axis, ranging from -20 to 60. The gain is constant at 60 dB until approximately 10^5 Hz, then decreases. A vertical line marks the Gain Bandwidth Product (GBW) at 1.6 GHz. The gain reaches -20 dB at 10^{10} Hz.

The bottom plot shows Phase Angle (deg) on the y-axis, ranging from -200 to 0. The phase is constant at 0 degrees until approximately 10^5 Hz, then decreases, reaching -180 degrees at 10^{10} Hz. A vertical line marks the phase margin $\varphi_m = 48.783^\circ$.

Figure 4.16: Two stage OP-amp open loop Gain and Phase

To reduce flicker noise, length of the input transistor have been chosen to be comparatively large and widths were scaled to satisfy the proper width per length

ratio. The values of the OP-amp had been conclusively chosen as shown in the figure, after we could successfully get it to a promising working condition in the receiver architecture. The design of the OP-amps have been refined for the use case requirements for the typical modifications namely, TIA and the summing amplifier which are discussed in the following sections.

4.3.4.1 Trans-Impedance Amplifier (TIA)

A fully differential single-pole TIA, a class of active filter is designed which composes of a OP-amp and passive components i.e. resistors and capacitors. The TIA works in a negative feedback configuration. This filter has bandwidth of 686kHz and 1.5MHz for the single ended Frequency Translational Noise Canceling RX and gain switching LNTA based RX respectively. The purpose of this TIA filter is to amplify the small IB current to a large voltage by providing a large trans-impedance gain, while rejecting any large OB current signal. In addition to this large trans-impedance and low-pass response, the TIA should have a close to zero input impedance, which manifests the voltage swing at the input to be very low irrespective of large incoming current signal. This helps to maintain high linearity of TIA and passive mixers. The filtering in the analog domain also helps to relax requirements of the ADC block.

The trans-impedance gain is defined as the output voltage divided by input current. The gain of the TIA is expressed in terms of Ω . This gain is always equal to the feedback impedance ($R_f + C_f$).

The input impedance ($Z_{i,TIA}$) of the circuit is given by :-

$$Z_{i,TIA} = \frac{Z_{TIA}}{1 + A_v} \quad (4.6)$$

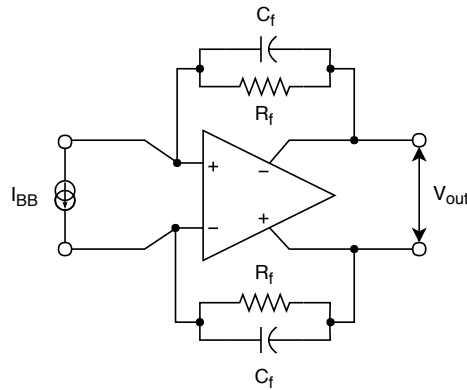


Figure 4.17: Trans-Impedance Amplifier (TIA) with single-pole

where, A_v is the open loop DC gain of the OP-amp and Z_{TIA} is the total feedback impedance.

Equation (4.6) shows that the input impedance of the TIA increases as the open loop DC gain for the OP-amp decreases, which implies, higher open loop DC gain is required to support current mode operation.

As per equation (4.1), for FTNC RX topology, as matching is directly related to TIA input impedance, a single stage OP-amp was used to design the TIA. To operate more in good current mode by lowering the input impedance of TIA, a two stage OP-amp was used to design TIA in the gain switching LNTA based RX topology as two stage OP-amp has the advantage of higher open loop DC gain compared to single stage.

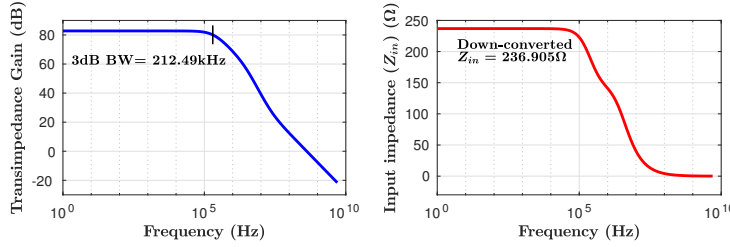


Figure 4.18: Main path TIA

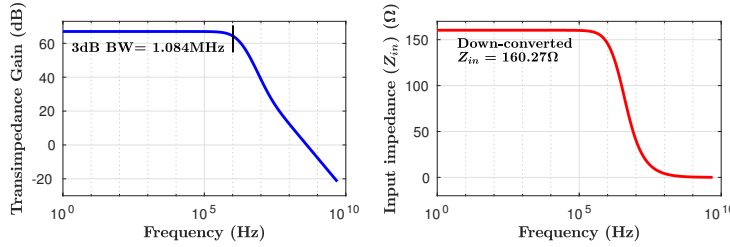


Figure 4.19: Auxiliary path TIA

In FTNC RX topology, in the main path, the value R_f, C_f was chosen to be $7k\Omega$ and $100pF$ respectively to meet the matching requirements. Figure 4.18 plots TIA input impedance with corresponding up-converted input impedance is 35.53Ω and trans-impedance gain is $82.77dB$. In Auxiliary path the value R_f, C_f have been chosen to be $1.2k\Omega$ and $100pF$ respectively to support current mode operation, while simultaneously meeting the noise canceling condition (equation 4.1). The up-converted input impedance is 24.04Ω and trans-impedance gain is $67dB$ as shown in Figure 4.19. The Figures have also depicted the value of down-converted input impedance, which actually corresponds to the value of $Z_{BB}\{\Delta\omega\}$ in the equation 4.2.

In gain switching LNTA based RX topology the value for R_f, C_f have been chosen to be $2k\Omega$ and $100pF$ respectively, to operate in current mode and with a reason-

able bandwidth. The corresponding down converted input impedance is 5.36Ω and trans-impedance gain is 72.02dBV, shown in Figure 4.20.

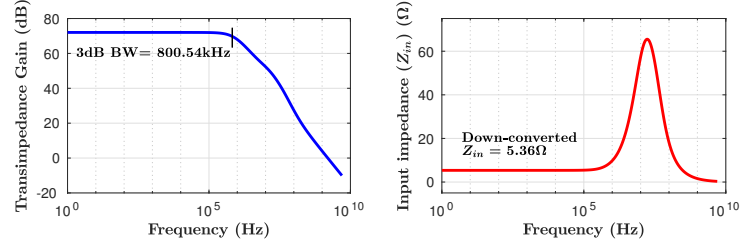


Figure 4.20: TIA Gain plot for LNTA first architecture

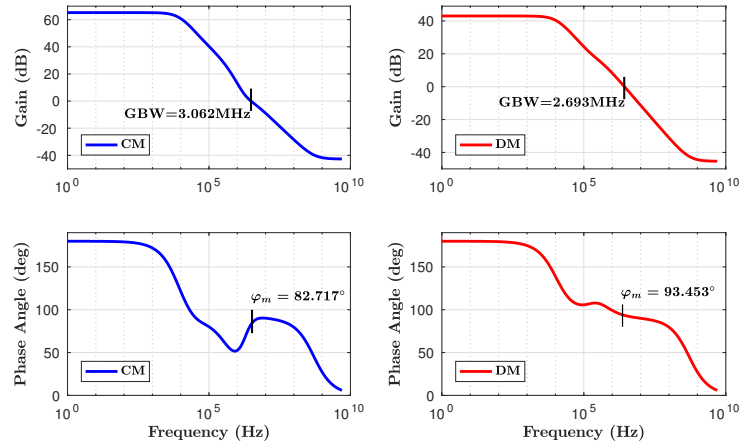


Figure 4.21: Stability plot for Main path TIA

To analyze the stability of the circuit, Loop Stability Analysis with the aid of Spectre's Stability (STB) analysis was performed using CM-Difference Mode (DM) probe. As shown in Figure 4.21, Figure 4.22 the CM loop gain has been found to be equal to 63.23dB, 65.313dB with corresponding phase margin to be equal to 82.71° , 81.59° and DM loop gain has been found to be equal to 43.01dB, 43.21dB with corresponding phase margin to be equal to 93.45° , 91.79° for the main path and auxiliary path TIAs respectively.

Whereas for the TIA used in LNTA first RX the CM loop gain has been found to be equal to 106.4dB with phase margin to be equal to 61.04° and DM loop gain has been found to 66.08dB with phase margin 60.23° . Plots are shown in Figure 4.23.

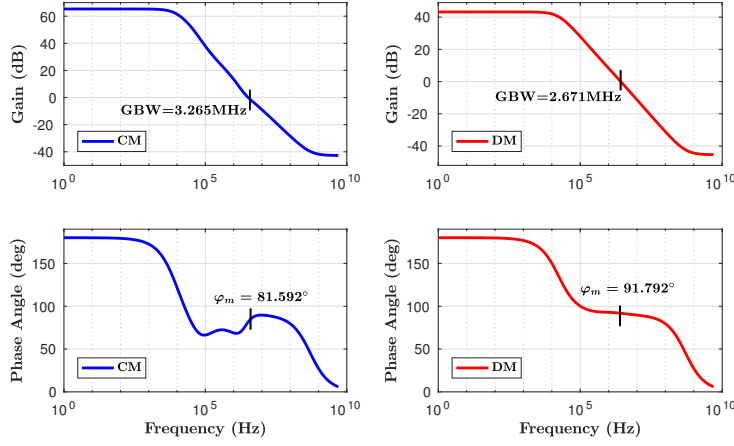


Figure 4.22: Stability plot for Auxiliary path TIA

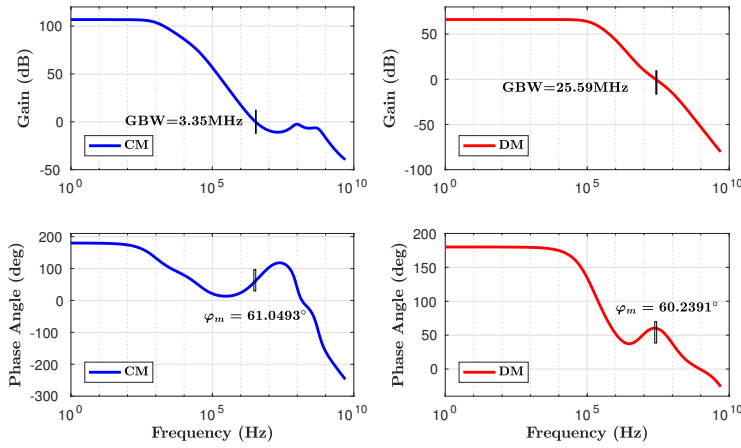


Figure 4.23: Stability plots of TIA used in LNTA first architecture

As phase margin (ϕ_m) are above 60° with reasonable gain values, which is the condition generally defined to ensure a stable system, we can confirm that TIA designed to be highly stable without sacrificing the input impedance and obtained competitive values for bandwidth with respect to our requirements.

4.3.4.2 Summing Amplifier

Following the TIA a Harmonic weighting and recombination stage is used where all the six signals from the TIAs are recombined to produce simple differential I

and Q signals as shown in Figure 4.24 .

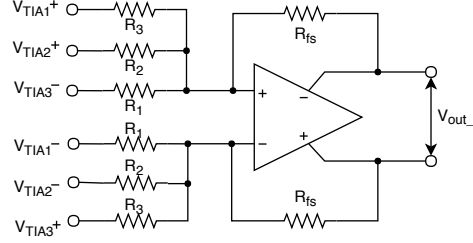


Figure 4.24: Summing amplifier block diagram (shown for I channel)

This combinational network is designed using an summing amplifier. The summing amplifier produces an output voltage (V_{out}) by performing the algebraic sum of input voltages V_1, V_2, V_3 with each branch having individual input resistor values equal to R_1, R_2, R_3 and feedback resistor equal to R_f . To achieve 3rd order harmonic rejection and to obtain symmetrical I and Q signal generation, the equations 4.8, 4.9 have been used. The weighting for the resistors is scaled using these equations. The detailed analysis can be found in [27]. All the input signals are effectively isolated from each other due to virtual ground node at the input of both terminals of the OP-amp.

$$V_{out} = R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \quad (4.7)$$

$$V_i = \frac{1}{\sqrt{3}} \left(\frac{V_1}{\left(\frac{1}{\sqrt{3}+2}\right)} + \frac{V_2}{\left(\frac{1}{\sqrt{3}+1}\right)} - V_3 \right) \quad (4.8)$$

$$V_q = \frac{1}{\sqrt{3}} \left(-V_1 + \frac{V_2}{\left(\frac{1}{\sqrt{3}+1}\right)} + \frac{V_3}{\left(\frac{1}{\sqrt{3}+2}\right)} \right) \quad (4.9)$$

Where V_1, V_2, V_3 are the branch nodes voltages at the input of each terminals and V_i, V_q is the output voltages of I and Q stages respectively.

Using this relation a good third order harmonic rejection of 48dB, and 56dB has been obtained for the single ended Frequency Translational Noise Canceling RX and gain switching LNTA based RX respectively. As theoretical values of weighting was considered which assumes an ideal conditions, finite third order harmonic rejection ratio was observed in this work. Third order harmonic rejection >60dB could be achieved by varying the values of weighting by a small amount, until, an optimized condition is obtained.

Simulations and Results

Detailed trials and simulations have been carried out at each and every level of the design phase. The simulations were performed in the Virtuoso Analog Design Environment L [37] with the aid of Spectre-RF simulator. To study the operations and performance of the circuits, data from various simulations namely, transient responses, Alternating Current (AC) and DC simulations, Periodic Steady State (PSS) responses, periodic small-signal analyses, Periodic Transfer Function (PXF), Periodic S-parameter (PSP) , noise simulations, loop stability checks using Periodic Stability (PSTB) have been recorded. Not only the shooting method, but Harmonic Balance (HB) method is also used for convergence in PSS simulations. This exercise has made us thoroughly understand the functioning of each block in the circuit, and helped us to tune the values in accordance to the design specifications.

This chapter discusses the simulations which were performed over the selected receiver systems and subsequent comparisons that were deduced for an in-depth understanding of the two selected receiver architectures. For simplicity, the block level simulations have already been included in the previous chapter. A variety of variable sweeps have been specifically selected with the intention to find the pitfalls of the design and also to identify the possible scopes of improvement. The results of the simulations run are presented and a comparison is made among the two architectures in the end.

5.1 Receiver simulations

The receiver architectures are designed and simulated in the Cadence Virtuoso [37] software. The simulation targets set are for the nominal Typical-Typical (TT) process corner at a temperature setting of 27°C. The Spectre-RF simulator is used for obtaining the most accurate results. Further, the Monte Carlo simulation involving mismatches in transistors is considered as a special case for finding the trends in LO signal leakage from the mixer to the RF port and to measure IIP2 of

the receivers. The user manuals for these tools have been referred continuously to aid the simulations with the procedures, tips and tricks included within them. The entire exercise has been described in this section and the results obtained have been summarized.

Before going into the detail of the simulations techniques considered and the results obtained for the two selected receiver architectures, a summary on the series of analyses performed in this thesis which are particularly used in RF circuit design are discussed as follows.

5.1.1 Analyses

1. **DC analysis:** This is run to verify the DC operating points, and to ensure that all the transistors are biased properly according to the required regions of operation.
2. **Transient (TRAN) analysis:** This is a normal transient analysis, run to verify the signal transitions in various parts of the circuit under different signal inputs.
3. **AC analysis:** This is a frequency sweep using a small signal model, which outputs the Bode plots of any given outputs with respect to a swept input frequency.
4. **Transfer Function (XF) analysis:** In this the output frequency is swept, and the Bode plots are plotted with respect to any of the input small signal source.
5. **Noise analysis:** This is a small signal analysis, which gives the noise power spectral variations for the given circuit for any identified output port from any given input port.
6. **STB analysis:** The STB analysis is run to find out the loop stability conditions of any closed loop circuits.
7. **PSS analysis:** This is a large signal simulation which is used to obtain the large signal model of the receiver circuit over which other simulations can be run. Here a transient is run for a specific user set time, after which the software runs one more iteration for a period of the fundamental frequency component, and extracts a wide range of values ranging from voltage, current, power etc., plotted against a spectrum or any sweep variable. There are two modes to run PSS namely, the HB method and the shooting method, where the former is based in frequency domain trying to balance out the harmonics while the latter tries to attempt convergence by superimposing the oscillations over the fundamental time period.
8. **HB analysis:** This is another competing approach to simulate the Radio Frequency Integrated Circuits (RFICs) using HB algorithm. The HB algorithm is very efficient, flexible and actually calculates the steady state solution directly. HB is a pure frequency domain technique. The entire circuit

to be simulated is first separated into its linear and non linear sections. A HB solution is found if the interconnect currents for the linear section are the same as the interconnect currents for the non-linear section. Therefore the currents of the linear and the non-linear sections are balanced at each harmonic frequency.

The simulations such as Harmonic Balance AC (HBAC), Harmonic Balance Noise (HBNOISE) and Harmonic Balance S-parameter (HBSP) analyses are run on top of the operating point set using HB analysis.

9. **PXF analysis:** On top of the PSS large signal model, the output frequency is swept logarithmically as a small signal and the transfer functions with respect to the individual signal sources are extracted.
10. **Periodic AC (PAC) analysis:** Again a PSS large signal model is extracted and a small AC signal is run. On contrary to the PXF analysis, the frequency now swept is at the input and the effect off the signal is recorded at the output.
11. **PSP analysis:** This analysis gives the periodic steady state s-parameters measured using the large signal model from PSS.
12. **Periodic Noise (PNOISE) analysis:** This is another analysis which uses the operating point obtained after PSS. It then runs a small signal analysis to identify the noise conditions in the circuit with a sweep over frequency variable.
13. **Quasi-Periodic Steady State (QPSS) analysis:** This analysis gives a faster but lesser accurate periodic state operating point of the circuit. The simulations such as Quasi-Periodic Transfer Function (QPXF), Quasi-Periodic AC (QPAC) and Quasi-Periodic S-parameter (QPSP) analyses are run on top of the operating point set using QPSS. As discussed earlier, QPSS also have two methods of simulation namely, the HB method and the shooting method which behave in the same way as explained earlier.

5.1.2 Simulation techniques

The simulation techniques associated to the RX design are discussed below.

1. **Operating points simulation:** This is mainly the DC simulation to identify the small signal operating points of the circuit, and at the places where we have a large signal, the PSS simulation is run. For the smaller blocks such as the OP-amp, the operating points are set at block level, and since the set value at CM is 600mV in each of the blocks it is visible at the architecture level too. DC power consumption of the circuits are also recorded using this type of simulations.
2. **Frequency response simulation:** This is run using AC or XF for small signals, and their periodic equivalents for large signals. Since the receiver is simulated as a whole, PXF is considered. The frequency at BB output of the

whole RX chain is swept in the simulation, to obtain the gain and bandwidth of the down converted signal as a function of input frequency axis. XF analysis is used when TIA is simulated stand-alone.

3. **Noise Figure simulation:** The NF is simulated using the PNOISE simulation on top of the PSS with setting the output at the BB and plotting the logarithmic equivalent of the measured noise factor, which is duly obtained from the measurements of signal power and noise power at the output and the input source. Its is also used to simulate the phase noise arising from the LO circuits.
4. **Compression curve simulation:** This is the first order linearity simulation run for the whole RX as well as LNTA stand-alone. The single tone in the frequency of interest, just the same as LO is fed at the input port in the RX test bench with variable input power. A PSS simulation is now run sweeping the input power with the HB method. The curve is then plotted for the output power against the swept input power. The point where the curve starts to deviate from slope 1 linearity by 1dB is measured as the 1dB Compression point (CP1dB).
5. **Cross compression simulation:** In addition to Compression curve simulation, the cross compression simulation is run with the combination of PSS and PAC. This simulation helps us to understand at what OB input blocker power the RX gets compressed. The blocker power at a large offset of 100MHz is swept at the input port and the large signal operating point is obtained using PSS. A PAC simulation is run on top of it, with a small offset $\approx 100\text{kHz}$ from the LO frequency without any variable sweep. This returns the plot with Power gain against the blocker input power value.
This same exercise can also be performed using HB analysis along with HBAC simulation to achieve faster results.
6. **Higher order linearity simulation:** The Intercept points extracted out of the power transfer characteristics with the extrapolated lines from the second order and third order output harmonics with the fundamental correspondingly refers to 2nd order intercept point (IP2) and 3rd order intercept point (IP3). The points determine the second order and third order linearities of the receiver circuit. To simulate this curve, a QPSS simulation is run with two large tones with a fixed offset from the LO is input at the port such that their IM3 product is always IB of the receiver, a simultaneous power sweep of both tones are simulated and the possible combinations of frequency domain products are summarized into a table after the simulation. From the list in the table, the required harmonics are selected and plotted to get the IP2 and IP3.

In order to plot IB and OB third order linearity in a signal curves respectively HB analysis have been used. Two tones with a constant amplitude were considered at $F_{lo} + (2 \cdot \text{offset})$ and $F_{lo} + 110\text{kHz} + \text{offset}$, and the offset were varied simultaneously from 1kHz to 100MHz so that their 3rd order inter-modulation (IM3) product appears at 110kHz offset from DC. The power of the IM3 products was recorded for each offset which was

extra-polated using co-ordinate geometry along with a first order IB signal with same amplitude to drive the IIP3 curve. Similar exercise was performed to simulate IIP2 with respect to offset but in this case, the tones were set at $F_{lo} + offset$ and $F_{lo} + 110kHz + offset$, whereby their IM2 products appear IB. A Monte Carlo simulation was run on top of it to consider the variation with respect to mismatches.

7. **Monte Carlo simulation:** The simulation technique involves introduction of mismatches among transistors and over the process corners to get a good estimate on the expected deviations that can occur as an outcome of the potential fabrication run. The output is a histogram with the statistical values of the design namely, mean, variance, standard deviation, etc,. A given parameter or expression is set as the output and the associated simulation is run over a large number of points, where more the number, the better the estimates. This process helps to find the variations with respect of process and mismatches and hence the yield of such a design fabrication run.

The above techniques have been rigorously employed in the experiments conducted in the work. The simulations were run with a clear trade off between precision versus time taken. Typical examples included such as QPSS being a faster simulation compared to PSS, the former was used to repeatedly tune the receiver for various parameters including CP1dB, IIP3, IIP2, and finally running PSS once the tuning was complete. This is in support with the fact that the PSS simulations are much more precise than QPSS.

5.1.3 Frequency Translational Noise Canceling- RX

In FTNC- RX, the simulations are run for two sets of conditions namely, the noise canceling OFF and noise canceling ON. In Noise canceling OFF condition, only the main path is active and as a result the DC power consumption is recorded low with a value of 18.63mW at $f_{lo} = 925\text{MHz}$ as shown in Figure 5.1.

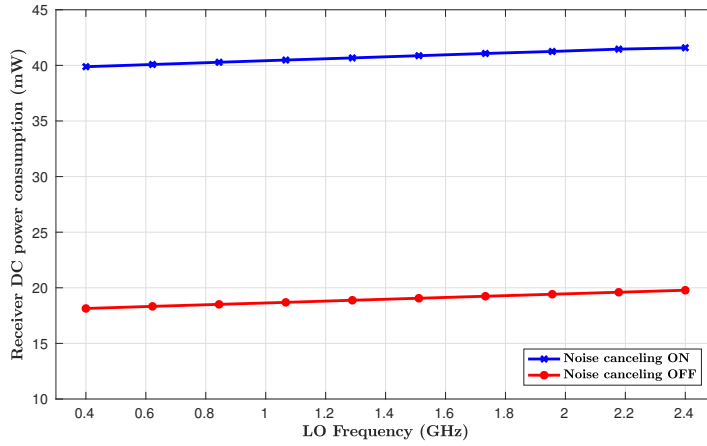


Figure 5.1: Simulated DC power consumption versus LO frequency

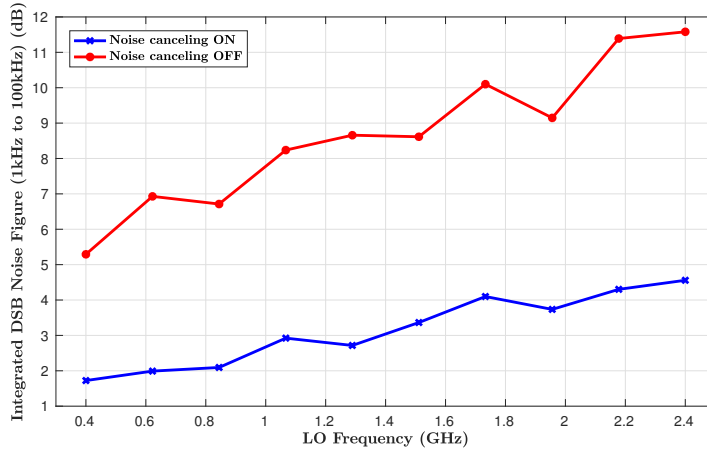


Figure 5.2: Simulated integrated NF versus the LO frequency

From the simulation curves as shown in Figure 5.2, it is evident that low power consumption comes at the cost of NF which is simulated to be 7dB integrated over a bandwidth of 1kHz to 100kHz with $f_{lo} = 925\text{MHz}$. With the idea to im-

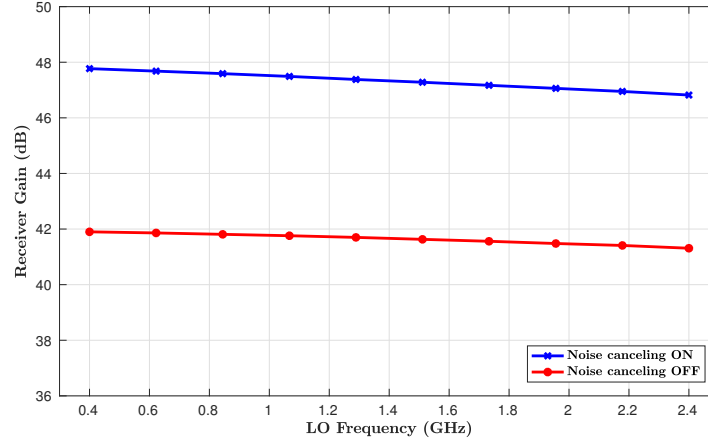


Figure 5.3: Simulated RX gain versus the LO frequency

prove the NF, if the auxiliary path is included in the simulation, the NF drops ≈ 2 dB which is also shown in the Figure 5.2. The equivalent penalty in the DC power is ≈ 40 mW as given in the Figure 5.1 which compares the both cases. The corresponding gain obtained is 41.9 dB and 47.8 dB for the noise canceling OFF and noise canceling ON conditions respectively over the range of RF frequency of operation for RX front-end is shown in the Figure 5.3. NF increases at higher frequency as flicker noise arising from LO dividers become more profound.

Figure 5.4 shows simulated S11 with the courtesy of main path which is < -10 dB over the wide frequency bandwidth of operation assuming RF port impedance to be equal to 50Ω implying a very good matching being achieved.

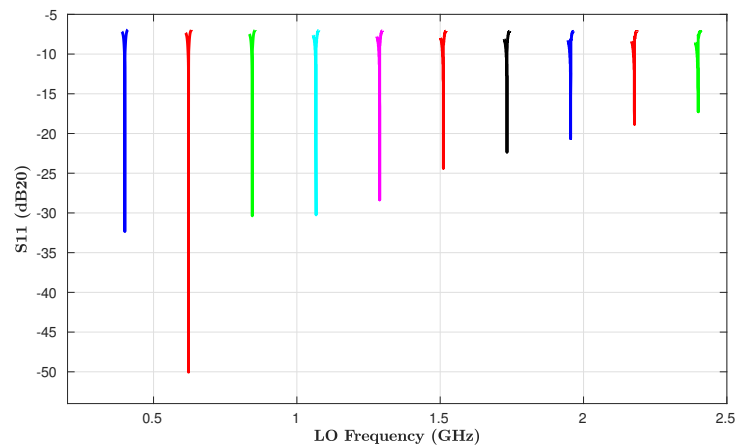


Figure 5.4: Simulated S11 versus the LO frequency

A very good performance of LO leakage has been recorded as shown in Figure 5.5 which plots spurious emission from LO circuits over the wide frequency bandwidth of operation under matched condition and Figure 5.6 which plots the LO leakage considering process and variation mismatches which is same for both conditions with are convincingly $< -59\text{dBm}$ to adhere the IoT specifications. Being a mixer first architecture, LO leakage has been found considerably lower compared to the gain switching receiver which will be discussed in the next section.

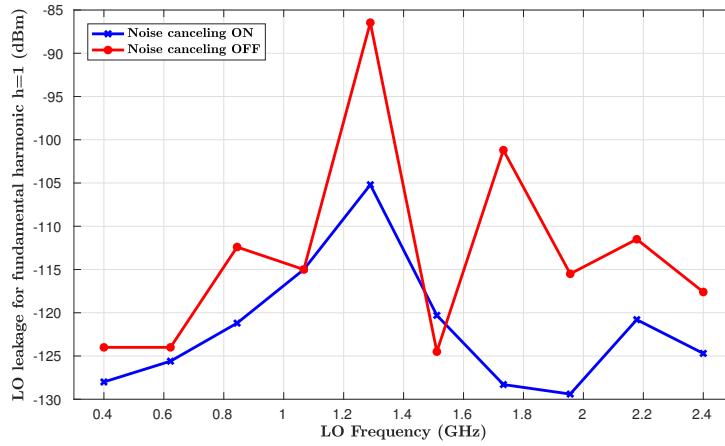


Figure 5.5: Simulated LO leakage at the RF port versus the LO frequency

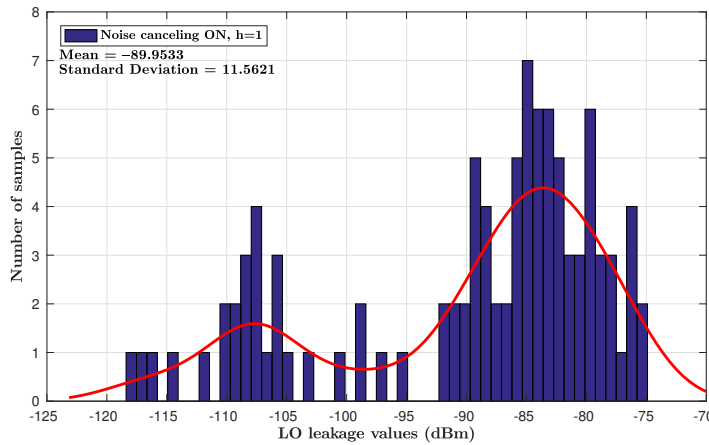


Figure 5.6: Simulated LO leakage at the RF port with respect to mismatch at $f_{lo} = 925\text{MHz}$

Unacceptable aliasing of signal at third order harmonic of wanted frequency is

avoided with a decent third order harmonic rejection $>39\text{dB}$ as shown in the Figure 5.7 for both the conditions. Third order harmonic rejection is lowered when auxiliary path is turned off due to limited loop gain in the main path.

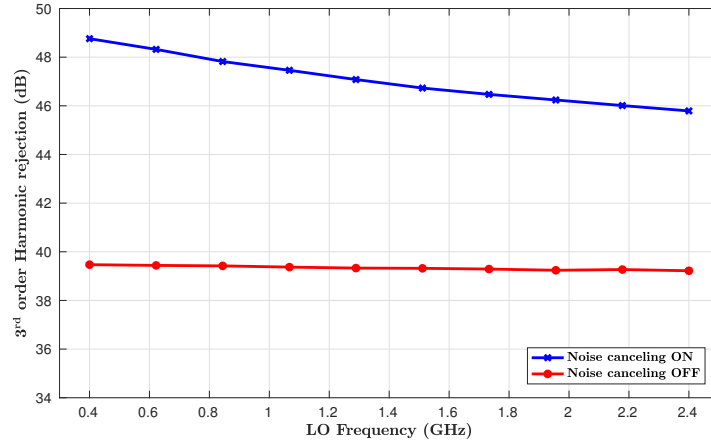


Figure 5.7: Simulated 3rd order harmonic rejection versus the LO frequency

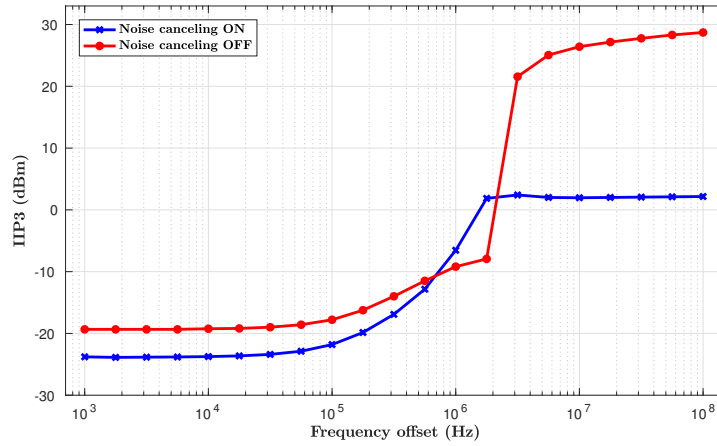


Figure 5.8: Simulated IIP3 using two-tone test with respect to offset frequency at $f_{lo} = 925\text{MHz}$ and input power of wanted signal to be equal to -60dBm

The 2nd order and 3rd order linearities for the architecture are substantially high in the presence of OB unwanted signal. An OB IIP3 value of $>0\text{dBm}$ is obtained which is true for both cases as portrayed by the plotted curves in the Figure 5.8

and considering mismatches, an OB IIP2 value of >30dBm is achieved for noise canceling on condition which is the worst case having highest gain as shown in Figure 5.9. Noise-canceling off mode being a mixer first RX topology, OB IIP3 are found to be substantially high. Also IB IIP3 of -15dBm to -25dBm and IIP2 of >20dBm have been achieved. Difference in IB IIP3 is seen due to increase in gain as Auxiliary path is turned on.

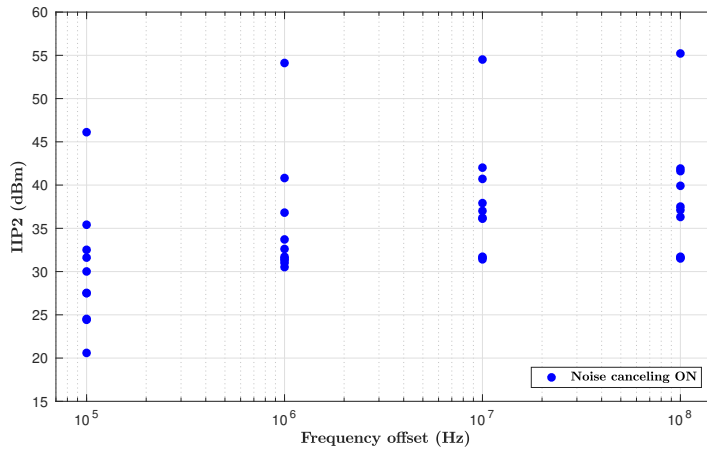


Figure 5.9: Simulated IIP2 using two-tone test with respect to offset frequency for Noise canceling on condition at $f_{lo} = 925\text{MHz}$ and input power of wanted signal to be equal to -60dBm

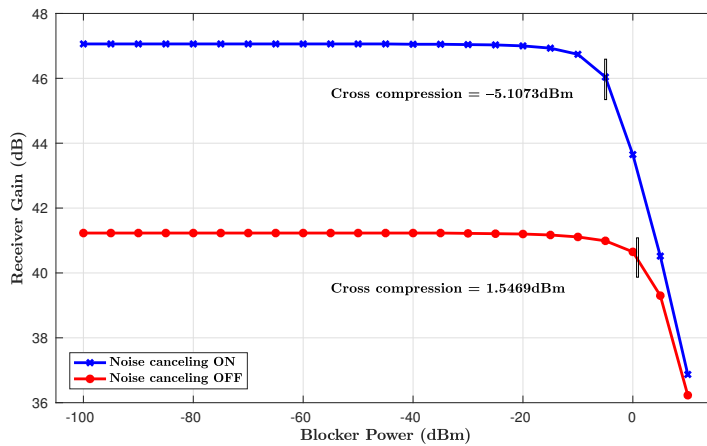


Figure 5.10: Simulated receiver gain with blocker signal located at 100MHz offset at $f_{lo} = 925\text{MHz}$

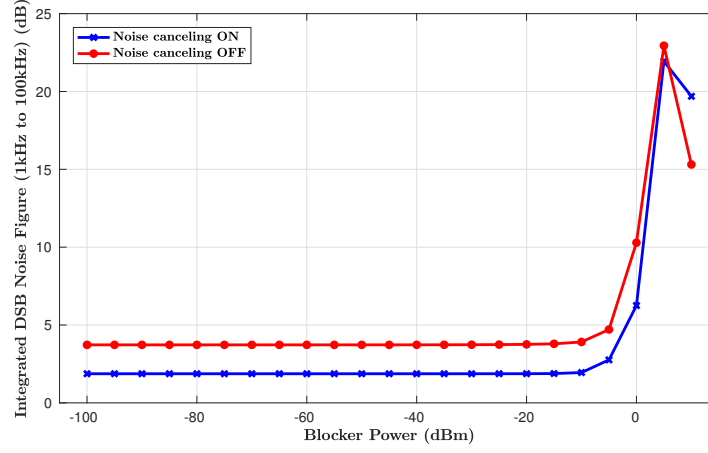


Figure 5.11: Simulated NF with blocker signal located at 100MHz offset at $f_{lo} = 925\text{MHz}$

The simulated gain and NF with respect to swept power of OB blocker signal at 100MHz offset and a small wanted signal at 100kHz offset and $F_{lo} = 925\text{MHz}$ is shown in the Figure 5.10 and Figure 5.11. Expectedly the receiver could tolerate blocker signals as high as -6dB and NF is only degraded by roughly 2dB in the presence of -15dBm blocker signal. For noise canceling ON condition the receivers gets compressed at a lower input power compared to noise canceling OFF conditions because gain get increased when Auxiliary path is switched on.

5.1.4 Gain switching LNTA based RX

Following results are for LNTA based RX with LNTA in gain reduction modes (-3dB and -6dB) as shown in the Figure 5.12. The advantage of variable gain control at RF is to lower the DC power consumption in the presence of large wanted signal and improve linearity. The power consumption reduces by 7mW and 14mW respectively, shown in Figure 5.13 by disabling some of the g_{mp} and g_{mn} stages in the LNTA. This gain reduction leads NF to degrade by ≈ 1 dB to 3dB shown in Figure 5.14. NF increases at higher frequency as flicker noise arising from LO dividers become more prominent.

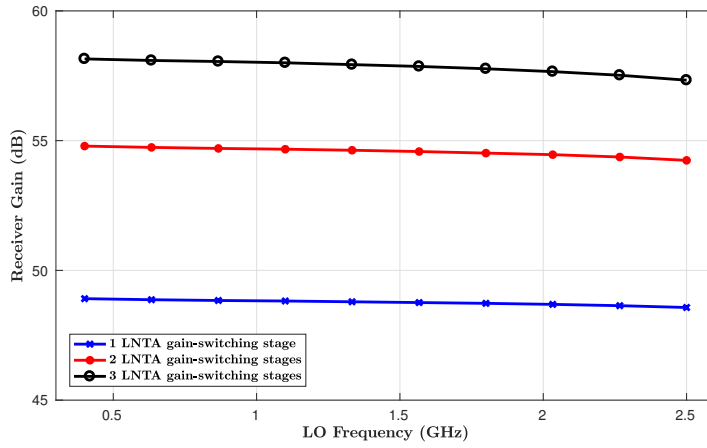


Figure 5.12: Simulated gain versus the LO frequency

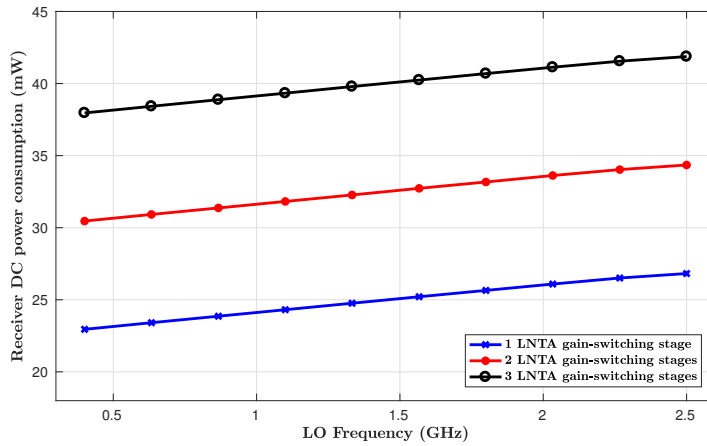


Figure 5.13: Simulated DC power consumption versus the LO frequency

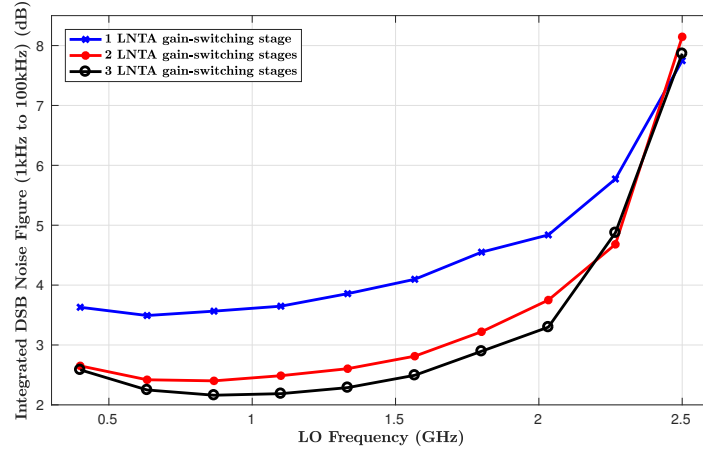


Figure 5.14: Simulated integrated NF versus the LO frequency

Figure 5.15 shows decent matching performance of $<-15\text{dBm}$ with respect 50Ω load for the wide frequency bandwidth of operation for RX front-end.

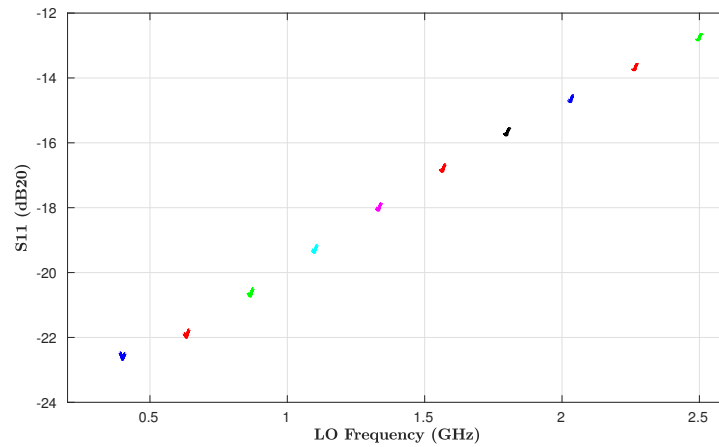


Figure 5.15: Simulated S11 versus the LO frequency

As shown in the Figure 5.16 spurious emission from LO circuits are significantly $<-59\text{dBm}$ over the range of frequency of operation which meets the requirements. Figure 5.17 plots the LO leakage considering process and variation mismatches which is same for all modes of operation with are convincingly $<-59\text{dBm}$ whereby adheres to the NB-IoT specifications. LNTA is connected to the antenna followed by a double balanced mixer helps to reduce LO leakage.

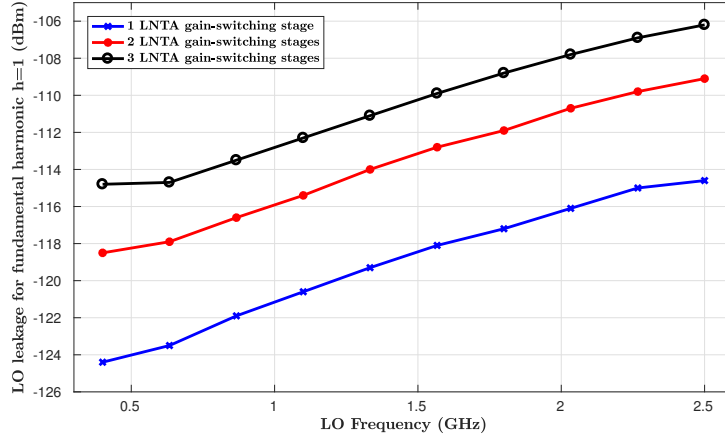


Figure 5.16: Simulated LO leakage at the RF port versus the LO frequency

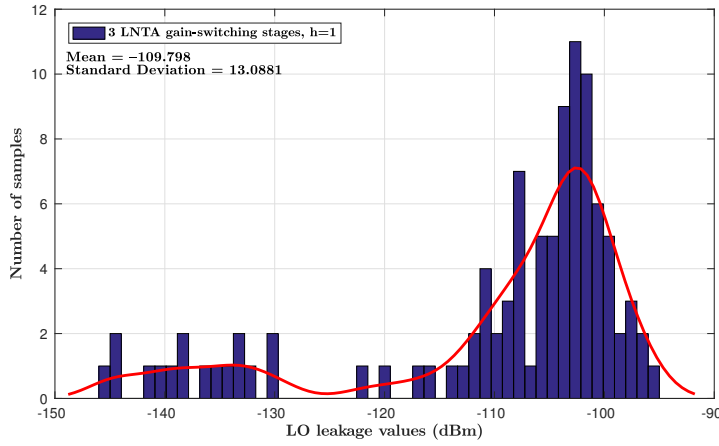


Figure 5.17: Simulated LO leakage at the RF port with respect to mismatch at $f_{lo} = 925\text{MHz}$

A excellent 3rd order rejection of >52dB is recorded with negligible variations observed when LNTA operated in different modes as shown in the Figure 5.18.

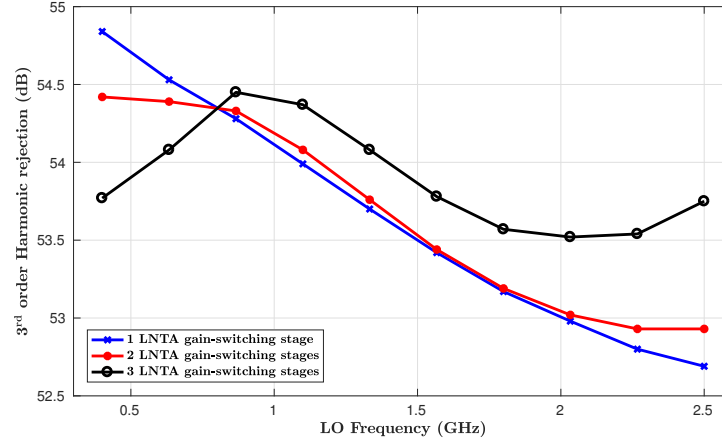


Figure 5.18: Simulated 3rd order harmonic rejection versus the LO frequency

The 2nd order and 3rd order linearities for the architecture are reasonably high in the presence of OB unwanted signal. An IIP3 value of >-10 dBm for all the 3 modes is achieved as shown by the plotted curves in the Figure 5.19 and considering mismatches an IIP2 value of $+48$ dBm was achieved for worst case i.e., with all stages have been enabled as shown in Figure 5.20. Input power of the two tones were equal to -60 dBm. IB IIP3 varies from -9 dBm to -28 dBm due to limited loop gain of the RX which reduces as output resistance of the LNTA reduces, which gets lowered as more gain stages are enabled.

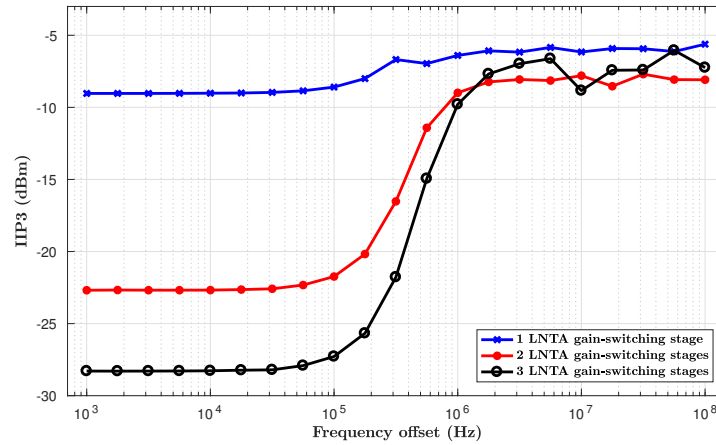


Figure 5.19: Simulated IIP3 using two-tone test with respect to offset frequency at $f_{lo} = 925$ MHz

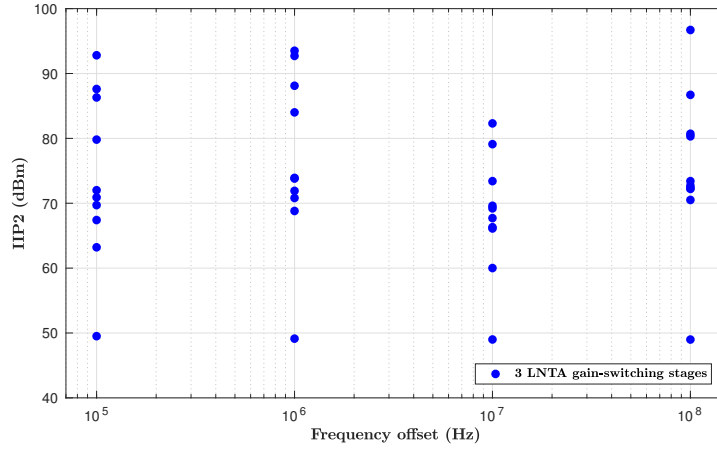


Figure 5.20: Simulated IIP2 using two-tone test with respect to offset at $f_{lo} = 925\text{MHz}$

The simulated gain and NF with respect to swept OB blocker at 100MHz offset with a small wanted signal at 100kHz offset and $F_{lo} = 925\text{MHz}$ is shown in the Figures 5.21 and 5.22 respectively. Remarkably the NF is 3dB in the presence of -15dBm blocker, but the receiver gain gets compressed when blocker power as low as -19dBm is present at the input.

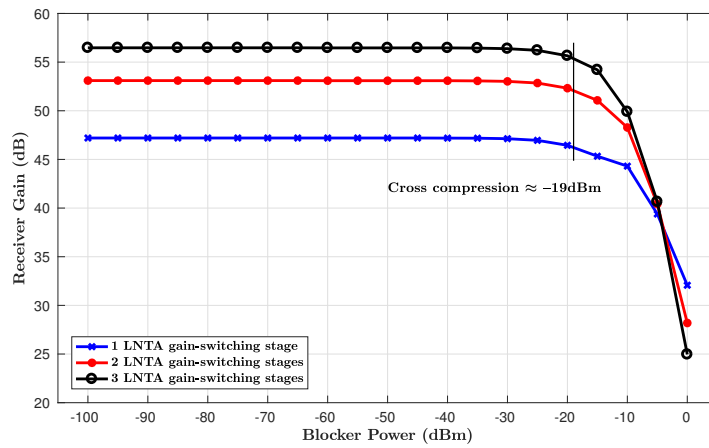


Figure 5.21: Simulated receiver gain with blocker located at 100MHz offset at $f_{lo} = 925\text{MHz}$

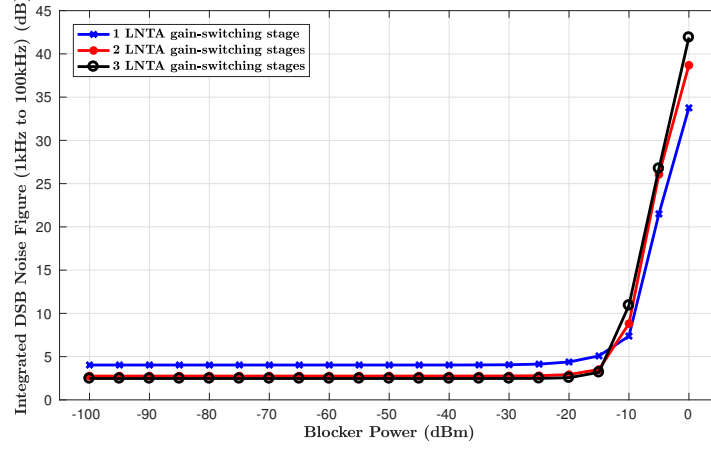


Figure 5.22: Simulated NF with blocker signal located at 100MHz offset at $f_{lo} = 925\text{MHz}$

5.2 Receiver comparisons

Parameter	FTNC RX	Gain switching RX
Architecture	Mixer first	LNTA first
RF Frequency [MHz]	450-2200	450-2200
RX Input	Single-Ended	Single-Ended
RX Gain [dB]	41.5-47.8	49-58
NF @ $F_{lo} = 925\text{MHz}$ [dB]	2-7	2.1-3.6
BB Bandwidth [kHz]	636	1619
NF w.r.t. -15dBm blocker @ 100MHz offset [dB]	2.1-4.8	2.5-5
Third order harmonic rejection [dB]	39-49	52-54.7
IB IIP3 [dBm]	(-25) - (-20)	(-28) - (-9)
IB IIP2 [dBm]	+20	+48
OB Blocker Tolerance @ 100MHz offset [dBm]	-5.1-1.54	-19
LO leakage with mismatch @ $F_{lo} = 925\text{MHz}$ [dBm]	< -91.61	< -114.265
S11 [dB]	< -18	< -12
DC power consumption [mW]	16-39	22-38
Supply voltage [V]	1.2	1.2
Process corners	TT	TT
CMOS Technology [nm]	40	40

Table 5.1: Receiver front-end comparisons

From the above set of simulations, it is very evident that each architecture has its own pros and cons which are the key identifiers for understanding the most promising one for the application of interest of this thesis. For this, a separate discussion is made in the next chapter where we bring about the conclusions of our study in this thesis.

Conclusions

A detailed study among front end RX architectures for the NB-IoT application have been carried out, leading to a selection of two promising architectures, which are designed at circuit level. The simulations run on them have helped to gain more insight with respect to their operational capabilities and performance. The exercise has also shown that a necessary but significant trade-off exists between the NF and the DC power. Linearity of the receivers can be maximized if the receivers are operated mostly in current mode and also with the use of simple designs such as inverter LNTA and passive mixers. The analysis also reveals that the noise canceling circuit techniques help to improve the NF of the receiver front end, not limiting its performance but with a decent gain and linearity.

The comparisons among the two selected architectures: a FTNC- RX and a gain-switching LNTA based RX shows that the former provide relaxed trade-offs between linearity and noise figure and can perform much better with respect to the blocker tolerance specifications while a better gain (which is also programmable) is achieved by the latter with reasonably larger noise figures. Both of them adhere to the 3GPP specifications for NB-IoT while achieving most of the thesis targets of wide-band, low-power and blocker tolerant, except the BB bandwidth of both receivers are at higher side and gain-switching LNTA based RX falls short of 4dBm with the OB blocker tolerance requirements mandated by the 3GPP which is -15dBm. In hindsight, both of these can perform much better and fulfill to 100% requirements if the power consumption limits can be enhanced by around 5-10mW from the ≈ 40 mW existentially consumed by either of them when they are best performing.

An important feature of the designs are that each of them are single ended at the RF input port, which enables a balun free operation, which thus indirectly aids to mitigate the insertion loss of such an element, if considered to interface at the antenna. The insertion losses could have directly impacted upon the NF values degrading them further. Also, each of the architectures are individually comparable to the performance of the receivers using an RF SAW filter while being largely tunable such that they could possibly accommodate a large RF bandwidth.

The thesis work could be completed within an approved time frame, and is considered to be largely successful. This was a good learning experience in terms of the study of RFIC design as well as the technological know how of the product design cycle in the industry. As students, this project has given us a good beginning to pursue an industrial career.

Future Work

The thesis work has accomplished the objectives largely, but however, a lot more work could be done with respect to refining the existing design and the exploration for newer solutions. A set of identified future works are discussed in this chapter.

With respect to the existing design, improvements can be made in the gain switching LNTA based RX, in order to tolerate large OB blockers of power -15dBm by either increasing the power supply voltage of the A_m stage or by redesigning the stage to give a better noise performance at a lower voltage gain. The linearity performance of the architecture can be enhanced by using sub-Vt transistors in parallel with the input transistors of g_{mp} stage as discussed in [9]. It has also been observed that the noise performance of both of the selected architectures degrade over increase in LO frequency. The cause for this has been identified as the flicker noise generated by LO divider circuitry at higher frequencies whose design improvements can also be carried out as a future work. Additionally, higher order baseband filtering using active filters can be provided after the TIA block in order to achieve sharper roll-offs for better selectivity in the receiver architectures.

The design of a complete RF front end with RF switch and ADC could be simulated and studied to find the robustness of the receiver design. This will also reveal onto exact measurement of the sensitivity of the receiver RF system. This can be then tested along with additional digital hardware for gain switching and Automatic Gain Control (AGC) of the receiver to test the performance degradation in the presence of a large modulated OB blocker as a future work.

A complete layout of the design can be drawn to find out how much variations can be expected with respect to the schematics in an actual implementation. Additionally, a chip tape out followed by a rigorous test cycle will reveal onto the extent of adherence of the real chip hardware with respect to the simulation results. This will help to understand the downsides of our design and shall enable us to improve further on it with respect to efficiency, power output, and area.

Methods of noise cancellation can be explored as given in the paper [38]. Newer architectures, [39,40], to mention a few of them could be explored, which tend

to achieve a good noise performance at a lower DC power. More architectures based on the methods mentioned in the above works can also be explored.

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