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Fully integrated standard cell digital PLL

T. Olsson and P. Nilsson

A fully integrated digital phase-locked loop (PLL) used as a clock multiplying circuit is designed. The PLL is made from standard cells found in almost any commercial standard cell library and therefore portable between processes in netlist format. Using a 0.35μm standard complementary metal-oxide-semicondctor CMOS process and a 3.0V supply voltage, the PLL is designed for a locking range of 170 to 360MHz and occupies an on-chip area of 0.06mm².

Introduction: The phase-locked loop (PLL) is a widely used circuit for clocking digital IP blocks. Traditionally, a PLL is made as a partly analogue building block. However, integrating an analogue PLL in a digital noisy environment is difficult. In addition, the analogue PLL is sensitive to process variations and must therefore be redesigned for each new process.

Robust and easily implemented fully digital clock multipliers without phase-locking are proposed in [1, 2]. However, for a number of applications, using for instance synchronous on-chip communication, a PLL is necessary to ensure correct functionality.

This Letter describes the implementation of a digital PLL. The digital PLL is designed as an IP block portable between technologies in netlist format using for instance VHDL or Verilog. For most digital applications, a netlist description of the PLL simplifies the design, since the design including the PLL becomes portable between technologies.

Implementation: The block structure of the digital PLL is divided into a phase detector, a loop filter and an oscillator. The phase detector is a slightly modified standard type IV detector [3]. The loop filter consists of a counter and a first-order digital recursive filter. The counter performs an integration of the output from the phase detector. The result is then filtered using the digital filter. The oscillator is a numerically controlled oscillator (NCO).

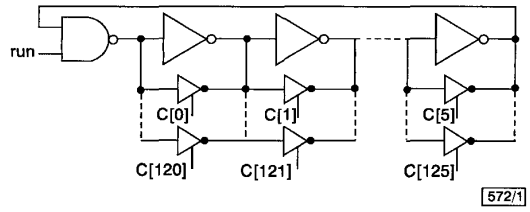

Fig. 1 *Numerically controlled oscillator*

Numerically controlled oscillator: The difficulty when making an all-standard cell PLL is often to implement an oscillator with high resolution. Often, a variable number of inverters are used for implementing a variable delay. However this results in delay steps of several hundred ps which gives an inaccurate and unstable phase-lock for high frequency applications.

The oscillator for the digital PLL is a seven-stage ring oscillator with one inverter replaced by a NAND-gate for shutting down the ring oscillator during idle mode. To change the frequency of the ring oscillator, a set of 21 inverting tri-state gates are connected in parallel with each inverter (see Fig. 1). When the tri-state gates are enabled additional current drive is added to each inverter stage. The tri-state gates are controlled by a 126 bit vector (**C**), which is decoded from a seven bit control word (W). The vector **C** is all ones for $W = 0$ and all zeros for $W = 125$ to 127. For $W < 126$, the number of zeros in **C** is equal to W.

The period time against digital control word for the NCO at 3.0V supply is shown in Fig. 2. The plot in Fig. 2 has a slope of between 10 and 55ps/bit. It is important to keep the slope low since the slope sets the resolution of the NCO. A negative slope must also be avoided, since this might cause the PLL to be unstable. However, because of how the decoding from W to **C** is made, the slope cannot be negative.

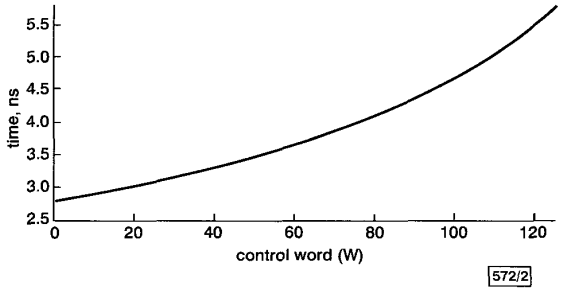

Fig. 2 *Period time against digital control word (W)*

Phase detector: The type IV phase has in its original configuration two outputs controlling the oscillator frequency: one for signalling 'UP' and one for signalling 'DOWN' for the duration of the phase error. This is slightly modified to produce one signal 'UP' or 'DOWN' and one signal 'EVENT' showing the length of the phase error.

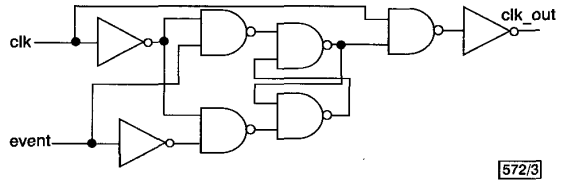

Fig. 3 *Clock gating circuit*

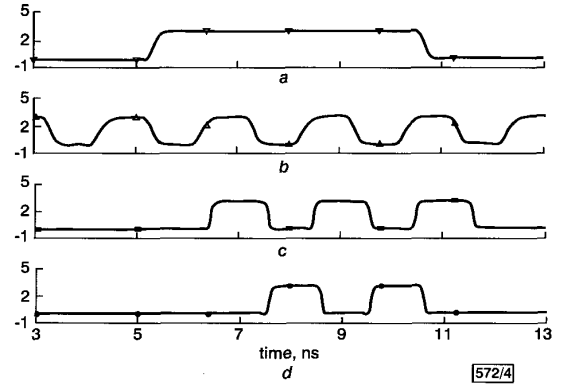

Fig. 4 *Gated clock pulses*

a Event
b clk
c clk_counter 1
d clk_counter 2

Loop filter: The loop filter consists of a counter and a first-order digital recursive filter. The counter measures the phase error and the result from the counter is used to update the control word for the NCO. To obtain a high resolution when measuring the phase error, the counter is preferably clocked at a frequency higher than the output from the NCO. To keep this frequency as low as possi-

ble, flanks instead of complete pulses are counted during the phase error. This enables use of the output from the NCO instead of implementing an extra oscillator. However, using flank counting and a faster oscillator gives a shorter lock time (step response) and less phase noise.

The circuit of Fig. 3 is used for gating a clock signal when 'EVENT' is low. The clock pulses at the output 'clk_out' are always complete pulses.

Two three bit counters are equipped with the circuit of Fig. 3. One counter is clocked with the gated version of the clock and the other counter is clocked with the gated version of the inverted clock. Fig. 4 is a simulation showing the 'EVENT' signal, the clock signal and the clock bursts counting up the two counters. The result from the two counters is then added to obtain the number of clock flanks during the phase error.

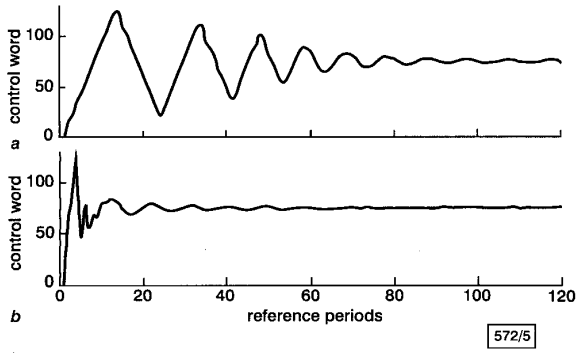

Fig. 5 *Step response*

a Before improvement
b After improvement

Since the counters are only three bit wide, they will often saturate during the initial phase of an impulse response. To achieve a faster impulse response and thereby a shorter lock time for the PLL, the output from the counters is multiplied by 4 whenever both counters are saturated. The effect of this is shown in Fig. 5, where the lower plot shows the improvement in step response.

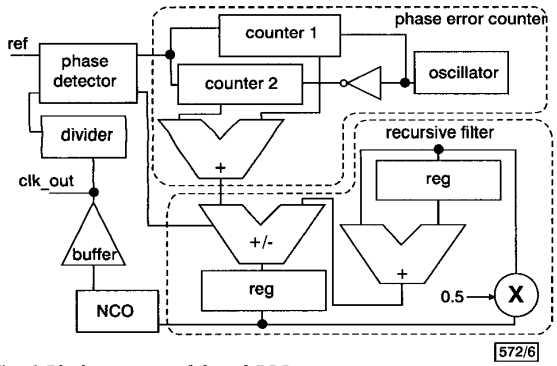

Fig. 6 *Block structure of digital PLL*

Design overview: Fig. 6 shows the block structure for the digital PLL. The phase detector is controlling the two counters, which in this configuration are clocked by an extra oscillator. The sum of the two counters is added to the output of the digital filter once each reference period. The output of the NCO is divided by the multiplication factor and then contrasted in phase to the reference.

Conclusions: A prototype of a standard-cell digital PLL clock multiplier is designed using a 0.35μm CMOS process. The digital PLL is designed for a frequency range of 170 to 360MHz and occupies 0.06mm^2 of on-chip area. Instead of a charge pump and an analogue filter, two three bit counters and a recursive digital filter are used as a loop filter. A numerically-controlled oscillator with high resolution is made from a ring oscillator with additional tri-state gates. The high resolution enables accurate frequency control and low phase noise. The digital PLL is implemented using cells found in an ordinary commercial standard cell library, which makes it portable between technologies in a netlist format.

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Switched-capacitor resonator structure with improved performance

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A novel switched-capacitor resonator circuit is proposed. Its centre frequency is insensitive to the finite bandwidth and gain of the opamps used.

Introduction: Bandpass ΔΣ modulators are used for the direct digitisation of the IF signals in wireless personal communication systems. They are usually implemented using switched-capacitor (SC) resonators [1 – 3]. These resonator circuits suffer from analogue circuit limitations when the clock frequency (f_{clk}) is high. The limitations include the finite unity-gain-bandwidth (f_u) and DC gain (A_{dc}) of the opamps used. If these two design parameters are not adequate, there will be both resonator gain loss and shift in the centre frequency location. The gain may be boosted with circuit techniques such as correlated-double-sampling (CDS) [4]; conversely, the shift in centre frequency will introduce large out-of-band noise into the desired signal band. Thus, it is desirable to have a resonator structure with a centre frequency that is insensitive to opamp nonidealities. The novel architecture proposed herein has two integrating paths. Hence, we named it integrating-2-path (I2P) structure. Its performance is contrasted, below, with three other well-known SC resonator structures, i.e. the pseudo-N-path (PNP) [1], the two-delay loop (TDLL) proposed by Longo and Hong [2], and the two-delay loop (TDLB) by Bazarjani and Snelgrove [3].

Resonator transfer function: The ideal transfer function of the resonator discussed is

$$H(z) = \frac{z^{-1}}{1 + z^{-2}} \tag{1}$$

This translates into the input-output relation; $v_o(n) = v_{in}(n-1) - v_o(n-2)$. Nonidealities of the opamp act to modify $H(z)$ into

$$H(z) = \frac{(1-a)z^{-1}}{(1-d) + bz^{-1} + (1-c)z^{-2}} \tag{2}$$

The peak gain loss results from error terms c and d, which affect the quality factor Q of the resonance peak. The shift in centre frequency is introduced by the error term b. The error term a also introduces a gain loss but this is very small contrasted to that caused by terms c and d.

Resonator structures: The I2P circuit is shown in Fig. 1. In this structure, the differential voltage occurring two clock periods before is stored in the C_1 capacitors during odd clock phases. This pair is then interchanged in the next clock phase to realise the resonator transfer function. The same operation is performed by the other pair (C_2) in even clock phases. This operation prevents the introduction of odd-order terms in the denominator of $H(z)$ and the mixing of the gain and leakage errors. The actual transfer function becomes