Nanoscale MOSFETs 2017 – Excercise 6

1. We will here compare the width efficiency for 2D and 1D transistors. For a gate overdrive of V_{GS}-V_T=0.3 V, calculate the current /μm for a 2D ballistic FET. If the FET is made of square 1D nanowires, how many nanowires /μm are needed to achieve the same on-current. Assume both devices are operating in the single subband limit. Use t_{ox}=2 nm, ε_r=25, m^*/m_0=0.05. If the nanowires have a square size with W=H=5nm, is this integration feasible?

2. The first two steps of the quantized conductance for a 1D FET (with parasitic source and drain resistances) with L_G=100 nm is measured at low temperature to 49 μS and 89.2 μS. Assuming that the transmission if the same for both steps, calculate the mean free path and the parasitic source and drain resistances.

3. The transconductance at $V_{DS,sat}$ from the device in #2 is also measured, and found to only be 10 μS. Show that this is smaller than expected (assuming g_d=0), and suggest one possible origin for the degraded g_m.

4. An 1D InAs FET has m^*/m_0=0.05, ε_r=25, t_{ox}=2 nm, r_{wire}=5 nm. Show that at T=300 K, C_{ox} >> C_q for all gate biases. The device is thus expected to operate very close to the QCL limit.

5. For a 10×10 nm^2 square InAs nanowire, calculate the two lowest subbands, assuming non-parabolicity. Compare with parabolic bands.