SiGe PLL design at 28 GHz

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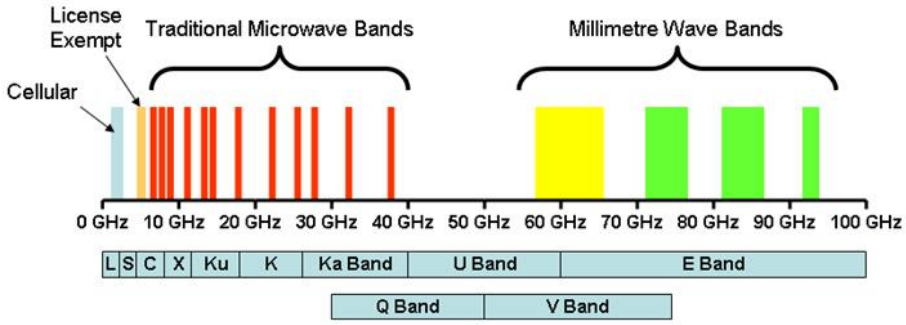
Presentation outline

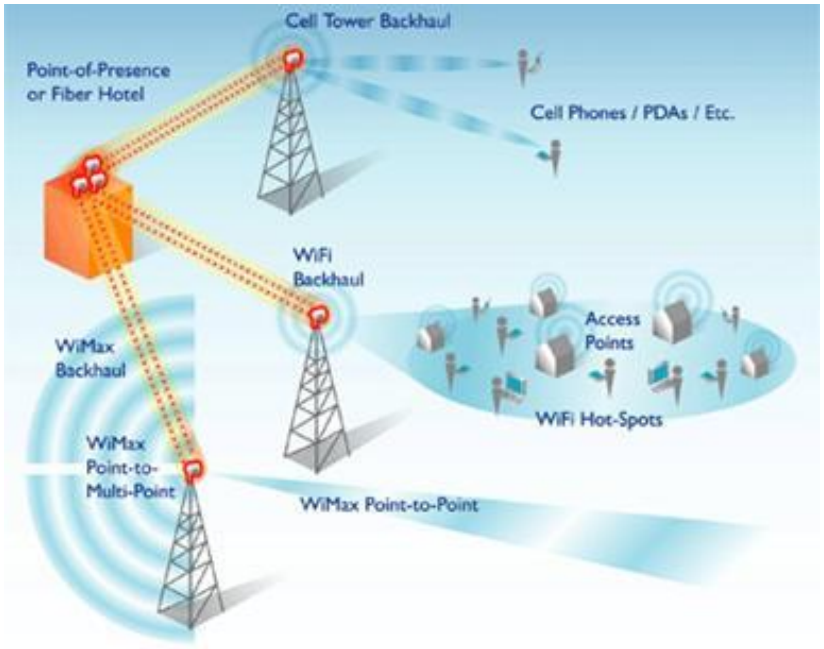
- **E-band wireless backhaul**
- **Beam forming concept**
  - Linear timed and phased arrays
- **Transmitter architecture**
- **PLL architecture**
  - 28 GHz QVCO
  - Current-Mode-Logic ÷16 divider
  - Gilbert mixer phase detector
  - Active low pass filter
  - Phase control by current injection into phase detector
- **Measurement setup**
- **Conclusions**

E-band wireless backhaul

- **The E-band at 71-76 GHz and 81-86 GHz: wireless point-to-point communication**

- 5 GHz of spectrum ⇒ data rates of Gb/s





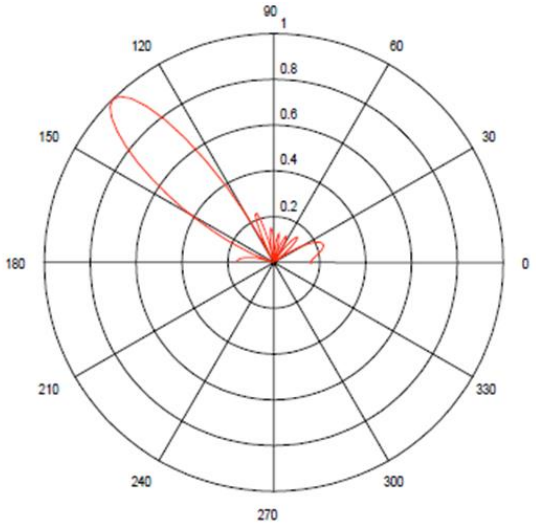
- costly optical fiber backhaul ⇒ wireless data link

- Heterogeneous networks: macro, pico and femto cells ⇒ **large number of base stations**

A wireless backhaul is highly advantageous

Beamsteering concept

- Beamsteering ⇒ equal to spatial filtering of radio signals
- Array of antennas ⇒ steered to block transmission to certain directions and to provide antenna gain to a desired direction

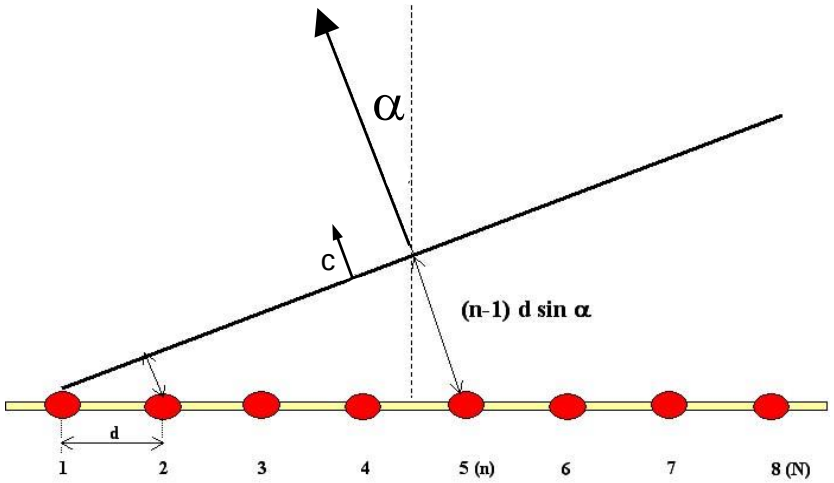


- Applications:

  - Radio communication
  - Surveillance
  - Radar
  - Sonar
  - Audio

Linear timed arrays

- Linear equally spaced array with 8 TX antenna elements
- Wave plane at transmit angle α



- Different time of departure Δt

$$\Delta t = \frac{(n-1)d \sin \alpha}{c}$$

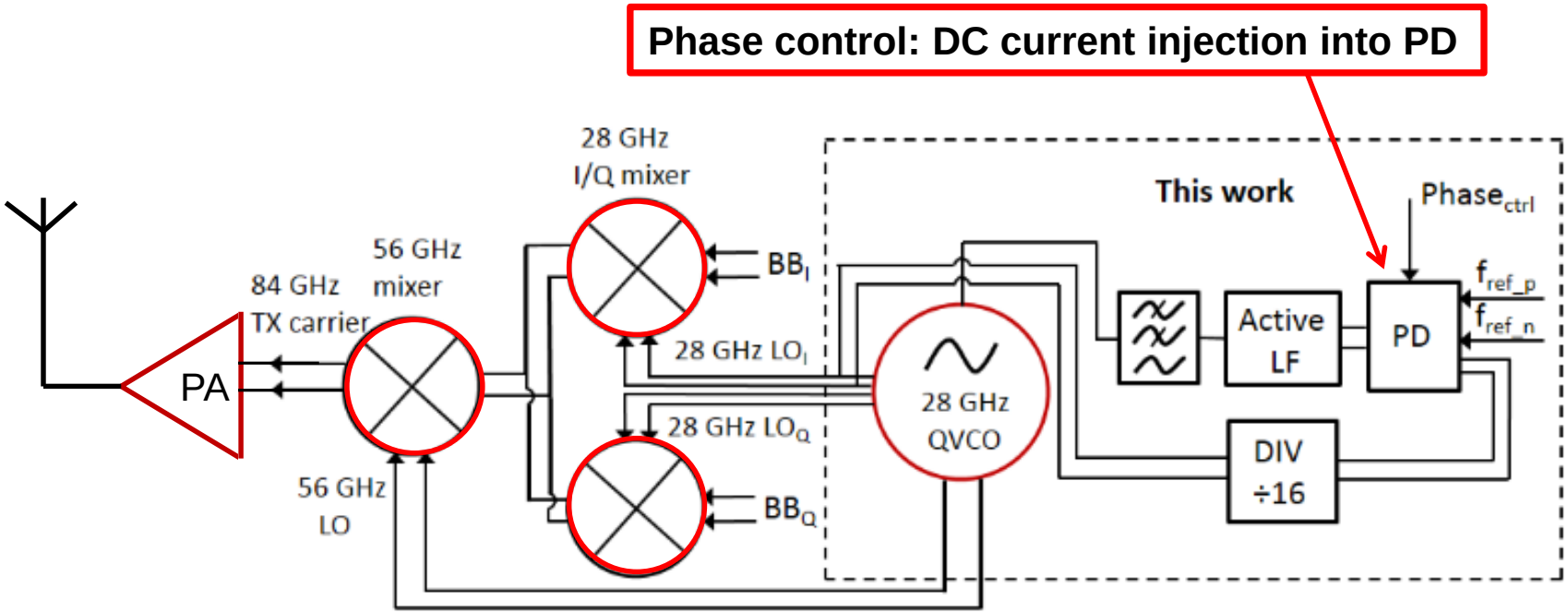
c= light speed, d = element spacing

- Beamforming TX: aligns the signals to the antenna elements in time

$\Rightarrow$ **Coherent combination to one direction and suppression to other directions**

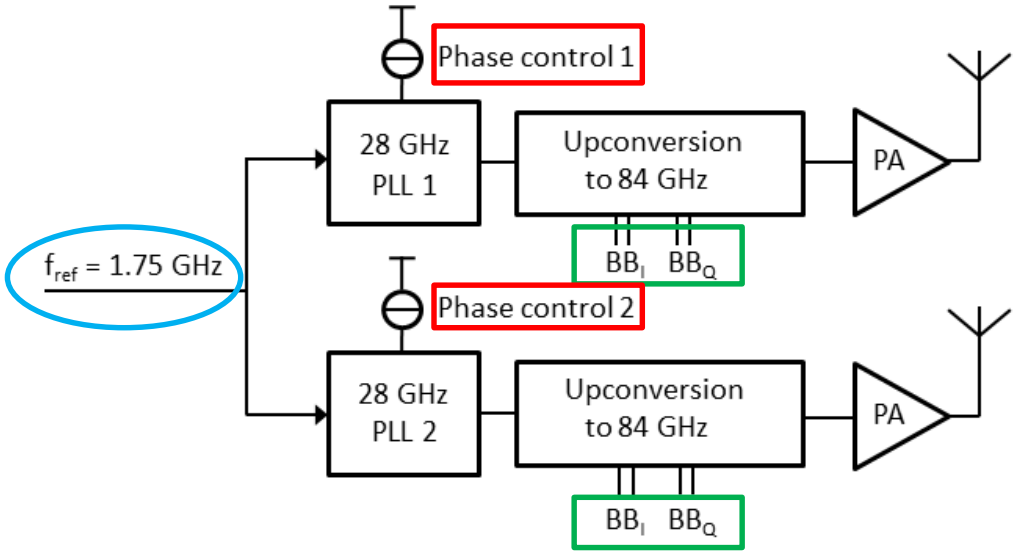
Use small fractional BW $\Rightarrow$ Realization of time delay with **fixed phase shift** $\Rightarrow$ **Linear phased array**

E-band transmitter architecture



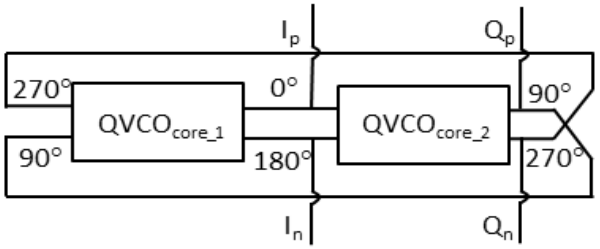
- 84 GHz TX carrier from a 28 GHz QVCO
- 28 GHz I/Q mixer: upconversion of BB signal.
- Mixing of 56 GHz second harmonic in QVCO tail with 28 GHz ⇨ 84 GHz carrier
- Less I/Q phase error compared 84 GHz QVCO
- Phase control: PD output $\propto \Delta\Phi$ of f_{div} and f_{ref} ⇨ Inj. DC: QVCO phase shift

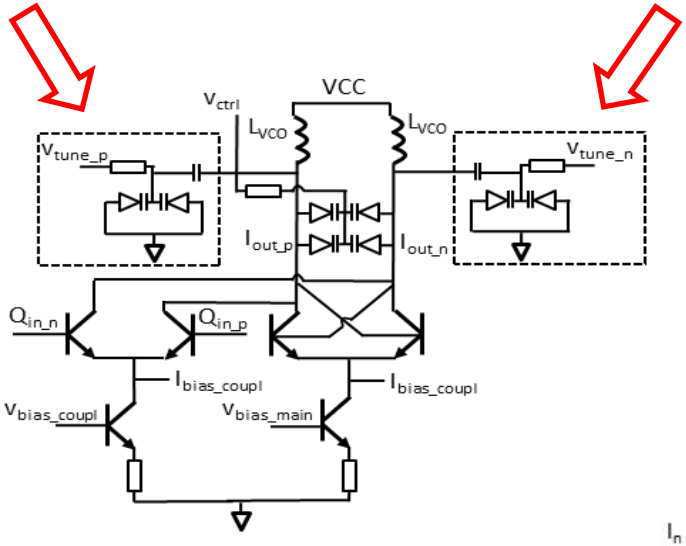
E-band beam steering architecture

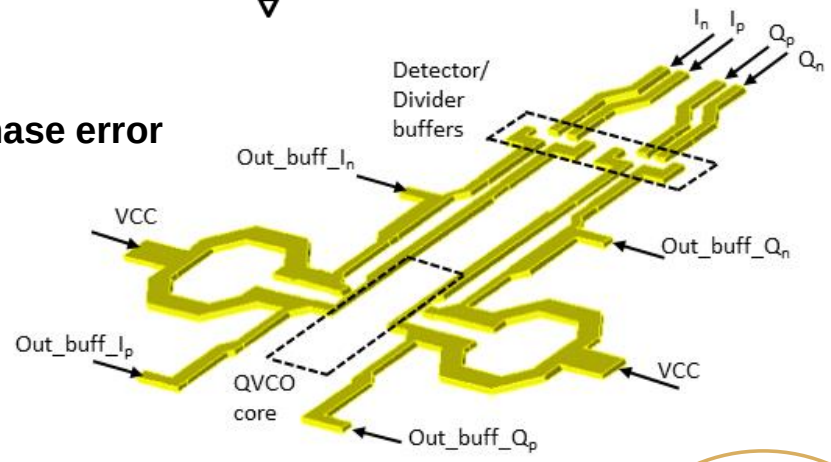


- **Beam steering for two TX paths**
- **Layout: PLLs close to mixers**
- **Phase control: PD DC current injection**
- **HF routing: Only f_{ref} ⟹ reduced phase/amp imbalance and P_{DC}**

28 GHz QVCO with I/Q phase error tuning







- **Radio link bit-error-rate highly sensitive to I/Q phase error**

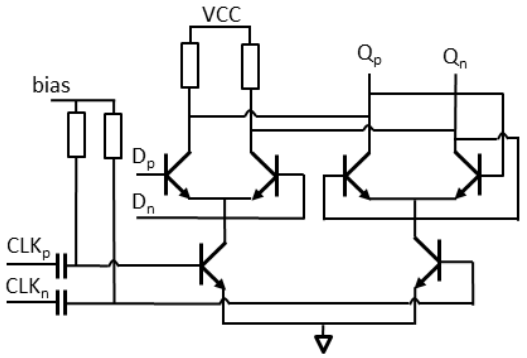
  ⇒ Phase error tuning with varactors

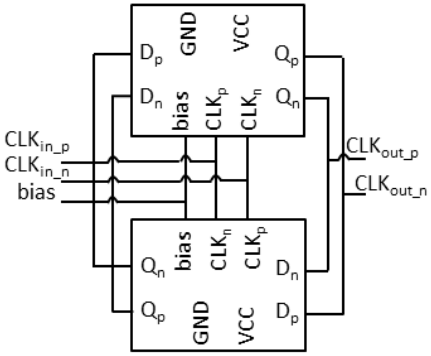
- **Supply voltage: 1.5 V for QVCO**

- **Current consumption: 15 mA from 1.5 V supply**
  Output buffers excluded

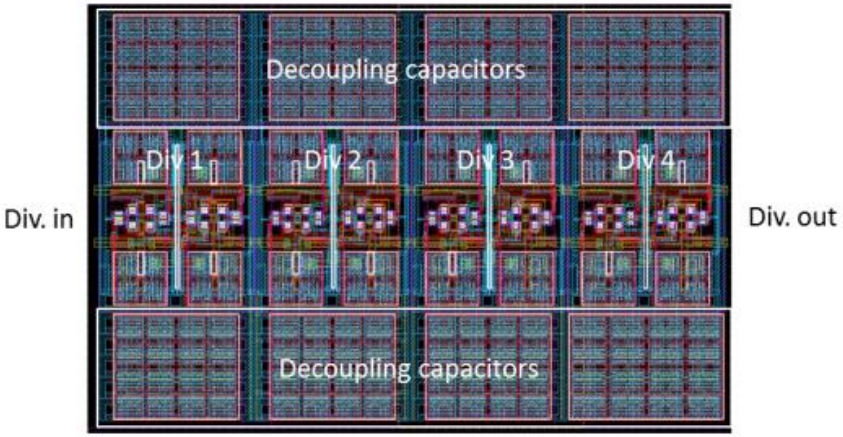
- **22 port s-parameter model for QVCO inductor plus routing**

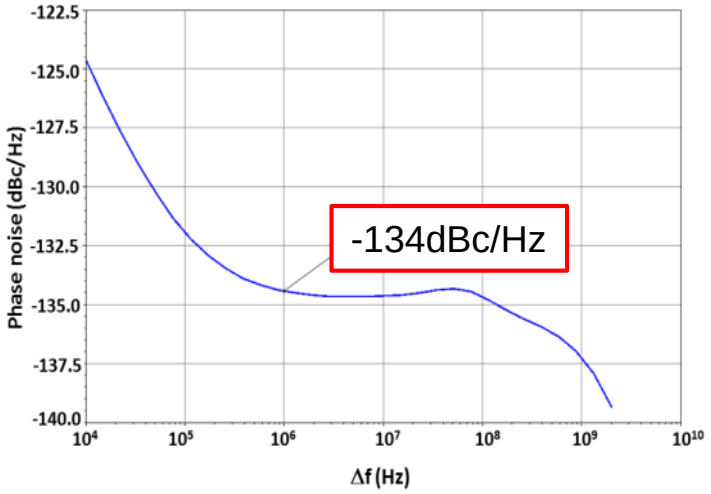
Divide by 16





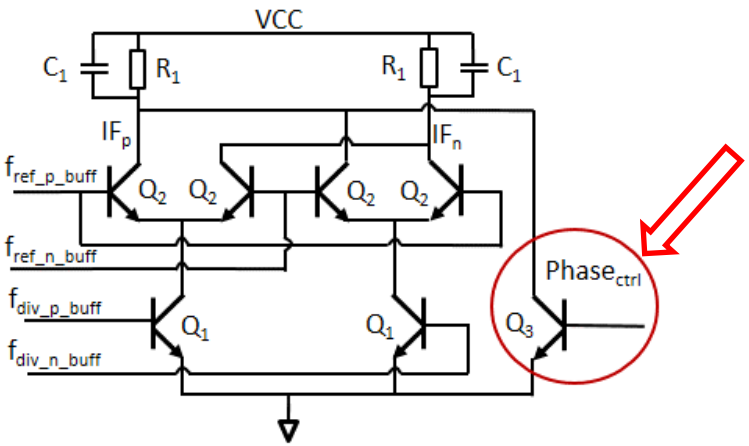
- **Divider implemented with four cascaded CML blocks**
- **1.5 V supply voltage Current consumption: 13mA**
- **PN at divider output: -134 dBc/Hz at 1 MHz offset**
- **Compared to -129 dBc/Hz from ideal division of min. sim. QVCO PN of -105 dBc/Hz @ 1MHz offset**



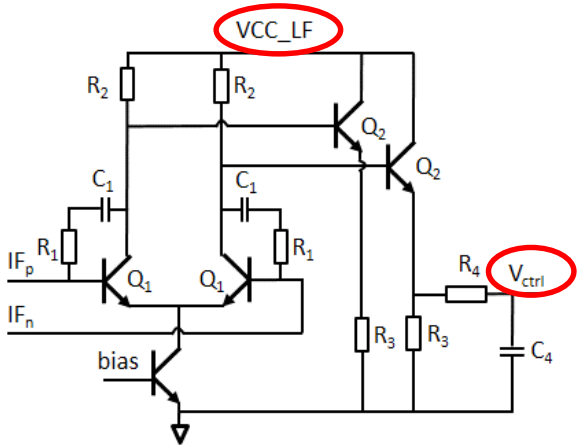


Phase detector and active loop filter

Gilbert phase detector



Active LF

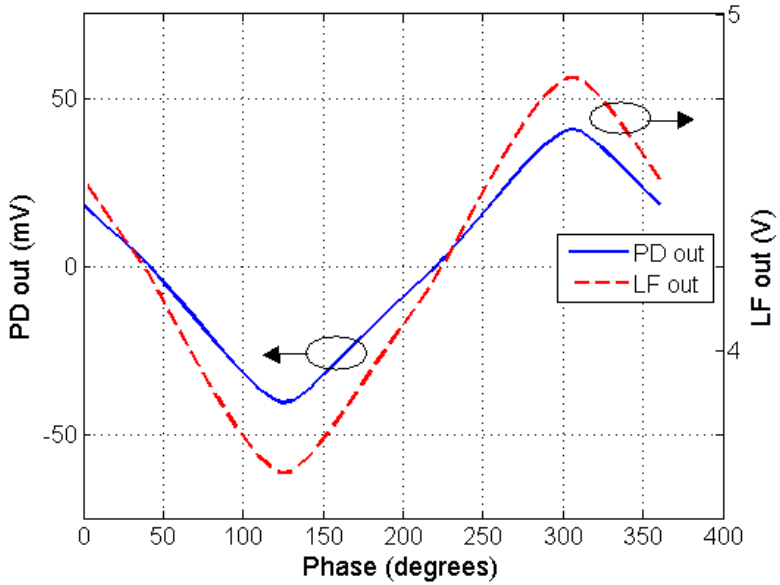


- **Phase control: DC current injection into PD**
- **PD output prop. to phase difference between f_{ref} and f_{div}**
- **$\Rightarrow$ Phase difference forced on QVCO for constant frequency**
- **I_{DC} = 1.3 mA**

- **Low pass filter: Active RC filter plus passive RC pole**
- **I_{DC} = 1 mA**
- **Alter VCC_LF $\Rightarrow$ tuning range** ↗

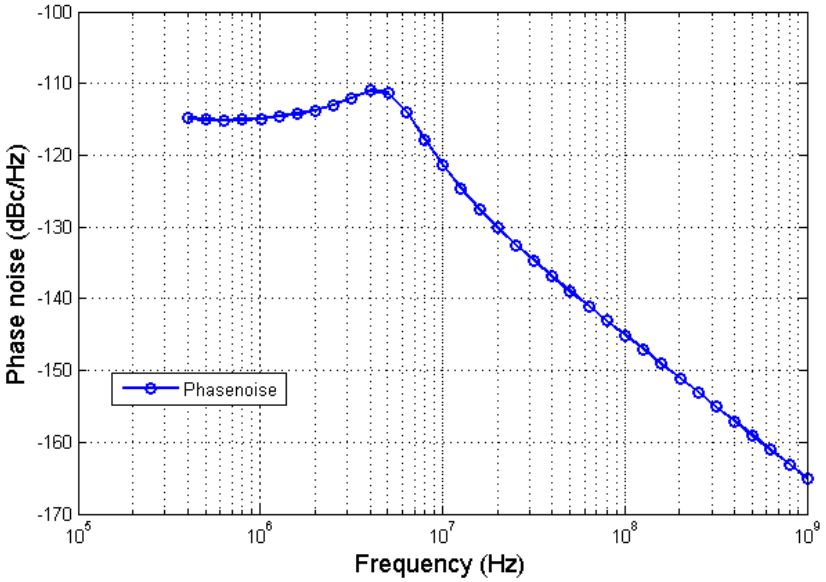
Phase detector and active loop filter

Simulation results: PD and LF gain



- **PD out prop. to phase difference of f_{ref} and f_{div}**
- **PD: I_{DC} = 1.3 mA**
  LF: I_{DC} = 2 mA
- **PD gain: 0.55 mV/degree**
- **PD +LF gain: 8.6 mV/degree**
- **24 dB gain in active LF**
- **1.2 V output range**

PLL simulation results

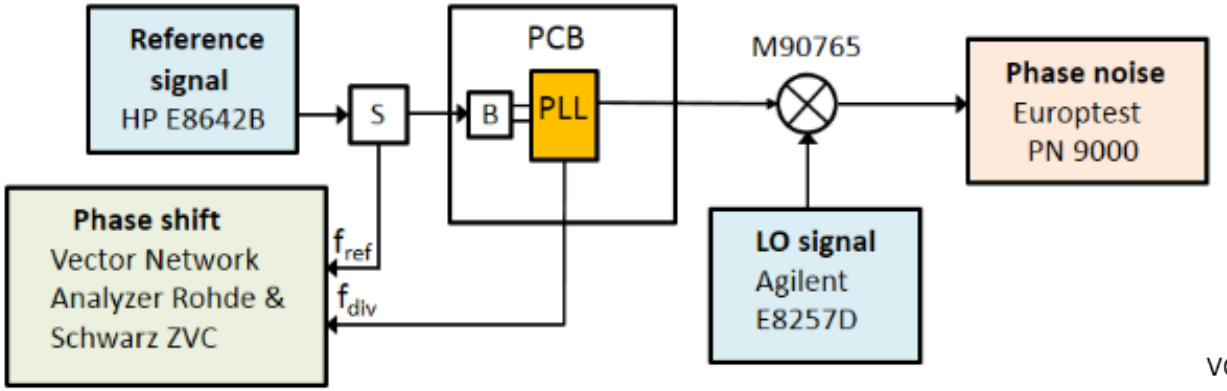


Simulator convergence within 10 minutes !

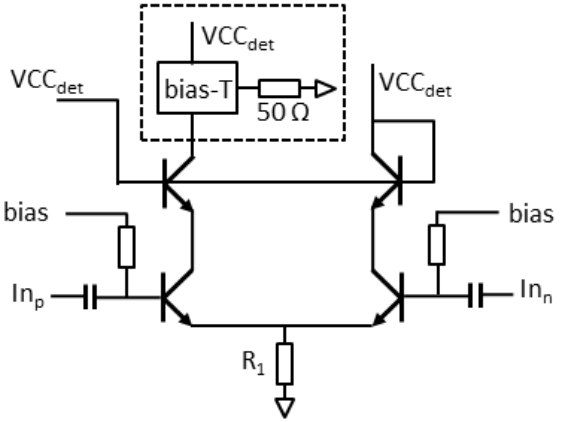
- **Simulation tool: Cadence Spectre RF**
- **Extremely difficult to simulate a complete PLL**
- **⇒ Use combination of Verilog-A modeling and schematics**
- **This work: Verilog-A model of QVCO**
- **Mimics QVCO with phase noise and K_{VCO}**
- **Spectre RF PSS + pnoise + pstb**

  ⇒PN, BW and phase margin
- **Phase margin: 44° at 4.1 MHz offset**

Measurement setup



Divider output buffer



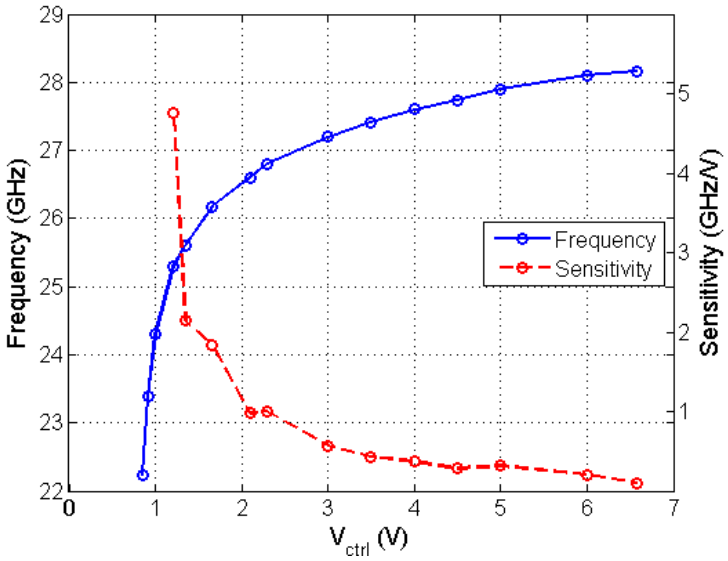
- **1.75 GHz reference signal: split to balun + VNA input 1**
- **VNA input 2: Divider output ⇒ ΔΦ measurement**
- **PN measurement: 28 GHz output down converted with LO >=26 GHz**

28 GHz QVCO with phase error detector and tuner

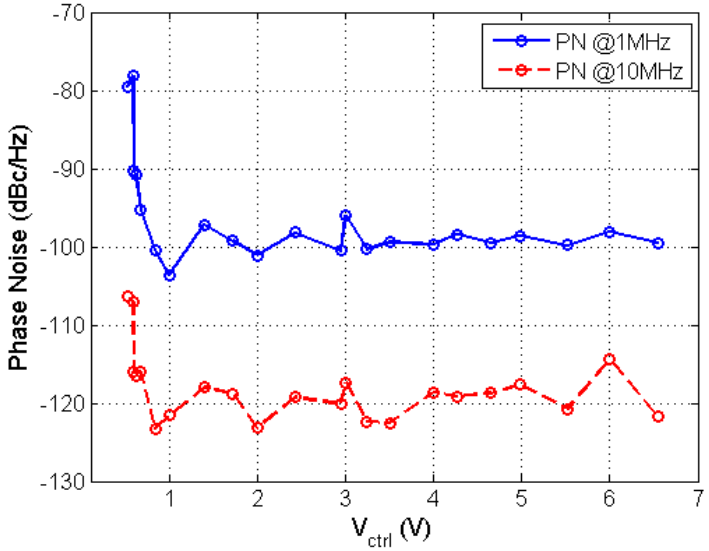
QVCO measurement results

Measured on previous chip

Tuning range and K_{VCO}



PN vs V_{ctrl}



- K_{VCO} dependency of varactor voltage: K_{VCO} = 200 MHz/V @ V_{ctrl} = 6.0 V
- PN = -100 dBc/Hz
- At low V_{ctrl} : VCO varactor forward biased ⇒ PN ↗

PLL beam steering measurements

Conclusions

- **Project status September 2015**

- **Beam steering 28 GHz PLL performance verified**
  - 28 GHz QVCO
  - CML divider
  - PD with phase control
  - Active LF for extended tuning range

- **Remaining work:**
  - Simulation test bench for complete TX
  - Measure three previously taped out SiGe E-band PAs