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REVIEW

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Tunnel field-effect transistors as energy-efficient electronic switches

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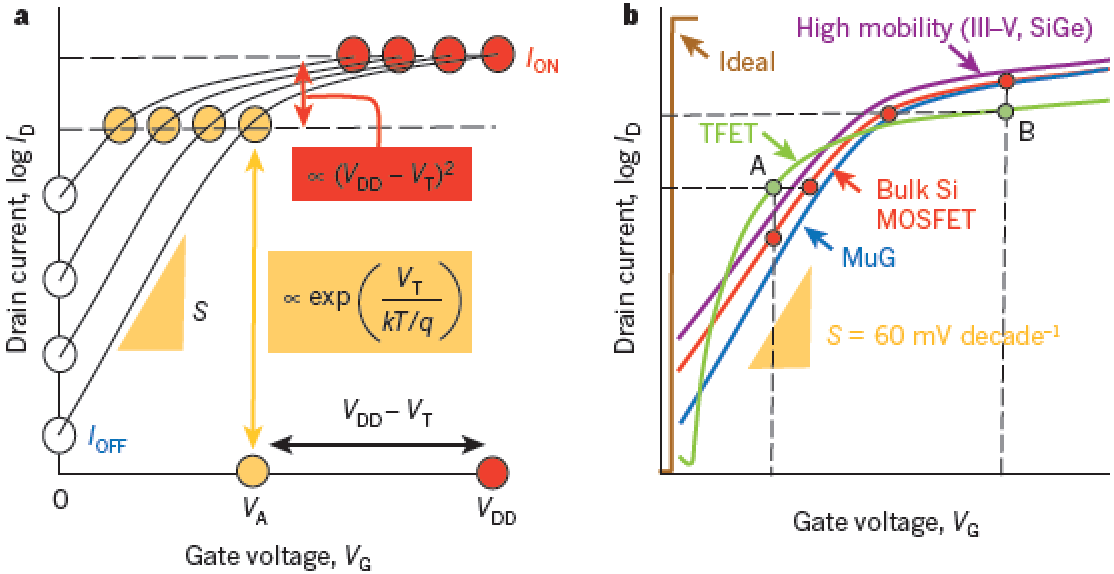
Power dissipation is a fundamental problem for nanoelectronic circuits. Scaling the supply voltage reduces the energy needed for switching, but the field-effect transistors (FETs) in today's integrated circuits require at least 60 mV of gate voltage to increase the current by one order of magnitude at room temperature. Tunnel FETs avoid this limit by using quantum-mechanical band-to-band tunnelling, rather than thermal injection, to inject charge carriers into the device channel. Tunnel FETs based on ultrathin semiconducting films or nanowires could achieve a 100-fold power reduction over complementary metal-oxide-semiconductor (CMOS) transistors, so integrating tunnel FETs with CMOS technology could improve low-power integrated circuits.

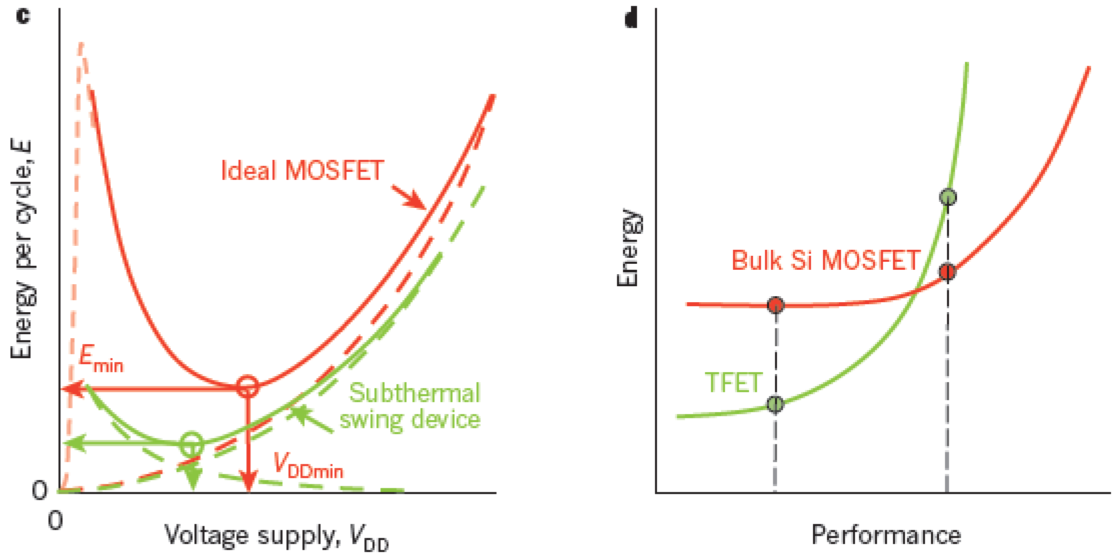


$$S = \underbrace{\frac{dV_G}{d\Psi_s}}_{m}\,\underbrace{\frac{d\Psi_s}{d(\log_{10} I_D)}}_{n} \cong \left(1 + \frac{C_d}{C_{ox}}\right)\ln 10\,\frac{kT}{q}$$

$$\rightarrow \frac{kT}{q}\ln 10 \cong 60\ \text{mV decade}^{-1}\,|\,T = 300\ \text{K}$$

Two a:pproaches to reduce Vdd:
- Reduce Vt to maintain (Vdd-Vt)
- Reduce S

Energy Required for Switching



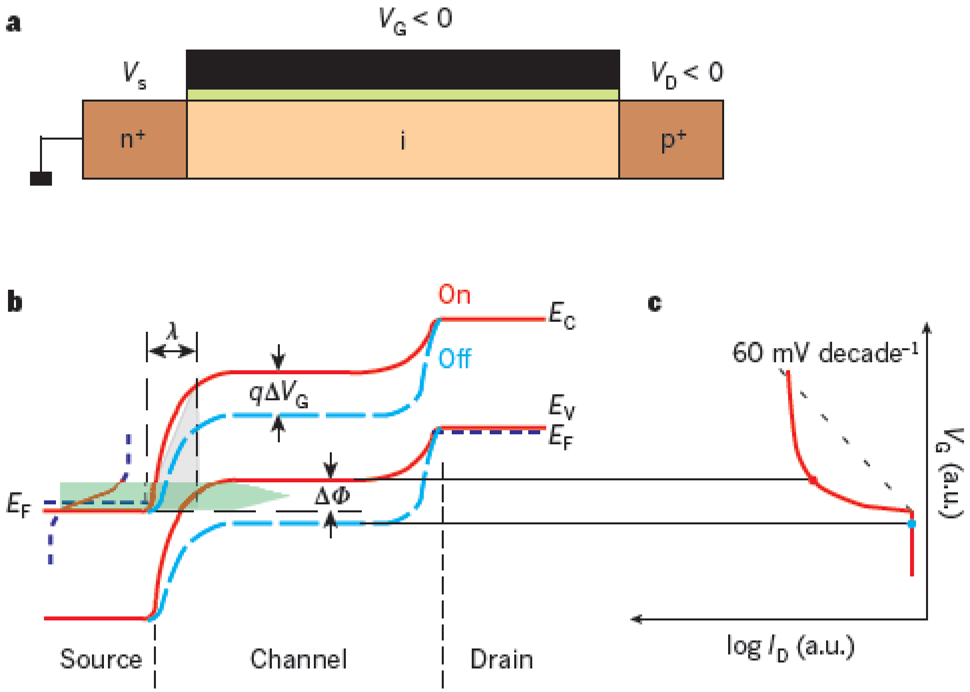
$$E_{total} = E_{dynamic} + E_{leakage} = \alpha L_d C V_{DD}^2 + L_d I_{OFF} V_{DD} \tau_{delay}$$

$$\approx \alpha L_d C V_{DD}^2 = L_d C V_{DD}^2 \frac{I_{OFF}}{I_{ON}} = L_d C V_{DD}^2 \left(\alpha + \frac{I_{OFF}}{I_{ON}}\right)$$

$$\approx L_d C V_{DD}^2 \left(\alpha + 10^{\frac{-V_{DD}}{S}}\right)$$

$$P = \alpha L_d C V_{DD}^2 f = I_{OFF} V_{DD} \approx K C V_{DD} = I_{OFF} V_{DD}^3$$

Principle of Operation



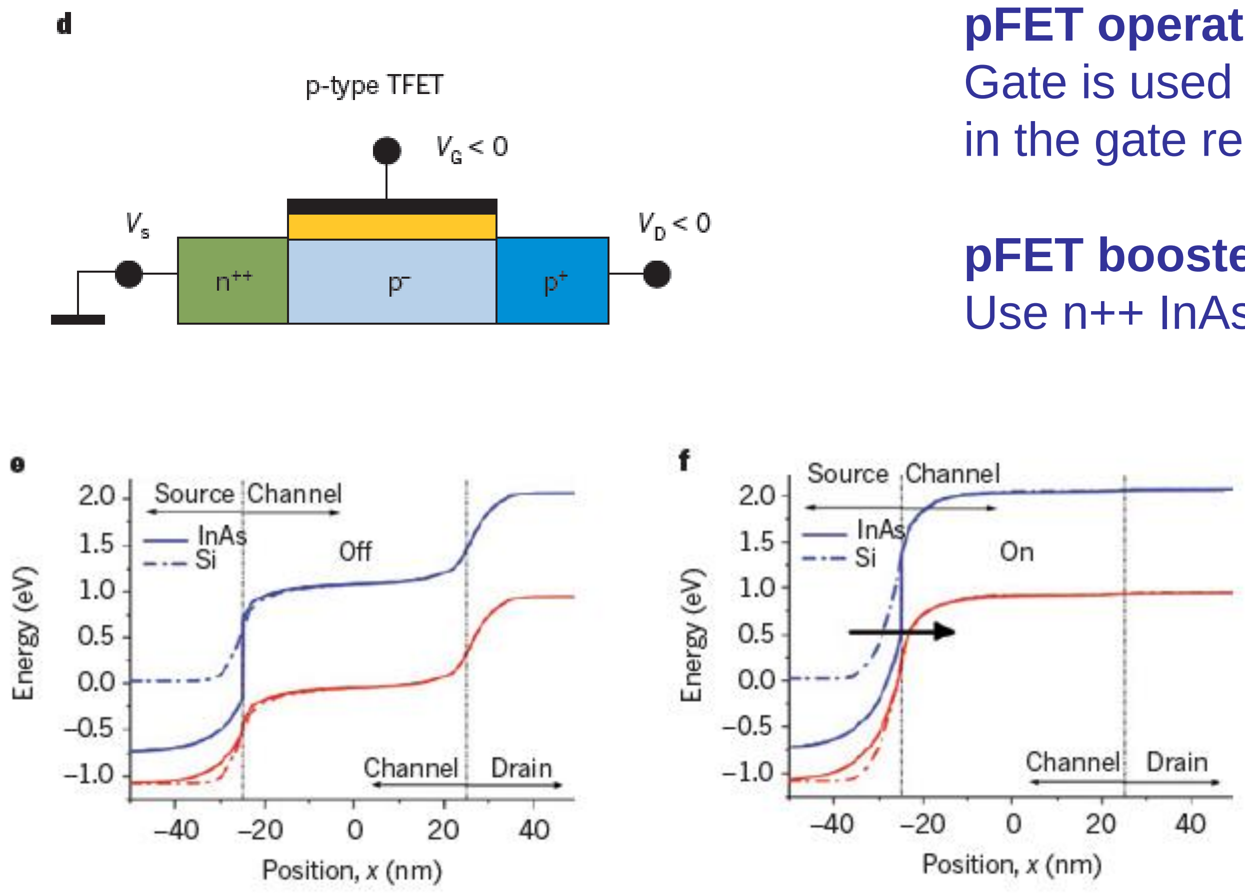
-On-state:
Carriers may tunnel from the source to the channel

-Off-state:
Tunneling from the source is restricted due to the band gap

Tunnel injection across triangular barrier

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar\,(E_g + \Delta\Phi)}\right)$$

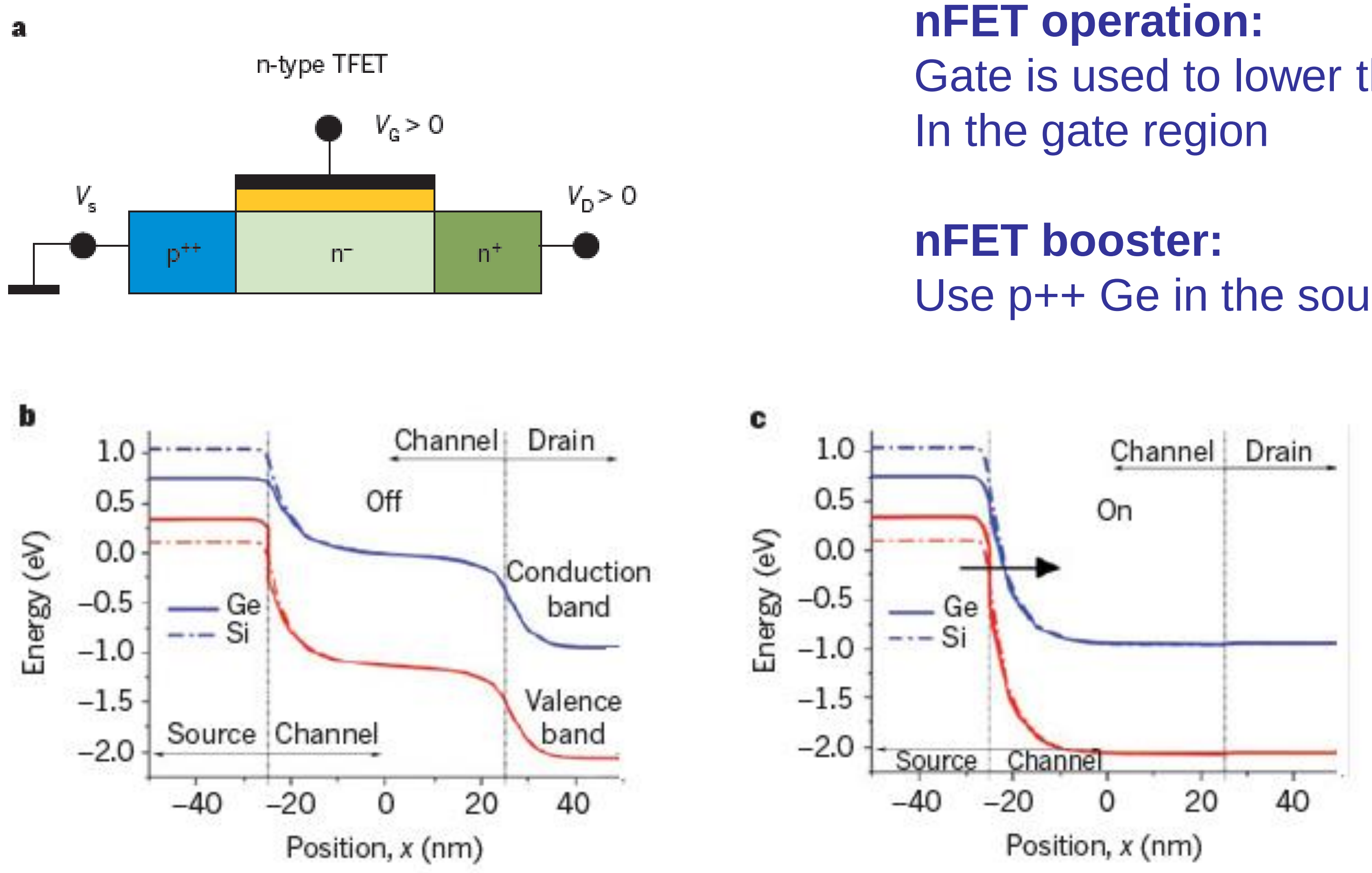
pFET Implementation



pFET operation:
Gate is used to lift the bands in the gate region

pFET booster:
Use n++ InAs in the source

nFET Implementation



nFET operation:
Gate is used to lower the bands
In the gate region

nFET booster:
Use p++ Ge in the source

Materials selection

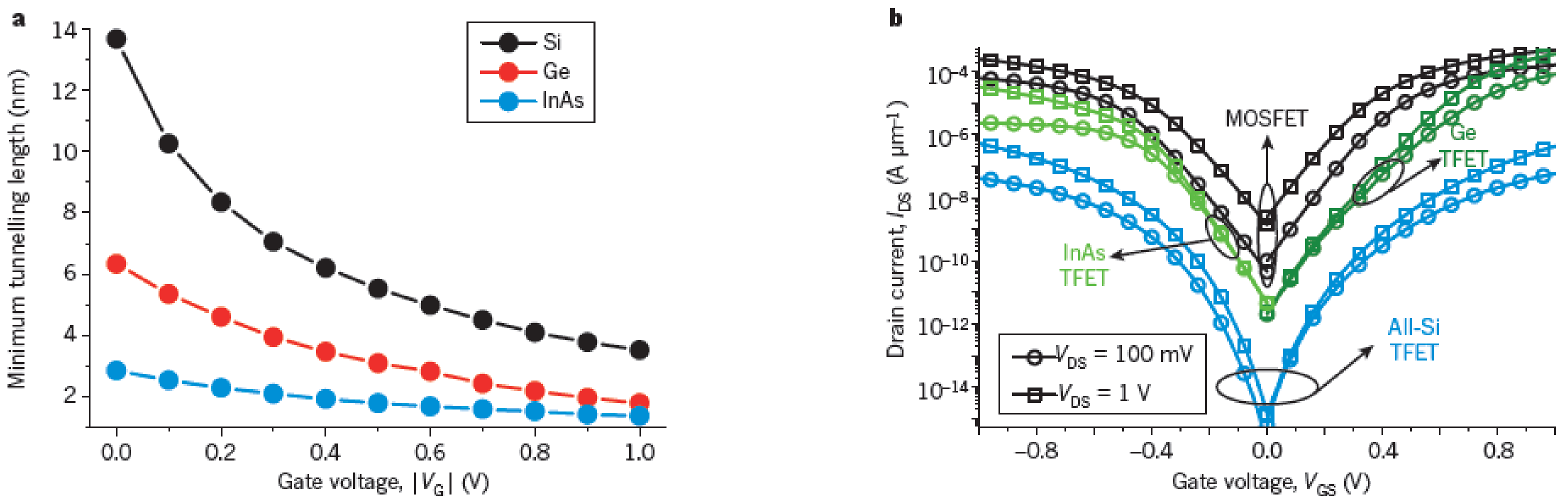


Figure 4 | Importance of the material system on TFET performance. **a**, Modulation of the minimum screening tunnelling length with the applied gate voltage in all-silicon (black), Ge-source (red) and InAs-source (blue) TFETs, showing the beneficial effect of a higher tunnelling rate due to the shorter tunnelling length in a heterostructure TFET with a low bandgap source material compared with silicon. By contrast, a higher ratio between the tunnelling length in the off and the on state reflects an improved I_{ON}/I_{OFF}. **b**, Corresponding transfer characteristics of a state-of-the-art 65-nm CMOS transistor (black), complementary Ge/InAs TFET (green) and complementary all-Si TFET (blue). The complementary Ge/InAs TFET achieves the best trade-off between a low I_{OFF}, a steep subthreshold swing and performance. I_{DS}, drain-to-source current; V_{DS}, drain-to-source voltage; V_{GS}, gate voltage at source.

Important to reduce the tunneling barrier. Use narrow band gap material or heterostructure design.

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar\,(E_g + \Delta\Phi)}\right)$$

Steep-slope Tunnel Field-Effect Transistors using III-V Nanowire/Si Heterojunction

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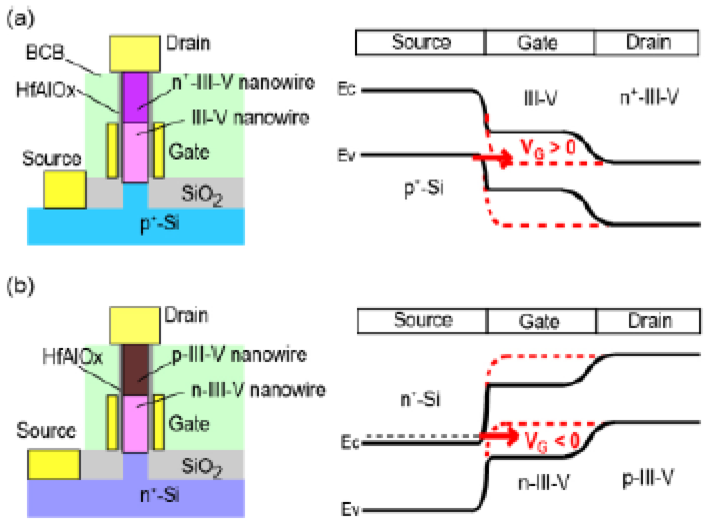
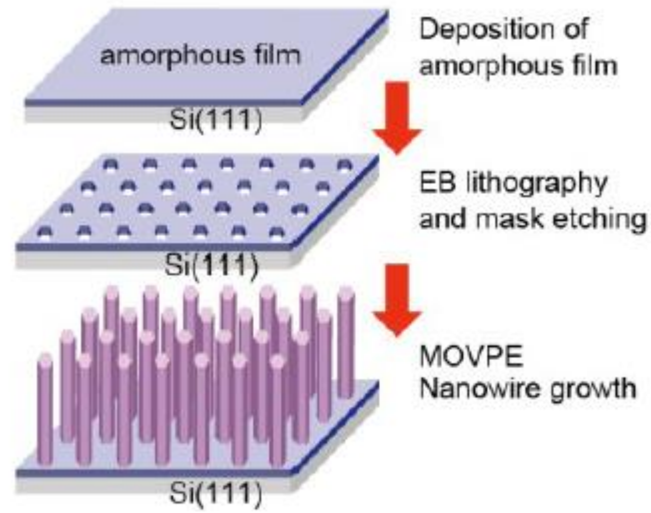
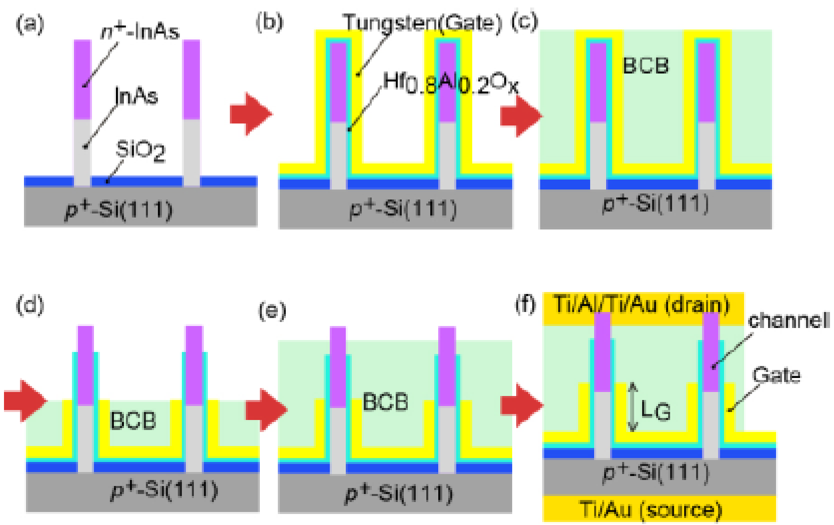
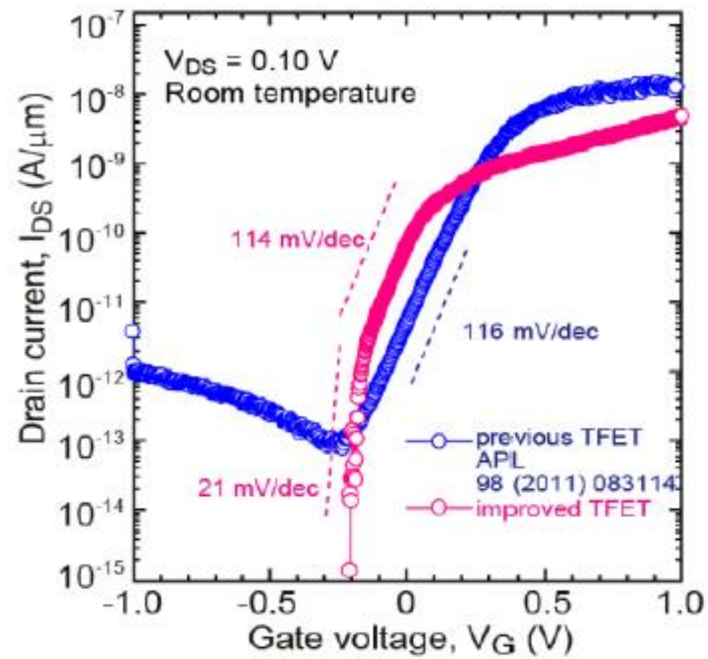


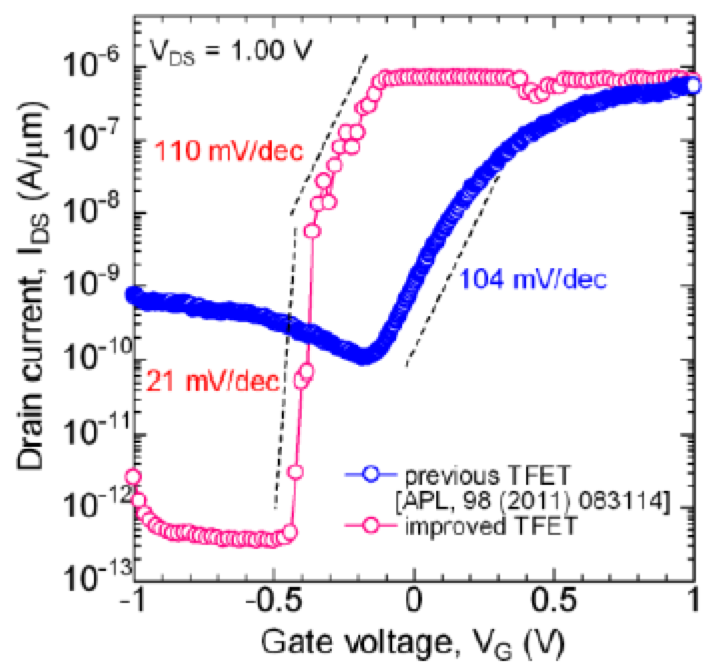


Measured Data



30 nm diameter required to get good device performance





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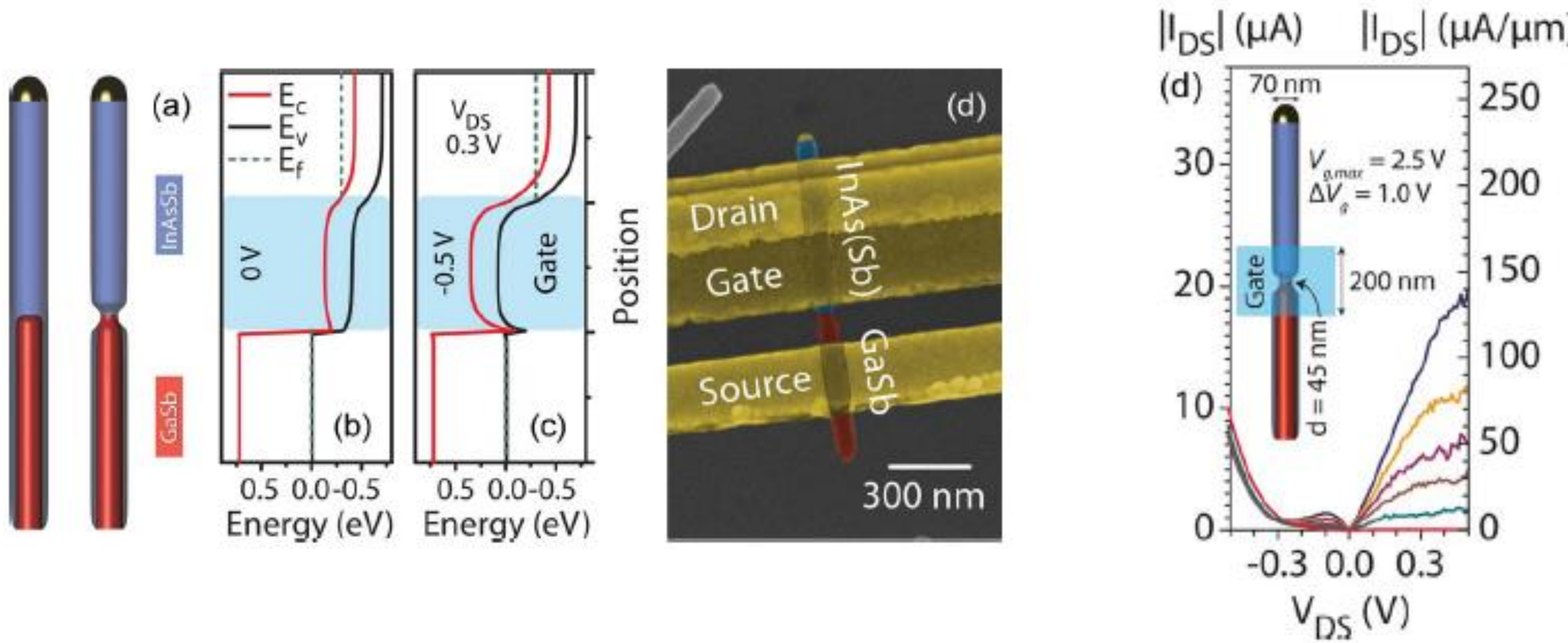
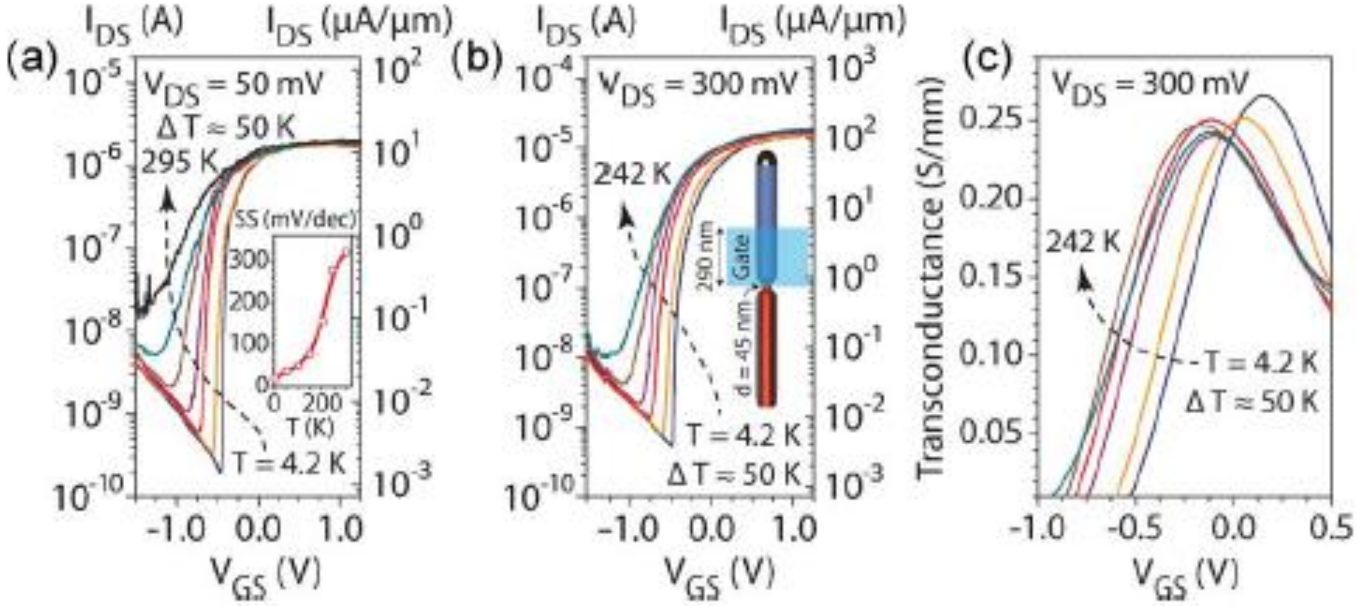
High-Current GaSb/InAs(Sb) Nanowire Tunnel Field-Effect Transistors

Anil W. Dey, *Student Member, IEEE*, B. Mattias Borg, Bahram Ganjipour, Martin Ek, Kimberly A. Dick, Erik Lind, Claes Thelander, and Lars-Erik Wernersson



Nanoelectronics: Low-swing Devices

Measured Data



Very high drive currents due to the broken gap. Decent off-state characteristics and high transconductance.

APPLIED PHYSICS LETTERS **90**, 142110 (2007)

Vertical surround-gated silicon nanowire impact ionization field-effect transistors

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(Received 22 December 2006; accepted 25 January 2007; published online 5 April 2007)

One of the fundamental limits in the scaling of metal oxide semiconductor field-effect transistor technology is the room-temperature (RT) limit of ~60 mV/decade in the inverse subthreshold slope. Here, the authors demonstrate vertical integration of a single surround-gated silicon nanowire field-effect transistor with an inverse subthreshold slope as low as 6 mV/decade at RT that spans four orders of magnitude in current. Operation of the device is based on avalanche breakdown in a partially gated vertical nanowire, epitaxially grown using the vapor-liquid-solid method. Low-power logic based on impact ionization field-effect transistors in combination with a vertical architecture is very promising for future high-performance ultrahigh-density circuits. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2720640]

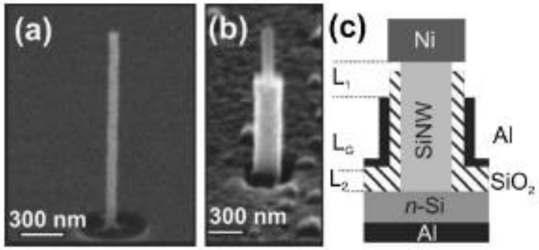

FIG. 1. Processing of vertical Si NW transistors. (a) 60-nm-diameter Si wire covered with 25 nm SiO_2 gate dielectric. (b) Wire with gate length defined by etching of Al. (c) Schematics of the surround-gated transistor displaying the gate length L_G and ungated regions L_1 and L_2.

-N-type substrate

- p-type wires

Nanoelectronics: Low-swing Devices

Forward bias characteristics

-High bias operation due to Schottky barrier at the top contact

- Good Ion/Ioff ratio

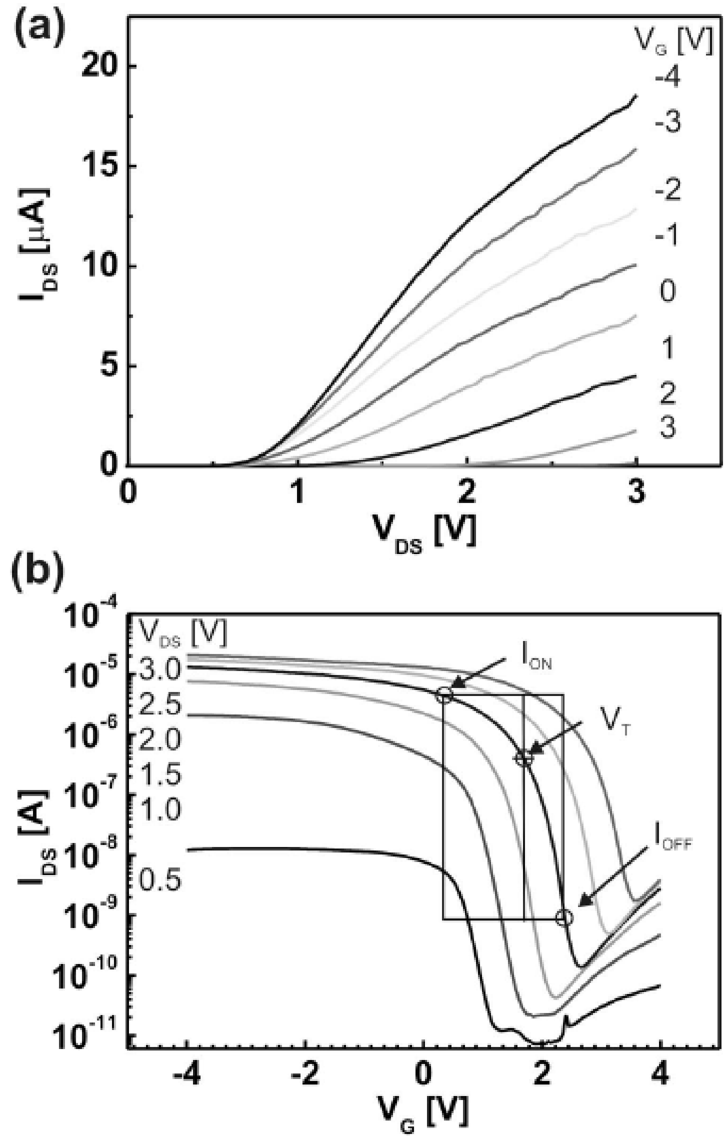

FIG. 2. Current-voltage characteristics of a forward-biased device. (a) Output characteristics for different gate voltages showing the accumulation behavior. (b) Transfer characteristics on a logarithmic scale for different V_{DS}. The three circles mark, from left to right, on current, threshold voltage, and off current at V_{DS}=2 V. The on-off current ratio of this device is 10^4.

Reverse bias characteristics

-Use the Schottky barrier to inject holes

-Change the properties of the
p/n junction

-Use the impact ionization process

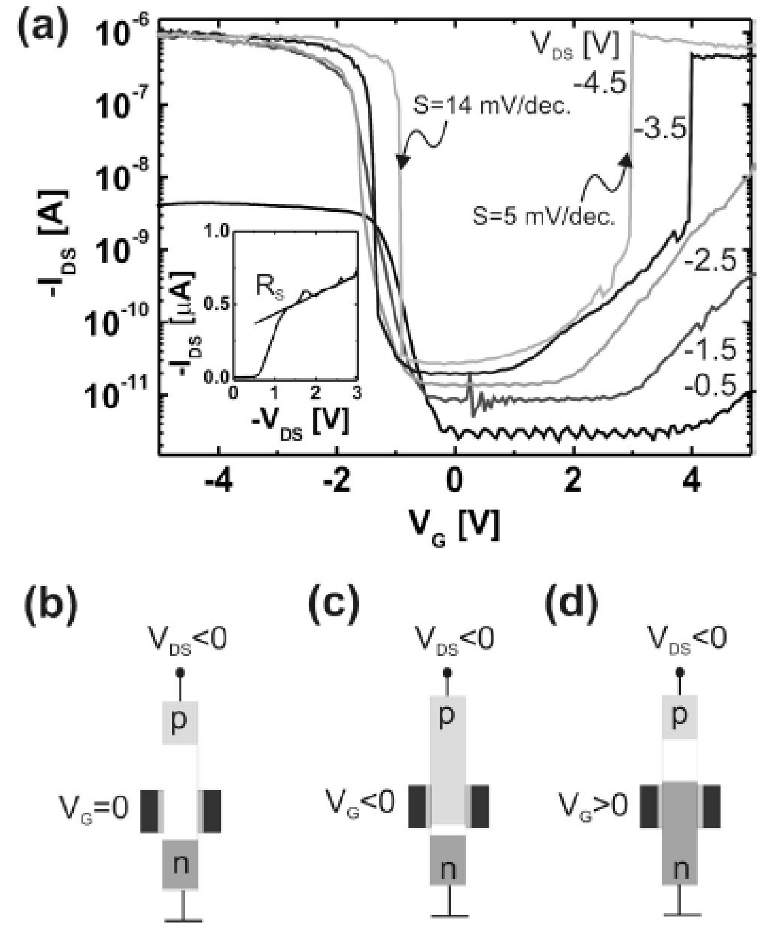

FIG. 3. Current-voltage characteristics of a reverse-biased device. (a) Transfer characteristics on a logarithmic scale. In accumulation, breakdown occurs at voltages greater than 2 V, yielding sharp transitions between on and off states with inverse subthreshold slopes as low as 6 mV/decade over four orders of magnitude in current. In inversion, swing values down to 5 mV/decade are obtained, but at slightly larger source drain voltages. Inset: the output characteristic of the device at $V_G=-3$ V. (b) Schematic of the device at $V_G=0$ V, where the wire is depleted. (c) At $V_G<0$ V, the breakdown occurs in accumulation mode at the bottom part of the gate, whereas for $V_G>0$ V (inversion under the gate), shown in (d), the breakdown occurs at the top part of the gate.

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Performance Comparison Between p-i-n Tunneling Transistors and Conventional MOSFETs

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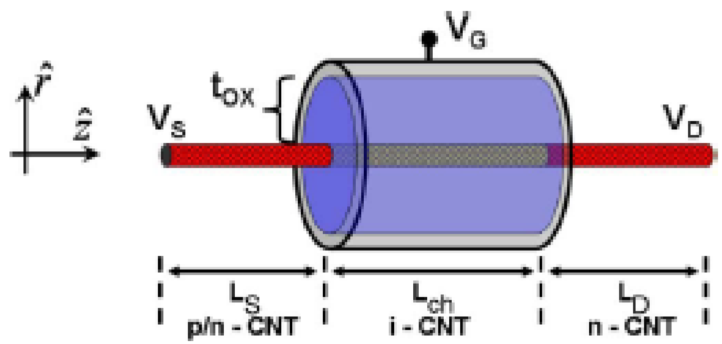


Fig. 1. Modeled device geometry used in this paper with cylindrically symmetric wrap-around gate electrode (see text for device parameters). The high-*k* oxide is removed from source/drain regions in order to reduce the fringing fields that adversely affect the drive current for the p-i-n TFET.

Nanotube used
for the modelling

15 nm gate length

Simulated Data

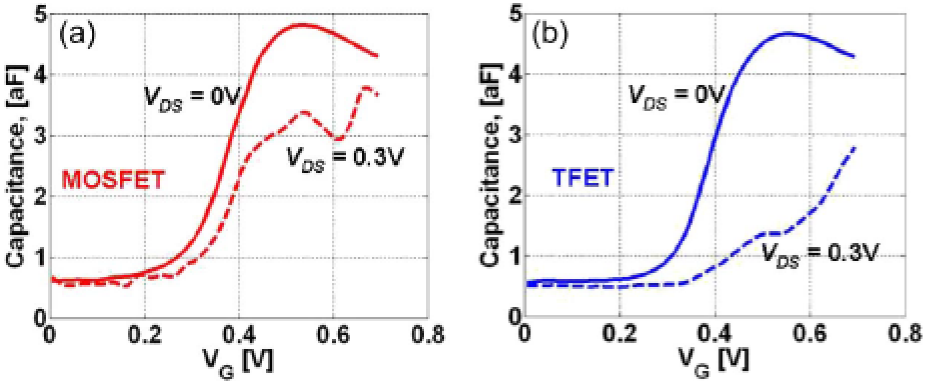
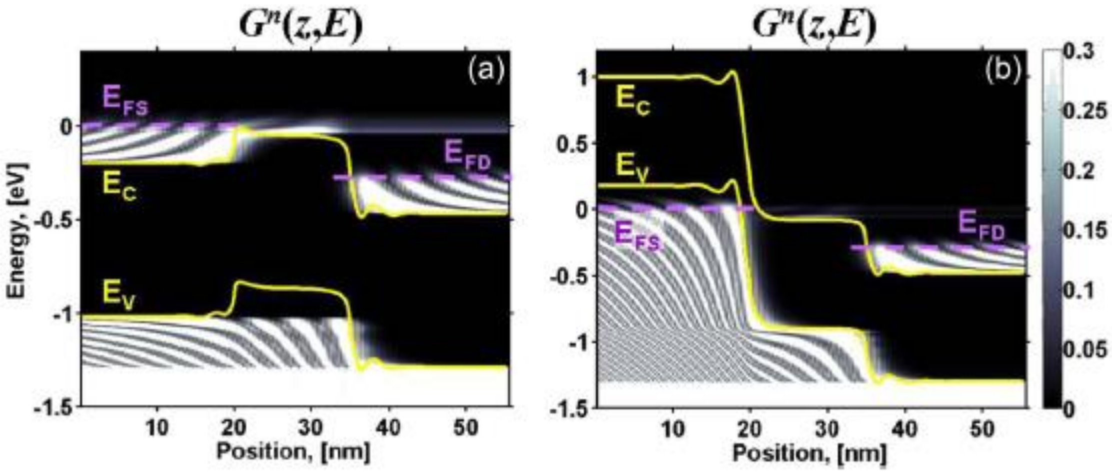


Fig. 2. Total gate capacitance (C_{tot}) versus V_{GS} comparison for (a) MOSFET and (b) TFET under dissipative transport. At small V_{DS}, both devices show similar characteristics. However, at larger V_{DS}, a fundamentally different behavior is observed; for the TFET device, capacitance remains small until larger gate biases are applied.

Reduced capacitance



Less carriers in the channel

Fig. 3. Energy-position-resolved electron distribution [i.e., diagonal elements of G^n in (5)] for (a) MOSFET and (b) TFET under ballistic transport at $V_{GS} = 0.5$ V, $V_{DS} = 0.3$ V. A significantly higher occupation of channel states is observed for the former.

N

Comparison MOSFETs and TFETs

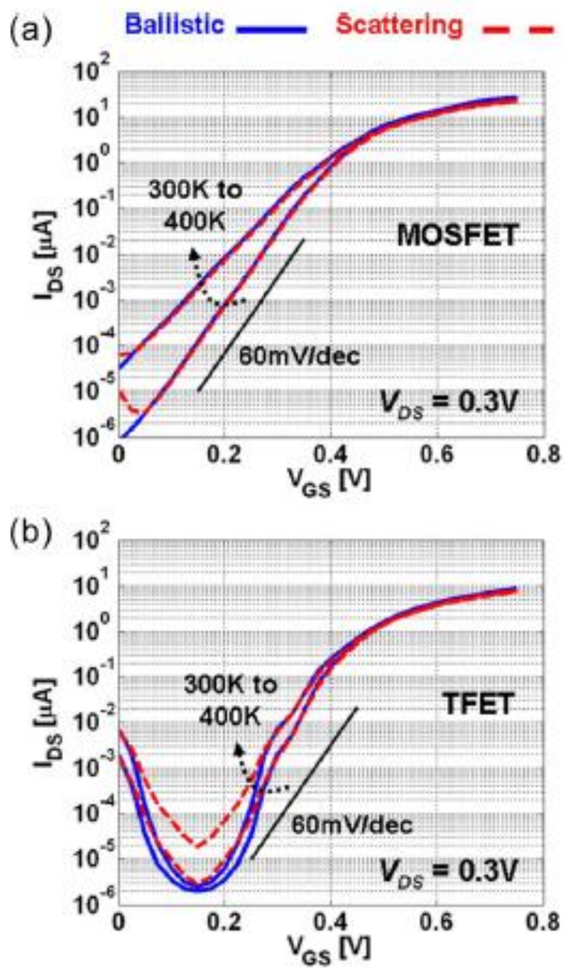


Fig. 5. I_{DS}–V_{GS} dependence on temperature for (a) MOSFET and (b) TFET under ballistic and dissipative transport. The latter has reduced temperature dependence under ballistic conditions. Phonon-assisted tunneling can, however, degrade the subthreshold characteristics.

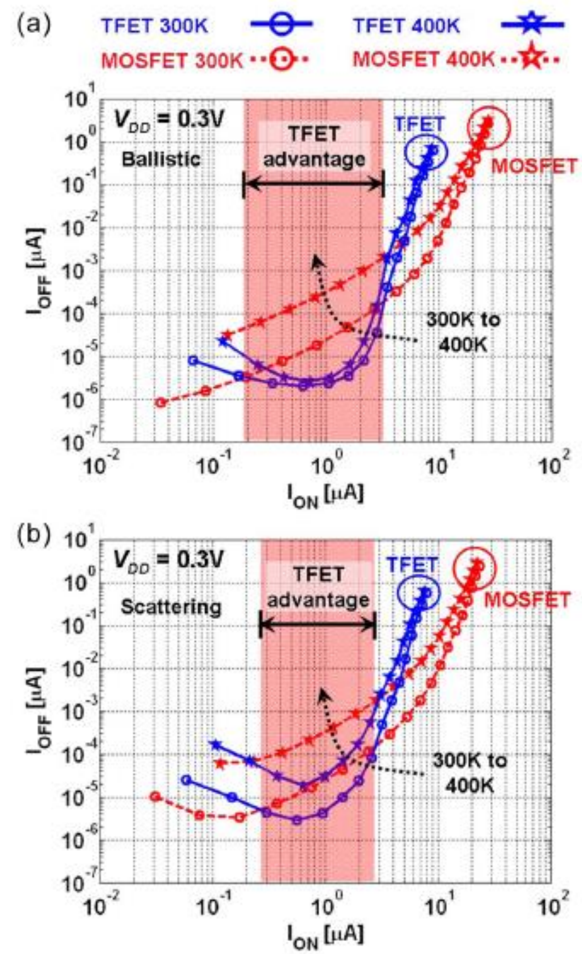


Fig. 6. I_{OFF} versus I_{ON} dependence on temperature at $V_{DD} = 0.3$ V under (a) ballistic and (b) dissipative transport. Shaded region is where the TFET has an advantage over the MOSFET due to larger I_{ON} with a smaller I_{OFF}. Temperature dependence of I_{OFF} for the TFET is also smaller than that for the latter.