Contents: Power and Delay

CMOS Static and Dynamic Power Consumption:
J Rabaey et al ”Digital Integrated Circutis”

Integration of III/V HEMTs on Si :
S Datta et al IEEE Electron Dev. Lett. 28, 2007 p 685 ” Ultrahigh-Speed 0.5 V Supply ...”

HEMTS for Beyond-CMOS:
D-H Kim et al IEEE Trans. Electron Dev. 54, 2007 p 2606 ” Logic Suitability of 50 nm ...”

CMOS Dynamic and Static Power Consumption

Advantages with CMOS:

Full logic swing
High noise margin
Superior robustness
Absence of steady state power consumption

Robust low-power digital technology

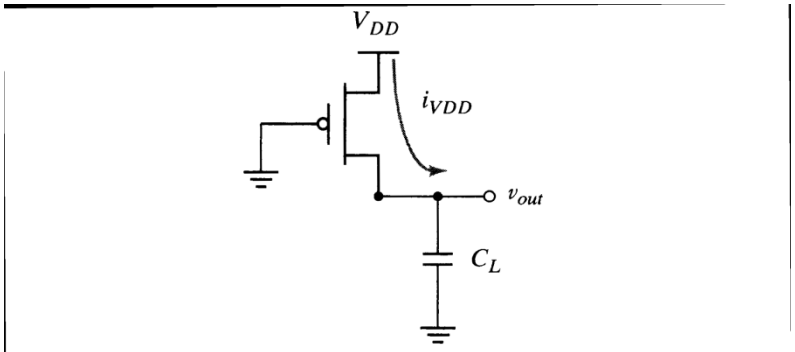


Figure 5-25 Equivalent circuit during the low-to-high transition.

Calculate the charging energy:

$$E_{VDD} = \int_0^\infty i_{VDD}(t) V_{DD} dt = V_{DD} \int_0^\infty C_L \frac{dv_{out}}{dt} dt = C_L V_{DD} \int_0^{VDD} dv_{out} = C_L V_{DD}^2$$

Calculate the stored energy:

$$E_C = \int_0^\infty i_{VDD}(t) v_{out} dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{VDD} v_{out} dv_{out} = \frac{C_L V_{DD}^2}{2}$$

Dynamic Power Consumption

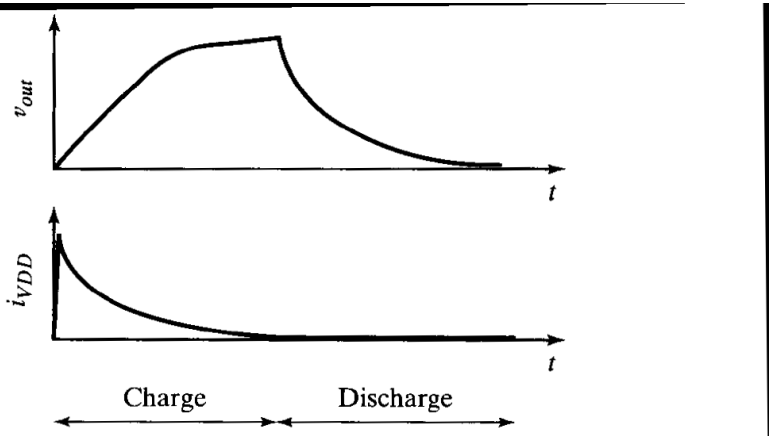


Figure 5-26 Output voltages and supply current during (dis)charge of C_L.

During charging (low-to-high transition) half energy is stored on capacitor, half energy is dissipated in the transistor

During discharging (high-to-low transition) half energy is stored on capacitor, the stored energy (half energy) is dissipated in the transistor

$$P_{dyn} = C_L V_{DD}^2 f_{0->1}$$

Example: 0.25 μm CMOS
f=500 MHz C_L=15fF/gate
V_{DD}=2.5V
P_{dyn}=50 μW

Direct-Path Current Power Consumption

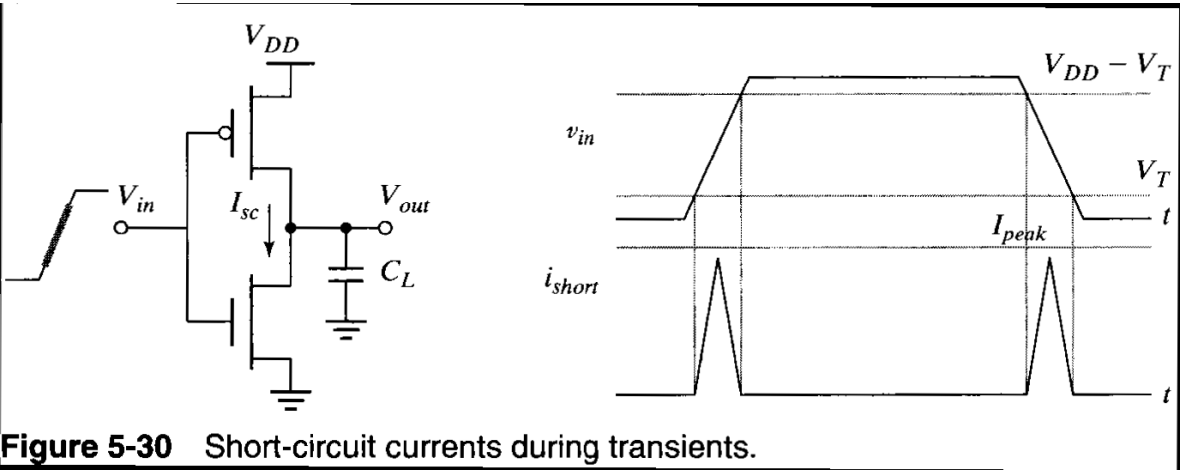


Figure 5-30 Short-circuit currents during transients.

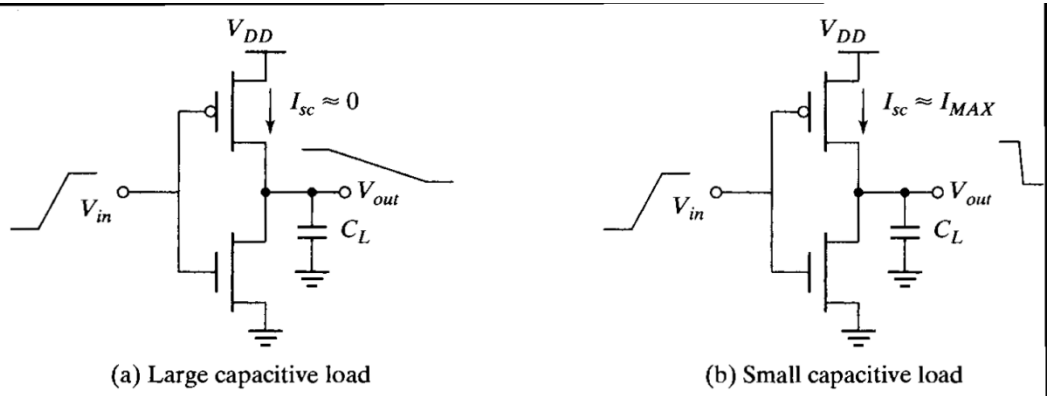
During the finite time switching, a direct current is flowing in the transistor pair

Assume triangular current peaks

$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = t_{sc}V_{DD}I_{peak}$$

$$P_{dp} = t_{sc}V_{DD}I_{peak}f = C_{sc}V_{DD}^2 f$$

Reduction via Design of Load Capacitance



(a) Large capacitive load (b) Small capacitive load

Figure 5-31 Impact of load capacitance on short-circuit current.

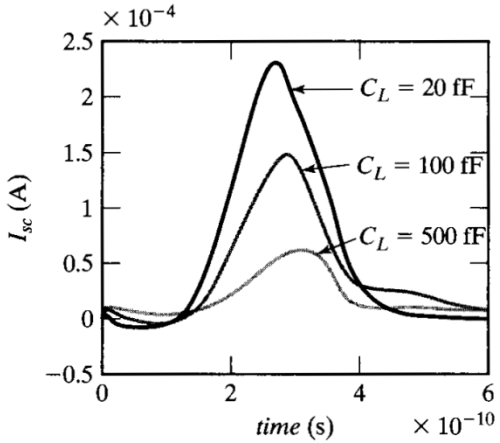
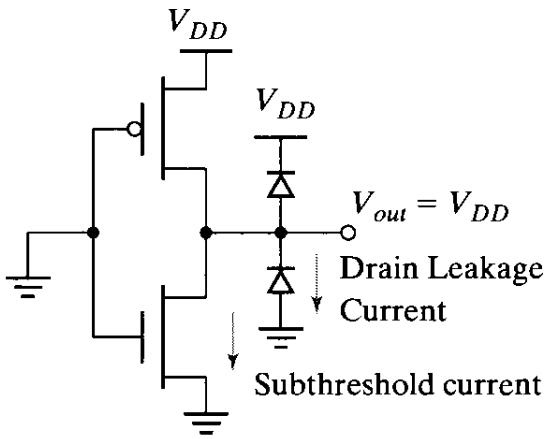


Figure 5-32 CMOS inverter short-circuit current through NMOS transistor as a function of the load capacitance (for a fixed input slope of 500 ps).

Using a large load capacitance, the voltage remains across the NMOS transistor during the switching cycle, which limits the current flow in the direct current path.

Static Power Consumption

Leakage current typically 10-100 pA/μm^2. Drain area 0.5 μm^2 and 1 million gates with V_{DD}=2.5 V gives 0.125 mW. But strong temperature effects!



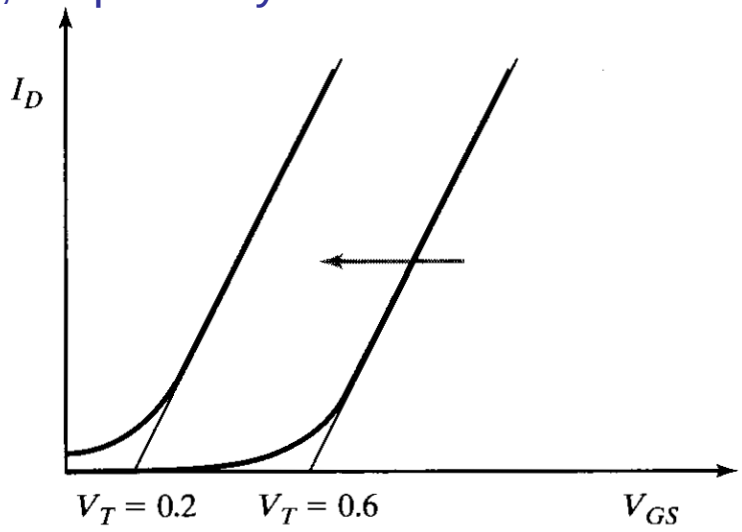
$$P_{stat} = I_{stat} V_{DD}$$

Figure 5-34 Sources of leakage currents in CMOS inverter (for V_{in} = 0 V).

Subthreshold Leakage

As the drive voltage is reduced, the threshold voltage should also be scaled (recall $V_t \sim V_{DD}/3$!). This implies that the subthreshold current is substantially increased.

Consider a 0.25 μm NMOS transistor with SS of 90 mV/dec. and V_t=0.5 V. At V_{GS}=0 V it consumes about 10^{-11} A. Reducing the threshold to 0.3 V increased the Current a factor 170! This gives a power consumption of $10^6 \times 170 \times 10^{-11} \times 1.25$=2.6mW. A reduction in V_t to 0.1 V gives a power consumption of 0.5 W!
The threshold voltage reduction corresponds to a performance improvement of 25 and 40 %, respectively.



POWER DOWN!

Figure 5-35 Decreasing the threshold increases the subthreshold current at $V_{GS} = 0$.

Put It All Together!

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat} = \left(C_L V_{DD}^2 + V_{DD} I_{peak} t_s \right) f_{0->1} + V_{DD} I_{leak}$$

Typically dominant

Can be reduced

Will be more important in scaled technologies

The Power-Delay Product

Introduce the power-delay product
as a quality measure of a logic gate:

$$PDP = P_{av} t_p$$

If the gate is switched at full speed, the PDP corresponds
To the average energy consumed per switching event
(0->1 or 1->0 transition)

$$PDP = C_L V_{DD}^2 f_{\max} t_p = \frac{C_L V_{DD}^2}{2}$$

Better, The Energy-Delay Product

Introduce the energy-delay product, which
balances the performance and energy consumption!

$$EDP = PDP \times t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$

t_p is the propagation delay (gate delay) and $f_{max}=1/(2t_p)$

Voltage Dependence on EDP!!!

$$EDP = PDP \times t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$

$$t_p \approx \frac{\alpha C_L V_{DD}}{(V_{DD} - V_T)^2}$$

$$EDP = \frac{\alpha C_L^2 V_{DD}^3}{2(V_{DD} - V_T)^2}$$

$$V_{DDopt} = \frac{3}{2} V_{TE}$$!!!!!!

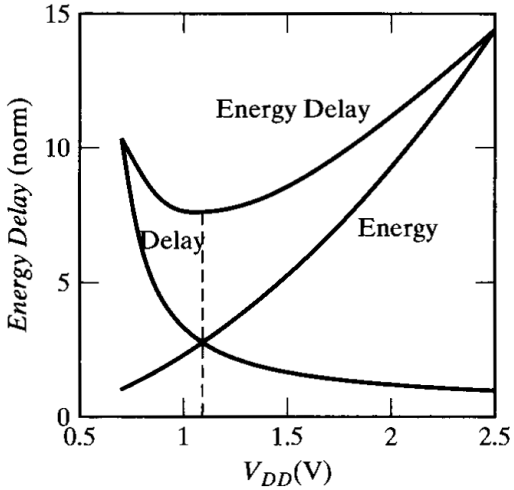


Figure 5-36 Normalized delay, energy, and energy-delay plots for CMOS inverter in 0.25-µm CMOS technology.

But what is α and V_{Te}??

Transistor model in linear region:

$$I_D = \frac{\mu\varepsilon_{ox}}{t_{ox}}\frac{W}{L}\left[(V_{GS}-V_t)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

Transistor model in saturation region:

$$I_D = \frac{\mu\varepsilon_{ox}}{2t_{ox}}\frac{W}{L}(V_{GS}-V_t)^2$$

Compare ballistic model:

$$I_{Dsat} = v_{inj}\frac{\varepsilon_{ox}}{t_{ox}}W(V_{GS}-V_t)$$

But what is α and V_{Te}??

Use the average transistor resistance:

$$R_{eq} = -\frac{1}{V_{DD}/2}\int_{V_{DD}}^{V_{DD}/2}\frac{V}{I_{DSAT}}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}$$

Expand linear model to saturation region ($V_{DSAT}=V_{GS}-V_T$):

$$I_{DSAT} = \frac{\mu\varepsilon_{ox}}{t_{ox}}\frac{W}{L}\left(V_{DD}-V_t\right)^2$$

Note $V_{GS}=V_{DD}$!!:

Calculate t_p:

$$t_p = \frac{t_{pHL}+t_{pLH}}{2} = \ln 2 \times C_L\left(\frac{R_{eqn}+R_{eqp}}{2}\right)$$

$$t_{pHL} = \ln 2 \times \frac{3}{4}\frac{C_L V_{DD}}{(W/L)_n\left(\mu_n\varepsilon_{ox}/t_{ox}\right)\left(V_{DD}-V_{tn}\right)^2}$$

$$t_{pHL} = \ln 2 \times \frac{3}{4}\frac{C_L}{(W/L)_n\left(\mu_n\varepsilon_{ox}/t_{ox}\right)V_{DD}} \quad \text{if} \quad V_{DD} >> V_{Tn}$$

But what is α and V_{Te}??

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = \ln 2 \times C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$$

$$t_{pHL} = \ln 2 \times \frac{3}{4} \frac{C_L V_{DD}}{(W/L)_n \left(\mu_n \varepsilon_{ox} / t_{ox} \right) \left(V_{DD} - V_{Tp} \right)^2}$$

α_n

Assume equal threshold voltages and saturation voltages for NMOS and PMOS!

$$t_p = \alpha_n \frac{C_L V_{DD}}{\left(V_{DD} - V_{Tn} \right)^2} + \alpha_h \frac{C_L V_{DD}}{\left(V_{DD} - V_{Tp} \right)^2} = \alpha \frac{C_L V_{DD}}{\left(V_{DD} - V_T \right)^2}$$

Ultrahigh-Speed 0.5 V Supply Voltage $In_{0.7}Ga_{0.3}As$ Quantum-Well Transistors on Silicon Substrate

Suman Datta, *Senior Member, IEEE*, G. Dewey, J. M. Fastenau, *Member, IEEE*, M. K. Hudait, D. Loubychev, W. K. Liu, *Senior Member, IEEE*, M. Radosavljevic, W. Rachmady, and R. Chau, *Fellow, IEEE*

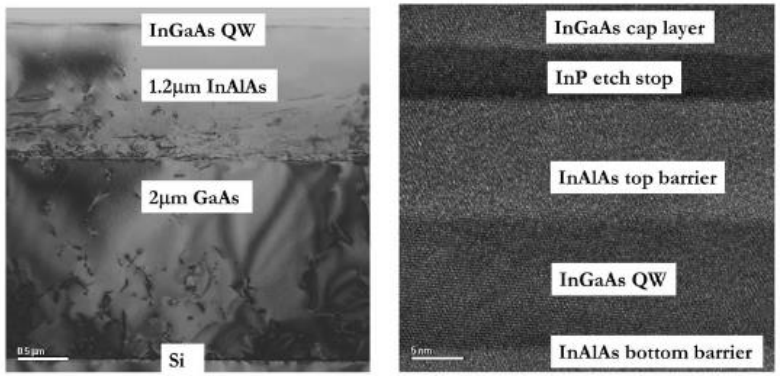


Fig. 1. Cross-sectional TEM images of $In_{0.7}Ga_{0.3}As$ QW structures on Si using metamorphic buffer architecture: (a) Entire layer structure. (b) magnification of $In_{0.7}Ga_{0.3}As$ QW along with bottom and top barrier layers. The misfit dislocations are predominantly contained in the buffer layer.

- buffer layer techniques are available
- comparable mobility

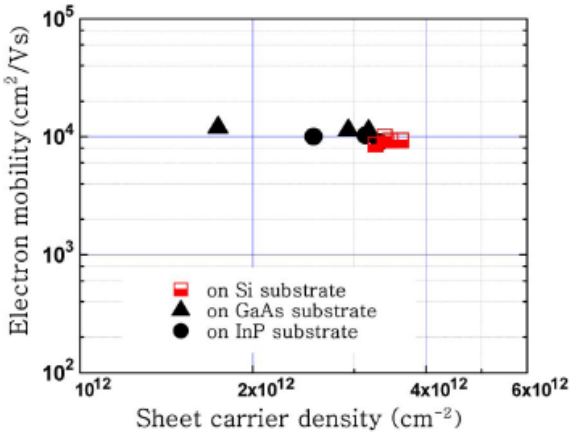


Fig. 2. Electron mobility versus sheet carrier density in n-channel $In_{0.7}Ga_{0.3}As$ QW device layers grown on Si, GaAs, and InP substrates. In all cases, $In_{0.52}Al_{0.48}As$ is the bottom and top barrier layer.

Comparable RF-data!

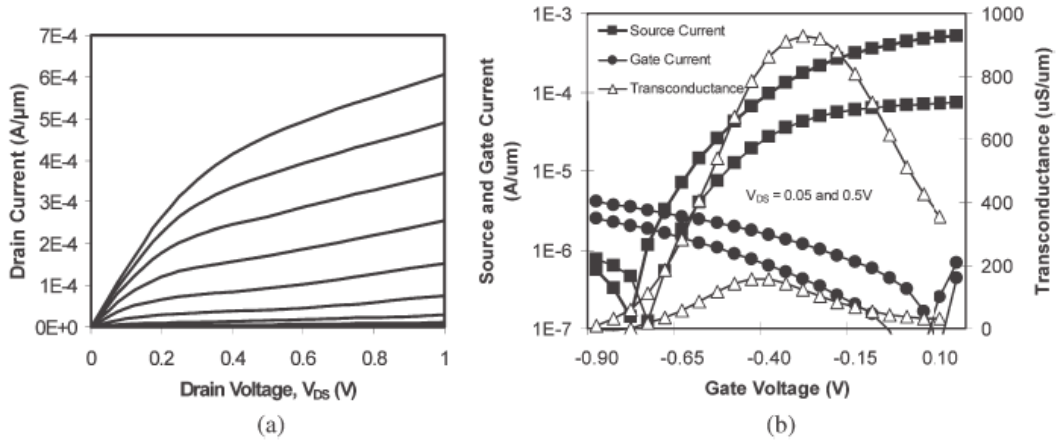


Fig. 3. (a) Output characteristic for 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistor on 3.2-μm metamorphic buffer on silicon (gate voltage V_G is swept from 0.0 to -0.8 V in -0.1-V steps). (b) Transfer characteristic for 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistor on 3.2-μm buffer on silicon with $V_{DS} = 0.5$ and 0.05 V. Peak transconductance g_m for this device was 930 $\mu S/\mu m$ at $V_{DS} = 0.5$ V.

- well behaved IV characteristics!
- good DC numbers at 80 nm Lg
- comparable RF data to lattice matched devices

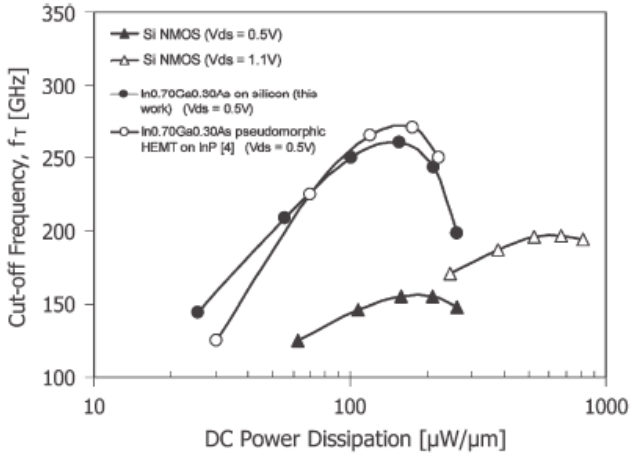


Fig. 4. Plot of deembedded unity gain cutoff frequency as a function of dc power dissipation for 0.5-V V_{DS} 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistors on both silicon and InP substrates, benchmarked against 60-nm L_g silicon NMOS transistors at $V_{DS} = 0.5$ and 1.1 V.

Logic Suitability of 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs for Beyond-CMOS Applications

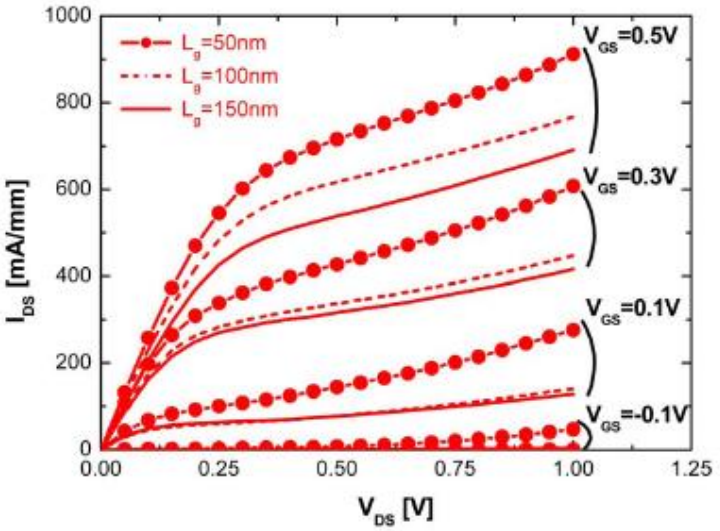
Dae-Hyun Kim, Jesús A. del Alamo, Jae-Hak Lee, and Kwang-Seok Seo

n+ Cap	InGaAs, x = 0.53	20 nm
Stopper	InP	6 nm
Barrier	InAlAs, x = 0.52	8 nm
δ-doping	Si	-
Spacer	InAlAs, x = 0.52	3 nm
Channel	InGaAs, x = 0.53	3 nm
	InGaAs, x = 0.7	8 nm
	InGaAs, x = 0.53	4 nm
Buffer	InAlAs, x = 0.52	500 nm
3 Inch S. I. InP Substrate		

Fig. 1. Epitaxial layer structure of the $In_{0.7}Ga_{0.3}As$ HEMTs that are fabricated in this paper.

TABLE I
DETAILED GATE STRUCTURAL INFORMATION FOR FOUR TYPES OF $In_{0.7}Ga_{0.3}As$ HEMTs THAT ARE FABRICATED IN THIS PAPER

	Type-A	Type-B	Type-C	Type-D
Barrier	$InP/In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$
Stack	Ti/Pt/Au	Ti/Pt/Au	Pt/Ti/Mo/Au	Buried-Pt/Ti/Mo/Au
t_{ins} [nm]	17	11	11	7
Φ_B [eV]	~0.4	~0.6	~0.7	~0.8



(d)

- 4 types of transistors
- Schottky barrier and insulator thickness
- good DC characteristics
- weak scaling with gate length

Scaling with Schottky barrier and insulator thickness

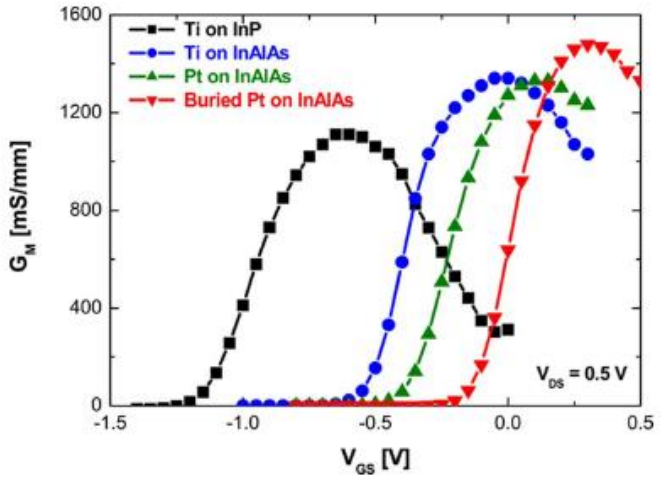


Fig. 5. Transconductance (G_m) characteristics of all 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs at $V_{DS} = 0.5$ V.

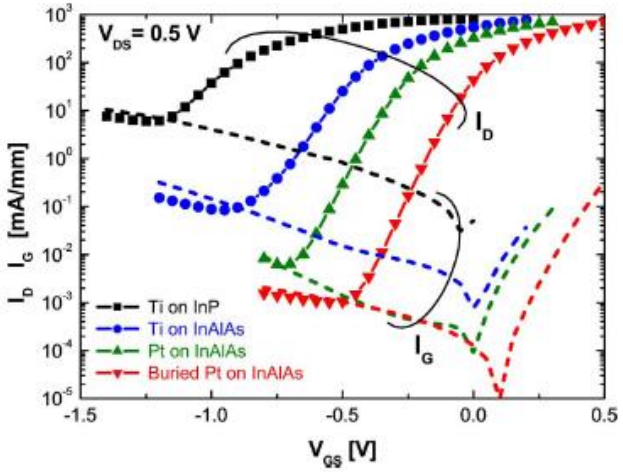


Fig. 6. Semilog plot of I_D and I_G of all 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs at $V_{DS} = 0.5$ V.

- Tight control needed to improve the performance

TABLE II
SUMMARY OF LOGIC FIGURES OF MERIT FOR FOUR TYPES OF 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs

	V_T [V]	DIBL [mV/V]	S [mV/dec]	I_{ON}/I_{OFF}
Type-A	-1.10	300	200	63
Type-B	-0.65	220	130	1×10^3
Type-C	-0.55	180	100	7.2×10^3
Type-D	-0.20	160	86	1.7×10^4

Improved speed and/or reduced power consumption

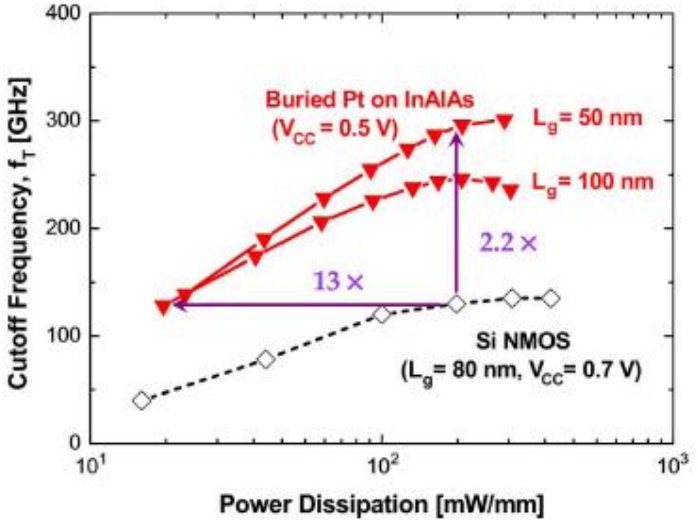


Fig. 11. Cutoff frequency (f_T) of our 50- and 100-nm type D $In_{0.7}Ga_{0.3}As$ HEMTs and 80-nm Si MOSFETs as a function of the dc power dissipation.

- Well selected technology is required to maximize Ion/Ioff ratio

- Depending on bias condition benefits can be found in the areas of speed and/or power dissipation

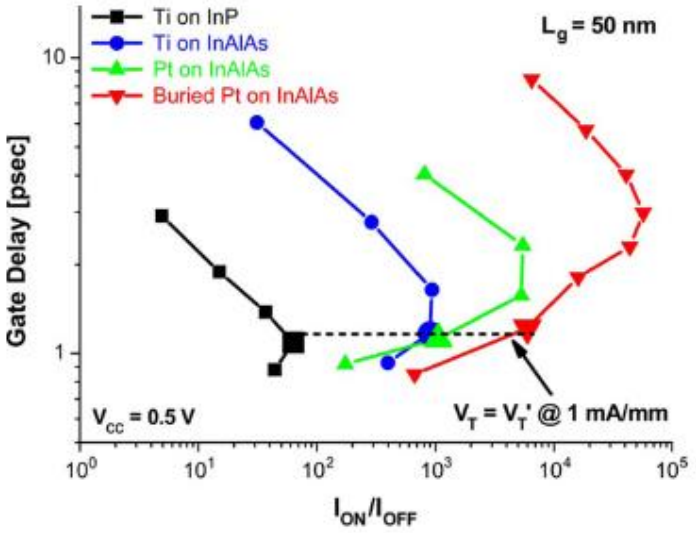


Fig. 14. Gate delay (CV/I) of all 50-nm $In_{0.7}Ga_{0.3}As$ as a function of I_{ON}/I_{OFF}.