Lecture 2: Scaled CMOS

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Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications

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Transistor evolution:

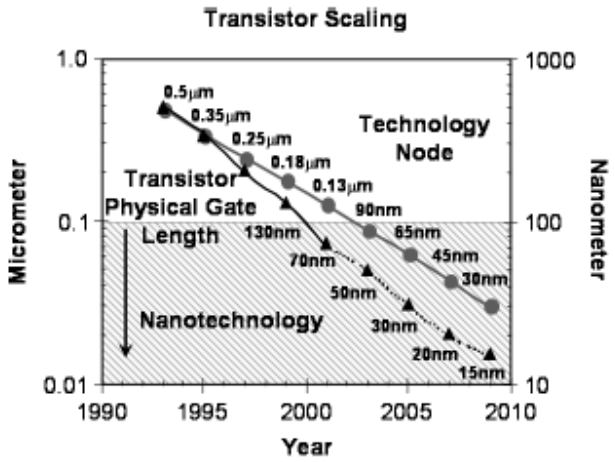

Fig. 1. Scaling of transistor size (physical gate length) with technology node to sustain Moore's Law. Nodes with feature size less than 100 nm can be referred to as nanotechnology. By 2011, the gate length is expected to be at or below 10 nm. Transistor scaling will be enabled by integration of emerging nanotechnology options on to the Si platform.

Four key metrics for logics:

Speed
Intrinsic speed (CV/I)

Switching energy
Energy-delay product ($CV/I*CV^2$)

Scalability
Subthreshold slope vs L_g

Off-state leakage
CV/I vs I_{on}/I_{off}

Method for benchmarking

Typical nanotube characteristics:

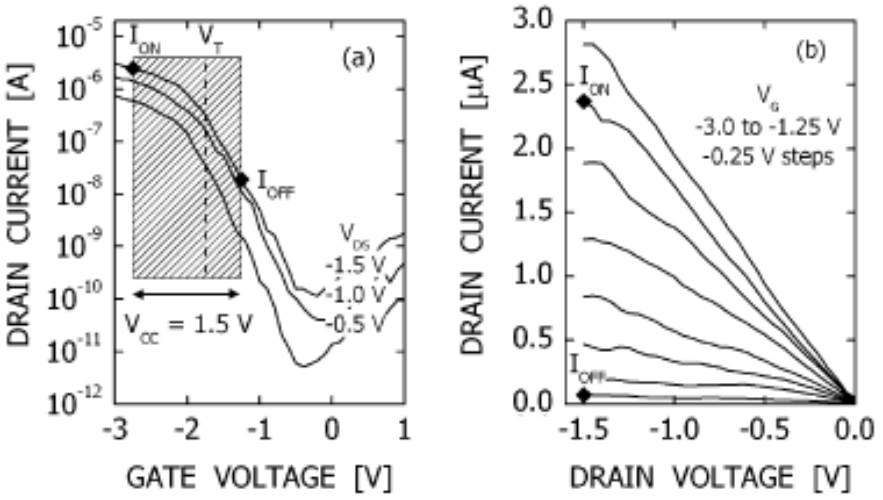

Fig. 3. Example (a) I_D–V_G and (b) I_D–V_{DS} characteristics of a CNT FET illustrating our benchmarking procedure. The V_{CC} choice is made by selecting the highest available V_{DS}, which, in this example, is 1.5 V. The shaded box in (a) is anchored around $V_G = V_T$, as discussed in the text. The width of the box denotes the V_G swing of 1.5 V, which is consistent with the V_{CC} choice. The values of I_{ON} and I_{OFF} are shown as black diamonds in both (a) and (b).

Definition of data points:

$|V_{DS}|=V_{CC}$

V_g 2/3 above V_t gives I_{on}
V_g 1/3 below V_t gives I_{off}
Calculate/measure the capacitance

Cylindrical devices:

$$C_{TOTAL}^{-1} = C_{OX}^{-1} + C_{QM}^{-1}$$

$$C_{OX} = 2\pi\varepsilon_0\varepsilon_r / \ln(2h/R)$$

Normalization by width $2\pi R$

Gate Delay

NMOS:

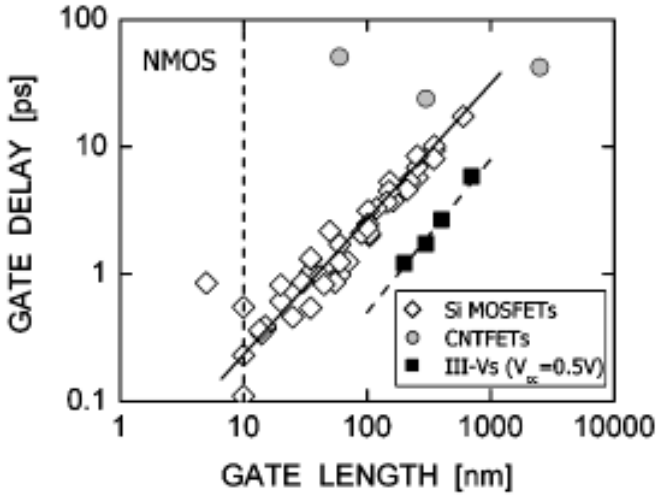

Fig. 5. Gate delay (intrinsic device speed, CV/I) versus transistor physical gate length of NMOS devices.

PMOS:

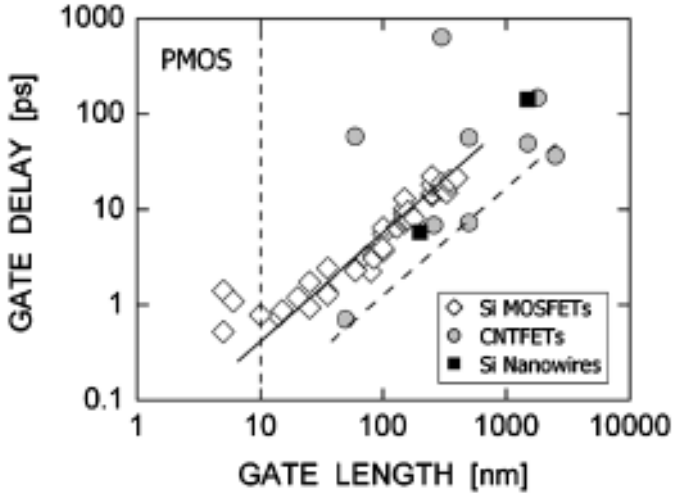

Fig. 4. Gate delay (intrinsic device speed CV/I) versus transistor physical gate length of PMOS devices.

III/V NMOS have better performance!

Energy-delay product

NMOS:

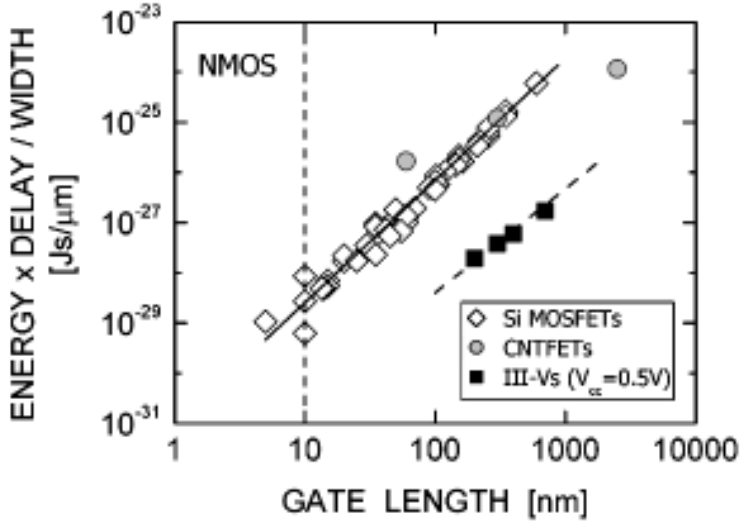

Fig. 7. Energy-delay product per device width versus transistor physical gate length of NMOS transistors.

PMOS:

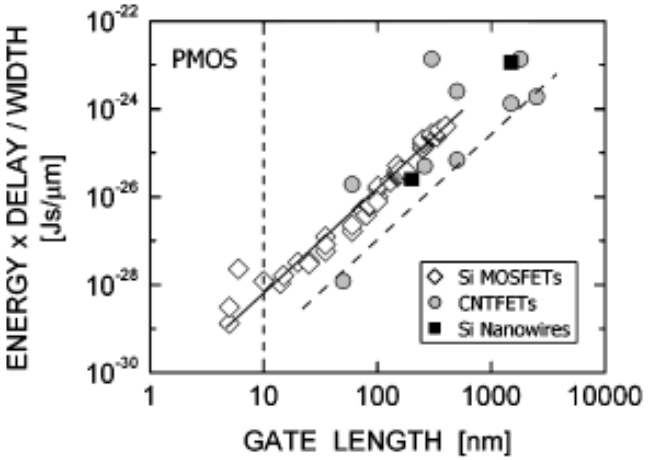

Fig. 6. Energy-delay product per device width versus transistor physical gate length of PMOS transistors.

III/V NMOS have better performance!

Scalability and leakage

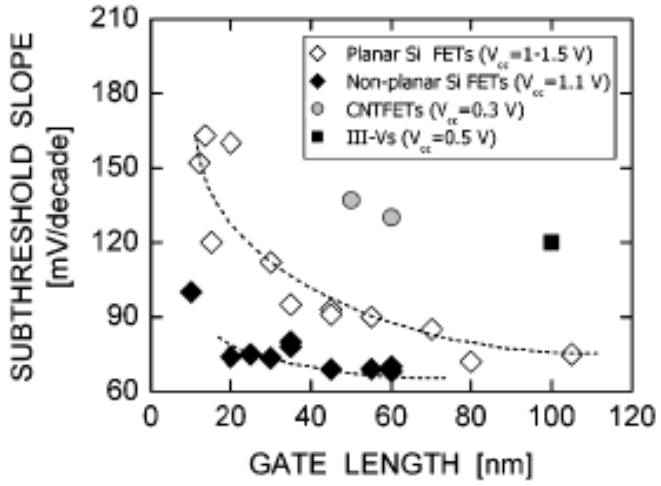

Fig. 8. Subthreshold slope versus transistor physical gate length. The planar and nonplanar Si FETs as well as the III–V planar devices are n-channel transistors, while the CNT FETs are p-channel transistors.

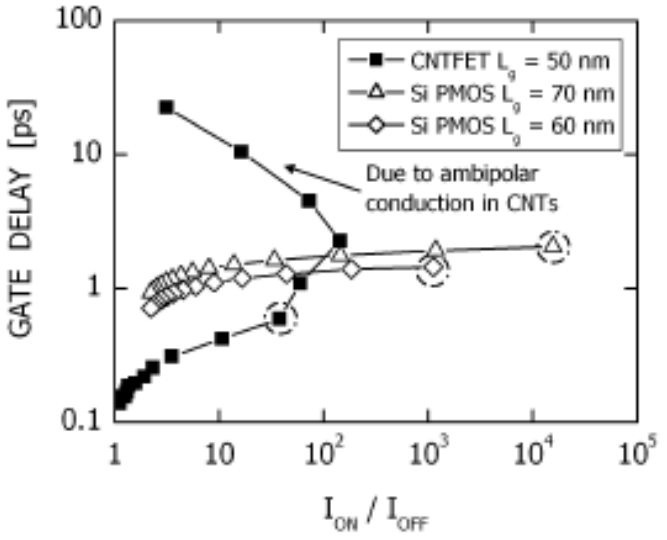

Fig. 11. Gate delay (intrinsic device speed, CV/I) versus on-to-off state current ratio I_{ON}/I_{OFF} of Si PMOS transistors with $L_g = 60$ nm and 70 nm at $V_{CC} = 1.3$ V, and a CNT PMOS transistor with $L_g = 50$ nm and $V_{CC} = 0.3$ V [15]. The three circled points were used in the PMOS CV/I versus L_g plot in Fig. 4, where the V_G swing is anchored around $V_G = V_T$.

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High Performance Fully-Depleted Tri-Gate CMOS Transistors

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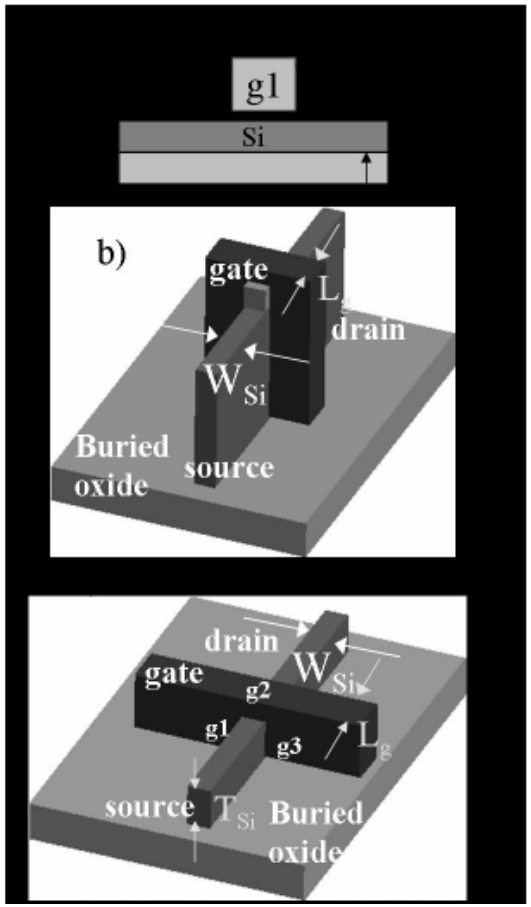
Advanced Device Architectures:



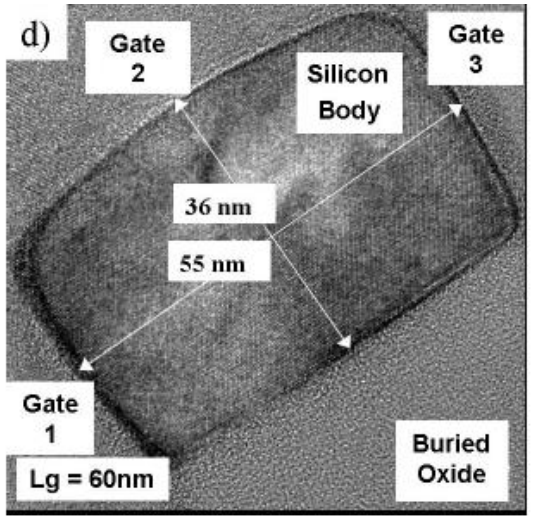
Planar single gate

Double-gate
(fin width one third of gate length)

Tri-gate
(body thickness about gate length)

CMOS

Si body of Tri-gate transistor



Performance of 60 nm gate length

I_{on}=0.52 mA/μm
I_{off}=24 nA/μm
SS=69.5 mV/dec

I_{on}=1.14 mA/μm
I_{off}=70 nA/μm
SS=68 mV/dec

DIBL=48 mV/V

DIBL=41 mV/V

DIBL=$V_{g@Vd=1.3V}$-$V_{g@Vd=0.05V}$/(1.3-0.05)
V_g taken at I_d=0.1 μA/μm

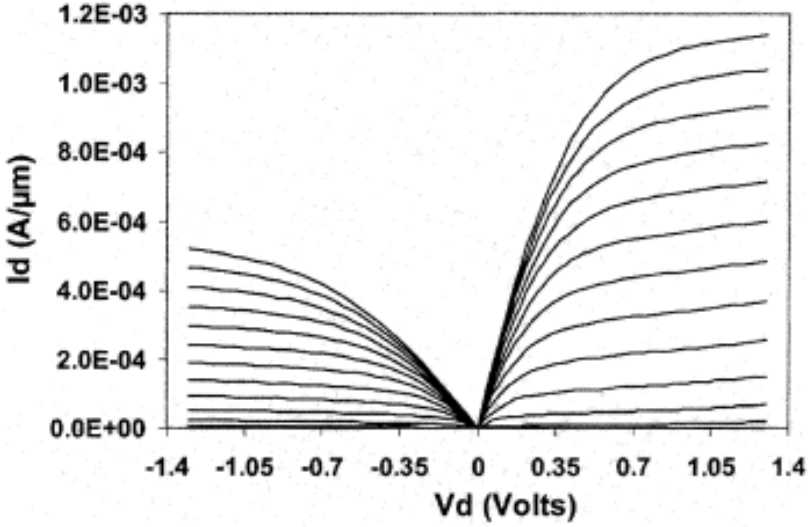


Fig. 3. I_d–V_d characteristics of the 60 nm N- and P-MOS devices of Fig. 2. The gate voltage was ramped to 1.3 V in increments of 0.1 V.

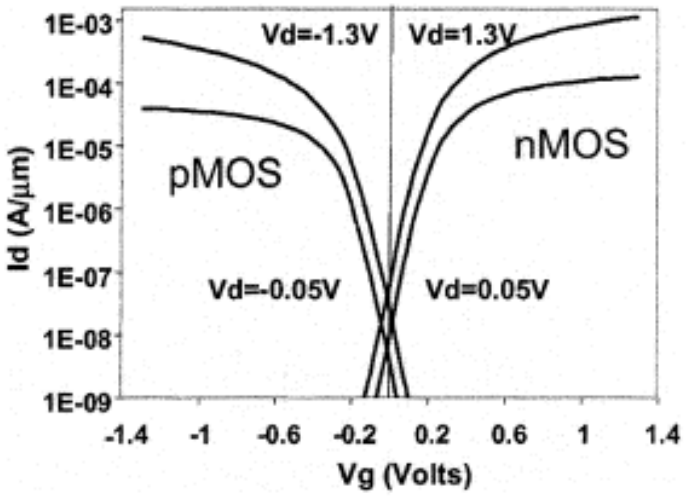


Fig. 2. I_d–V_g characteristics of 60 nm gate length NMOS and PMOS transistors. The current I_d is normalized to the width (Z) in all cases, where $Z = 2 * T_{Si} + W_{Si}$.

15 Å oxide thickness

Comparable to well-optimized planar devices!

Extreme Scaling with Ultra-Thin Si Channel MOSFETs

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Planar devices on Si SOI substrates

Reduces parasitics and leakage

Wafer thinning to 6±2 nm Si films!!!

But mobility degrades as the film is thinned down

Performance of ultra-thin Si channel MOSFETS

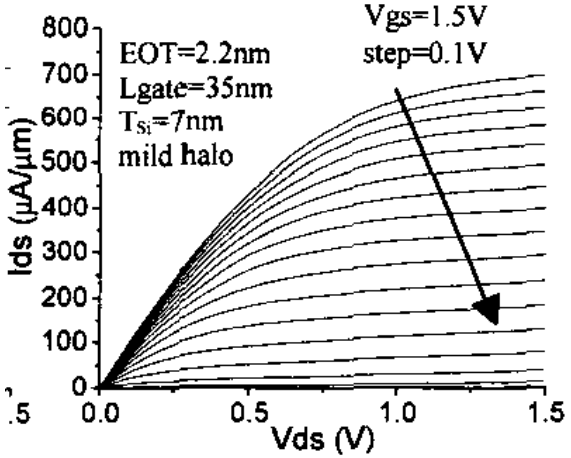

Fig. 7: Id-Vds characteristic of an nFET with a mild halo

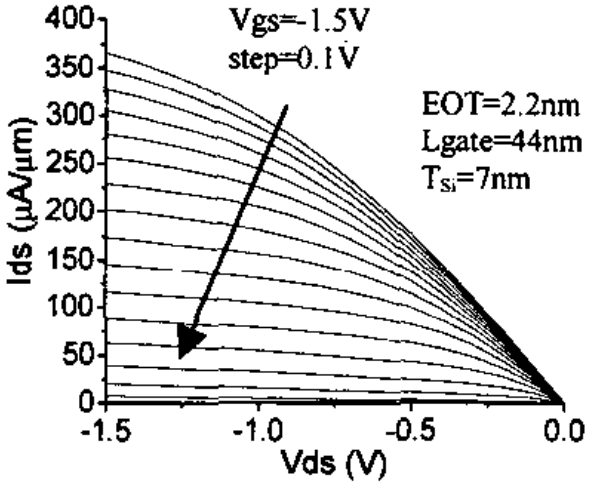

Fig.3: Ids-Vds characteristic of a pFET with thick gate dielectric

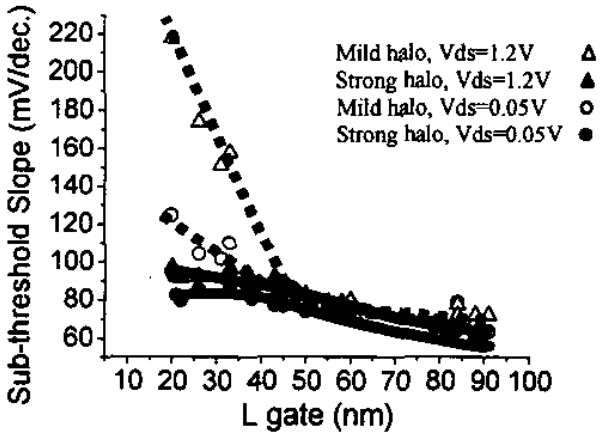

Fig.10: Sub-threshold slope for nFETs with thick gate dielectric and different halos

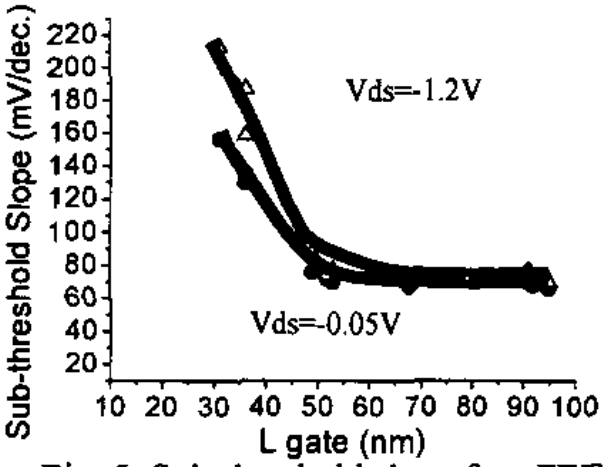

Fig. 5: Sub-threshold slope for pFETs with thick gate dielectric

Performance of 26 nm CMOS circuit

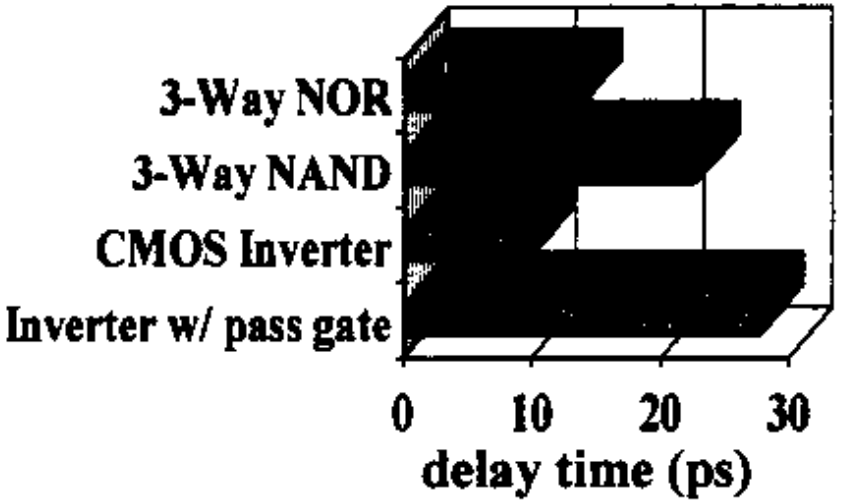

Fig.11: 26nm gate length CMOS ring-oscillator delays

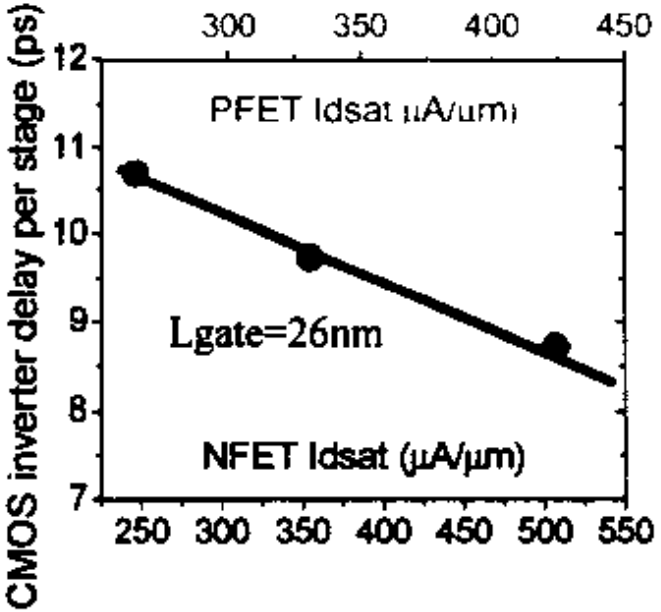

Fig.12: 26nm gate length CMOS inverter delays vs. Idsat

6 nm pFET: It works!

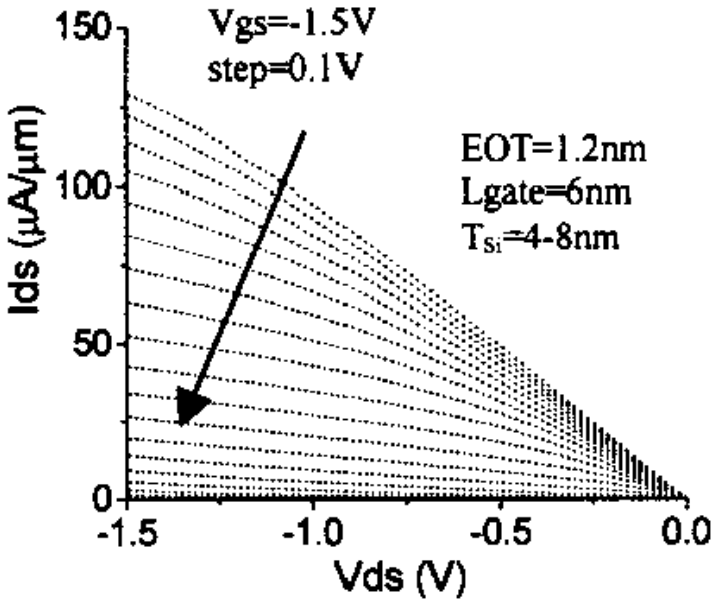

Fig.19: Ids-Vds characteristic of a 6nm pFET

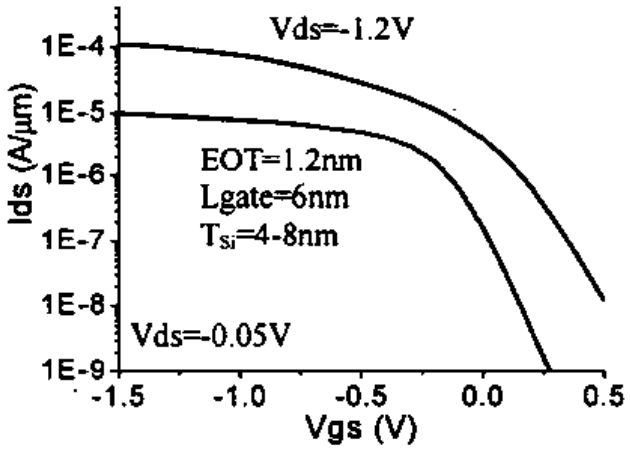

Fig.18: Ids-Vgs characteristic of a 6nm pFET

APPLIED PHYSICS LETTERS VOLUME 82, NUMBER 15 14 APRIL 2003

Study of interfacial reaction and its impact on electric properties of Hf–Al–O high-*k* gate dielectric thin films grown on Si

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Strong process dependence

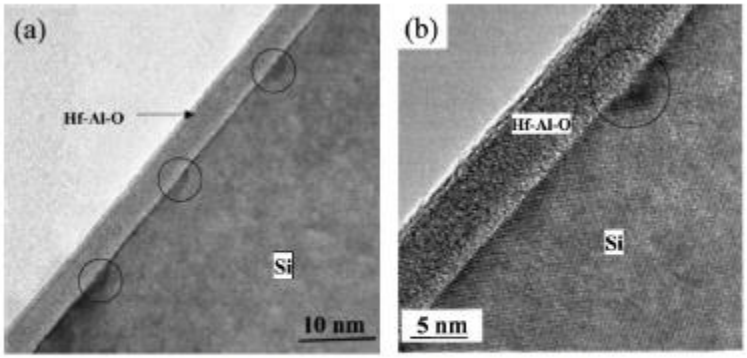

FIG. 1. Cross-sectional TEM images of a thin Hf–Al–O film on a (100) Si substrate. (a) Low magnification and (b) high resolution. The circles indicate the interfacial reaction.

Deposition techniques

PLD
ALD
Sputtering

Physical effects

Amorphous/crystalline
Amount of oxygen, stochiometry
Annealing
Interface reactions

Effects of Interface reactions

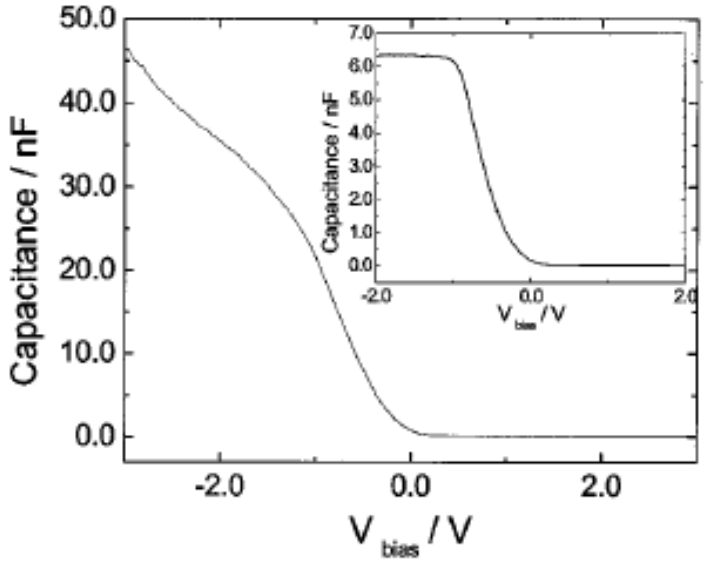

FIG. 3. High frequency (1 MHz) $C-V$ curve of a thin Hf–Al–O film with silicide reaction at the interface. The inset shows a well-behaved $C-V$ curve of a sample without interfacial reaction.

CV-technique

MOS capacitor
Effects of traps in the film and at the interfaces
Frequency response gives time scale
Minority carrier in inversion
Used to determined the charge
Split CV

$$\mu_{eff} = \frac{L}{W}\frac{g_d(V_g)}{qN_s(V_g)}$$

$$qN_s(V_g) = \int_{-\infty}^{V_g} C(V_g)dV_g$$