Lecture 2: Scaled CMOS

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R Chau et al IEEE Nanotech 4, 2005, p 153 "Benchmarking Nanotechnology for ...

Advanced CMOS Design:
B Doyle et al IEEE Electron Dev. Lett. 24, 2003, p. 263 ”High-performance Fully-Depleted Tri-gate ...

Extremely scaled MOSFETs:

High-k dielectrics on Si:
P Lee et al Appl. Phys. Lett.. 82, 2003, p 2419 ”Study of interfacial ....”
Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications

Robert Chau, Fellow, IEEE, Suman Datta, Member, IEEE, Mark Doczy, Brian Doyle, Ben Jin, Jack Kavalieros, Amlan Majumdar, Matthew Metz, and Marko Radosavljevic

Transistor evolution:

Four key metrics for logics:

**Speed**
Intrinsic speed (CV/I)

**Switching energy**
Energy-delay product (CV/I*CV^2)

**Scalability**
Subthreshold slope vs L_g

**Off-state leakage**
CV/I vs I_{on}/I_{off}

Nanoelectronics: Scaled CMOS
Method for benchmarking

Typical nanotube characteristics:

- \( |V_{DS}| = V_{CC} \)
- \( V_g \) 2/3 above \( V_t \) gives \( I_{on} \)
- \( V_g \) 1/3 below \( V_t \) gives \( I_{off} \)

Calculate/measure the capacitance

Cylindrical devices:

\[ C_{TOTAL}^{-1} = C_{OX}^{-1} + C_{QM}^{-1} \]

\[ C_{OX} = \frac{2\pi \varepsilon_0 \varepsilon_r}{\ln(2h/R)} \]

Normalization by width \( 2\pi R \)
Gate Delay

NMOS:

PMOS:

III/V NMOS have better performance!

Fig. 4. Gate delay (intrinsic device speed $CV/I$) versus transistor physical gate length of PMOS devices.

Fig. 5. Gate delay (intrinsic device speed $CV/I$) versus transistor physical gate length of NMOS devices.

Nanoelectronics: Scaled CMOS
Energy-delay product

**NMOS:**

![Graph showing energy-delay product for NMOS transistors](image)

*Fig. 7. Energy-delay product per device width versus transistor physical gate length of NMOS transistors.*

**PMOS:**

![Graph showing energy-delay product for PMOS transistors](image)

*Fig. 6. Energy-delay product per device width versus transistor physical gate length of PMOS transistors.*

**III/V NMOS have better performance!**
Scalability and leakage

Fig. 8. Subthreshold slope versus transistor physical gate length. The planar and nonplanar Si FETs as well as the III–V planar devices are n-channel transistors, while the CNT FETs are p-channel transistors.

Fig. 11. Gate delay (intrinsic device speed, $CV/I$) versus on-to-off state current ratio $I_{ON}/I_{OFF}$ of Si PMOS transistors with $L_g = 60$ nm and $70$ nm at $V_{CC} = 1.3$ V, and a CNT PMOS transistor with $L_g = 50$ nm and $V_{CC} = 0.3$ V [15]. The three circled points were used in the PMOS $CV/I$ versus $L_g$ plot in Fig. 4, where the $V_G$ swing is anchored around $V_G = V_T$. 
High Performance Fully-Depleted Tri-Gate CMOS Transistors

B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, Member, IEEE, A. Murthy, R. Rios, Member, IEEE, and R. Chau, Senior Member, IEEE

Advanced Device Architectures:

Planar single gate

Double-gate (fin width one third of gate length)

Tri-gate (body thickness about gate length)

Si body of Tri-gate transistor
Performance of 60 nm gate length

$I_{on}=0.52 \text{ mA/\mu m}$
$I_{off}=24 \text{ nA/\mu m}$
$SS=69.5 \text{ mV/dec}$

$I_{on}=1.14 \text{ mA/\mu m}$
$I_{off}=70 \text{ nA/\mu m}$
$SS=68 \text{ mV/dec}$

$DIBL=48 \text{ mV/V}$

$DIBL=V_{g@V_d=1.3V}-V_{g@V_d=0.05V}/(1.3-0.05)$

$V_g$ taken at $I_d=0.1 \text{ \mu A/\mu m}$

15 Å oxide thickness

Comparable to well-optimized planar devices!

Nanoelectronics: Scaled CMOS
Extreme Scaling with Ultra-Thin Si Channel MOSFETs


IBM Semiconductor Research and Development Center (SRDC)
Microelectronics Division, Hopewell Junction, NY 12533
IBM T. J. Watson Research Center, Yorktown Heights, NY 10598
e-mail: dorisb@us.ibm.com; phone: 845-892-3681

Planar devices on Si SOI substrates

Reduces parasitics and leakage

Wafer thinning to 6±2 nm Si films!!!

But mobility degrades as the film is thinned down
Performance of ultra-thin Si channel MOSFETS

Fig. 7: Id-Vds characteristic of an nFET with a mild halo

Fig. 3: Ids-Vds characteristic of a pFET with thick gate dielectric

Fig. 10: Sub-threshold slope for nFETs with thick gate dielectric and different halos

Fig. 5: Sub-threshold slope for pFETs with thick gate dielectric
Performance of 26 nm CMOS circuit

Fig. 11: 26 nm gate length CMOS ring-oscillator delays

Fig. 12: 26 nm gate length CMOS inverter delays vs. Idsat
6 nm pFET: It works!

Fig. 18: $I_{ds}$-$V_{gs}$ characteristic of a 6nm pFET

Fig. 19: $I_{ds}$-$V_{ds}$ characteristic of a 6nm pFET
Study of interfacial reaction and its impact on electric properties of Hf–Al–O high-k gate dielectric thin films grown on Si

P. F. Lee, J. Y. Dai, K. H. Wong, H. L. W. Chan, and C. L. Choy
Department of Applied Physics, The Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong, China

Strong process dependence
Deposition techniques

PLD
ALD
Sputtering

Physical effects
Amorphous/crystalline
Amount of oxygen, stochiometry
Annealing
Interface reactions

FIG. 1. Cross-sectional TEM images of a thin Hf–Al–O film on a (100) Si substrate. (a) Low magnification and (b) high resolution. The circles indicate the interfacial reaction.
Effects of Interface reactions

CV-technique

MOS capacitor
Effects of traps in the film and at the interfaces
Frequency response gives time scale
Minority carrier in inversion
Used to determine the charge

Split CV

\[ \mu_{eff} = \frac{L}{W} \frac{g_d(V_g)}{qN_s(V_g)} \]

\[ qN_s(V_g) = \int_{-\infty}^{V_g} C(V_g) dV_g \]