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LETTERS

Ge/Si nanowire heterostructures as high-performance field-effect transistors

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- Ge/Si core shell nanowires
- 15 nm core
- p-type conduction
- High-k dielectrics (ZrO_2)
- ballistic transport
- 500 nm mean free path

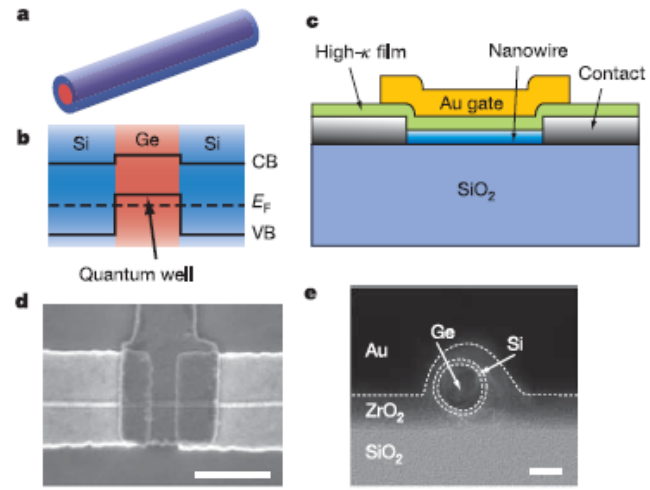
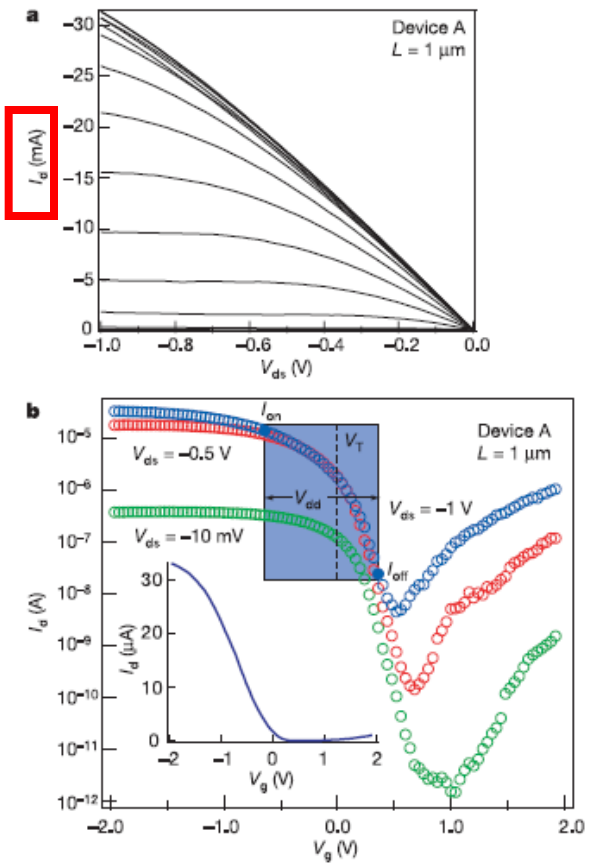


Figure 1 | Ge/Si core/shell NWFET. **a**, Schematic of a Ge/Si core/shell nanowire. **b**, Cross-sectional diagram showing the formation of hole-gas in the Ge quantum well confined by the epitaxial Si shell, where CB is the conduction band and VB is the valence band. The dashed line indicates the Fermi level, E_F. The valence band offset of ~500 meV between Ge and Si serves as a confinement potential to the hole-gas as discussed previously[7]. **c**, Schematic of the NWFET device with high-κ dielectric layer and Au top gate. **d**, Top-view SEM image of a typical device. The Au top gate overlaps with the Ni source/drain electrodes to ensure full coverage of the channel. Scale bar, 500 nm. **e**, Cross-sectional TEM image of a device prepared using 7 nm ZrO_2 dielectric. Dotted lines are guides to the eye showing boundaries between different materials denoted in the image. The nanowire is tilted off the imaging axis. Scale bar, 10 nm.

Device Characteristics



L_g=1 μm
g_m=26 μS
I_{dmax}=35 μA
Benchmark at 1V:
I_{on}=14 μA
g_m= 1.4 mS/μm
I_{on}=0.71 mA/μm

L_g=0.19 μm
g_m=60 μS
I_{dmax}=91 μA
Benchmark at 1V:
I_{on}=37 μA
g_m= 3.3 mS/μm
I_{on}=2.1 mA/μm
mobility=730 cm^2/V
SS=100 mV/dec.

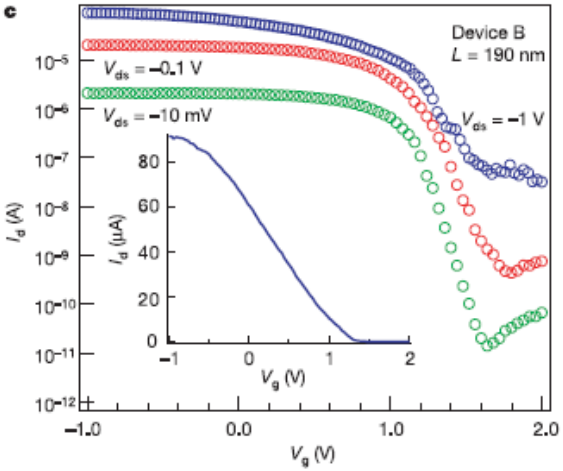


Figure 2 | Characteristics of high-performance Ge/Si NWFET. **a**, I_d–V_{ds} data for device A ($L = 1\,\mu m$, 4 nm HfO_2 dielectric) with $V_g = -2$ to 2 V in 0.25 V steps from top to bottom. **b**, I_d–V_g for device A with blue, red, and green data points corresponding to V_{ds} values of −1, −0.5 and −0.01 V, respectively. The leakage current through the gate electrode (I_g) is $<10^{-10}$ A, which excludes I_g as source of increase in I_d at $V_g > \sim 0.5$ V. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V. The blue-shaded area defines the 1 V gate voltage window described in the text, where V_T was determined from the intercept of the tangent of maximum slope (linear transconductance) region of the I_d–V_g curve[11]. **c**, I_d–V_g data for device B ($L = 190$ nm, 4 nm HfO_2 dielectric) with blue, red and green data points corresponding to V_{ds} values of −1, −0.1 and −0.01 V, respectively. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V.

Device Performance

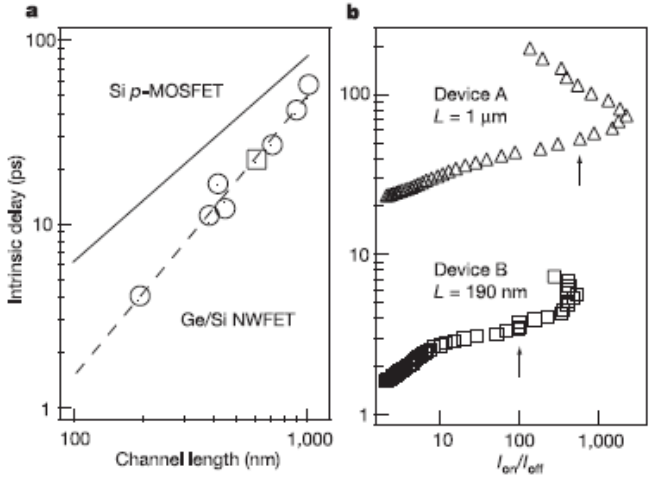


Figure 3 | Benchmark and comparison of Ge/Si FETs. **a**, Intrinsic delay τ versus channel length for seven different Ge/Si nanowire devices with HfO_2 dielectric (open circle) and ZrO_2 dielectric (open square). Data for devices A and B are included. The I_{on} values were measured at $V_{g(on)} = V_T - 0.7V_{dd}$, as discussed in the text. The dashed line is a fit to the data points while solid line is the Si p-MOSFET results from ref. 4. **b**, Intrinsic delay versus on/off ratio for the two devices in Fig. 2. Arrows indicate the values of intrinsic delay used in **a**.

V_T shift due to different work functions

Gate delay:

-L_g=1 μm => τ=57 ps
-L_g=0.19 μm => τ=4 ps

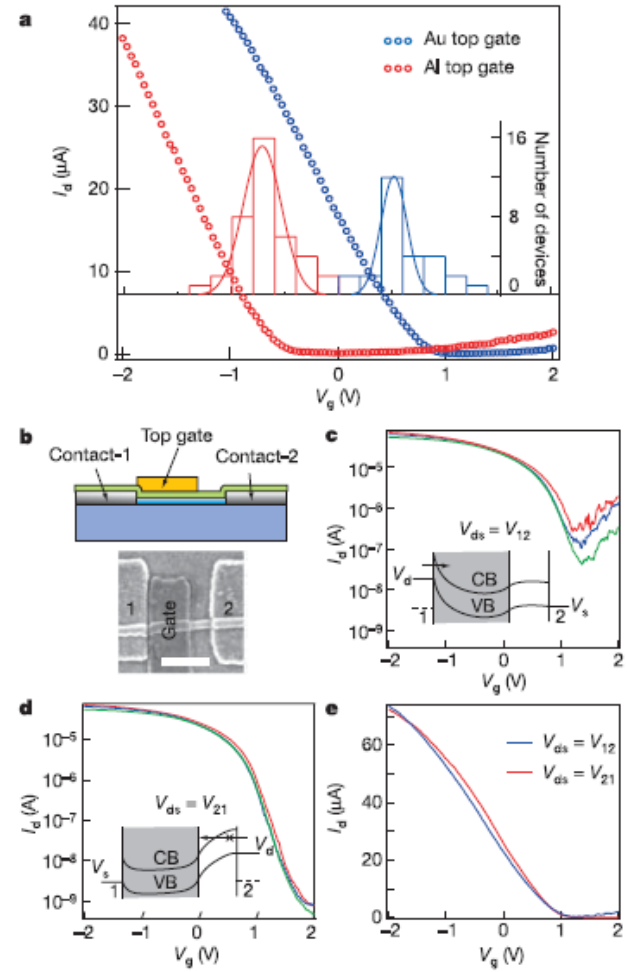
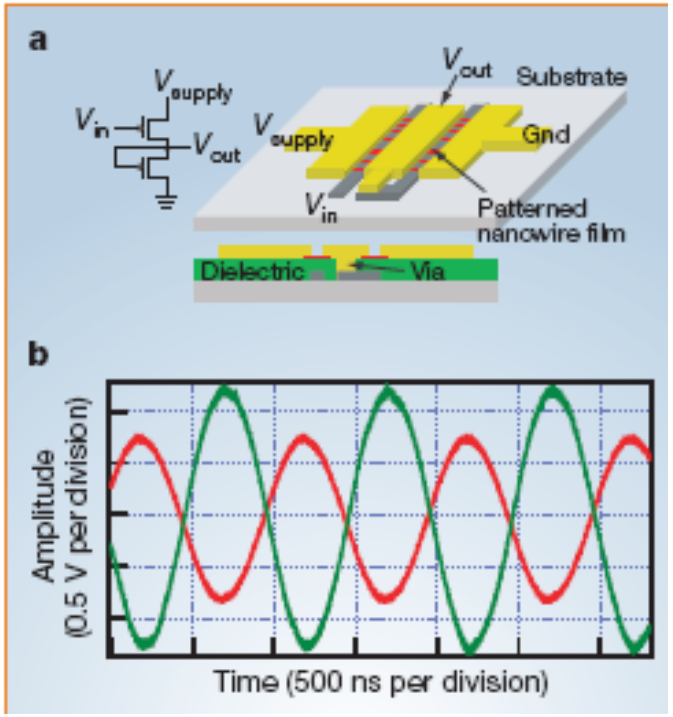


Figure 4 | Control of threshold voltage and ambipolar conduction through device design. **a**, I_d–V_g curves for two $L = 300$ nm devices with Au (blue) and Al (red) top gate electrodes ($V_{ds} = -1$ V). Inset shows histogram of V_T with the same V_g axis for a total of 68 $L = 300$ nm devices with Au (blue) and Al (red) top gates. Solid lines correspond to gaussian fits to the two distributions. **b**, Schematic and SEM image of the asymmetrical gate structure designed to suppress ambipolar conduction. Scale bar, 300 nm. **c**, I_d–V_g of partially gated device with ambipolar conduction; bias was applied to contact 1 ($V_{ds} = V_{12}$). Inset, schematic of band bending in the NWFET at finite bias. Arrow denotes electron injection at the drain contact. **d**, I_d–V_g for $V_{ds} = V_{21}$. Inset, schematic of band bending with electron injection denoted by arrow. The red, blue and green curves in **c** and **d** correspond to V_{ds} values of -1, -0.8 and -0.6 V, respectively. **e**, Linear scale I_d–V_g ($V_{ds} = -1$ V) for the devices in **c** and **d**. The two devices have the same peak $g_m = 35\,\mu$S and $I_{d(max)} = 73\,\mu$A.

Nanoelectronics: Si Nanowires

High-speed integrated nanowire circuits

Inexpensive sophisticated circuitry can be 'painted' on to plastic or glass substrates.



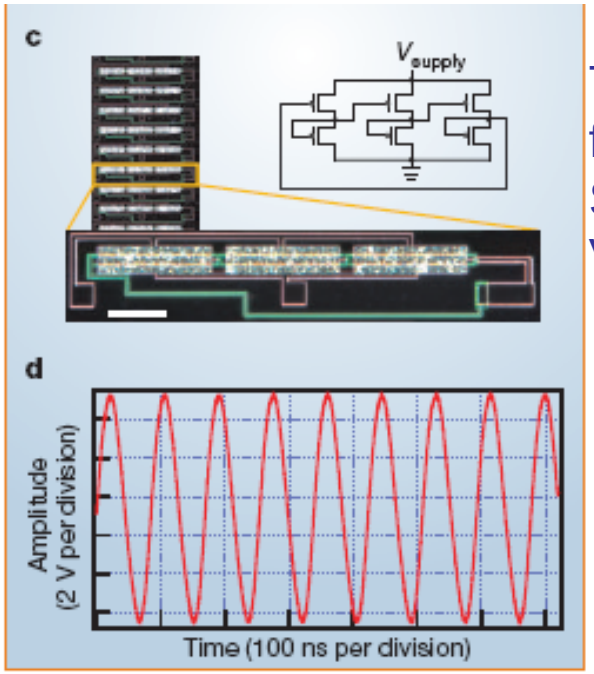


Figure 1 Alternating-current properties of integrated multi-nanowire circuits on glass. **a**, Circuit diagram and schematics of the multi-nanowire inverters. Labelled voltages are bias (V_{supply}), input (V_{in}) and output (V_{out}) voltage. The dielectric is omitted in the perspective schematic for clarity. 'Via' indicates one of a pattern of holes in the dielectric layer that are used to connect different metal layers. **b**, Output waveform (green) of an inverter fabricated on glass driven by a 1-MHz sine wave (red) with $V_{supply} = 15$ V. **c**, Optical images and circuit diagram of nanowire ring oscillators. The gate level edge, source-drain level edge and nanowires appear green, pink and white, respectively, in dark field. Scale bar, 100 μm. **d**, Oscillation of 11.7 MHz in a ring oscillator structure with $V_{supply} = 43$ V.

Three stage ring oscillator
f=11.7 MHz
Stage delay=14 ns
V_{dd}=43 V

Response of inverter with gain
1 MHz sine wave as drive
V_{dd}=15 V

Nanoelectronics: Si Nanowires

IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO. 3, MARCH 2007 211

Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors

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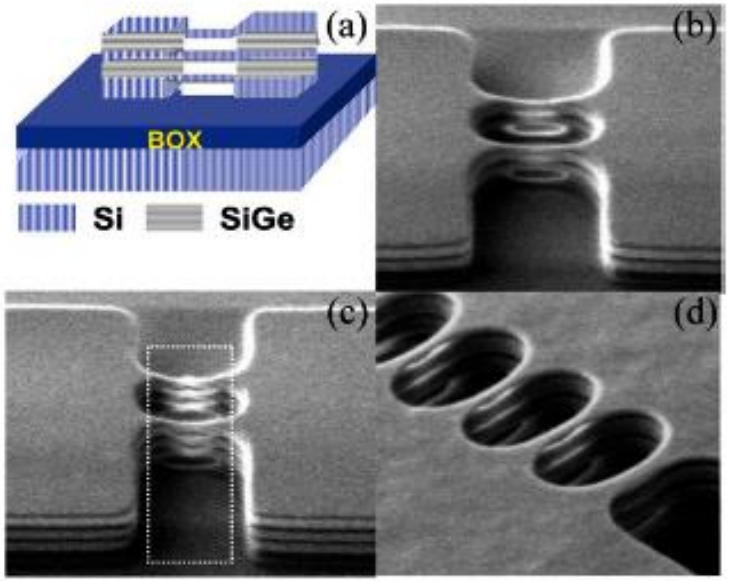

Fig. 1. Tilted view SEM images after release of stacked NW. (a) Schematic of SiGe NW stacks after oxidation and release. (b) 2X laterally arrayed three-stacked NWs. (c) 2X laterally arrayed four-stacked NWs with the dashed line indicating the gate layout. (d) 5X laterally arrayed four-stacked NWs.

-Ge condensation technigue

-- SiGe oxidizes faster than Si

-patterning of 100 nm fins

- cyclic oxidation and etching to 20-30 nm diameter wires

- 350 nm gate length, t_{ox} 4 nm

- i-Si and implantation of S/D regions

Device characteristics

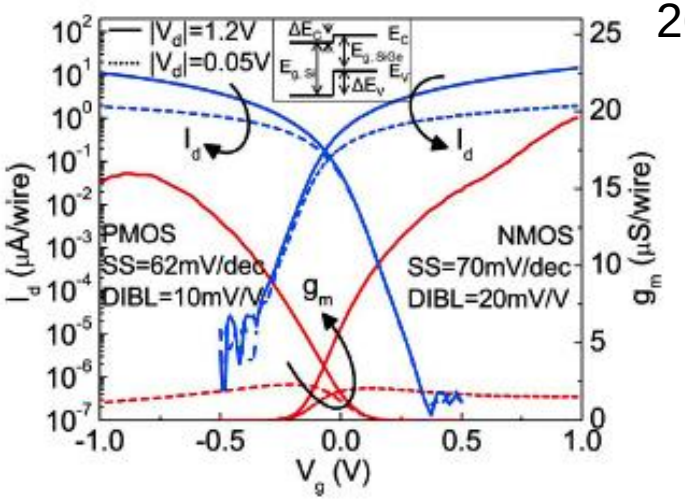

Fig. 2. Per NW I_d–V_g and g_m–V_g plots for stacked NW n-FETs and p-FETs with $L_g = 500$ nm and NW diameter ~30 nm.

265 mS/mm

159 mA/mm

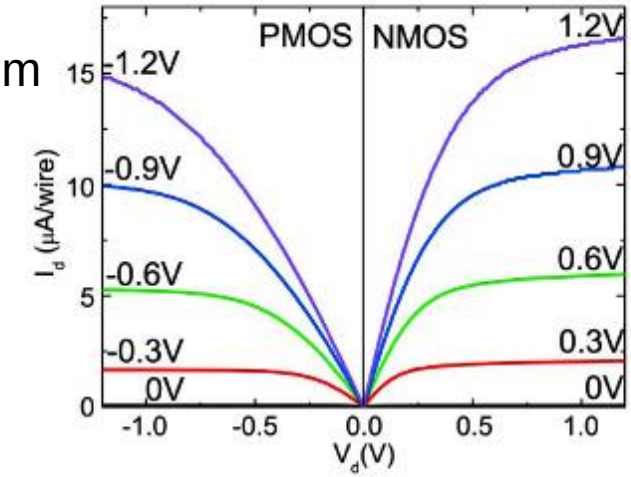

Fig. 3. Per NW I_d–V_d plot for n-FETs and p-FETs with gate overdrive voltage varying in steps of 300 mV.

Performance scales with number of wires in stack!
Surface is Ge rich
Hole accumulation at the surface and electrons in the core
Difference in scattering affects g_m

IEEE ELECTRON DEVICE LETTERS, VOL. 29, NO. 7, JULY 2008 791

Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET

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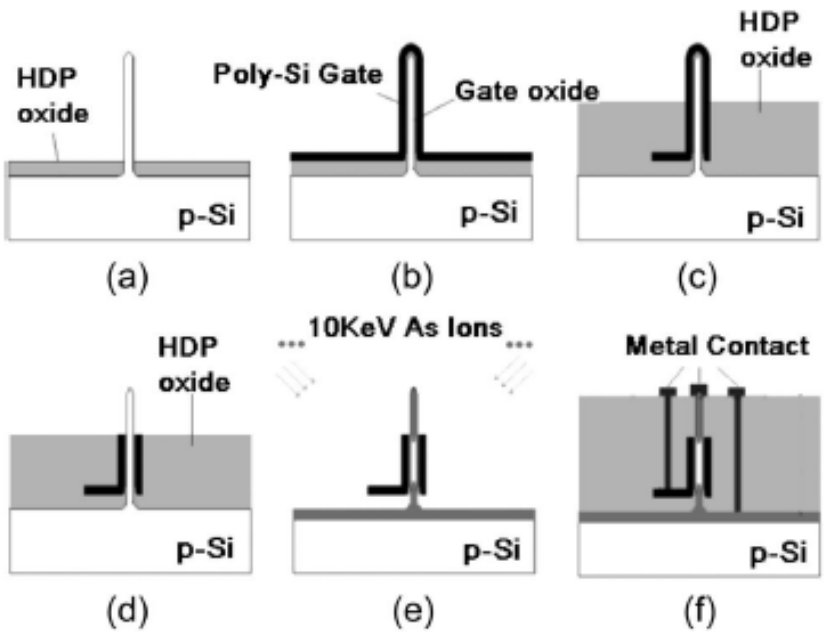

Fig. 1. Process flow for pillar and transistor formation: (a) Si pillar formed by dry etch with SiN hardmask and high-temperature oxidation trim. A spacer layer of HDP oxide was formed by deposition followed by etch back. (b) Polysilicon gate deposition. (c) Gate patterning followed by HDP Oxide deposition. (d) Removal of top polysilicon to expose the drain. (e) Implantation to form source and drain junction. (f) Metal contact formation.

-Cylindrical geometry offer better electrostatic control

- Resist pattern 160-600 nm diameter

-Oxidation to form 20 nm diameter wires

- Reduced oxidation at high curvature

- 150 nm gate length

- i-Si and implantation of S/D regions

Device characteristics

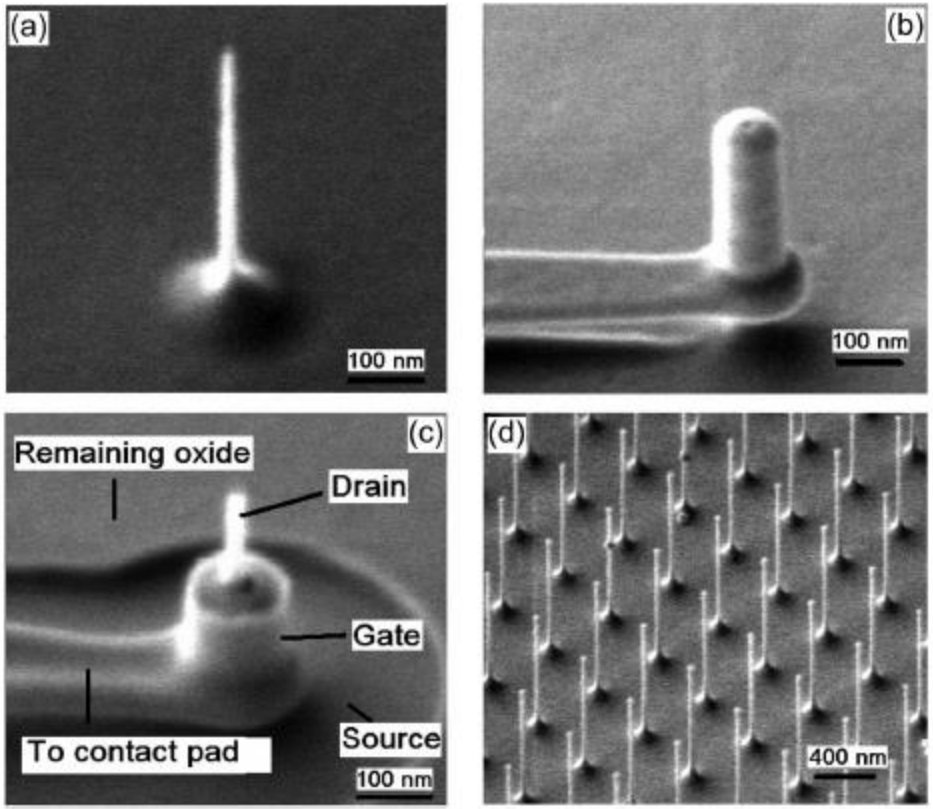

Fig. 2. SEM pictures of device fabrication: (a) Vertical nanowire with diameter ~20 nm. (b) After gate patterning by lithography but before exposing the drain (the tip of the pillar) of the transistor. (c) After the drain (pillar tip) is exposed. Metal contacts are made with such device structure. (d) Vertical nanowire arrays with pitch of 500 nm. Nanowires are 1 μm tall with a diameter of ~20 nm.

Device characteristics

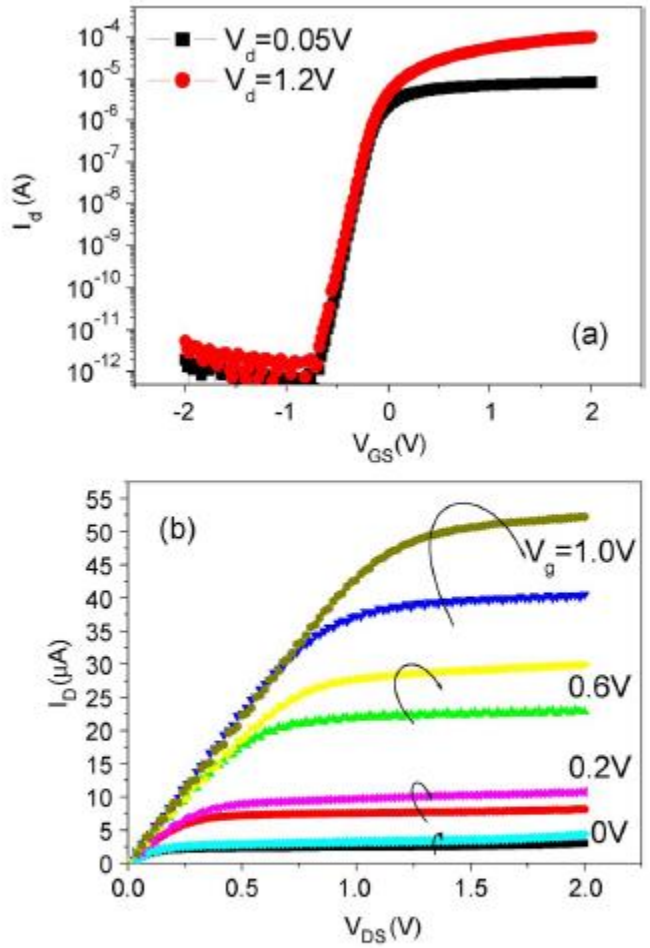

Fig. 3. Transistor performance: (a) I_d–V_g curve, the threshold voltages at $V_d = 1.2$ V and $V_d = 0.05$ V are −0.25 and −0.23 V, respectively. (b) I_d–V_d curve of the same device; each pair of curves contains I_d–V_d of the same gate voltage. The upper curve is obtained when the nanowire tip serves as the source, while the lower curve is obtained when the nanowire tip serves as the drain.

- L_g 160 nm, diameter 20 nm, t_{ox} 5 nm
- SS about 80 mV/dec
- I_{on} 1000 mA/mm
- I_{on}/I_{off} ~10^7

Device characteristics

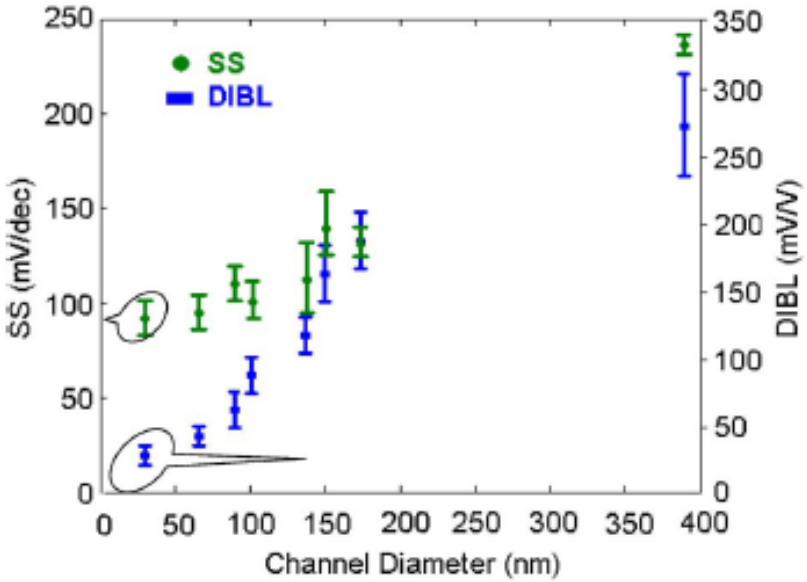

Fig. 4. Dependence of (a) DIBL and (b) SS on nanowire diameter. In total, about 30 devices were measured, and the error bar is estimated by the spread of the data. There are variations of gate lengths (up to ±20 nm) of devices with the same channel diameters due to nonuniformity of fabrication process.

-Aspect ratio of about 1 required to have optimum potential control

APPLIED PHYSICS LETTERS **92**, 052102 (2008)

Experimental evidence of ballistic transport in cylindrical gate-all-around twin silicon nanowire metal-oxide-semiconductor field-effect transistors

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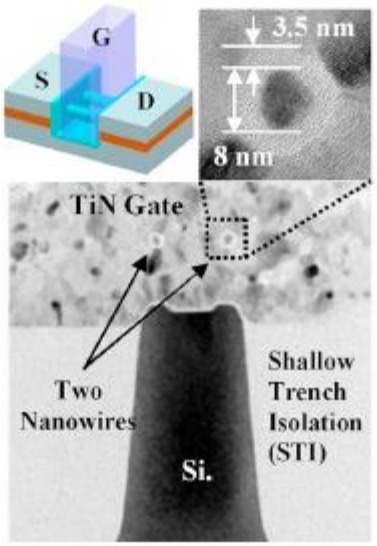

FIG. 1. (Color online) A schematic and TEM images of our CMOS based twin silicon nanowire MOSFET fabricated on Si bulk wafers.

-8 nm diameter

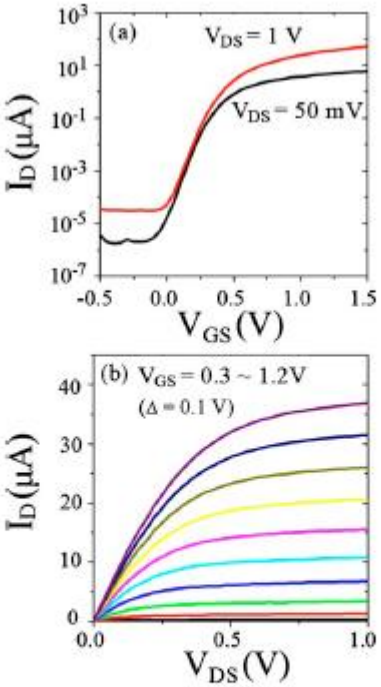

FIG. 2. (Color online) The typical *I-V* characteristics of L=22 nm TSN-WFET. (a) DIBL, SS, and the on-off current ratio from these characteristics are 26 mV/V, 75 mV/decade, and more than 10^6, respectively. (b) The values of I_{Dsat} are fitted as a function of $V_{GS}-V_T$ with the power law formula, $I_{Dsat} \propto (V_{GS}-V_T)^{\alpha}$. The fitted power α is ~1.44, suggesting that transport is not dominated by the drift-diffusion and velocity saturation.

Nanoelectronics: Si Nanowires

Overshoot in transconductance

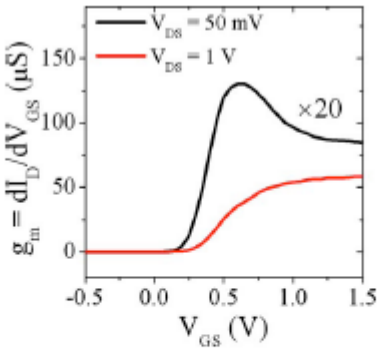

FIG. 3. (Color online) Measured g_m from the L=22 nm device is plotted. The overshoot of g_m in the low-bias regime and constant g_m at higher V_{GS} are clearly observed. The former can be interpreted as the off-equilibrium phenomenon due to the dramatic increase of velocity since g_m is a good velocity indicator of FETs, and the latter is attributed to the reduced transverse electric field due to the GAA structure and thin body.

$$I_D = C_{OX}\alpha v_{inj} W(V_{GS} - V_T)\left(\frac{1 - e^{-eV_{DS}/k_B\theta}}{1 + e^{-eV_{DS}/k_B\theta}}\right)$$

$$g_m = \frac{dI_D}{dV_{GS}} = C_{OX}W\left[\alpha v_{inj} + \frac{d\alpha}{V_{GS}} v_{inj}(V_{GS} - V_T) + \alpha\frac{dv_{inj}}{V_{GS}}(V_{GS} - V_T)\right]\left(\frac{1 - e^{-eV_{DS}/k_B\theta}}{1 + e^{-eV_{DS}/k_B\theta}}\right). \quad (1)$$

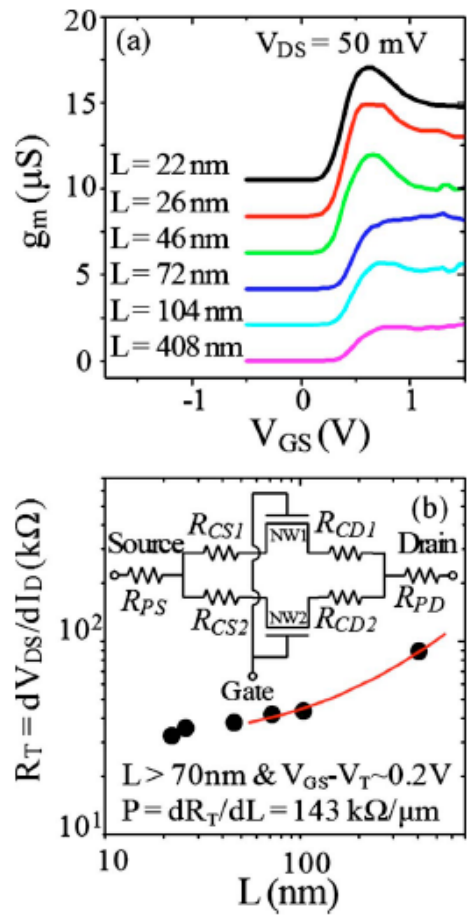

FIG. 4. (Color online) (a) Measured g_m-V_{GS} curves taken from six devices with L values ranging from 22 to 408 nm. The overshoot is observed when $L \leq 46$ nm. (b) We obtain 1D resistivity ρ=143 kΩ/μm from the plot, and get $l_0 \approx 45$ nm. The estimated l_0 almost matches the L value below where the g_m overshoot is observed.

1. SiGe / Si Growth
   & shallow trench isolation (STI).
2. Hard mask SiN trimming.
3. Oxide fill in STI & CMP
4. Damascene gate stack deposition
5. 1ST Damascene gate etch.
6. 2nd Damascene gate etch.
   (Hard mask SiN & Si)
7. Field oxide recess.
8. SiGe removal & H_2 anneal.
9. Gox and Gate material deposition.

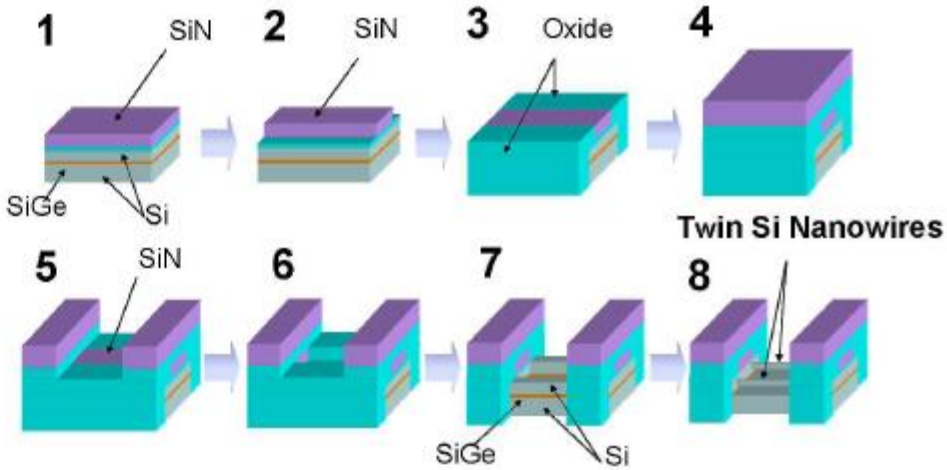

Fig. 1. Process flow sequence and brief schematic diagram for twin Si nanowire FET(TSNWFET) fabrication

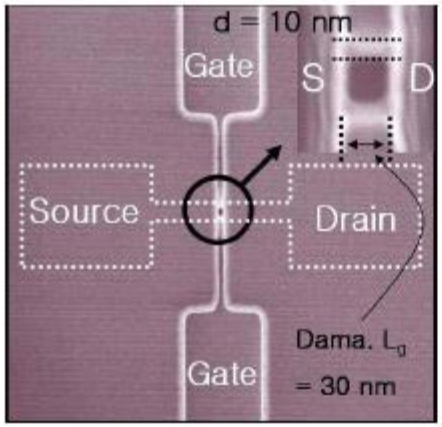

Fig. 2. Top view SEM image of nanowire after SiGe removal. Nanowire d=10nm and damascene-gate Lg=30nm.

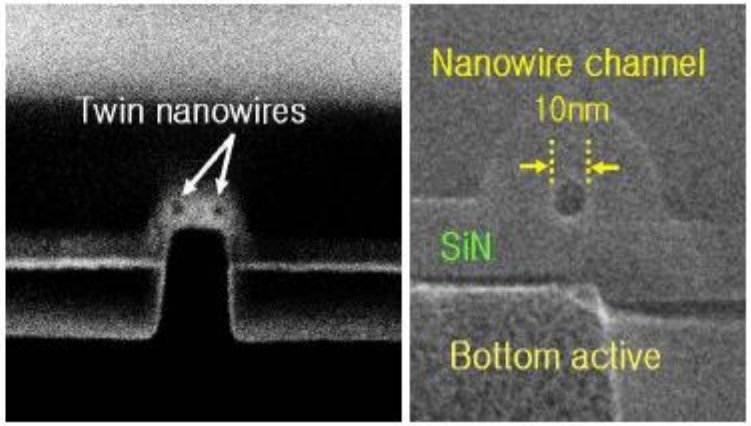

Fig. 3. Cross-sectional SEM image of nanowire decorated by SiN. Nanowire diameter is about 10nm.