Contents: III/V Nanowires

Vertical InAs NW transistors:
C Thelander et al IEEE Electron Dev. Lett. 29, 2008 p 206 ”Vertical Enhancement-Mode ...”

Lateral InGaAsAs NW transistors :
J Gu et al IEEE IEDM Tech Digest. 2012, p. 633 ”20-80 nm channel length InGaAs .... ”

Vertical InGaAs NW transitors:
K Tomioka et al Nature. 488, 2012 p. 189 ”A III-V nanowire channel on silicon ... ”

Nanowire CMOS:
A Dey et al Nano Lett 12, 2012, 5593 ”Single InAs/GaSb ...”

Scaling in quantum capacitance limit:
J Knoch et al IEEE Electron Dev. Lett. 29, 2008 p 372 ”Outperforming the Conventional...”

Nanowire FETs: Why InAs?

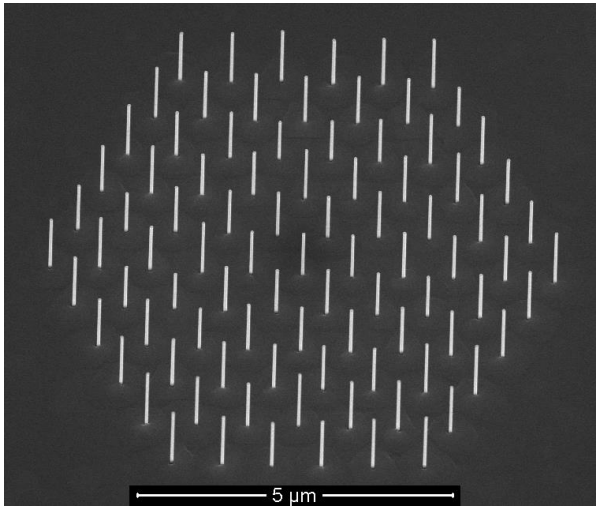
Surface pinning in conduction band and good ohmic contacts!

Material property	**Si**	**GaAs**	**$In_{0.53}Ga_{0.47}As$**	**InAs**	**InSb**
Electron mobility ($cm^2V^{-1}s^{-1}$)	1500	8500	14000	**33000**	**78000**
Saturation velocity (cms^{-1})	$1x10^7$	$1.2x10^7$	$8x10^6$	**$3.5x10^7$**	**$>5x10^7$**
Band gap (eV)	1.1	1.4	0.75	**0.36**	**0.17**
Effective mass	0.19	0.067	0.041	0.023	0.014

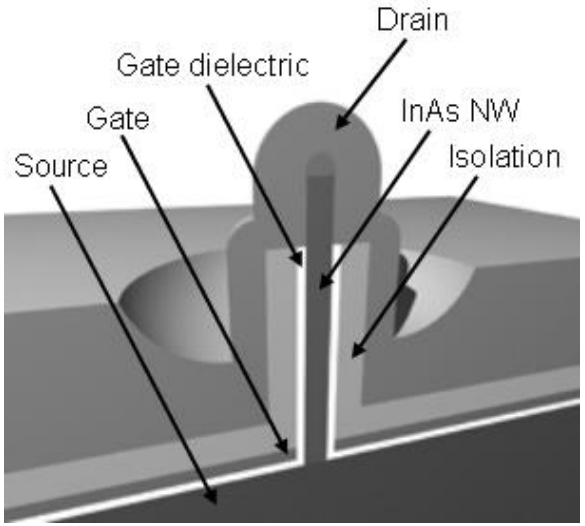
Ashley et al IEDM 97

Wrapped Insulator-Gate Nanowire Field-Effect Transistor (WIGFETs)

SEM image of a matrix of CBE grown nanowires



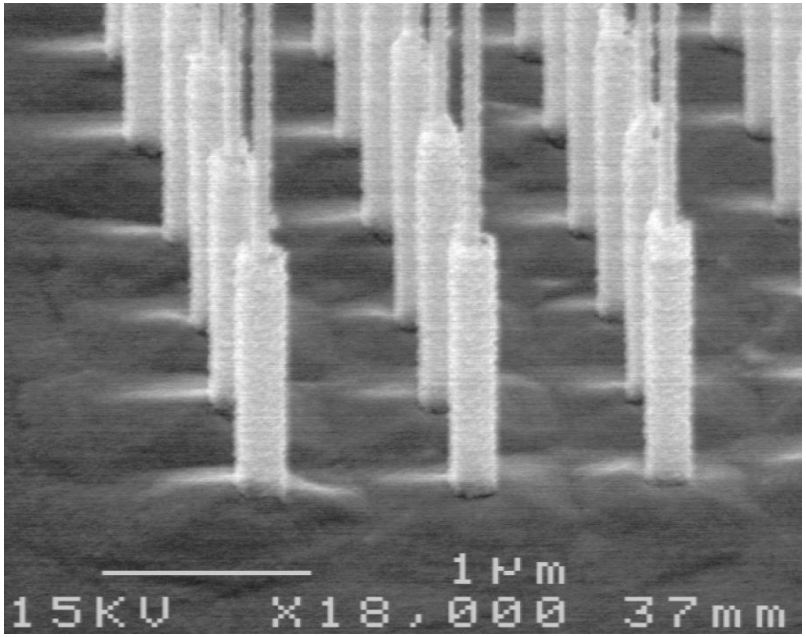
Layout of a nanowire FET



- Surround gate gives strong gate coupling
- InAs high mobility channel
- Can include heterostructures in the FET
- Easy scaling to high current levels
- 3D architecture

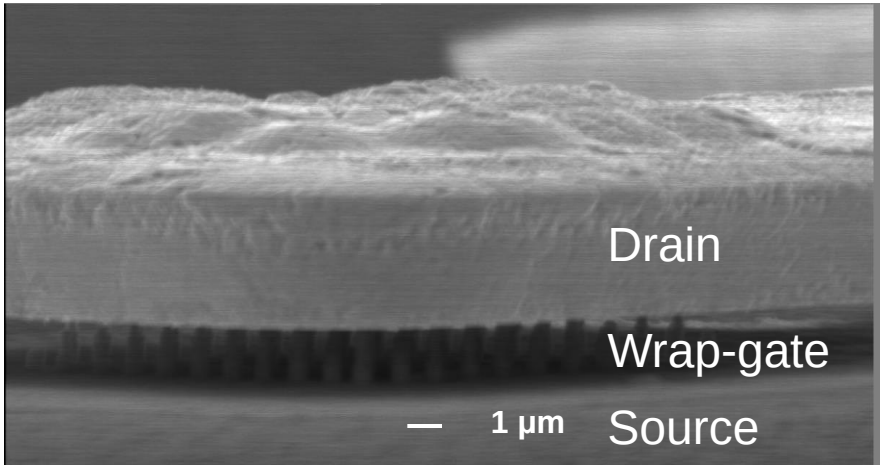
SEM Images of Wrap-Gate FETs

Wrap-gates



80 nm diameter
3 µm wire length
0.8 µm gate length
Not intentionally doped n~$2x10^{17}$ cm^{-3}

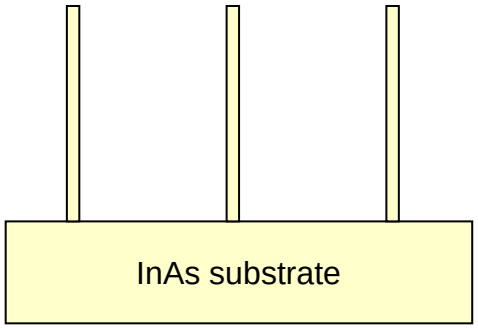
Nanowire Transistor



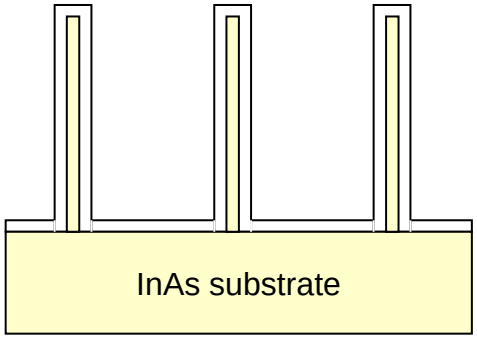
Bryllert et al DRC 2005
Wernersson et al IEDM 2005
Bryllert et al EDL 2006

Processing Flow Short Gate Lengths

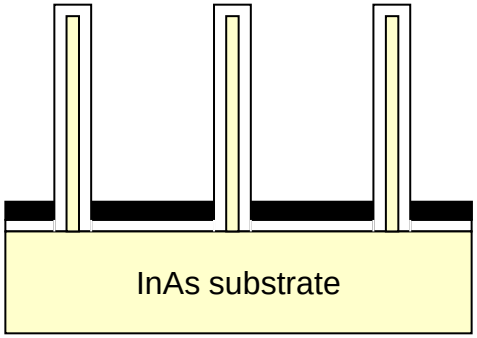
1. Nanowire growth



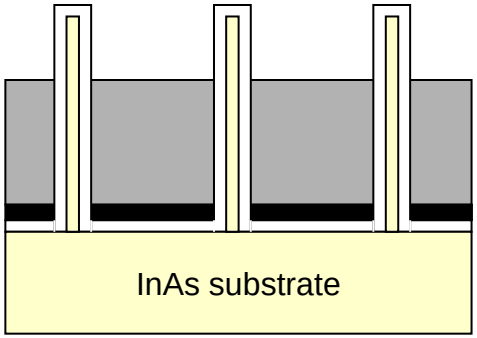
2. Deposition of SiN_x gate dielectric layer



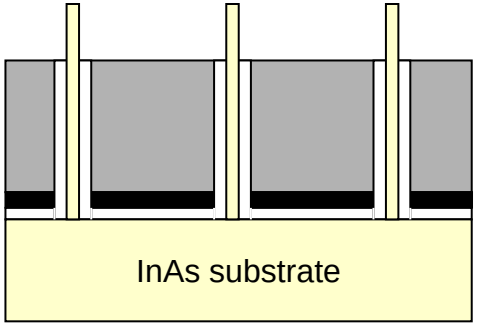
3. Evaporation of gate



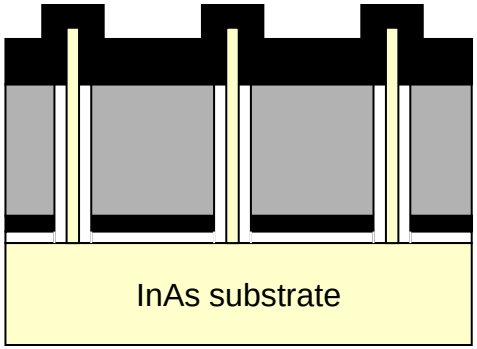
4. Spin-coating with BCB



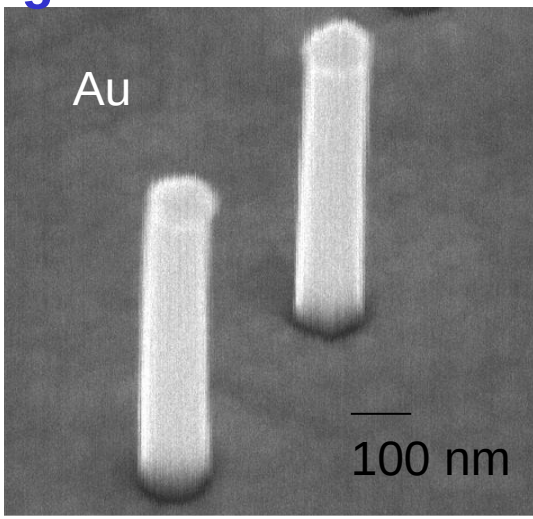
5. Wet etching of drain contacts



6. Evaporation of drain contact



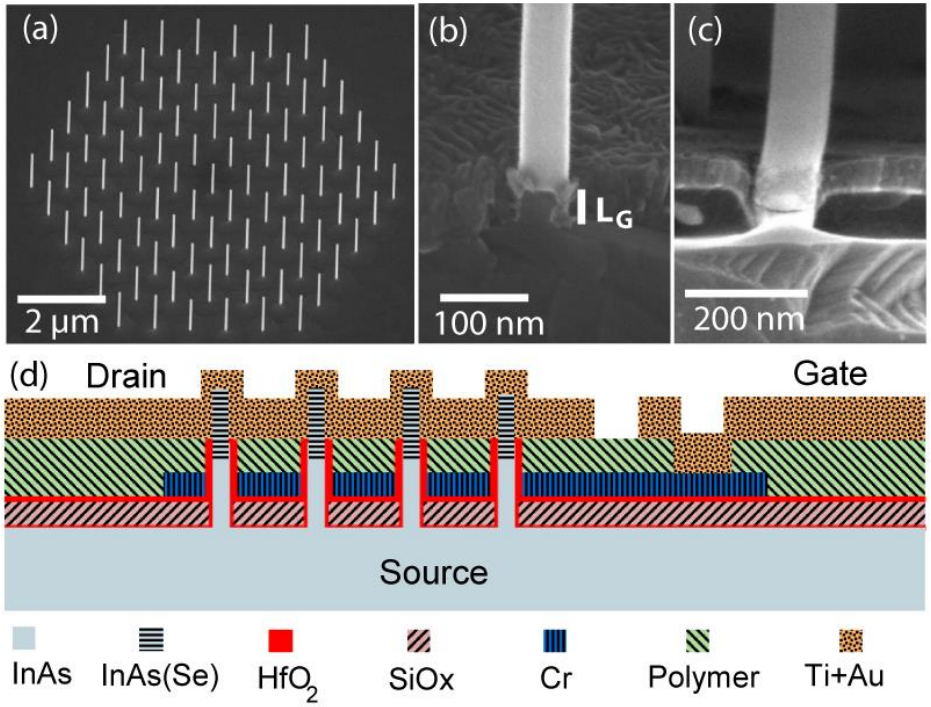
Nanowires after gate formation



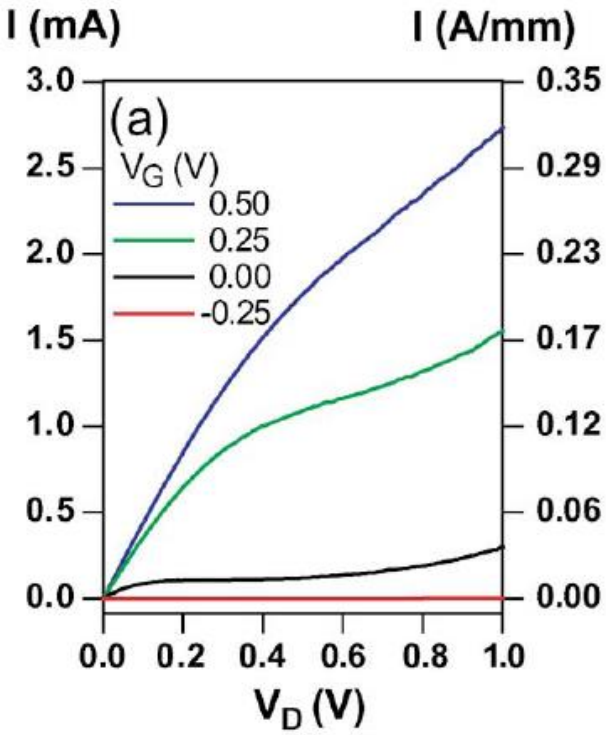
40 nm SiN_x thickness

Wernersson et al SSDM 2006

50 nm L_g Transistors with Elevation Layer



Good Output Characteristics

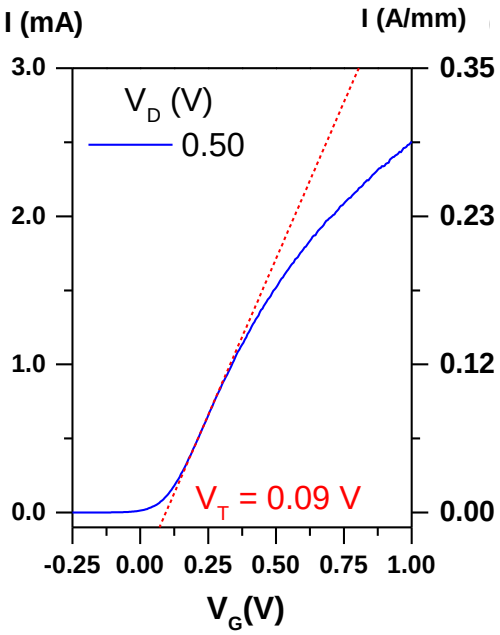


10 nm HfO_2, 91 Nanowires in matrix
Processed by QuMat

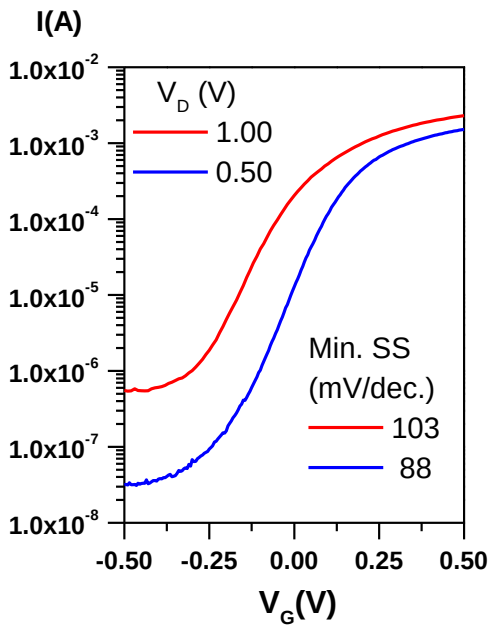
Thelander et al EDL 2008

50 nm Lg Transistors with Elevation Layer II

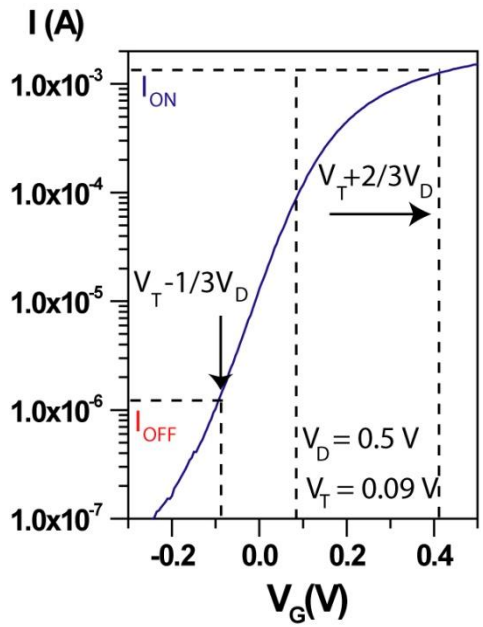
Enhancement mode operation



SS 80mV/dec.
DIBL 60mV/V below 0.7 V



High I_{on}/I_{off} ratio for V_d=0.5V (>1000)

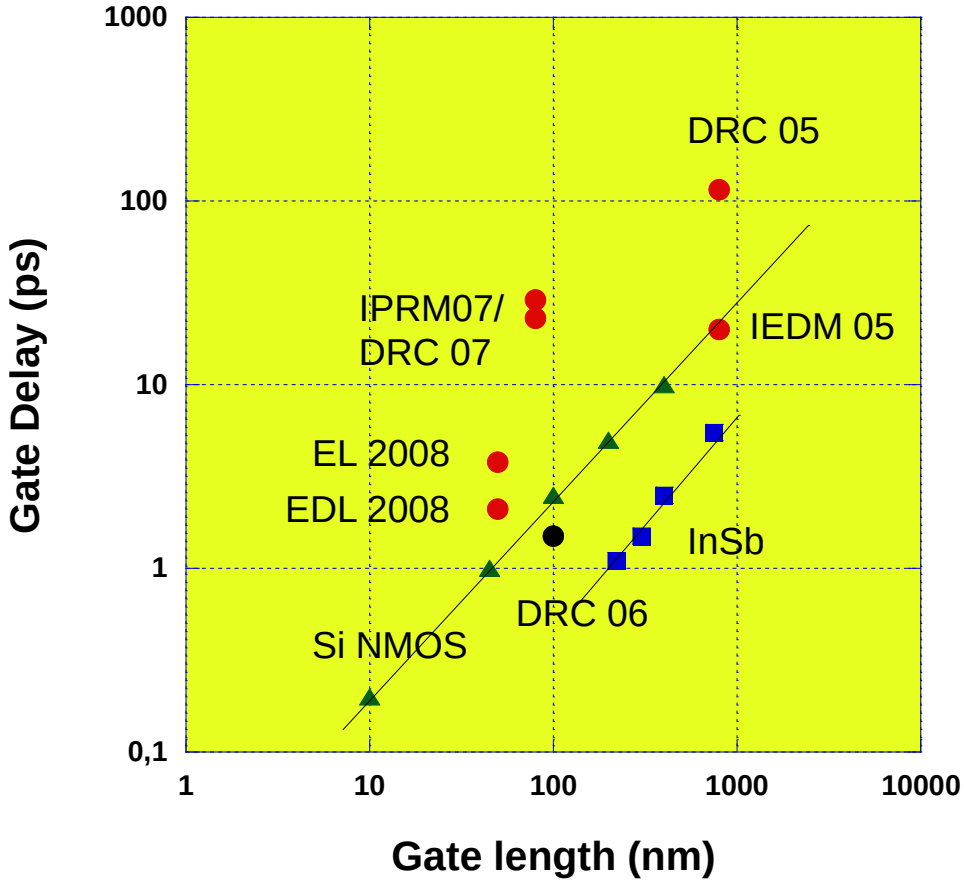


V_D (V)	Average V_T (V)	Average g_m (S/mm)	Max g_m (S/mm)	Average *SS* (mV/dec.)	Min. *SS* (mV/dec.)
0.50	0.05 ± 0.05	0.44 ± 0.06	0.52	100 ± 8	88
1.00	0.00 ± 0.04	0.58 ± 0.12	0.80	150 ± 43	103

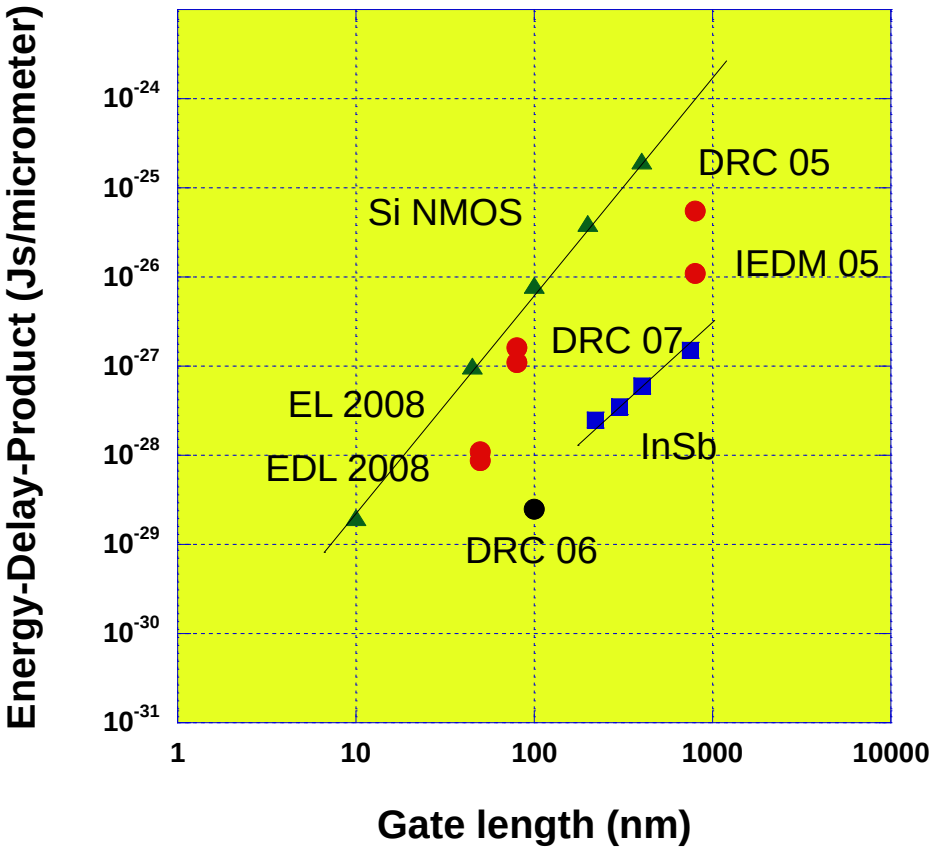
+ High g_m!
+ Good V_t control!
+ No gate leakage!
+ Low hysteresis (20mV)!

Benchmarking: MOS Devices

Gate Delay τ=(CV/I)

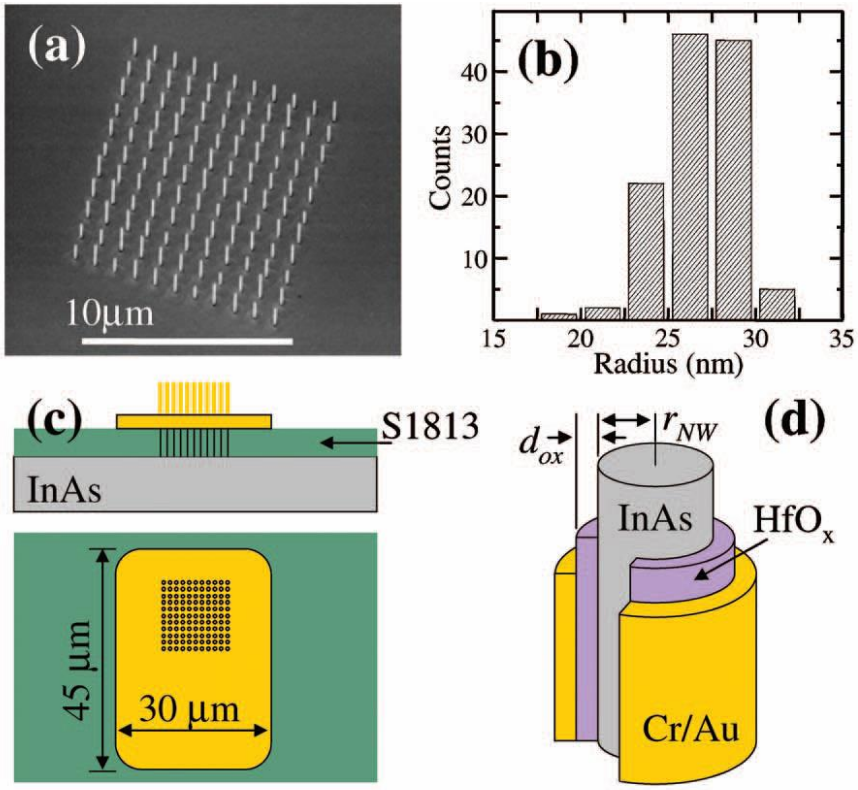


Energy Delay Product EDP=τ*CV^2



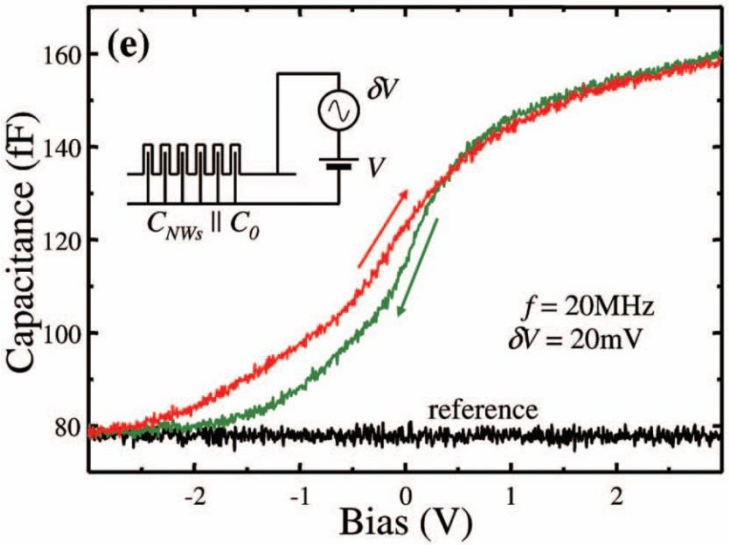
Nanowire Capacitors

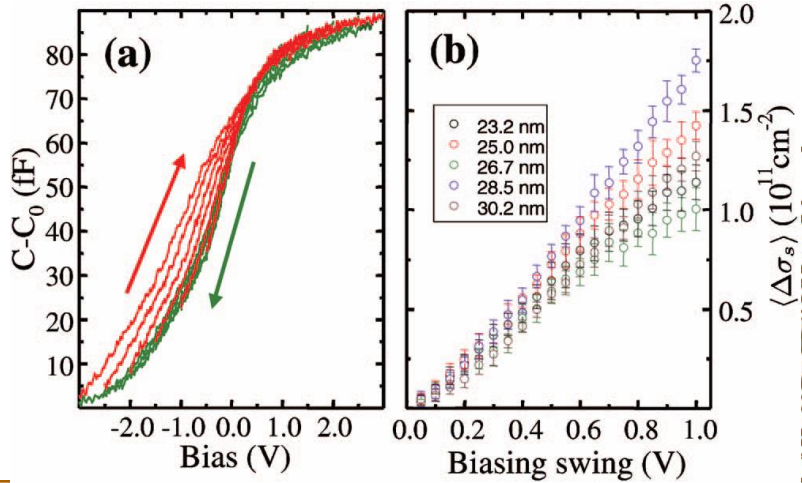
Device Structure



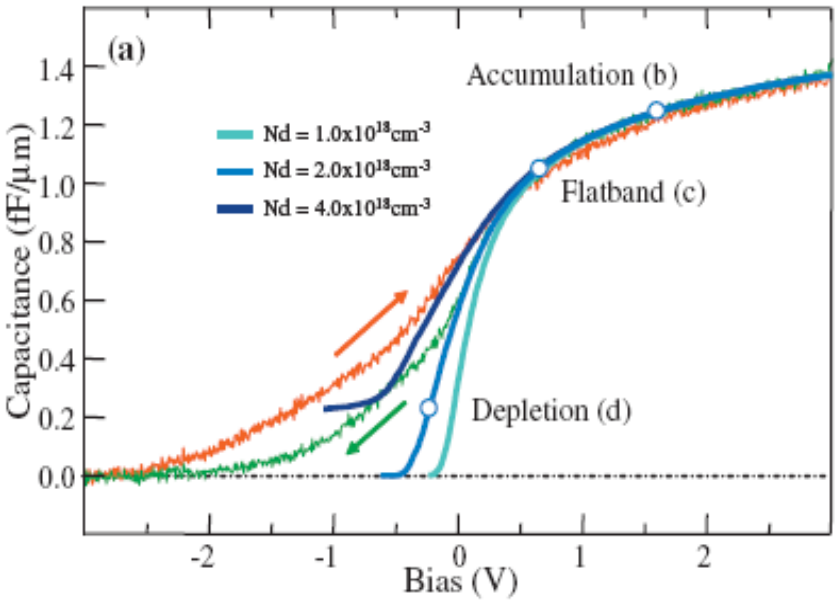
Roddaro et al APL 92, 253509 (2008)

Measured Data

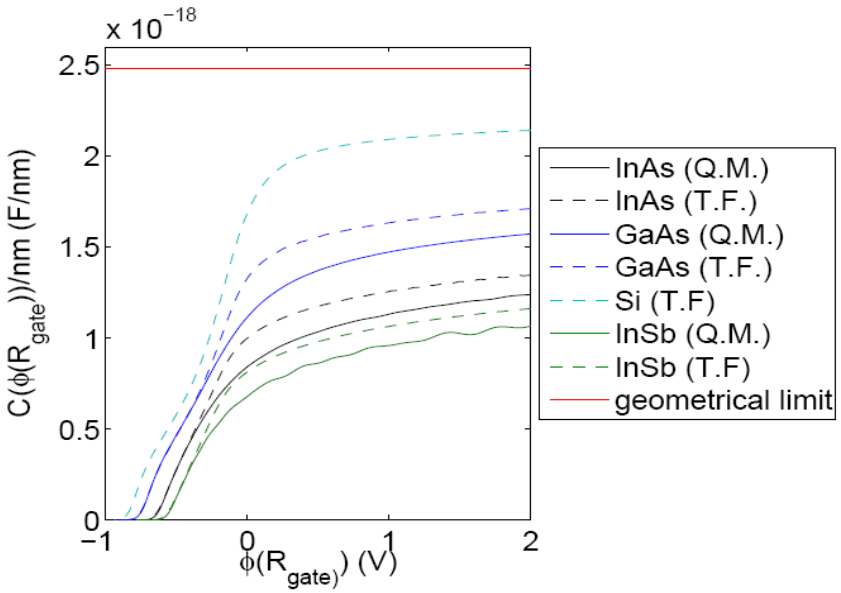


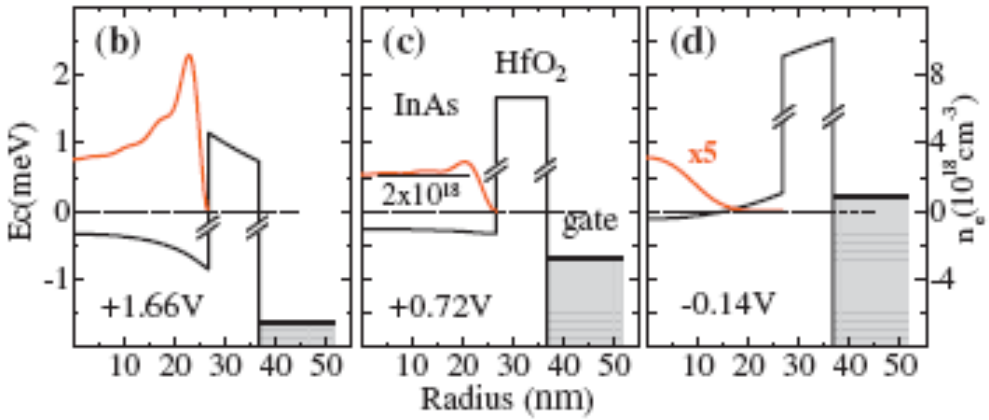


InAs NW MOS Capacitors



Carrier concentration $2x10^{18}$ cm^{-3}
Quantum capacitance at ø 50 nm





Karlström et al Nanotechnology, 253509 2008

20-80nm Channel Length InGaAs Gate-all-around Nanowire MOSFETs with EOT=1.2nm and Lowest SS=63mV/dec

J. J. Gu,[1] X. W. Wang,[2] H. Wu,[1] J. Shao,[3] A. T. Neal,[1] M. J. Manfra,[3] R. G. Gordon,[2] and P. D. Ye [1]

[1] *School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47906, U.S.A.*
[2] *Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, U.S.A.*
[3] *Department of Physics, Purdue University, West Lafayette, IN, 47906, U.S.A.*
Tel: 1-765-494-7611, Fax: 1-765-496-7443, Email: yep@purdue.edu, jjgu@purdue.edu

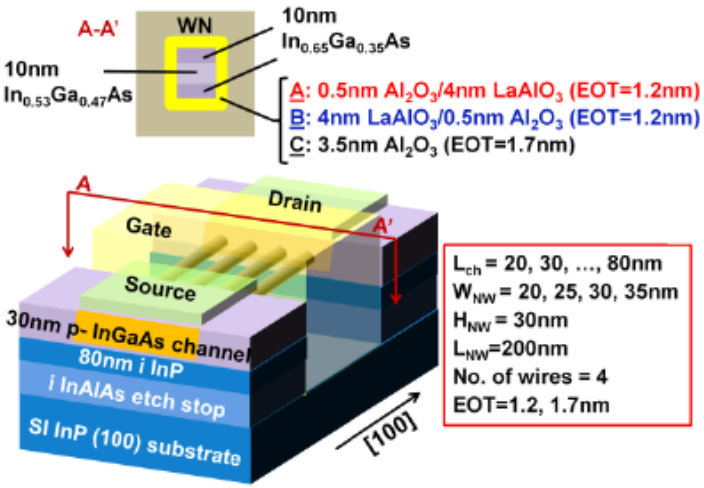


Fig. 1 Device structure, dimension and key parameters of InGaAs GAA MOSFETs.

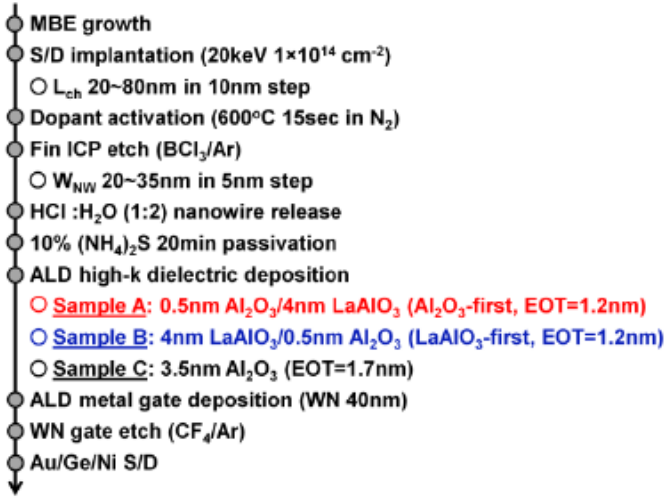


Fig. 2 Fabrication process flow and device splits of InGaAs GAA MOSFETs.

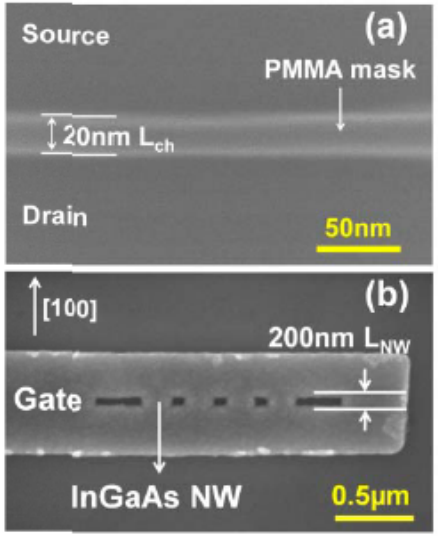


Fig. 3 SEM images of (a) PMMA mask defining 20nm L_{ch} (b) an InGaAs GAA FET with 4 wires.

Study on scalilng of gate length

Gate length 20-80 nm

Nanoelectronics: III-V Nanowires

Device Performance

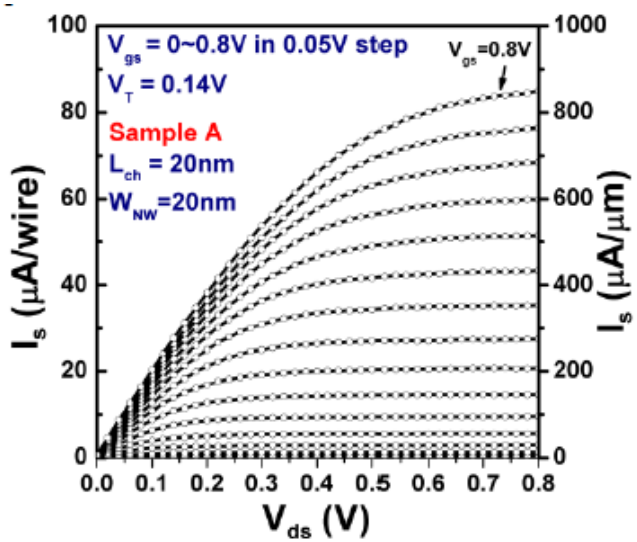


Fig. 4 Output characteristics of a 20nm L_{ch} InGaAs GAA MOSFET with $Al_2O_3/LaAlO_3$ gate dielectric (Sample A, EOT=1.2nm) and W_{NW}=20nm. I_s is used due to relatively large junction leakage current in I_d.

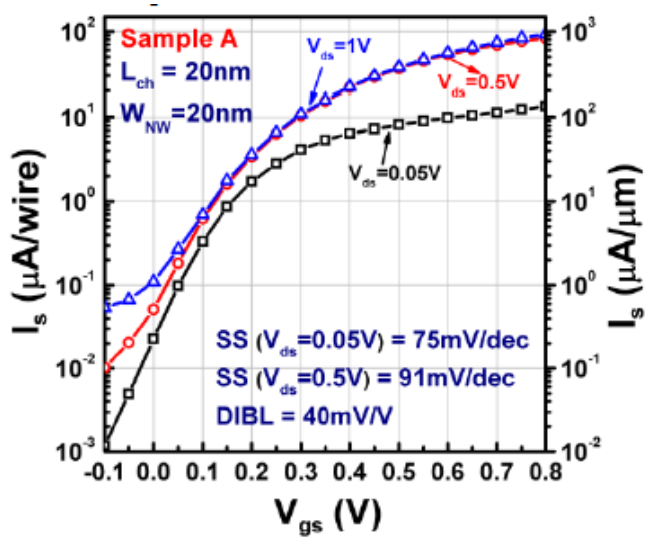


Fig. 5 Transfer characteristics of the same device shown in Fig. 4. W_G =100nm for W_{NW}=20nm normalized to perimeter.

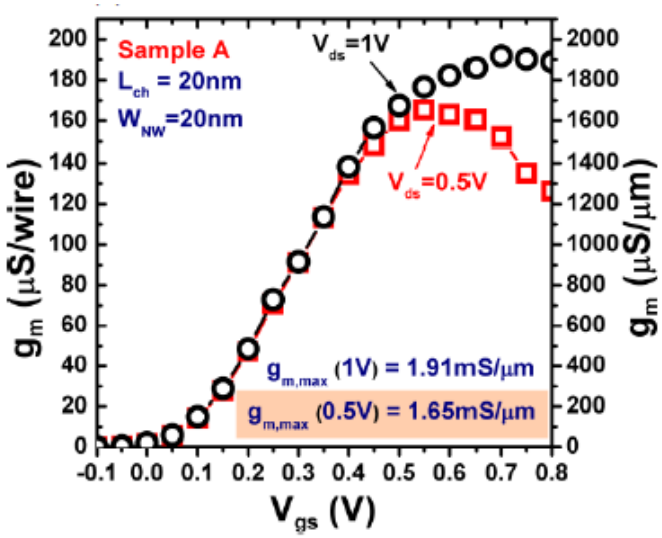


Fig. 6 Transconductance of the same device shown in Fig. 4.

Nanowire diameter 20 nm

Transconductance of 1.7 mS/μm at Vd=0.5V

Drive current of 0.63 mA/μm at Vd=0.5V

SS 75 mV/dec.

Device Performance II

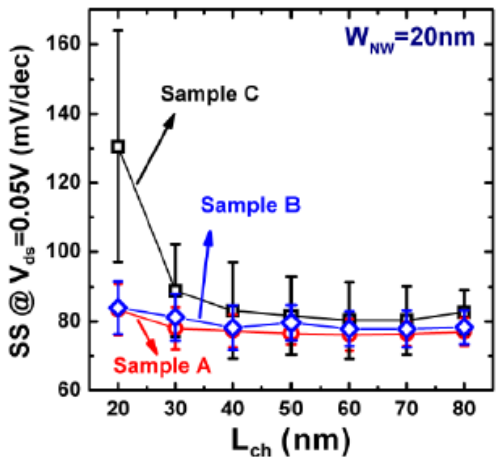


Fig. 19 SS scaling metrics for samples A, B, and C with W_{NW}=20nm.

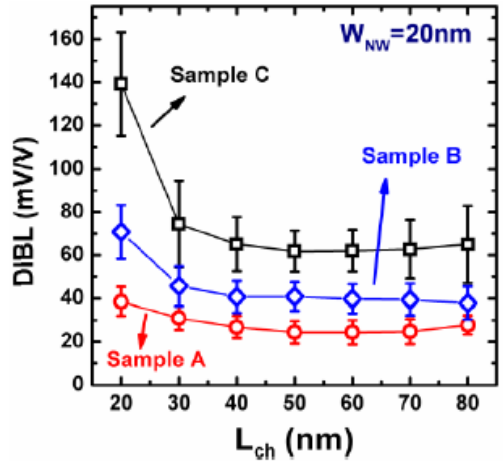


Fig. 20 DIBL scaling metrics for sample A, B, and C with W_{NW}=20nm.

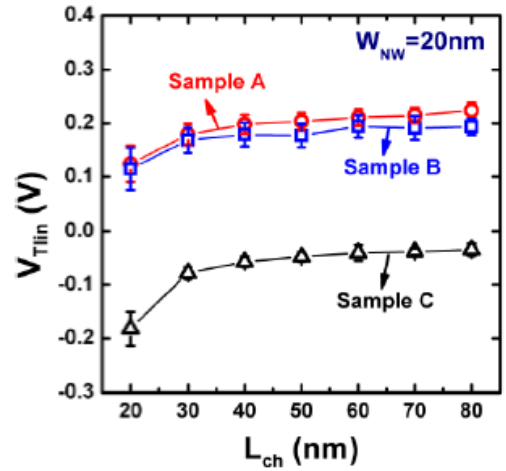


Fig. 21 V_T scaling metrics for sample A, B, and C with W_{NW}=20nm.

Table 1: Performance benchmark of typical non-planar and ETB InGaAs MOSFETs

	This work**	Ref. [1]	Ref. [4]	Ref. [5]	Ref. [6]	Ref. [7]	Ref. [8]
$In_xGa_{1-x}As$ (x)	0.65	0.53	0.7	0.7	1	0.7	1
Structure	GAA	GAA	Tri-gate	GAA	GAA	FinFET	ETB
Fabrication	Top-down	Top-down	Top-down	Bottom-up	Bottom-up	Top-down	Top-down
$L_{ch,min}$ (nm)	20	50	60	200	100	130	55
$W_{NW(Fin),min}$ (nm)	20	30	30	90	15	220	-
EOT (nm)	1.2	4.5	1.2	1.8*	1.1*	4.5*	3.5
SS [V_{ds}=0.5V] (mV/dec)	88	245	94*	98	140	-	-
SS [V_{ds}=0.05V] (mV/dec)	63	145	66	90*	-	230*	105
DIBL (mV/V)	7	210	60*	170*	60	135	84
$g_{m,max}$ (mS/μm) [V_{ds}=0.5V]	1.74	0.45	-	-	1.23	-	-

*Extracted/estimated from literature
**Reported values are best from all measured devices

Excellent scaling
for SS DIBL, and Vt

LETTER

doi:10.1038/nature11293

A III–V nanowire channel on silicon for high-performance vertical transistors

Katsuhiro Tomioka[1,2], Masatoshi Yoshimura[1] & Takashi Fukui[1]

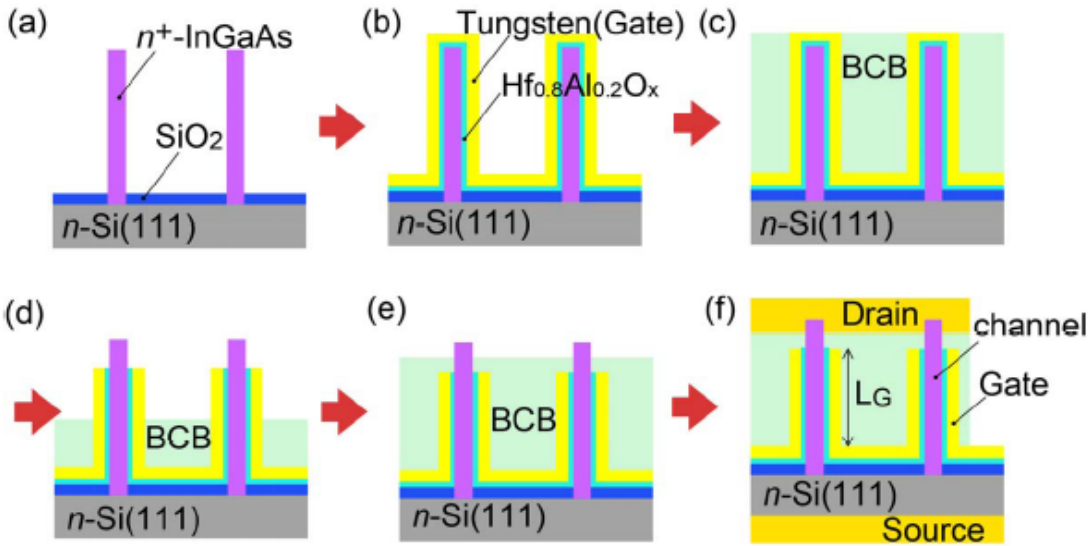
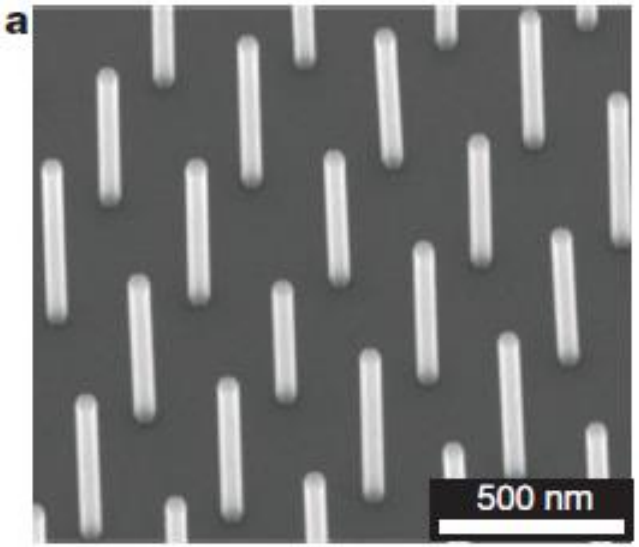
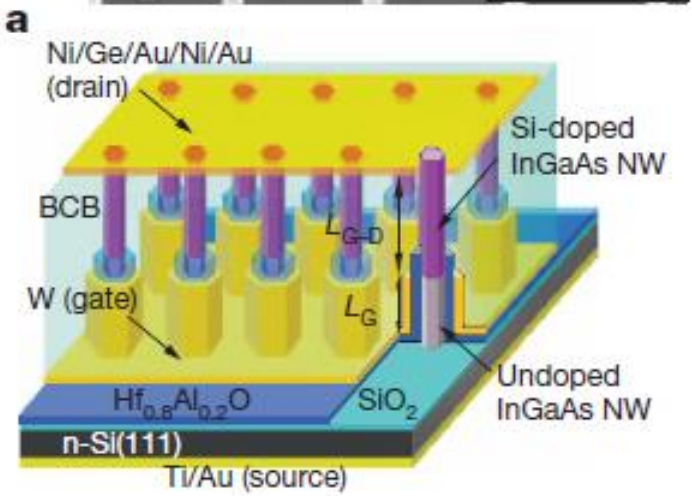


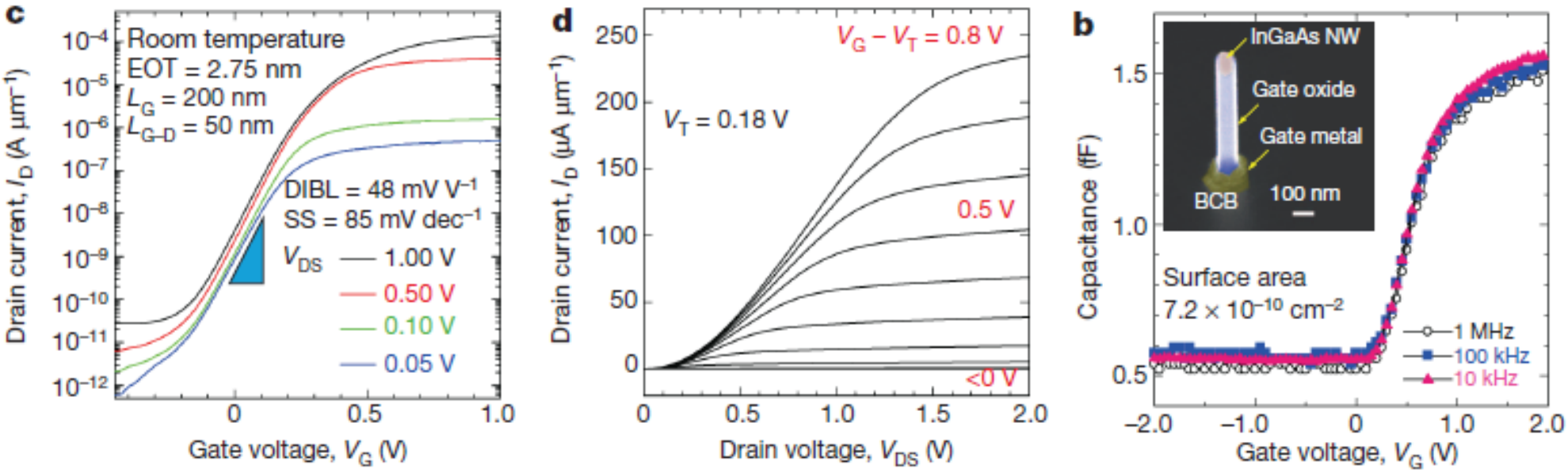
Figure 3: Device fabrication processes: (a) InGaAs NW growth. (b) Atomic layer deposition of $Hf_{0.8}Al_{0.2}O_x$ and sputtering of W-gate metal. (c) Spin-coating of BCB polymer. (d) RIE of BCB, gate oxide and W metal. (e) Spin-coating of BCB and RIE etch back for electrical separation layer formation. (f) Drain and source metal evaporation.





Nanoelectronics: III-V Nanowires

Device Performance



Gate length 200 nm

Nanowire diameter 60 nm

10 nanowires in the array

Transconductance of 280 µS/µm at Vd=1V

SS 98 mV/dec.

Device Performance

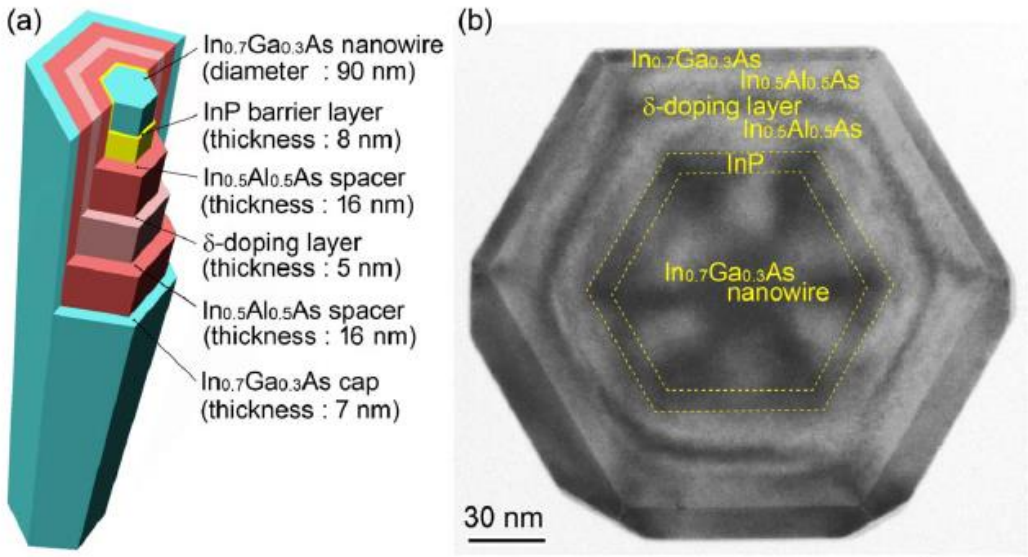
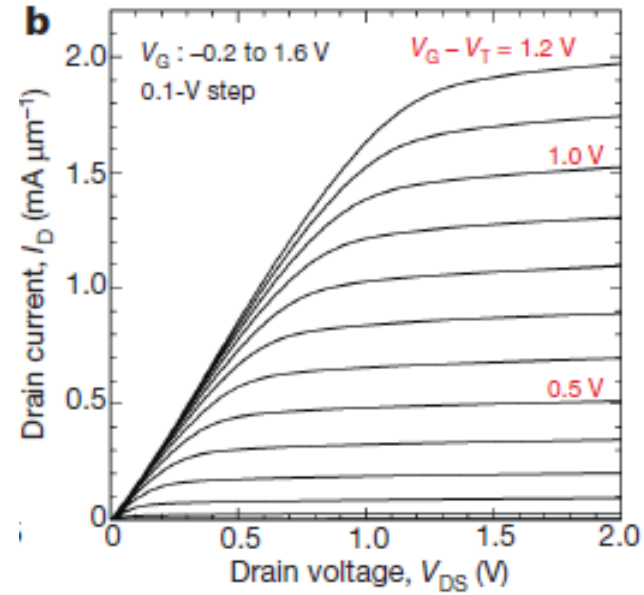
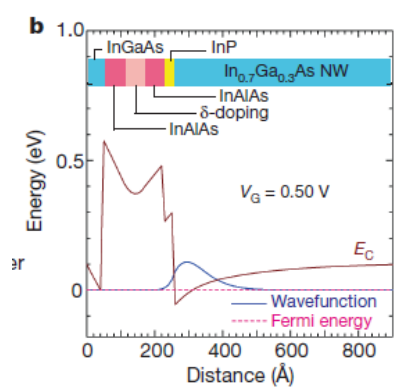
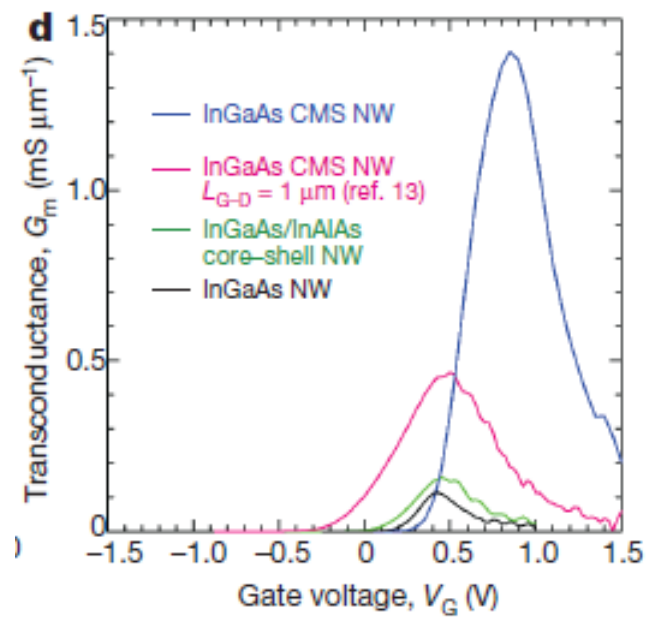


Figure 9: (a) Illustration of InGaAs/InP/InAlAs/δ-dope InAlAs/InAlAs/InGaAs core-multishell NW. (b) Cross-section TEM image of the growth results of Fig. 9(a). The InGaAs NW is 90 nm in diameter.







Gate length 200 nm

Nanowire diameter 90 nm

10 nanowires in the array

g_m=1.42 mS/μm at V_d=0.5 V

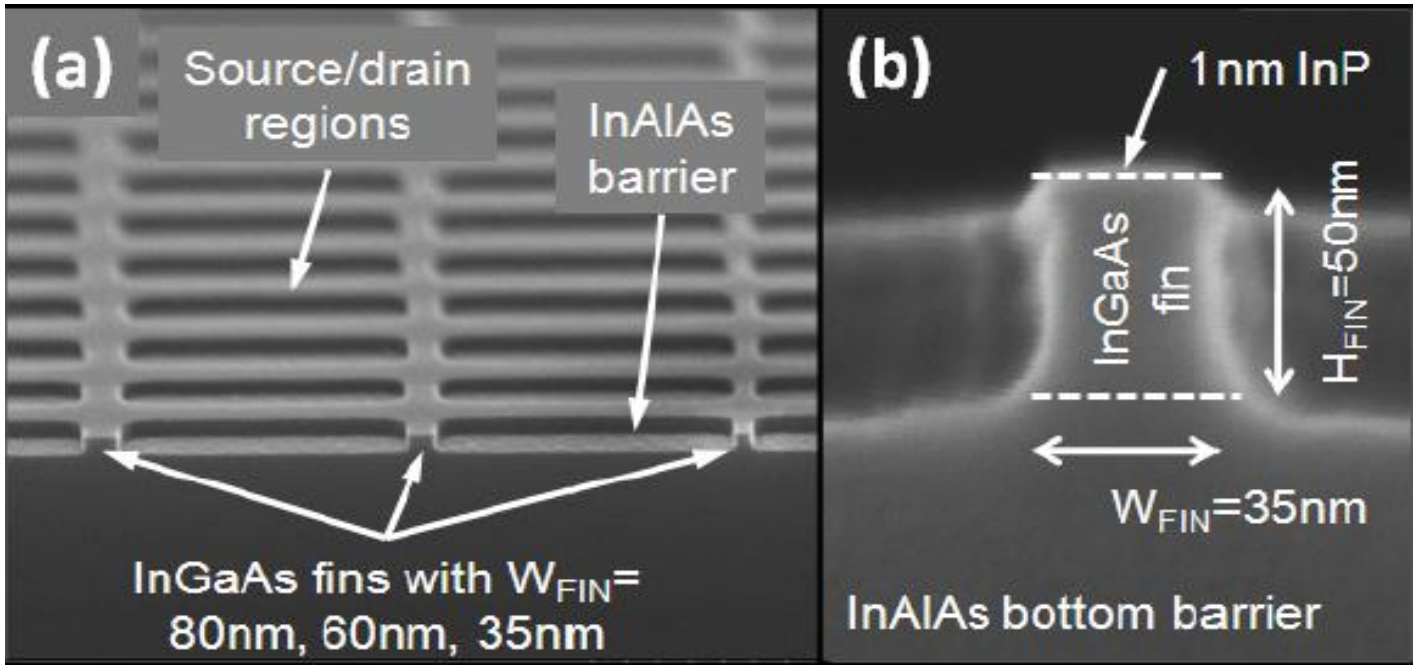
SS 75 mV/dec.

Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Logic Applications

M. Radosavljevic, G. Dewey, J. M. Fastenau*, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu*, D. Lubyshev*, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, and Robert Chau

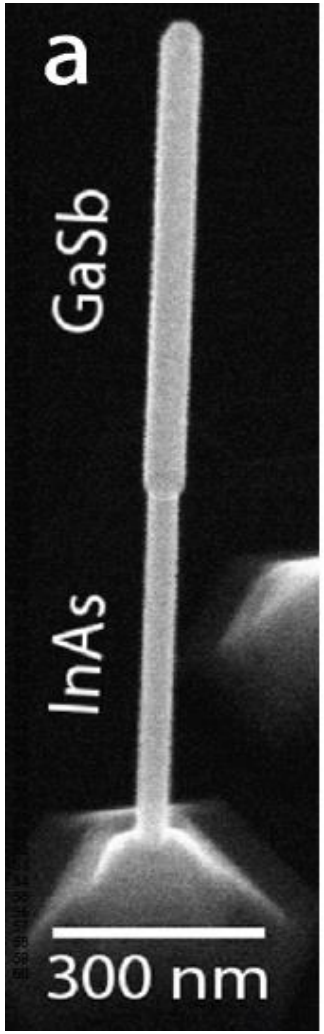
Intel Corporation, Technology and Manufacturing Group, Hillsboro, OR 97124, USA

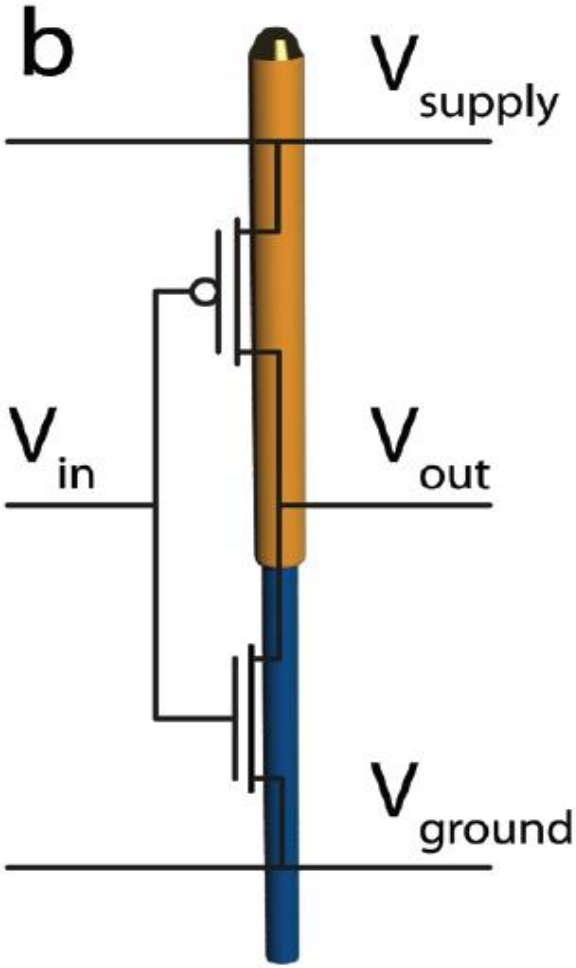
* IQE Inc, Bethlehem, PA 18015, USA

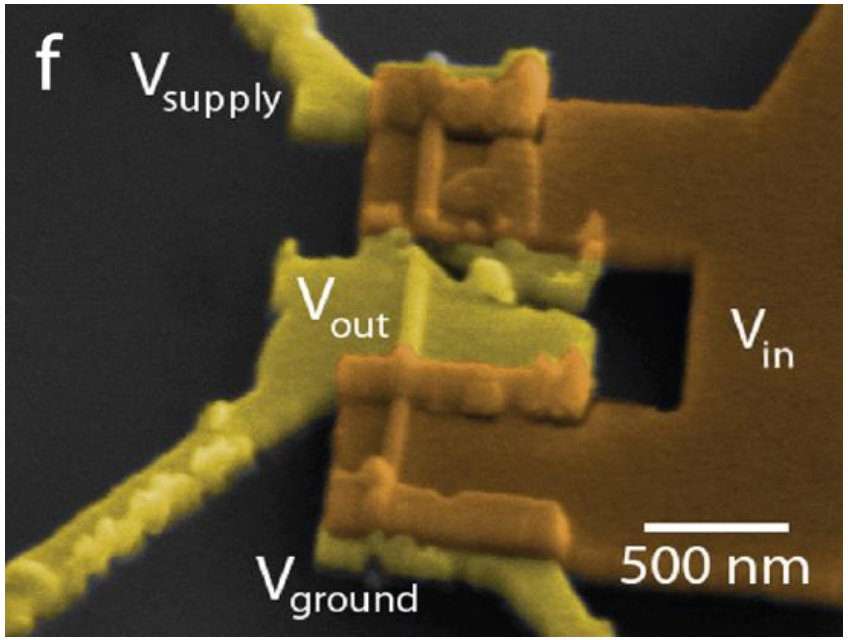


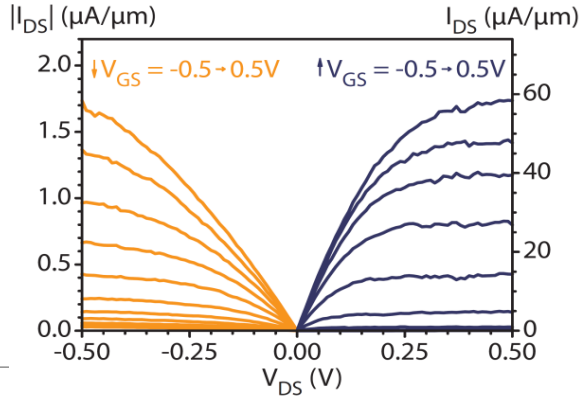
Intel IEDM 2010:

Nanowire Inverters

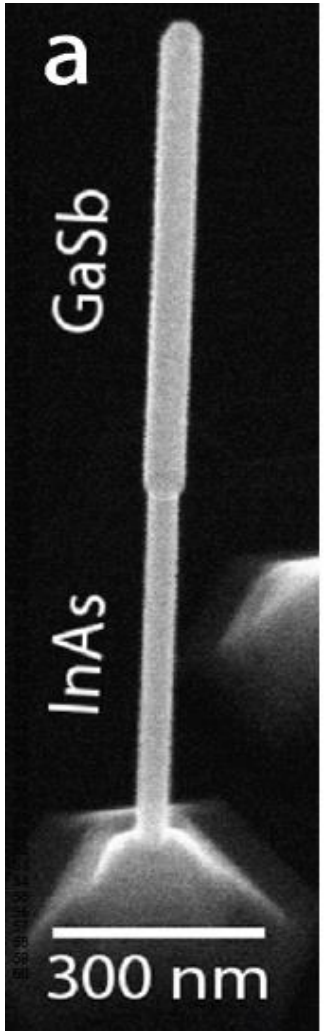


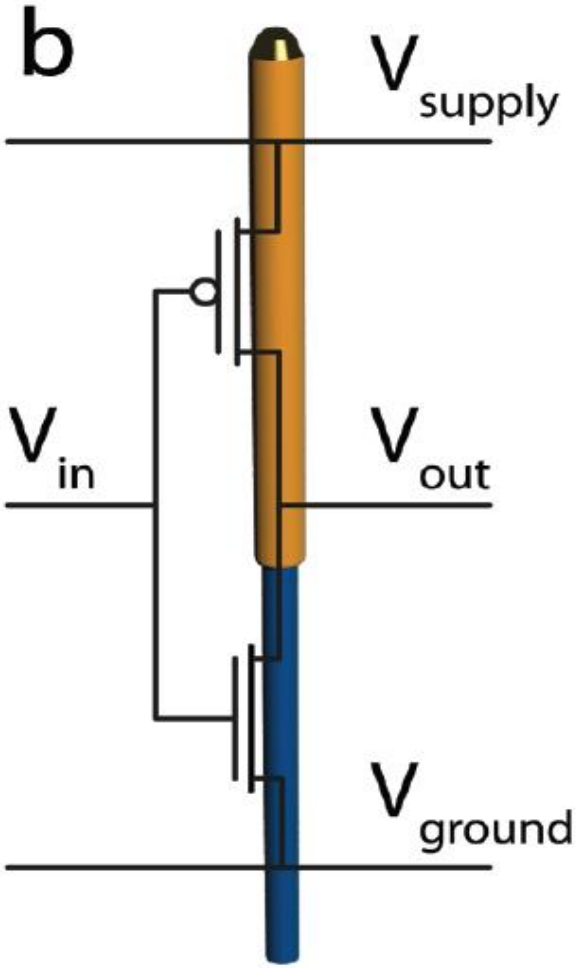


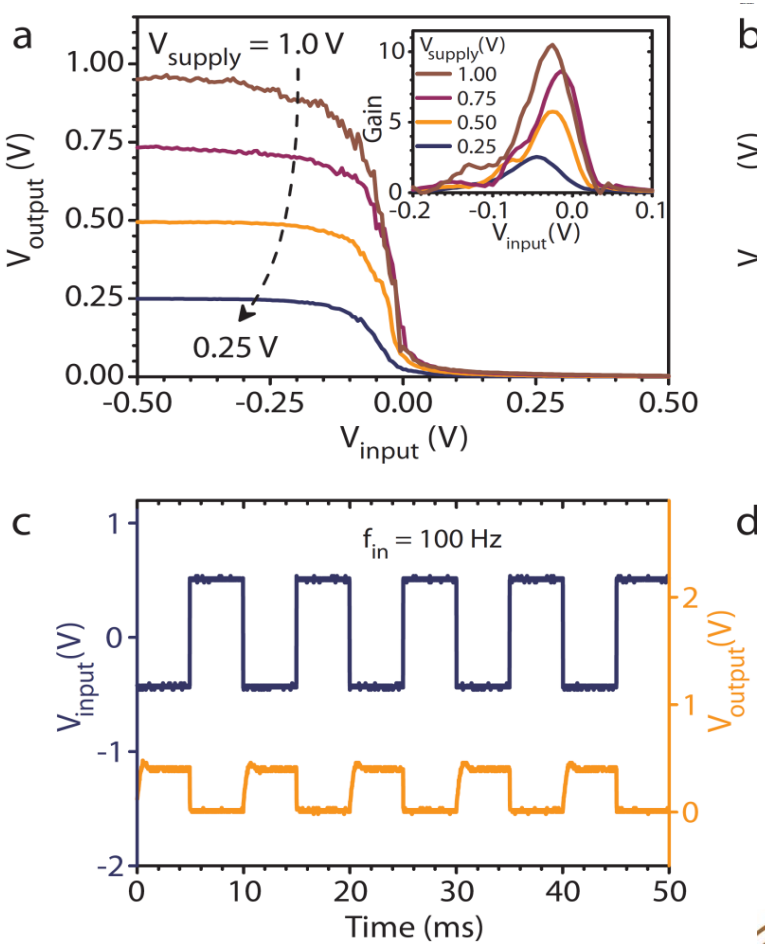




Nanowire Inverters

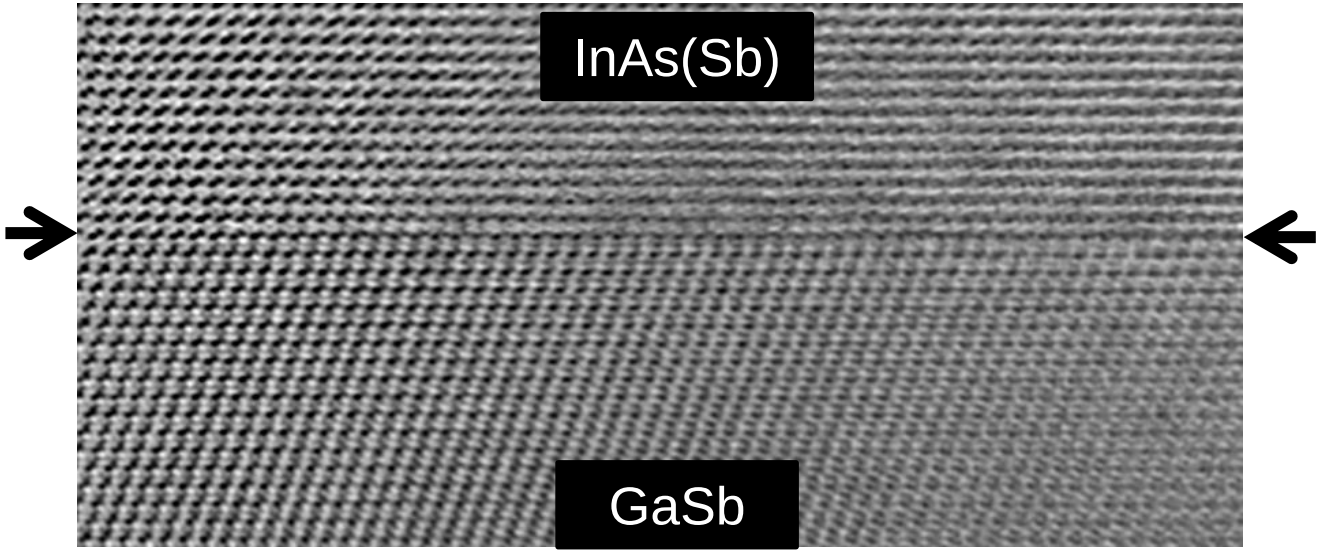






VERY abrupt heterojunction!

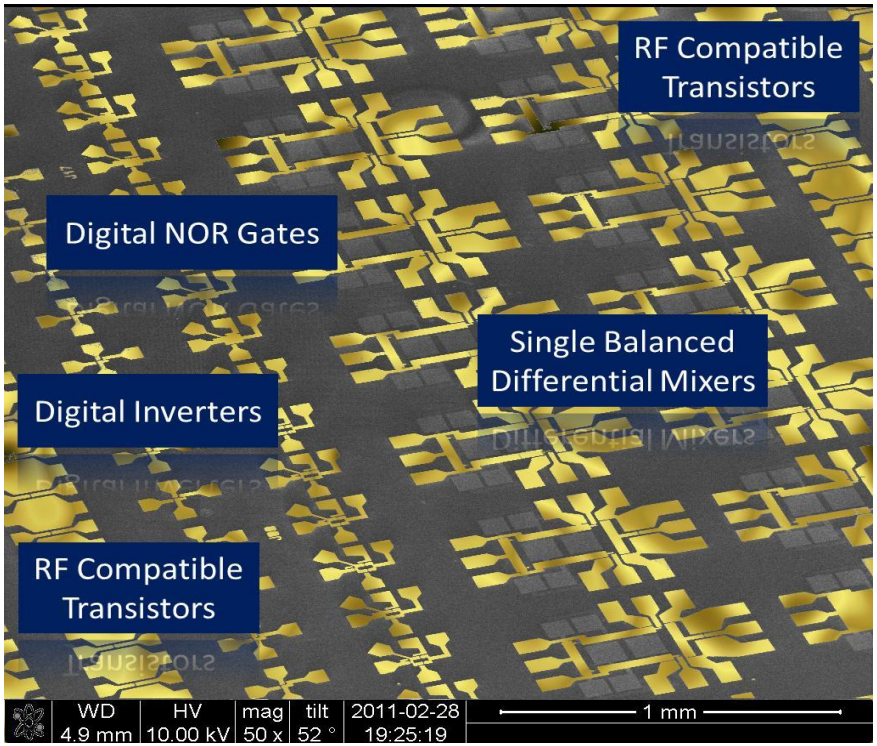
Sudden group-V contrast change indicates abrupt transition



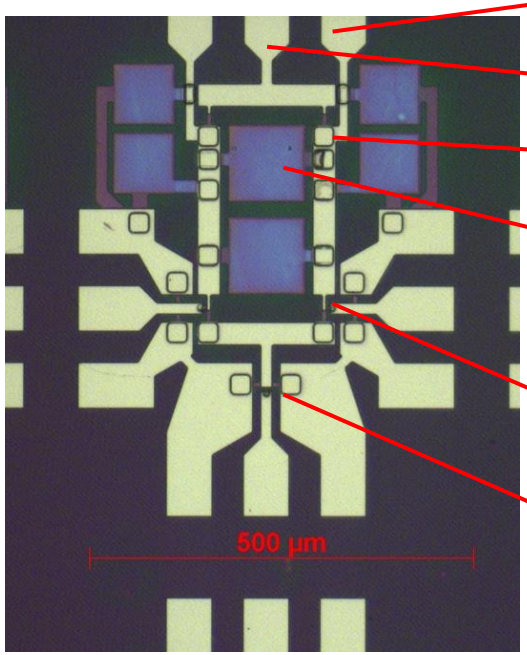
Courtesy of Martin Ek

InAs Circuits on 2” Si

Good wafers: 80% yield
Area: 2000x6000 µm²



First test circuit:
Balanced mixer



Output voltage

V_{dd}

Resistive loads

Capacitive decoupling

LO^+ and LO^- input

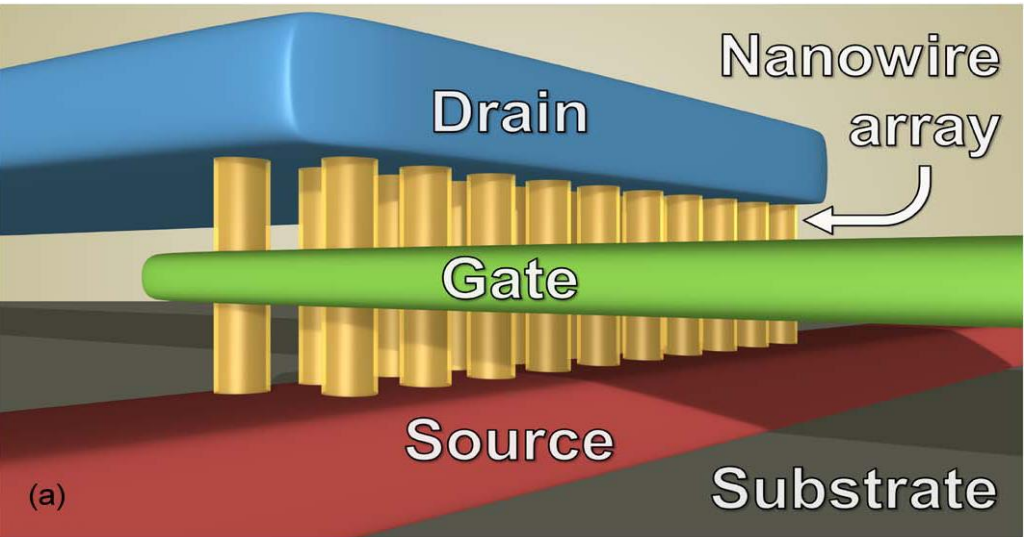
RF-input

Design with 52 nanowire transistors
Nanowire resistors
Designed for 1 GHz input

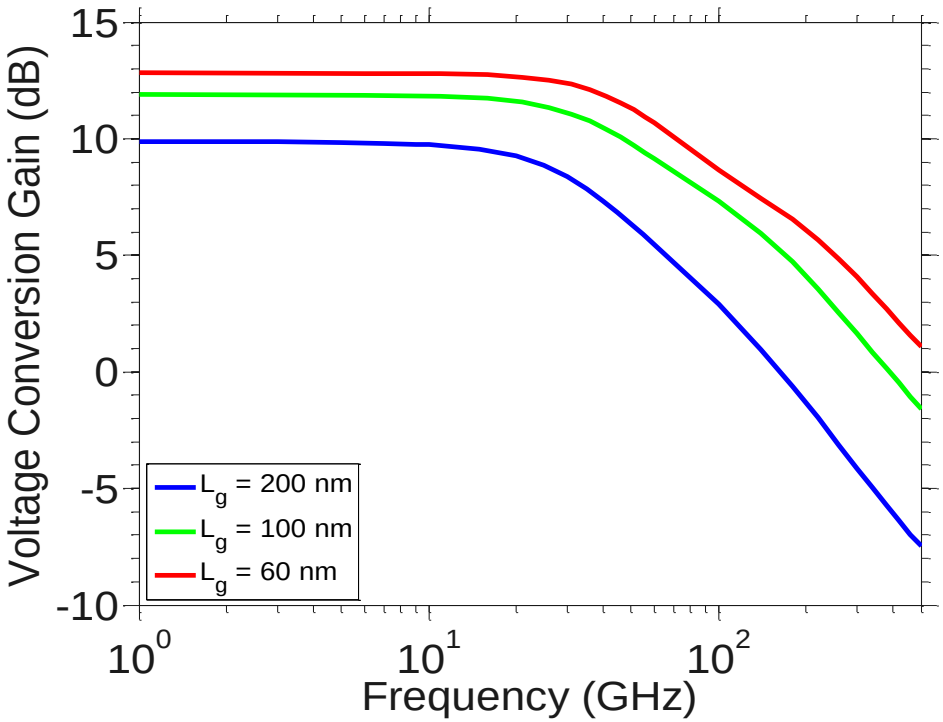
InAs Circuits on 2” Si

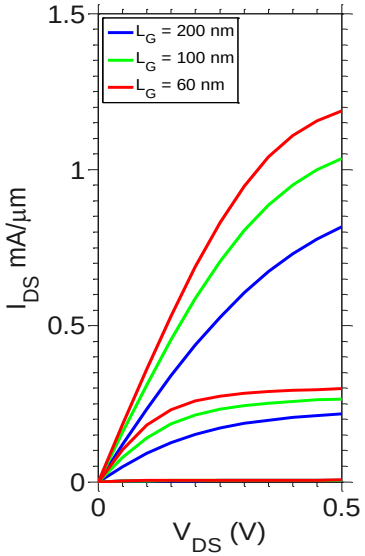
NANO ELECTRONICS GROUP

Device Architecture



Mixer Performance





Transistor Performance

RF FET: 36 NWs (6x6 array)
LO FET: 72 NWs (12x6 array)
NW Spacing: 200 nm
L_G: 200 nm, 100 nm, 60 nm

R_L: 2.5 kΩ
V_{DD} = 1.5 V
P_{DC} = 1 mW

Outperforming the Conventional Scaling Rules in the Quantum-Capacitance Limit

J. Knoch, W. Riess, and J. Appenzeller, *Senior Member*,

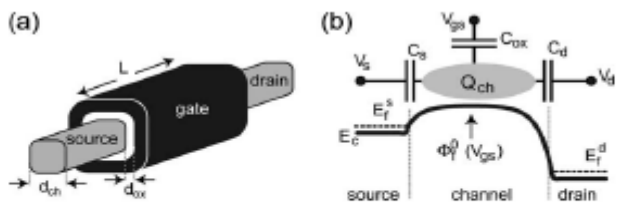


Fig. 1. (a) Schematics of the wrap-gate transistor design under consideration. (b) Surface potential along the direction of current transport. The total charge in the channel is determined by all terminal voltages.

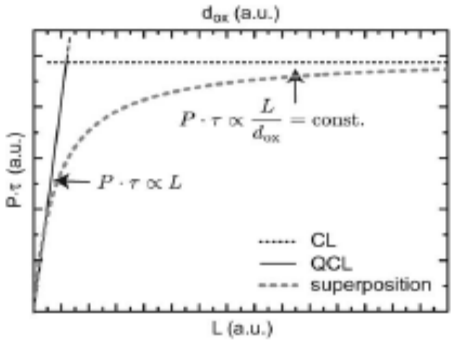


Fig. 2. Power delay product as a function of L and d_{ox}. The horizontal black dotted line shows the CL, where $P \cdot \tau =$ const., and the straight black line belongs to the QCL with $P \cdot \tau \propto L$. The gray dashed line is the superposition of the two limiting curves showing an increasing scaling benefit in the QCL.

	Gate delay (diffusive) $\tau = C_g V_{dd}/I_d$	Gate delay (ballistic) $\tau = C_g V_{dd}/I_d$	Power –delay product
Classical Limit, CL	$\tau \sim L^2$	$\tau \sim L$	constant
Quantum Capacitance Limit, QCL	$\tau \sim L^2$	$\tau \sim L$	$P*\tau \sim L$

$$I_d \propto \frac{l_{scat}}{l_{scat}+L}\frac{1}{L}\frac{C_{ox}C_q}{C_{ox}+C_q}(V_{gs}-V_t)v_{inj}$$

Simulated performance

Movement of the band with the gate bias

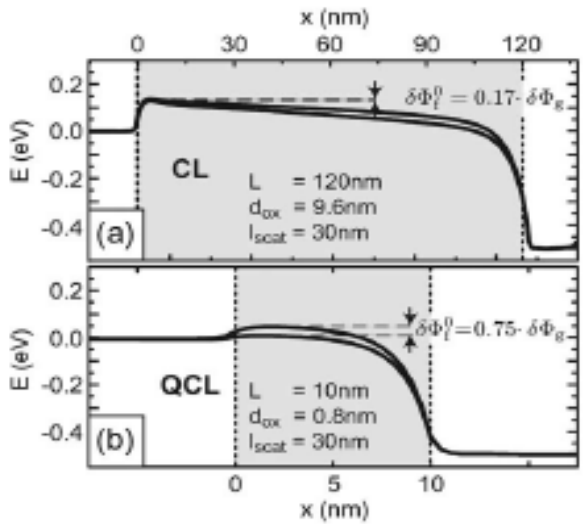
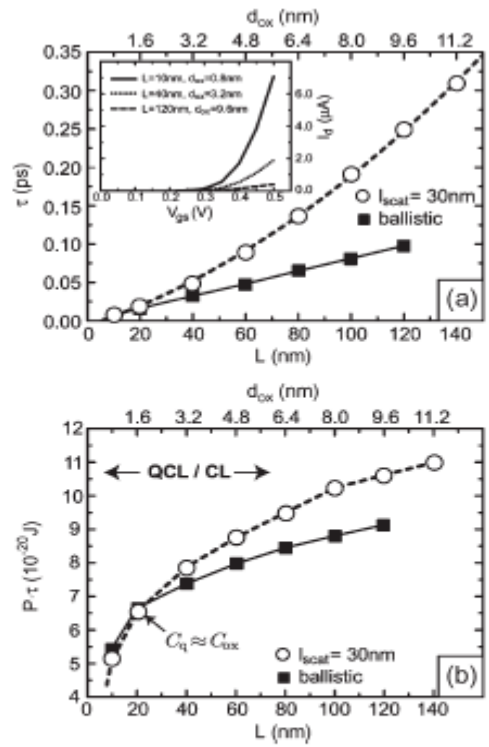


Fig. 3. Conduction band profile for (a) a device with $L = 120$ nm a $d_{ox} = 9.6$ nm and (b) for a FET with $L = 10$ nm and $d_{ox} = 0.8$ nm showi that (a) is rather in the CL, whereas (b) is scaled toward the QCL. He $V_{ds} = 0.5$ V, and $V_{gs} = 0.5$ and 0.55 V.

Simulations of devices were carried out with the following parameters: $E_f^{s,d} = 0.1$ eV, $m^* = 0.1 m_0$, and $d_{ch} = 3$ nm; a midgap work-function metal was assumed as gate electrode, and $\Phi_{bi} = 0.4$ eV. Furthermore, $\varepsilon_{ox} = 3.9$, and $\varepsilon_{ch} = 12$.

QCL vs CL limit



$$\tau = \int Q dV_{gs}/(V_{dd} I_d).$$

$$P \cdot \tau \quad \int Q dV_{gs},$$

Fig. 4. (a) Gate delay extracted from simulations versus L, d_{ox} for (hollow circles) scattering and (solid black squares) ballistic transport. The dashed black line is a quadratic fit to the data points. In the case of ballistic transport, the data points lie on a straight line. (b) Simulated $P \cdot \tau$ as a function of L and d_{ox}. The curves exhibit the same behavior as shown in Fig. 2, implying a significant scaling benefit in the QCL.