Lecture 4: III-V CMOS II

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GaSb Inversion-Mode PMOSFETs With Atomic-Layer-Deposited Al_2O_3 as Gate Dielectric

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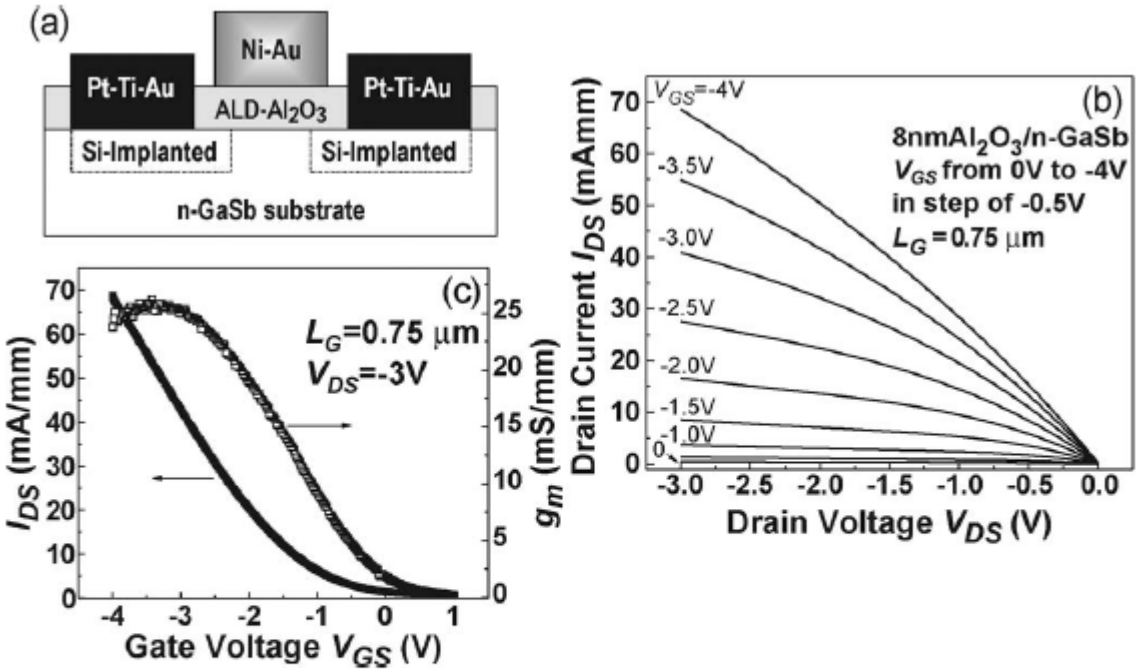

Fig. 1. (a) Schematic cross section of an inversion-mode GaSb PMOSFET with ALD Al_2O_3 as gate dielectric. (b) DC output characteristic of a 0.75-μm-gate-length device fabricated by Process I at $V_{DS} = -3$ V and $V_{GS} = -4$ V, showing the drain current potential at the current interface quality and dielectric strength. (c) DC transfer characteristics of the same device at $V_{DS} = -3$ V.

GaSb:

Large hole mobility

Large density of states in valence band

Low density of defects close to valence band

Electrical Characteristics

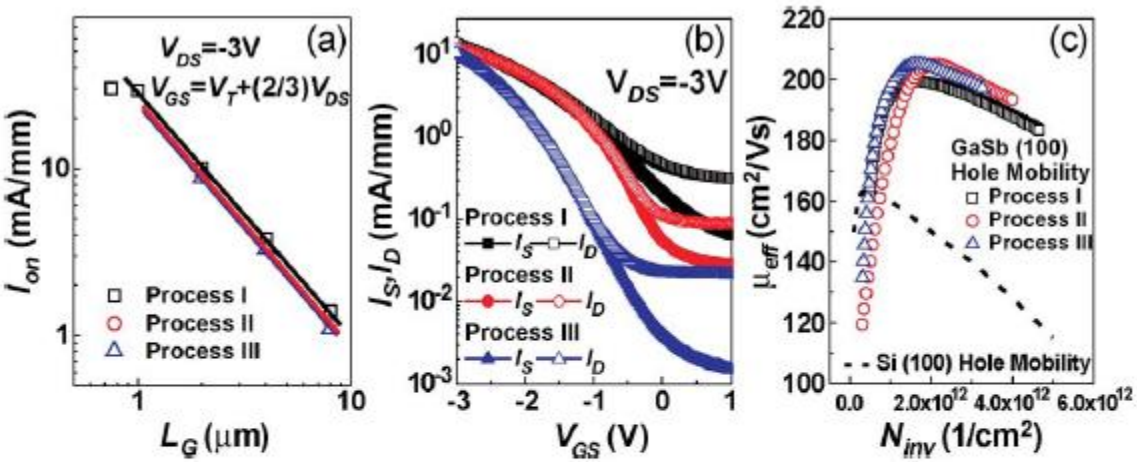

Fig. 2. (a) Comparison of scaling behavior of drain currents versus gate length L_G on three different processed samples at $V_{\mathrm{DS}} = -3$ V and $V_{\mathrm{GS}} = V_T + (2/3) \cdot V_{\mathrm{DS}}$. (b) (Empty signs) Drain currents and (solid signs) source currents versus gate bias V_{GS} on three different processed samples at $V_{\mathrm{DS}} = -3$ V. (c) Effective mobility (μ_{eff}) versus inversion hole charge density (N_{inv}). μ_{eff} is extracted from split C–V method with all three processes. The Si(100) universal hole mobility is also included for comparison.

Scaling of gate length Important due to larger effective mass

Process dependence (ohmic contacts)

Mobilities above 200 cm²/Vs

Interface quality

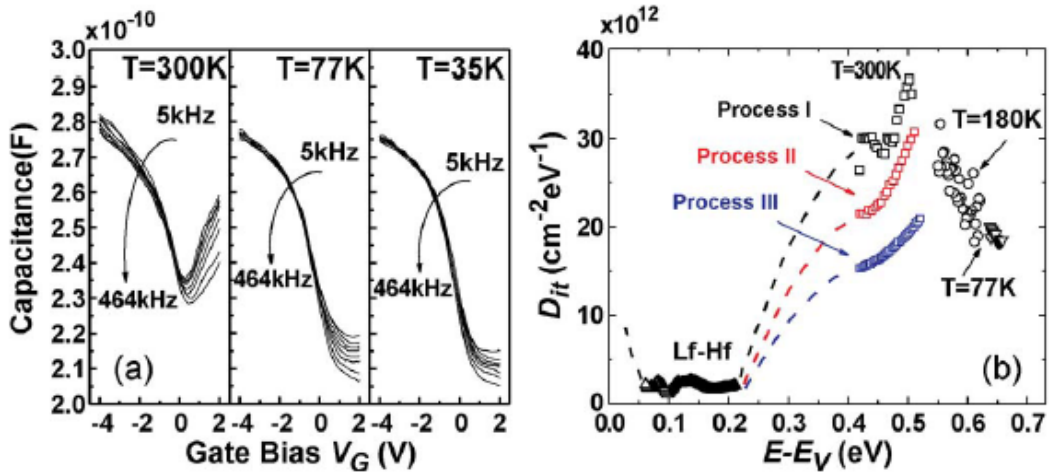

Fig. 3. (a) C–V plots of Au/ Ni/8-nm-Al_2O_3/p-GaSb at 300 K, 77 K, and 35 K. The excellent frequency-dispersion behavior at accumulation capacitance at all temperatures indicates true hole accumulation and a good interface near the valence band. The capacitor area is 3.14×10^4 μm^2 with a dielectric constant of ~8 for Al_2O_3. (b) Interface trap distribution near the conduction band is obtained from temperature-dependent conductance method on n-MOSCAPs at 300 K, 180 K, and 77 K, and that near the valence band is obtained from low-f–high-f C–V measurement on p-MOSCAPs at 35 K. The D_{it} distribution is similar to that on Ge without good surface passivation. The hole capture cross section in GaSb from 10^{-18} to $10^{-14}/cm^2$, depending on the energy level [20], is chosen to determine the D_{it} distribution. The dashed lines are guides to the eye. The square signs are obtained from conductance method performed at 300 K with the black signs for Process I, the red signs for Process II, and the blue signs for Process III. The black circle signs and down triangle signs are obtained from Process-I samples performed at 180 K and 77 K, respectively. Process I with a higher activation temperature of 650 °C results in a larger D_{it} since GaSb has a melting point of 712 °C and is easier to lose Sb at a higher processing temperature [10].

Comparably low density of defect levels close to valence band

High density of defect levels close to conduction band

Process dependence

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III–V Complementary Metal–Oxide–Semiconductor Electronics on Silicon Substrates

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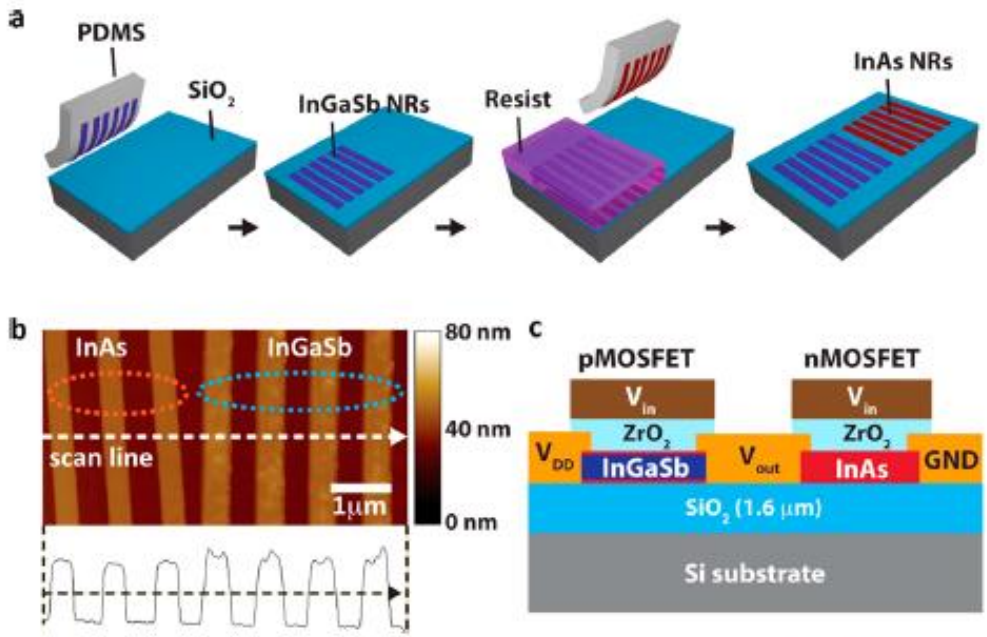

Figure 1. III–V XOI CMOS. (a) Process schematic for the heterogeneous integration of InAs and InAs/InGaSb/InSb XOI on a Si/SiO_2 substrate. (b) Atomic force micrograph of transferred InAs and InAs/InGaSb/InAs NRs, located adjacently. (c) Schematic representation of a top-gated CMOS inverter with InAs (n-type) and InGaSb (p-type) active layers, having 10 nm of ZrO_2 as the top-gate dielectric.

InAs/InGaSb Heterostructure:

Surface passivation

Non-doped ohmic contact formation

Provide strain to enhance mobility

Electrical Characteristics

InAs: 3 nanoribbons
340 nm L_g
μ 1190 cm^2/Vs
SS 84 mV/dec

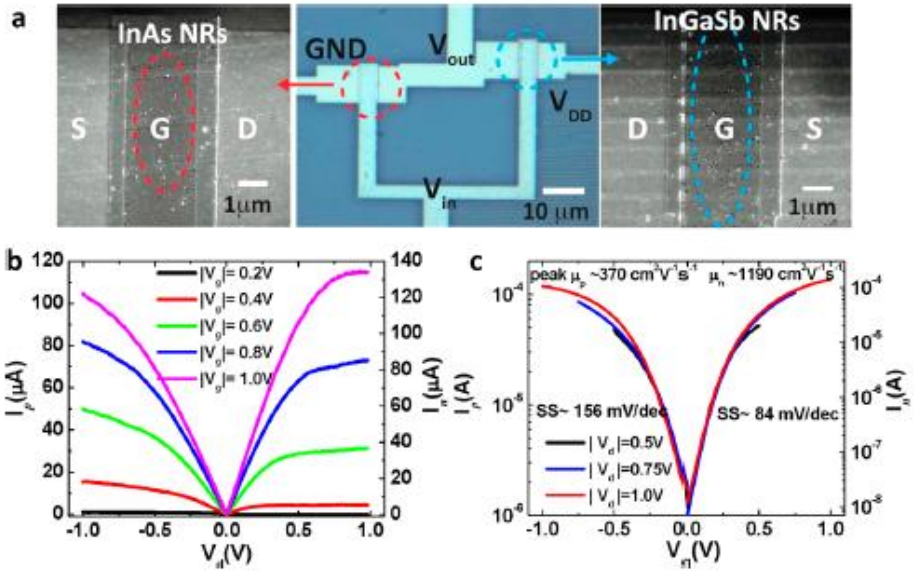

Figure 2. Performance of *p*- and *n*-type XOI MOSFETs. (a) Optical image (center) of a fabricated III–V CMOS inverter and the corresponding SEM images of each channel region (left: InAs; right: InAs/InGaSb/InAs). (b) Output and (c) transfer characteristics of *p*- (left axis) and *n*- (right axis) MOSFETs.

InGaSb: 9 nanoribbons
200 nm L_g
μ 370 cm^2/Vs
SS 156 mV/dec

Circuits

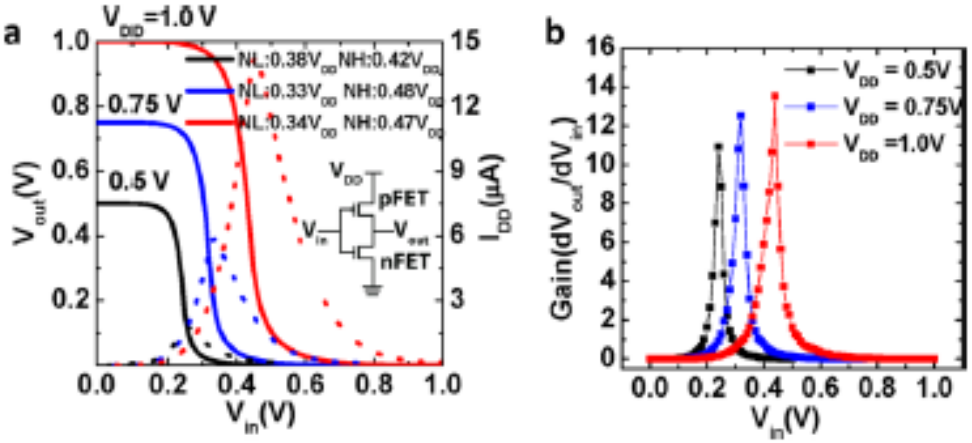

Figure 3. III–V CMOS inverter. (a) Transfer characteristics of a CMOS inverter, measured at different supply voltages (V_{DD}). Inset shows the circuit diagram for the fabricated inverter. (b) Inverter gain (dV_{out}/dV_{in}) dependence on the input voltage.

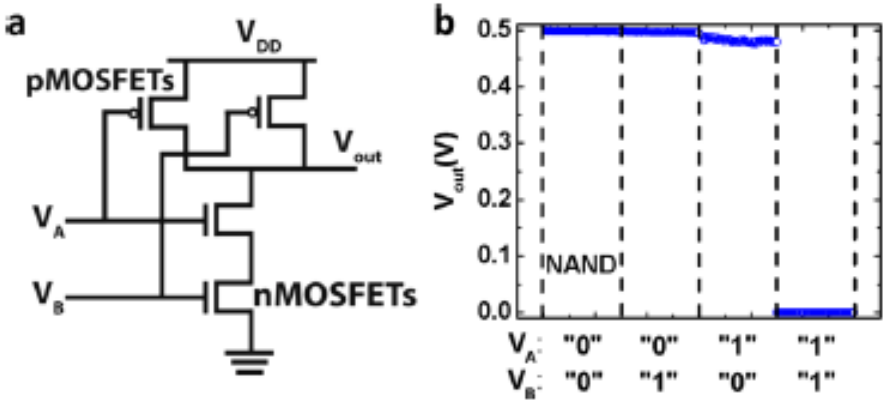

Figure 4. III–V CMOS NAND logic gate. (a) Circuit schematic of a CMOS NAND gate. The circuit is designed by connecting two p-MOSFETs in parallel and two n-MOSFETs in series. (b) Output voltage V_{out} for four different combinations of input states "0 0", "0 1", "1 0", and "1 1". The output is in the "low-state" only if the inputs are "1 1". Note: Input voltages of +0.5 and −0.5 V are treated as logic "1" and "0", respectively. The supply voltage (V_{DD}) for the circuit is 0.5 V.

MOS interface and channel engineering for high-mobility Ge/III-V CMOS

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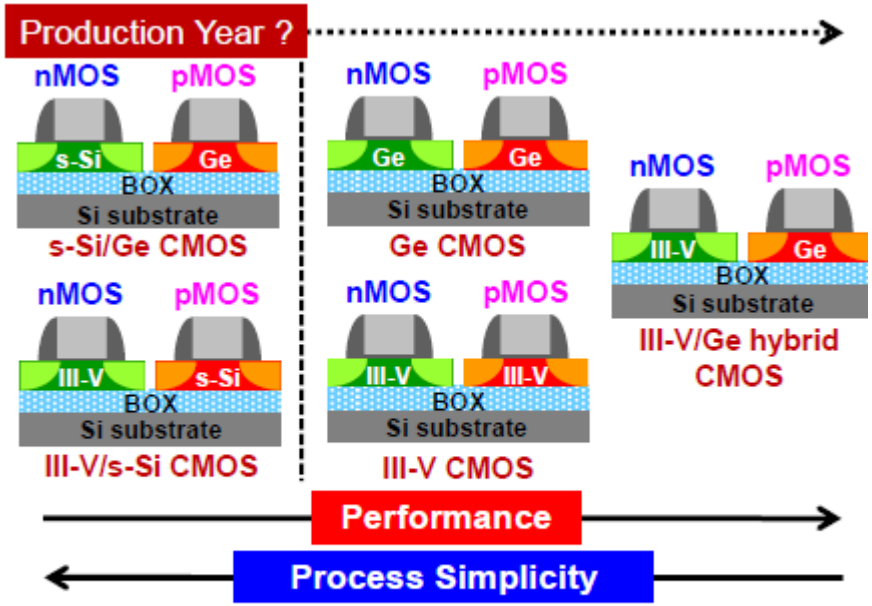


Fig.1: Several CMOS structures using Ge/III-V channels.

There are many challenges:

Scaling of Ge EOT

III-Vs on Si

n- and p-type Integration

Ge Technology

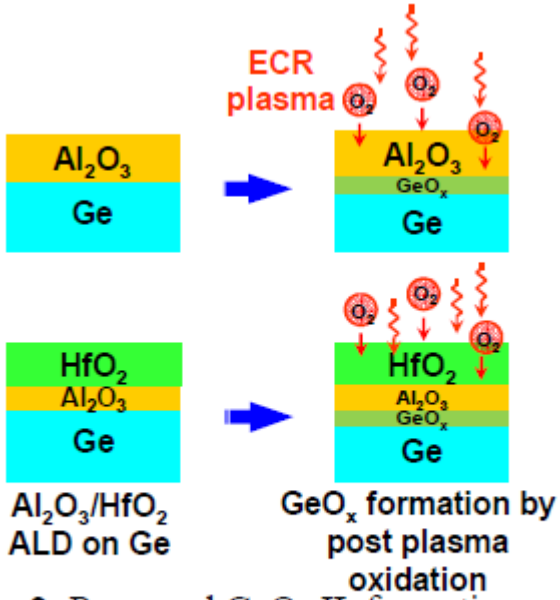


Fig. 2: Proposed GeO_x IL formation process by using ECR oxygen plasma oxidation through ALD Al_2O_3 and HfO_2/Al_2O_3.

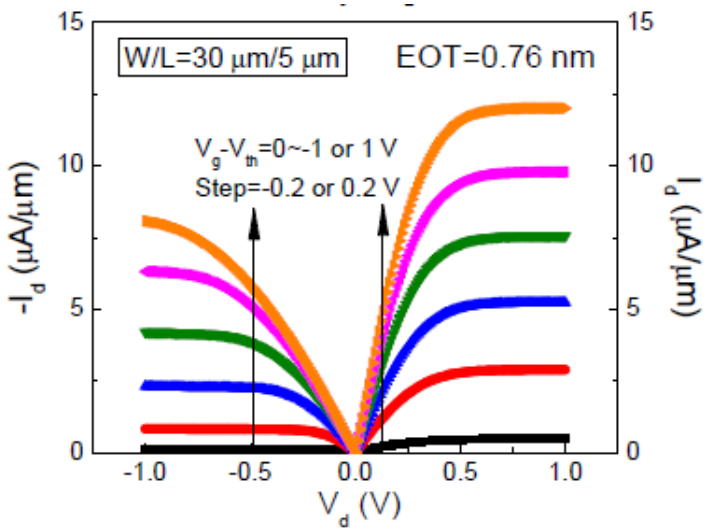


Fig. 7: I_d-V_d characteristics of Ge n- and pMOSFETs with $HfO_2/Al_2O_3/GeO_x/Ge$ gate stacks having EOT of 0. 76 nm.

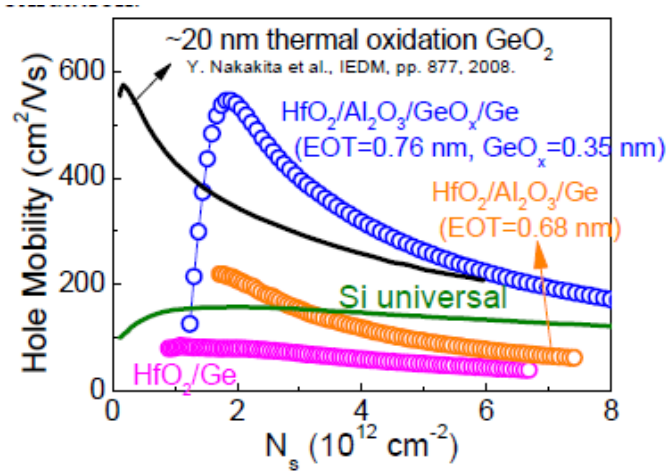
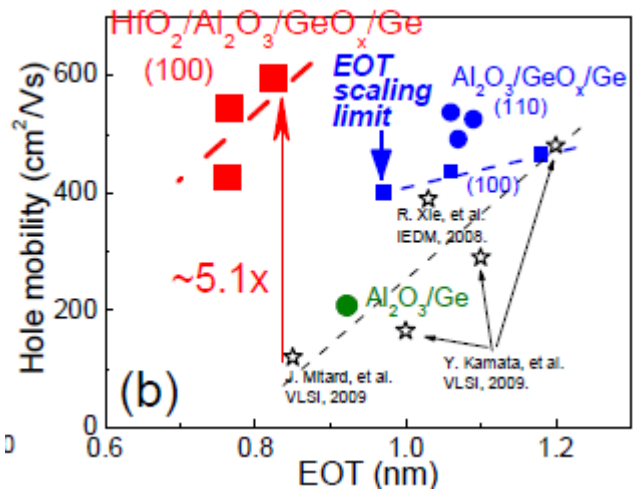


Fig. 9: Hole mobility of Ge pMOSFETs with a variety of MOS interfaces as a function of N_s



InGaAs on Si

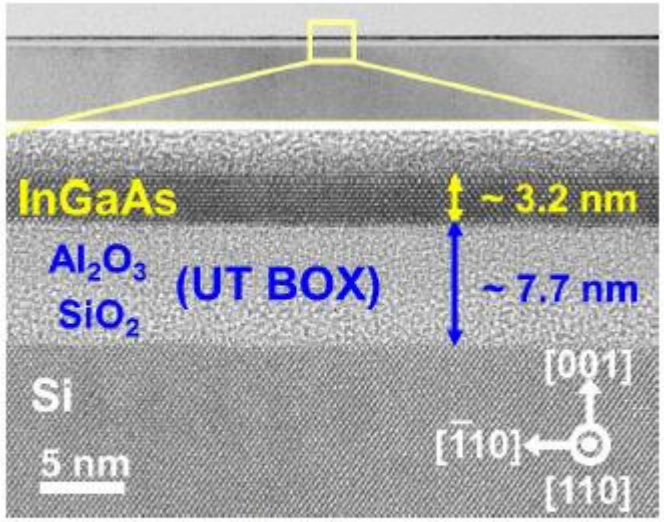


Fig. 13: TEM of a ultrathin body InGaAs substrate on Si with Al_2O_3/ SiO_2 BOX, fabricated by wafer bonding

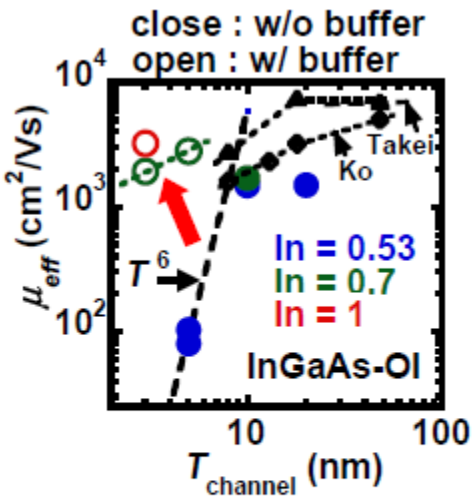


Fig. 14: Body thickness dependence of electron mobility in InGaAs/InAs-based MOSFETs.

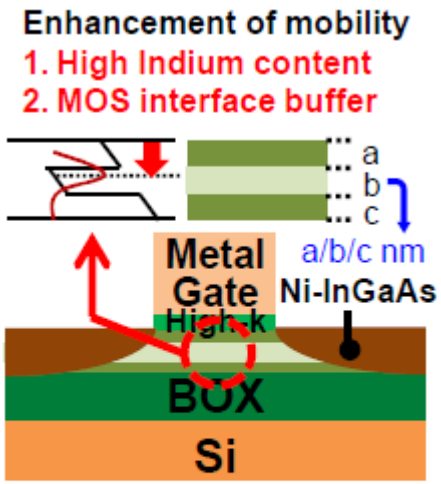


Fig. 15: MOS channel engineering for enhancing mobility in ultrathin body InGaAs-based MOSFETs.

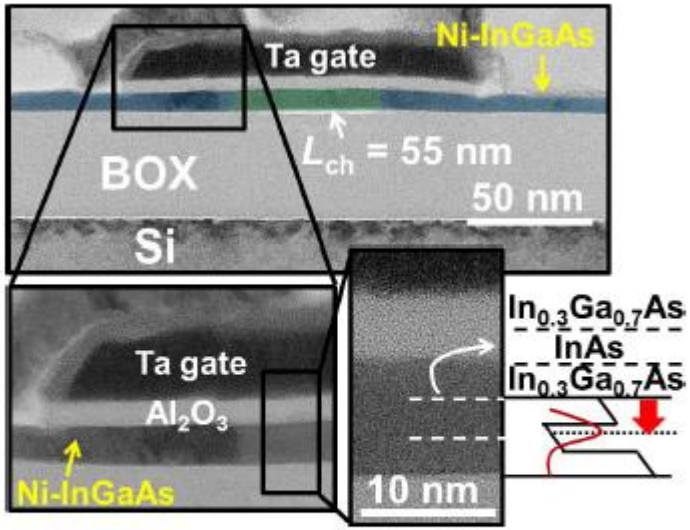


Fig. 16: TEM of 55-nm-L_g ultrathin body MOSFETs with $In_{0.3}Ga_{0.7}As$(3nm)/InAs (3nm)/$In_{0.3}Ga_{0.7}As$(3nm) and Ni-InGaAs metal S/D.

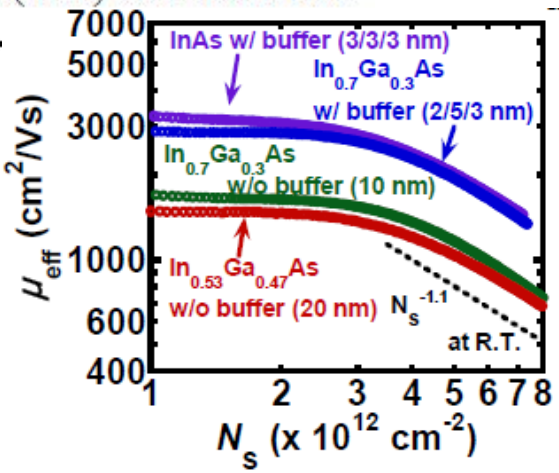


Fig. 19: N_s dependence of electron mobility at RT for InGaAs-based ultrathin body MOSFETs.

Ge and InGaAs Integration

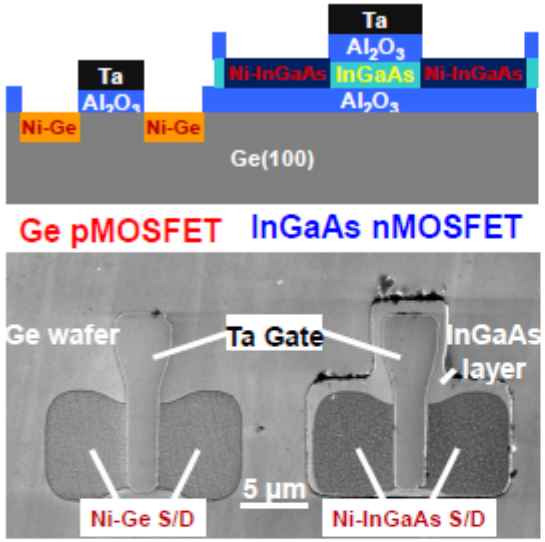


Fig. 27: Schematic view and a photograph of fabricated CMOS structure of InGaAs-OI nMOSFET and Ge pMOSFET by using common Al_2O_3-based gate stack and Ni-based S/D

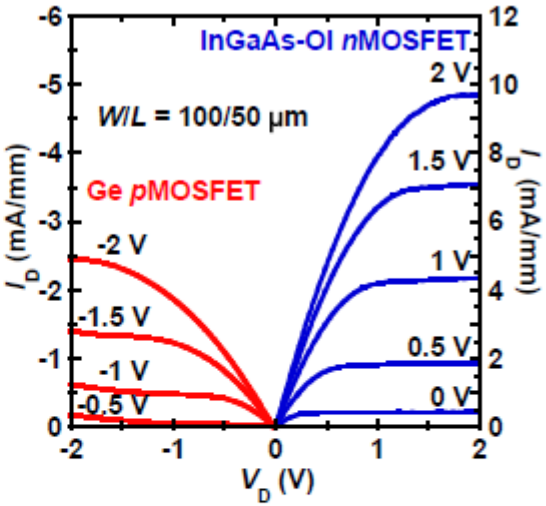


Fig. 28: I_d - V_d characteristics of a Ge pMOSFET and a 20-nm-thick InGaAs-OI nMOSFET, fabricated on a same wafer.

An Integration Path for Gate-first UTB III-V-on-insulator MOSFETs with Silicon, using Direct Wafer Bonding and Donor Wafer Recycling

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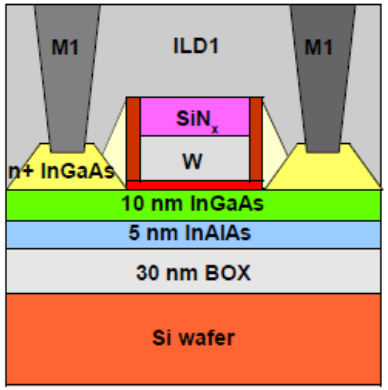


- UTB III-V transfer on Si
- High-k / Metal gate / Gate cap deposition
- Gate patterning
- Sidewall insulation
- III-V cleaning and S/D regrowth (600°C)
- ILD1 deposition and patterning
- M1 contacts

Fig. 11: Process flow and schematic for gate-first implant-free UTB InGaAs/InAlAs MOSFETs on silicon.

Wafers may be reused up to 25 times

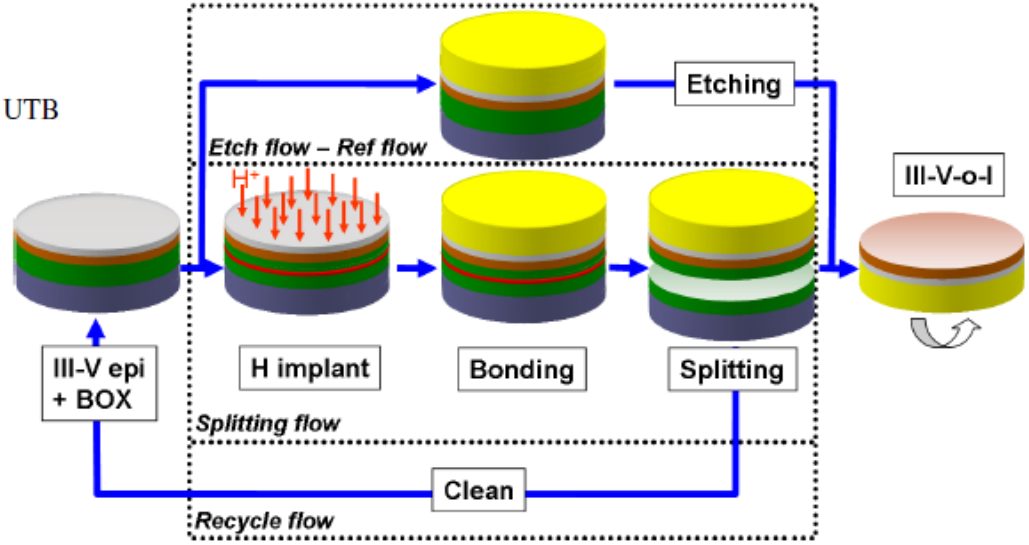


Fig. 2: Process flow of III-V-o-I wafer fabrication fully compatible with VLSI standards using DWB, hydrogen implantation, thermal splitting, selective etching and InP donor wafer re-use.

Nanoelectronics: III-V CMOSII

Materials Quality

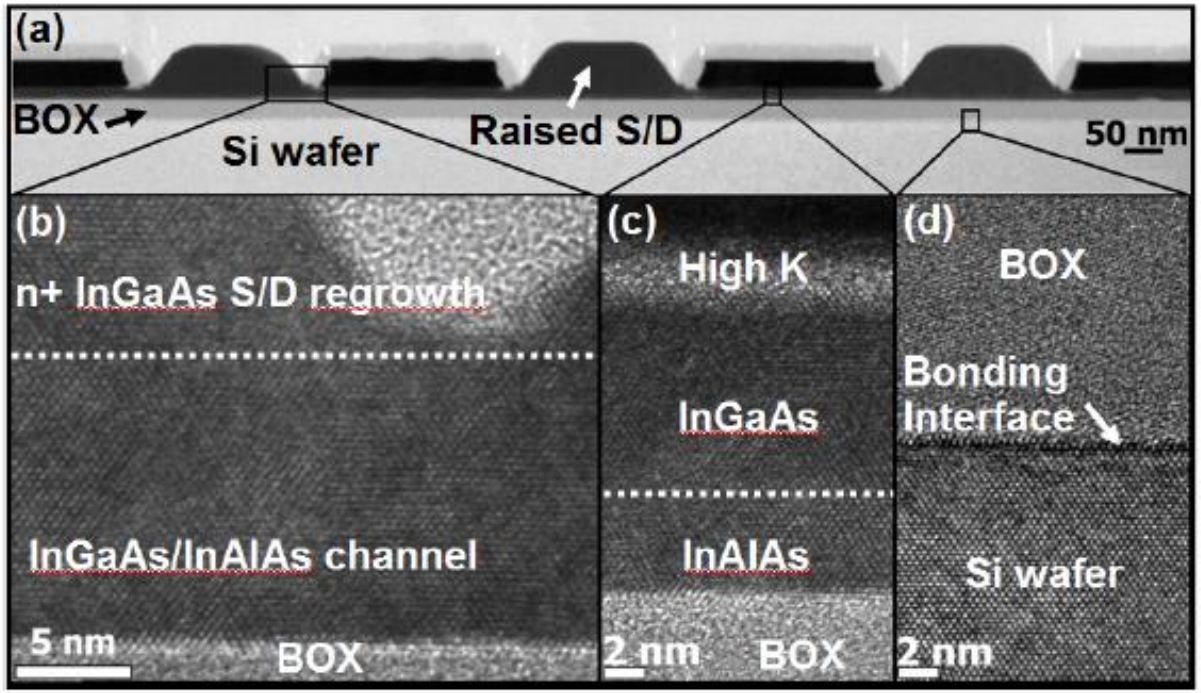
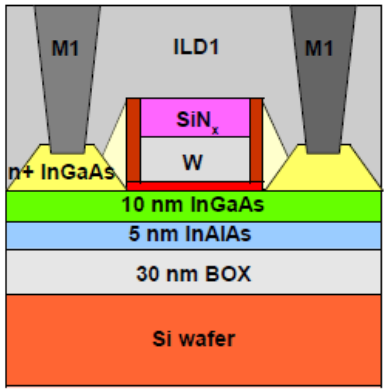


Fig. 12: (a) Cross-sectional STEM micrograph of gate-first implant-free UTB InGaAs/InAlAs MOSFETs on silicon, with raised S/D, 250 nm gate length and 500 nm gate pitch. (b) HRTEM cross-section of the UTB III-V / n+ regrowth interface showing ideal crystallinity. HRTEM cross-section of (c) the high-k / UTB III-V / BOX region and (d) the BOX-Si region showing sharp interfaces.

High material quality

InGaAs MOSFETs



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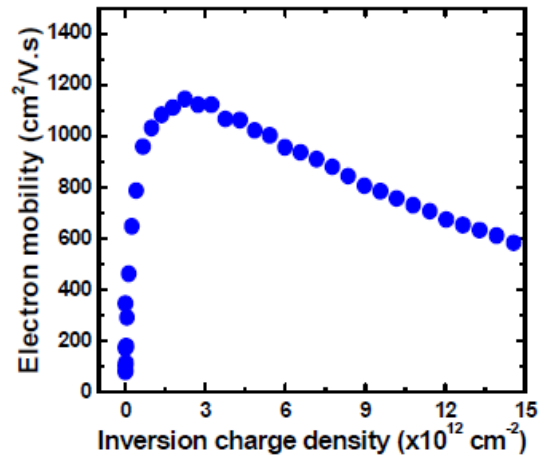
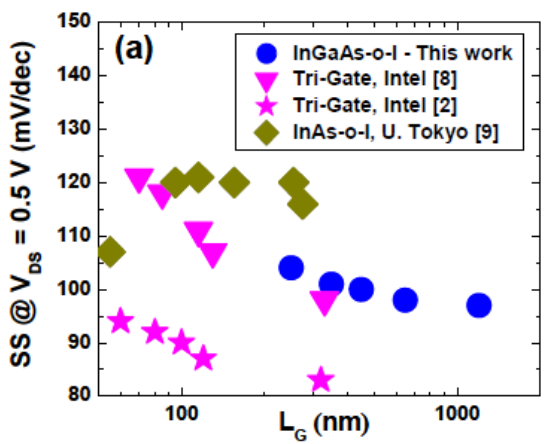
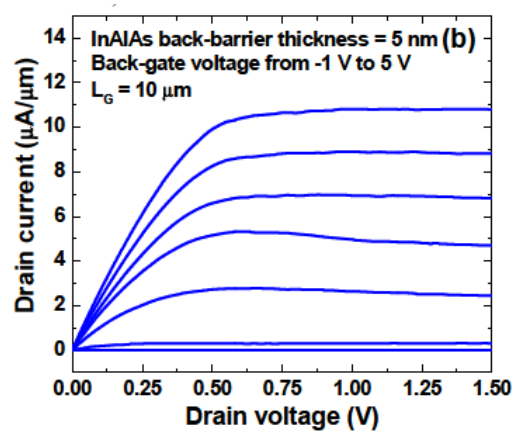


Fig. 14: Electron mobility vs inversion charge density on a long-channel MOSFET. This device exhibits a comparable mobility than previously reported devices with a similar process on bulk InP [4].





Very competitive transistor data