Integration of III-V semiconductors with Si

Mattias Borg

On the agenda

Part 1:

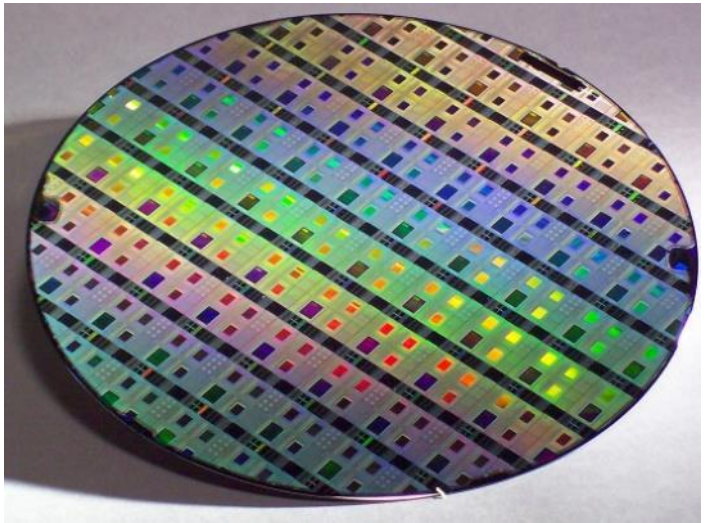
- Why go for III-Vs?
- Challenges of integration
- Integration techniques
  - Buffer layer epitaxy
  - ELO

Part 2:

- ART
- Nanowire epitaxy
- TASE
- RME
- The future

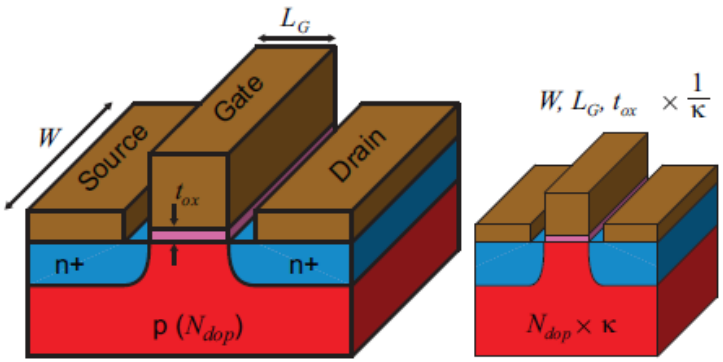
Si integrated circuits

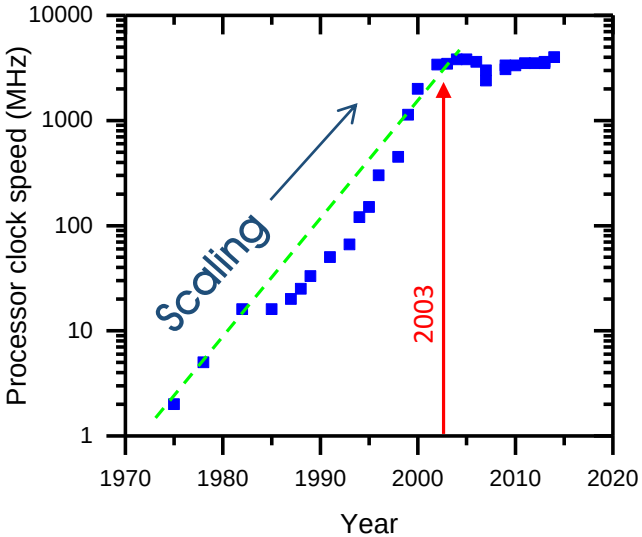
- Si electronics for 50+ years!
  →Established, inexpensive, versatile
- Billions of transistors/chip (all ”identical”!)
- Si CMOS → Greatest engineering feat of mankind

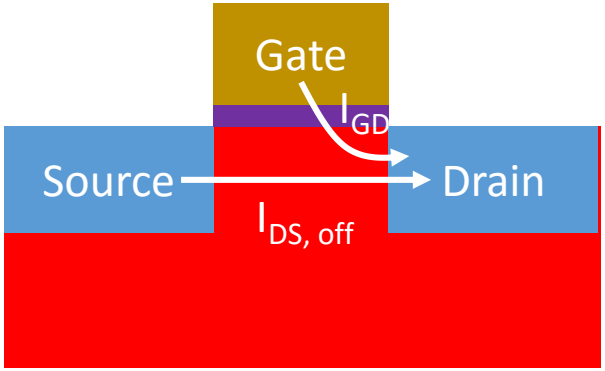


End of the Si roadmap

- Power leakage is the problem
  - Leakage through gate dielectric, I_{GD} (dynamic)
  - Leakage in off-state, $I_{DS,off}$ (static)
  - Core clock speed increase stalls





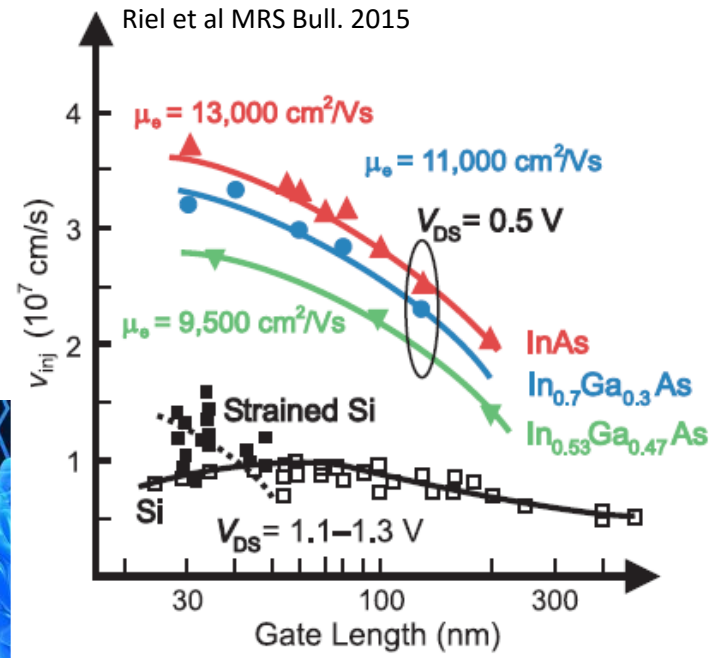


So why III-V's?

→ Electron mobility better

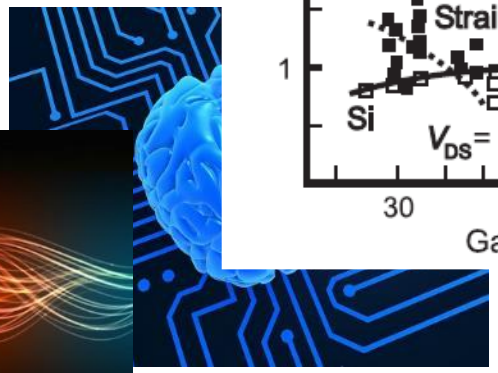
→ Direct band gaps

- III-V CMOS instead of Si?
- Can extend application space
- III-Vs should be integrated with Si!



optoelectronics

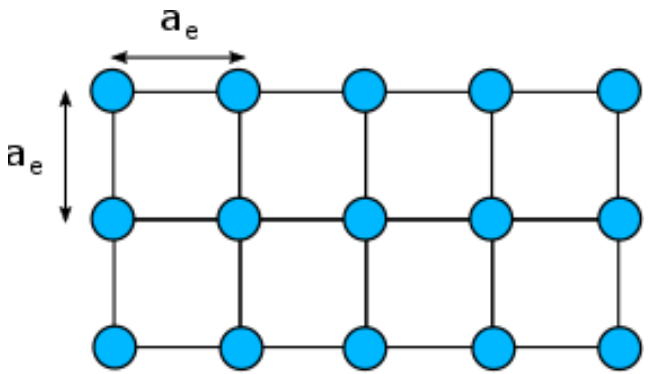
High-frequency communication



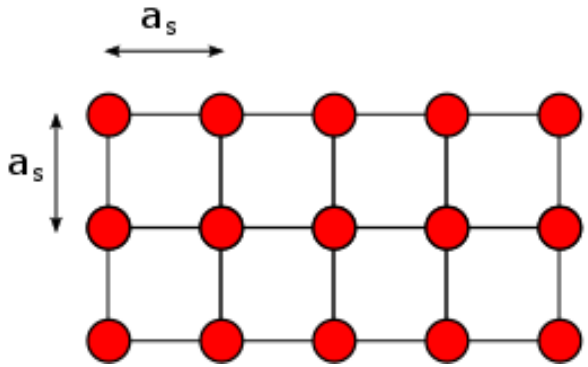
Quantum computing

Challenges of integration
Lattice-mismatch

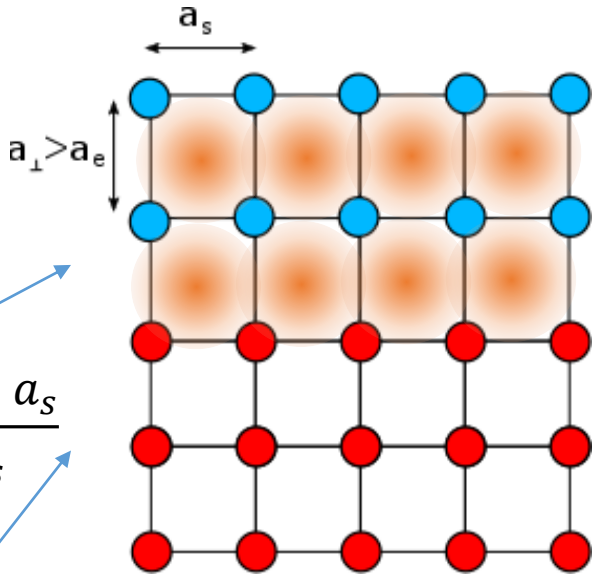
Epi material



Substrate



$$f = \frac{a_e - a_s}{a_s}$$



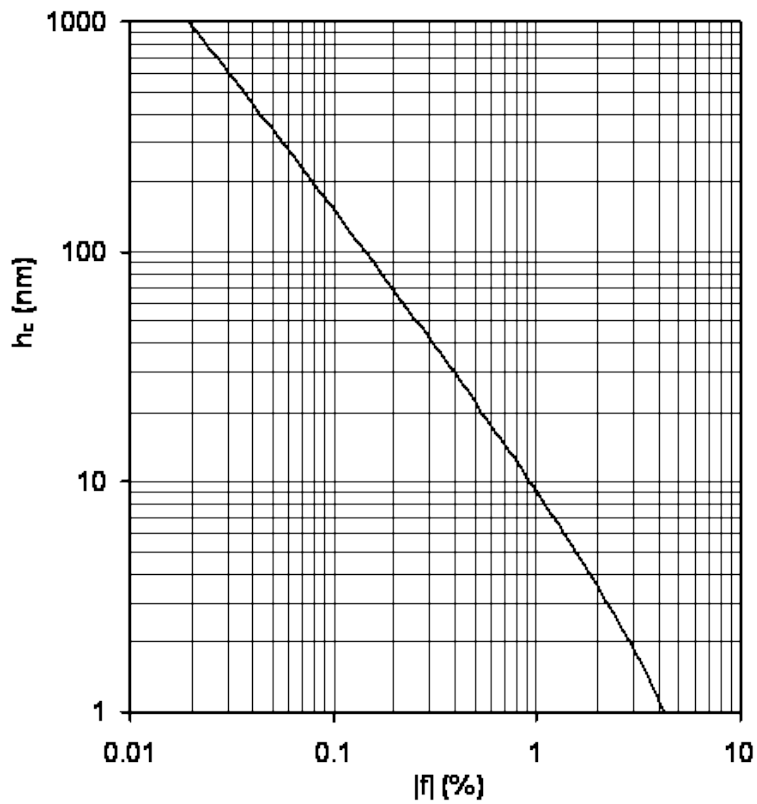
Pseudo-morphic heterostructure

Strain energy builds up with increased thickness

How thick can you grow?

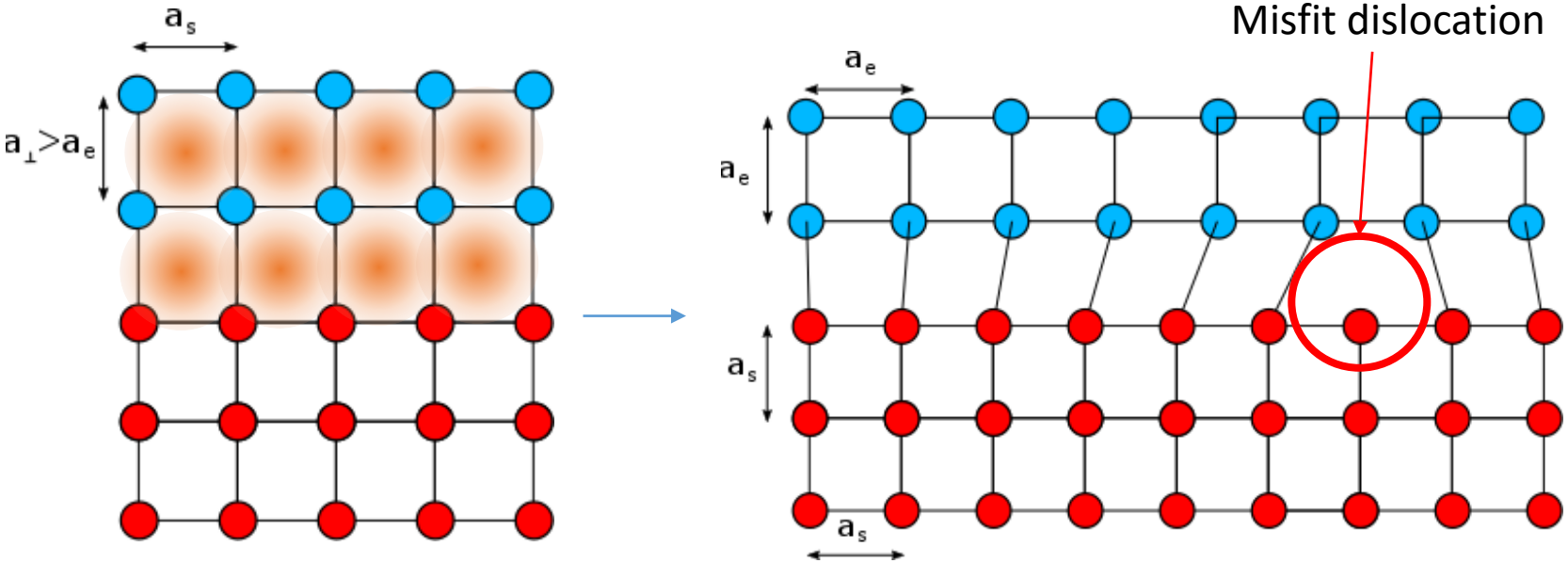
$h = layer\ thickness$

- $E_{strain} \propto h$
- Not stable when E_{strain} > critical thickness, h_c



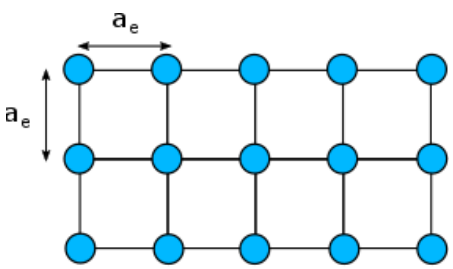
Matthews-Blakesly model

Strain relaxation

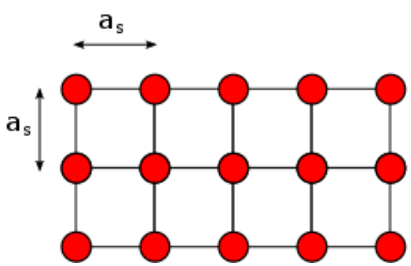


Pseudo-morphic heterostructure *Relaxed heterostructre*

Example – InAs on Si



<u>InAs</u>
a_e = 6.058 Å



<u>Si</u>
a_s = 5.431 Å

$$f = \frac{a_e - a_s}{a_s}$$

1. How large is the lattice mismatch (f)?
2. What is the critical thickness?
3. What growth mode to expect?

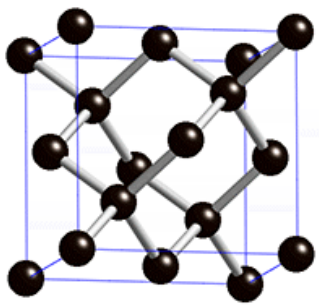
Answers:

1. **11.5%**
2. **Basically zero**
3. **Island growth**

→ InAs integration on Si seems quite hopeless

Challenges of integration
Crystal structure

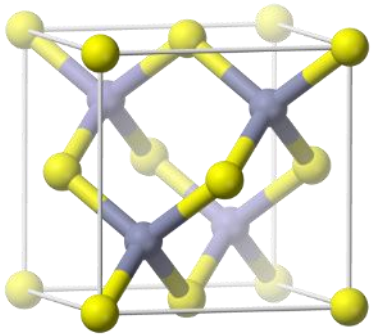
Si



Diamond structure

Two interlaced face-centered cubic (fcc) lattices
The second lattice is translated a/4*(1,1,1)

III-V

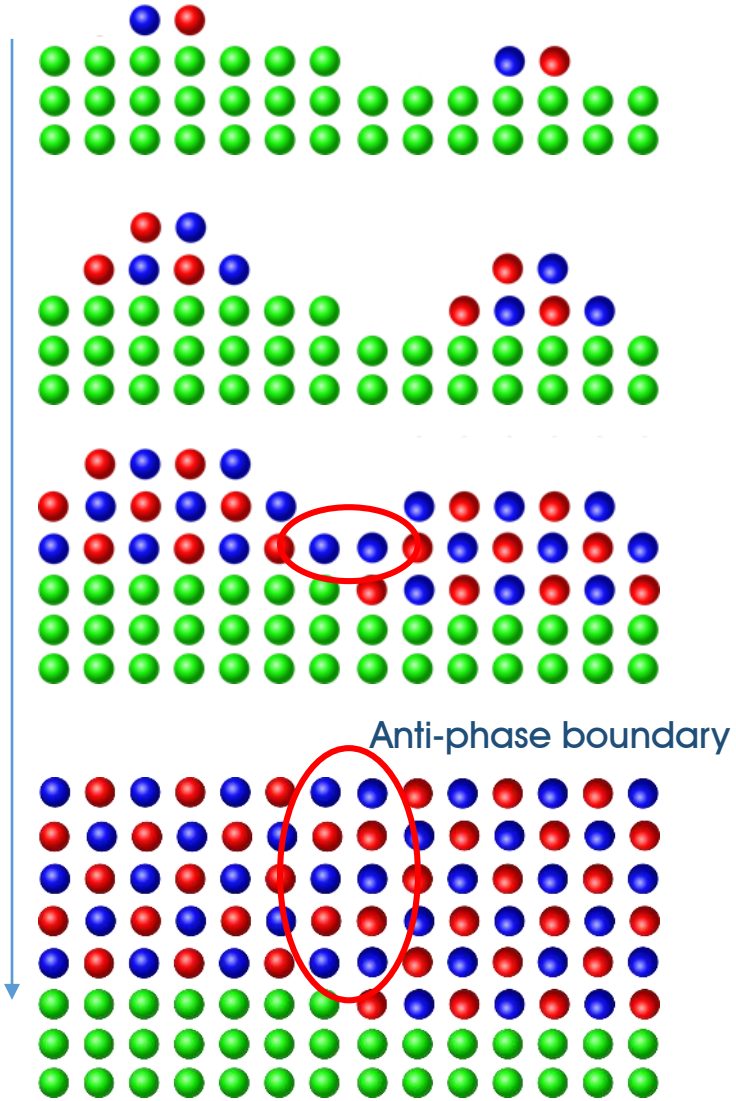


Zinc-blende structure

Same structure as diamond
but **one fcc lattice has group III**
and **the second one has group V species**

Anti-phase boundary defects

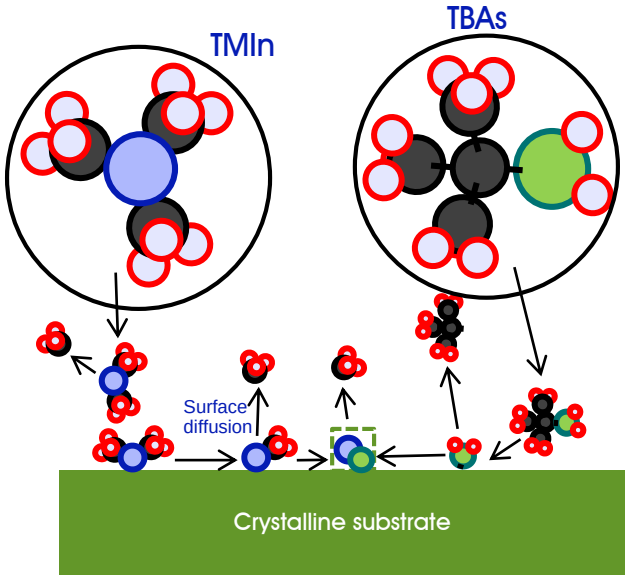
DF-TEM of CuAlNi shape-memory alloy
http://labs.mete.metu.edu.tr/tem/projects/apb/apb.html



Integration strategies

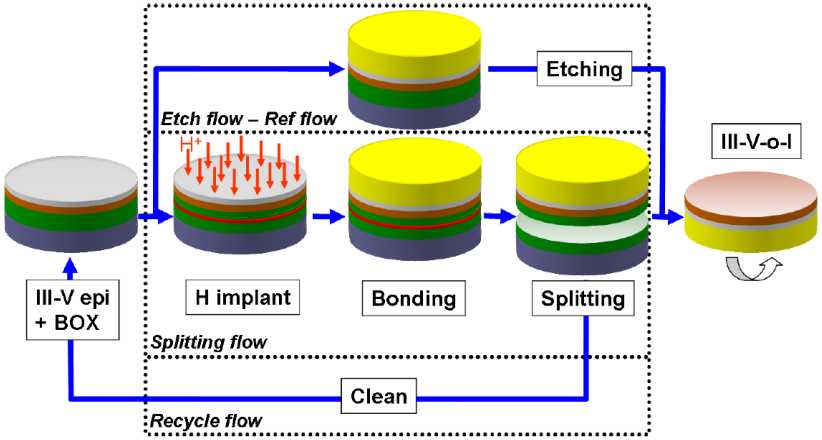
- **Goal:** Maximize quality, minimize cost

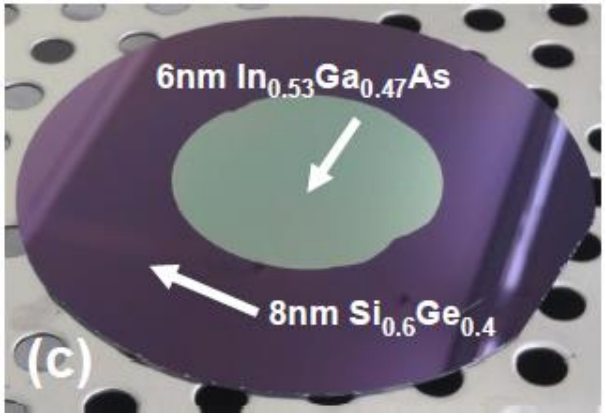
Epitaxy (MOVPE)



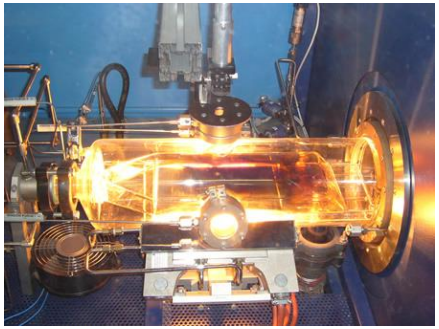
Typical Temperature: 500-800°C

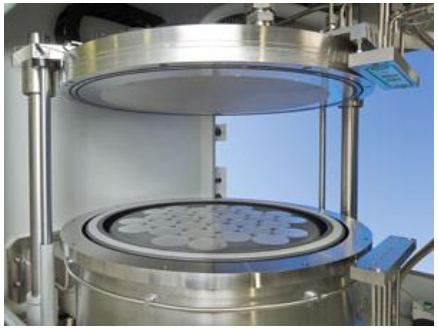
Wafer bonding





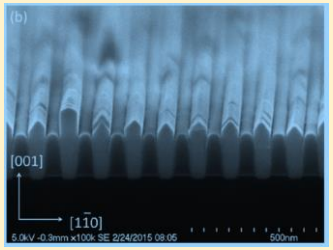
Czornomaz et al. IEDM 2013



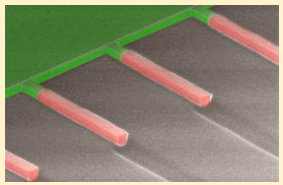


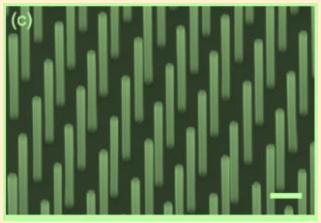
Epitaxial integration methods

Aspect ratio trapping (ART)

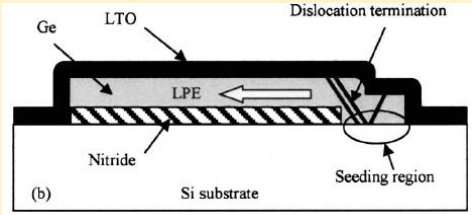


Template-assisted selective epitaxy (TASE)

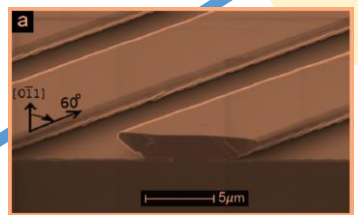




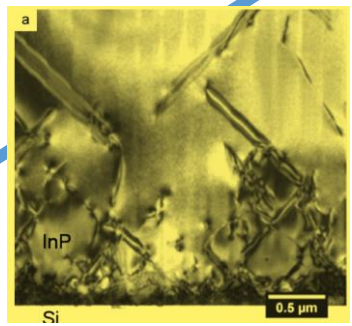
Nanowire epitaxy



Rapid Melt Epitaxy



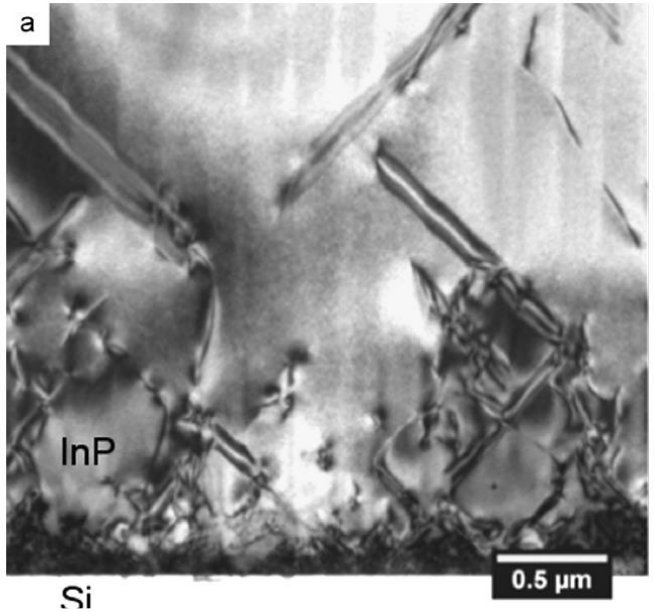
Epitaxial lateral overgrowth (ELO)



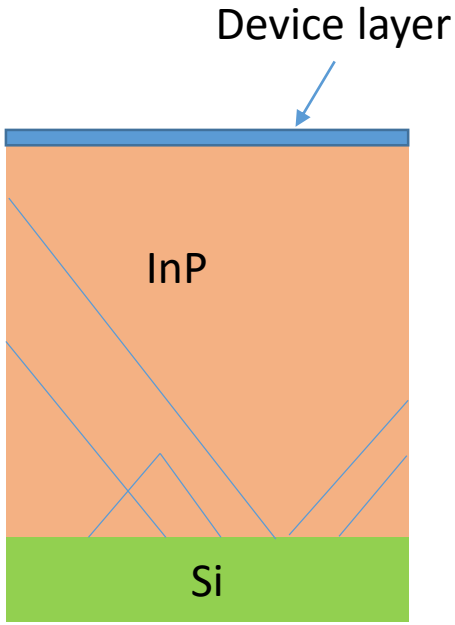
Buffer layer epitaxy

Buffer layer epitaxy

- Idea: Reduction of defects in top layer by containing defects in a thick ”buffer” layer.
- Why? Dislocations can terminate when merging



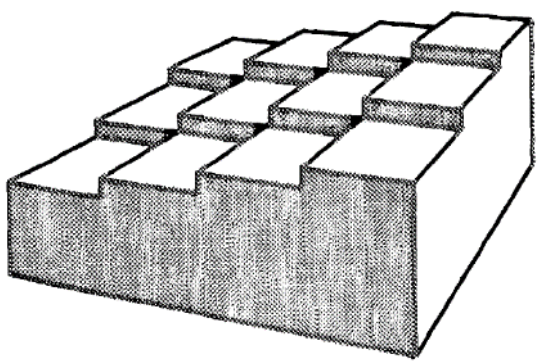
Julian et al JCG 2014



Common strategies

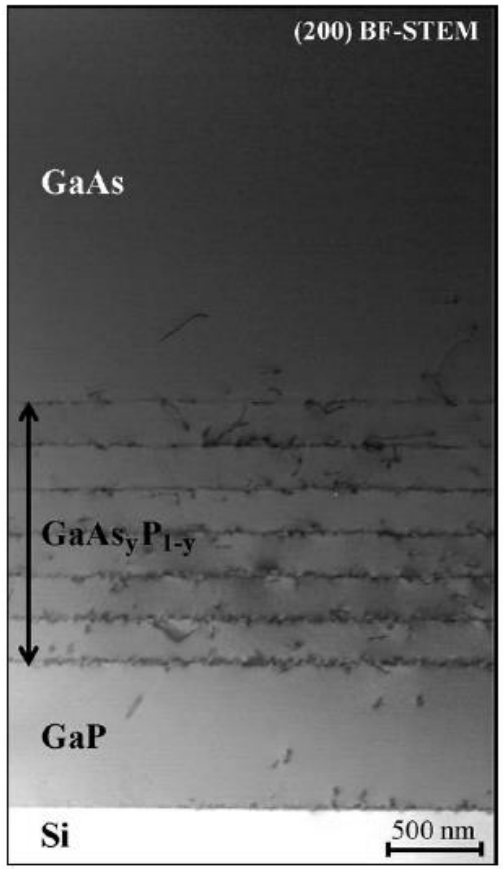
Off-cut substrates

Maximizes nucleation density



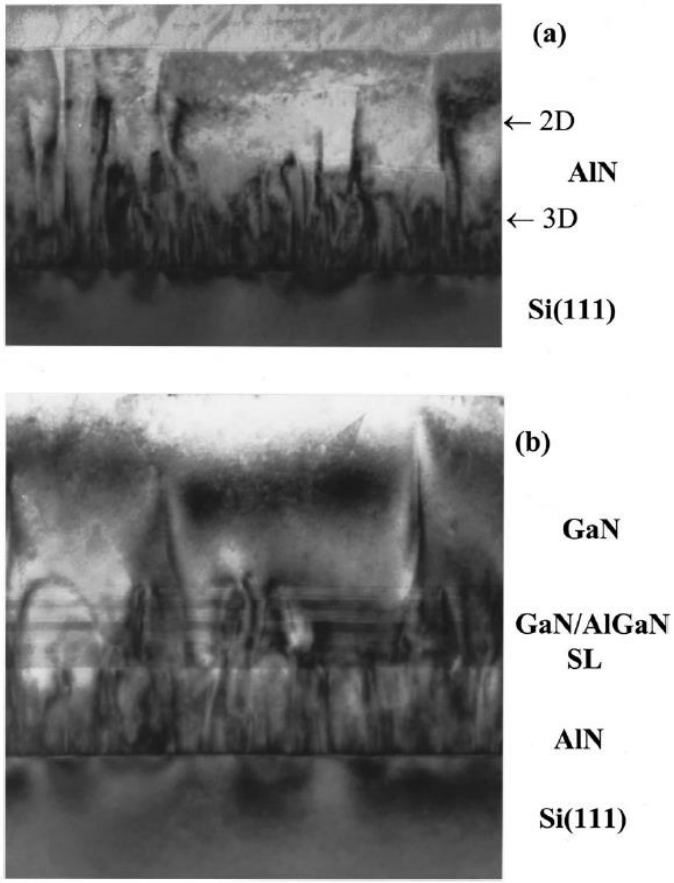
Fischer et al. JAP 1986

Graded buffers



Grassman et al. TED 2010

Superlattices

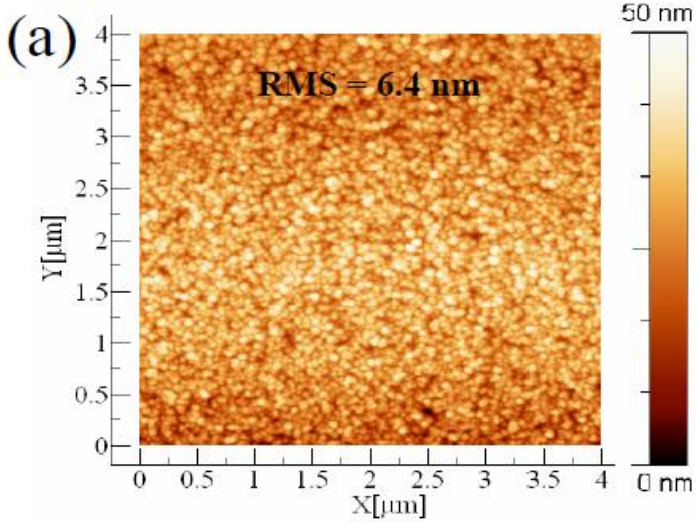


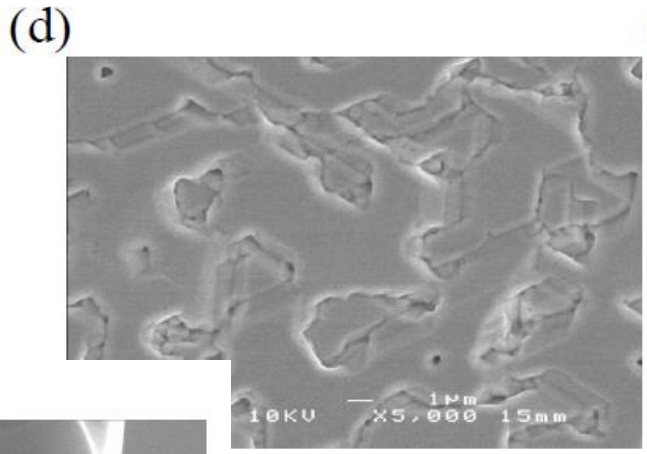
Nikishin et al. APL 1999

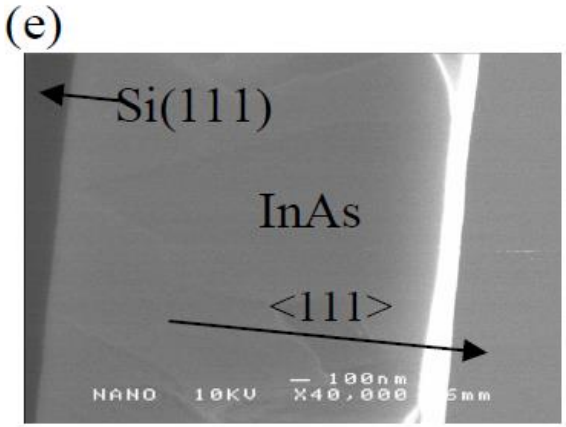
Two-step buffer

- **Nucleation step:** low temperature, high growth rate
  →Creates dense network of dislocated islands
- **Buffer step:** standard growth conditions to merge film

InAs on Si(111), nucleation @ 350 °C

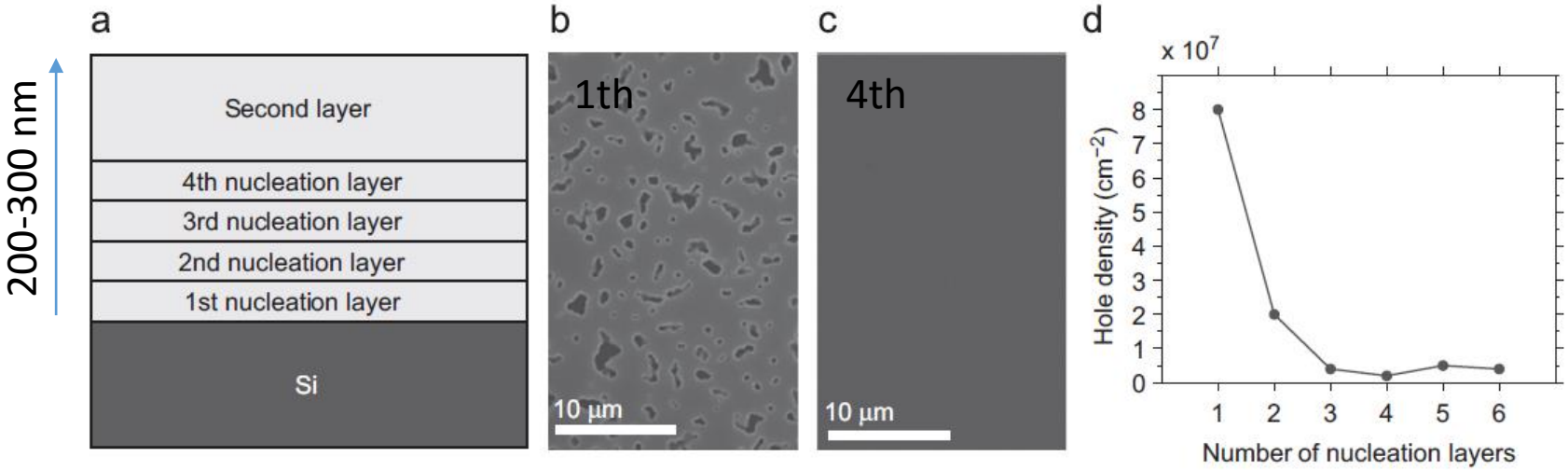


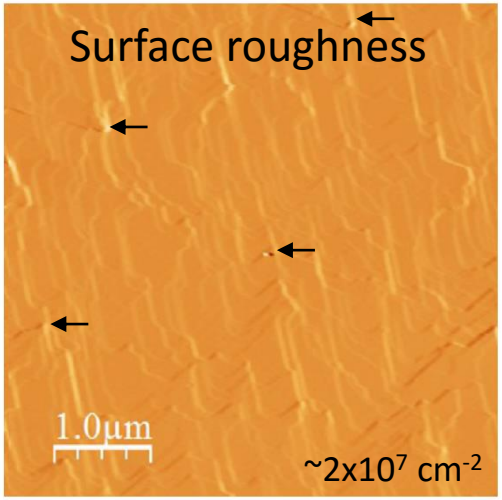




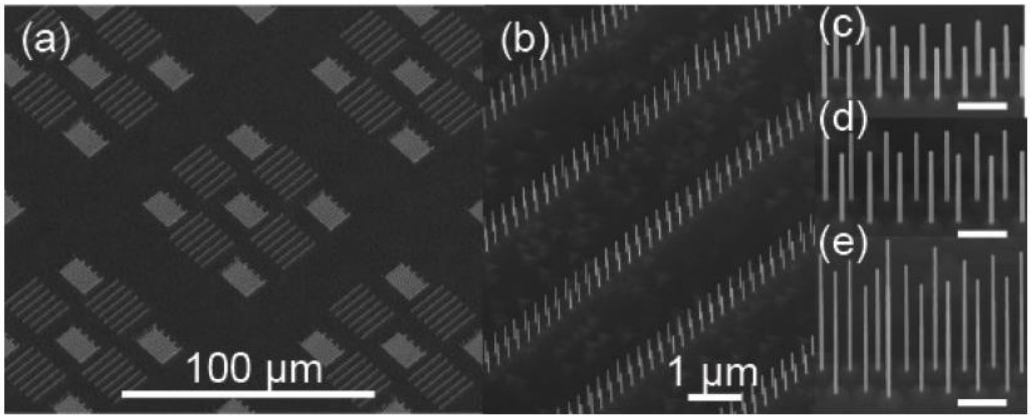
Multiple nucleation steps

Ghalamestani et al. JCG 2011

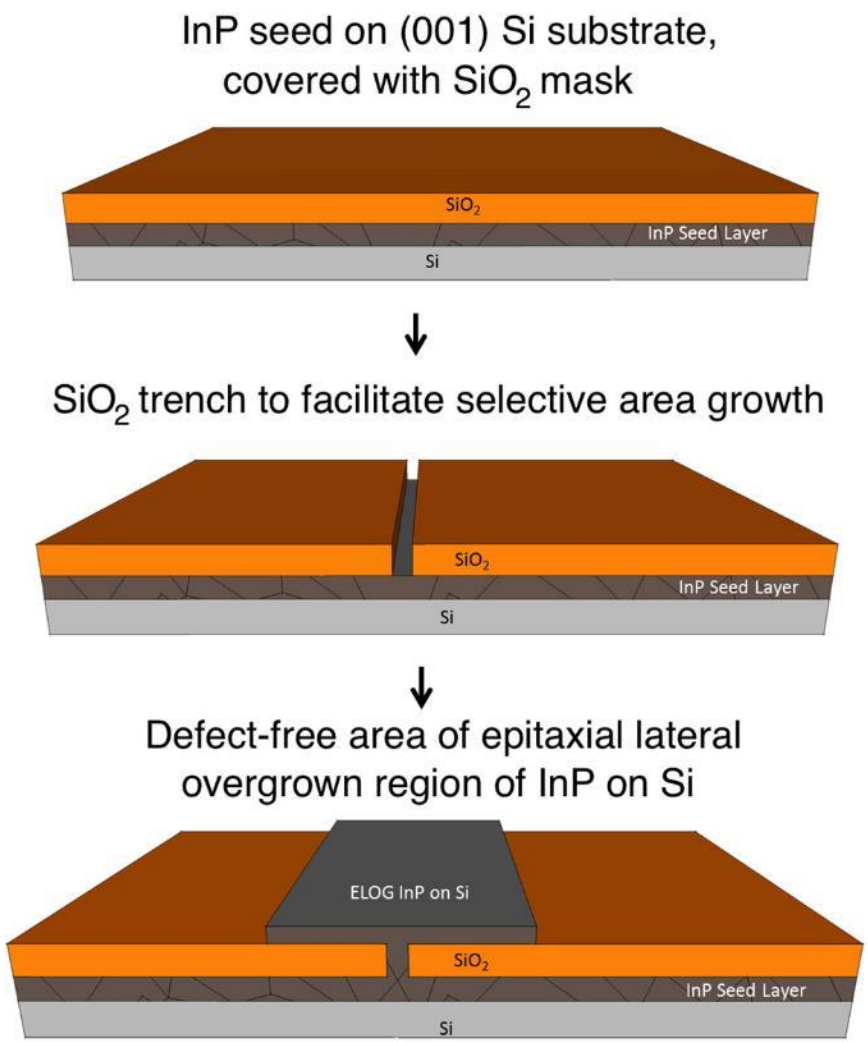


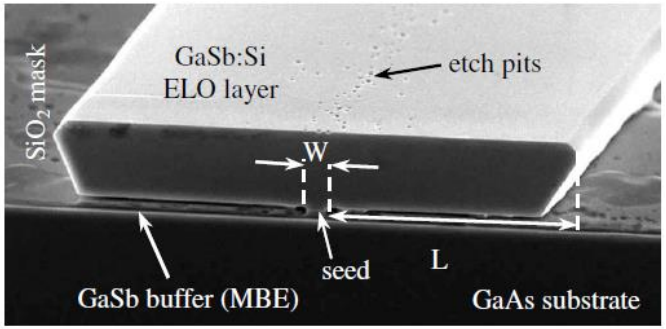


InAs nanowires grown on the InAs buffer



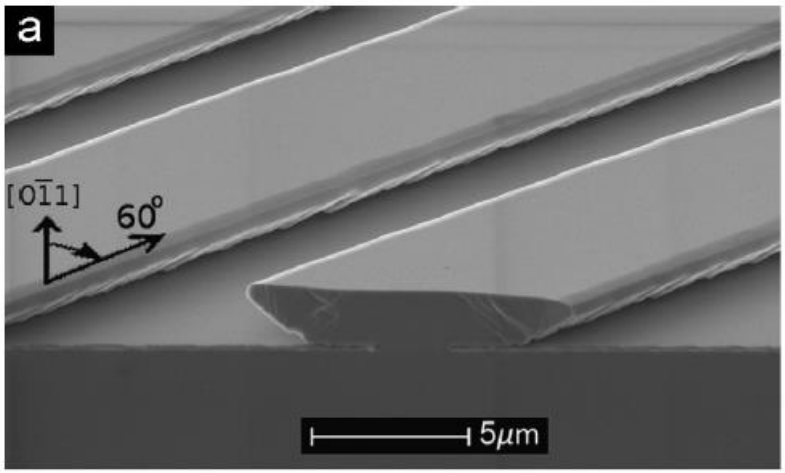
Epitaxial Lateral Overgrowth (ELO)

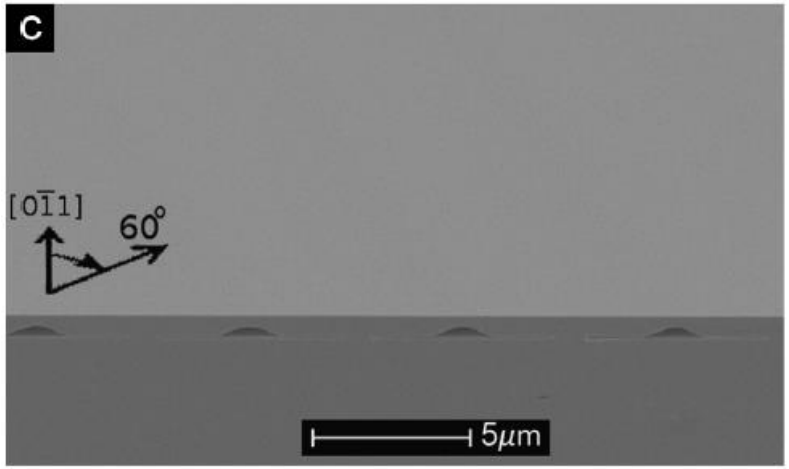


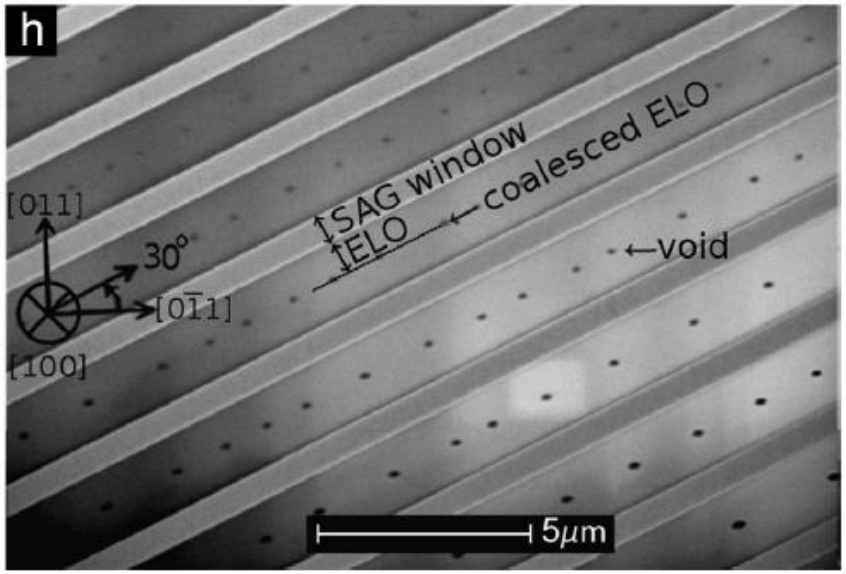


Wierzbicka et al. JAP 2009

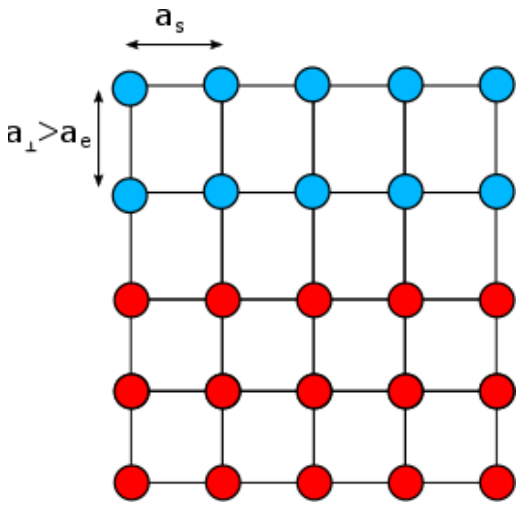
Problem of merging growth fronts

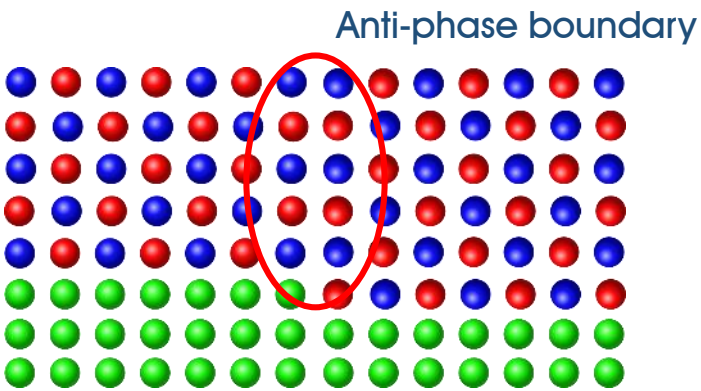




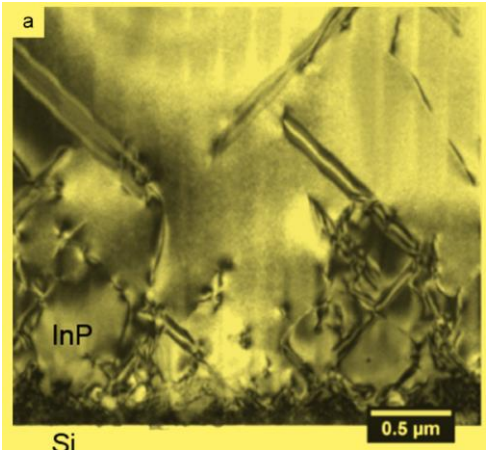


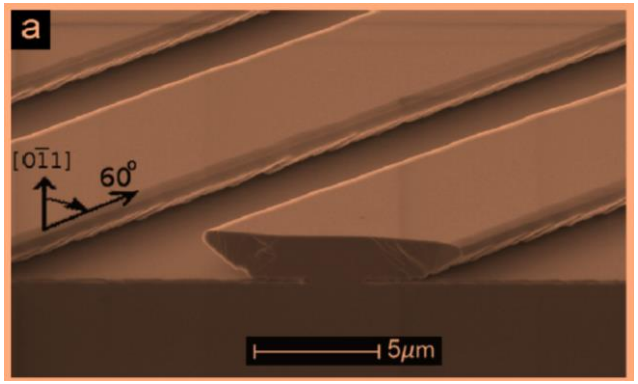
- Faceting can cause voids
- Crystal misalignment can cause defects





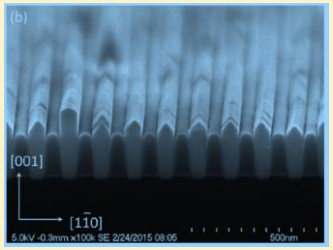
Break



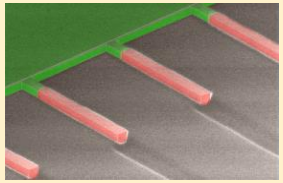


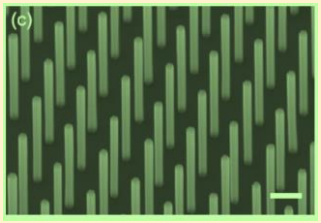
Epitaxial integration methods

Aspect ratio trapping (ART)

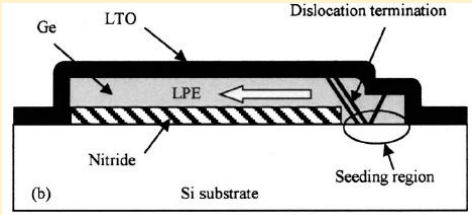


Template-assisted selective epitaxy (TASE)



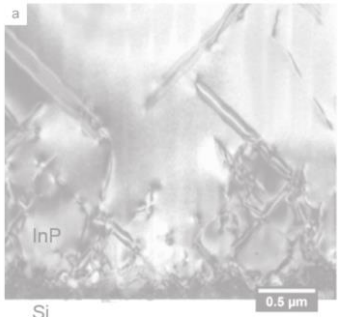


Nanowire epitaxy



Rapid Melt Epitaxy

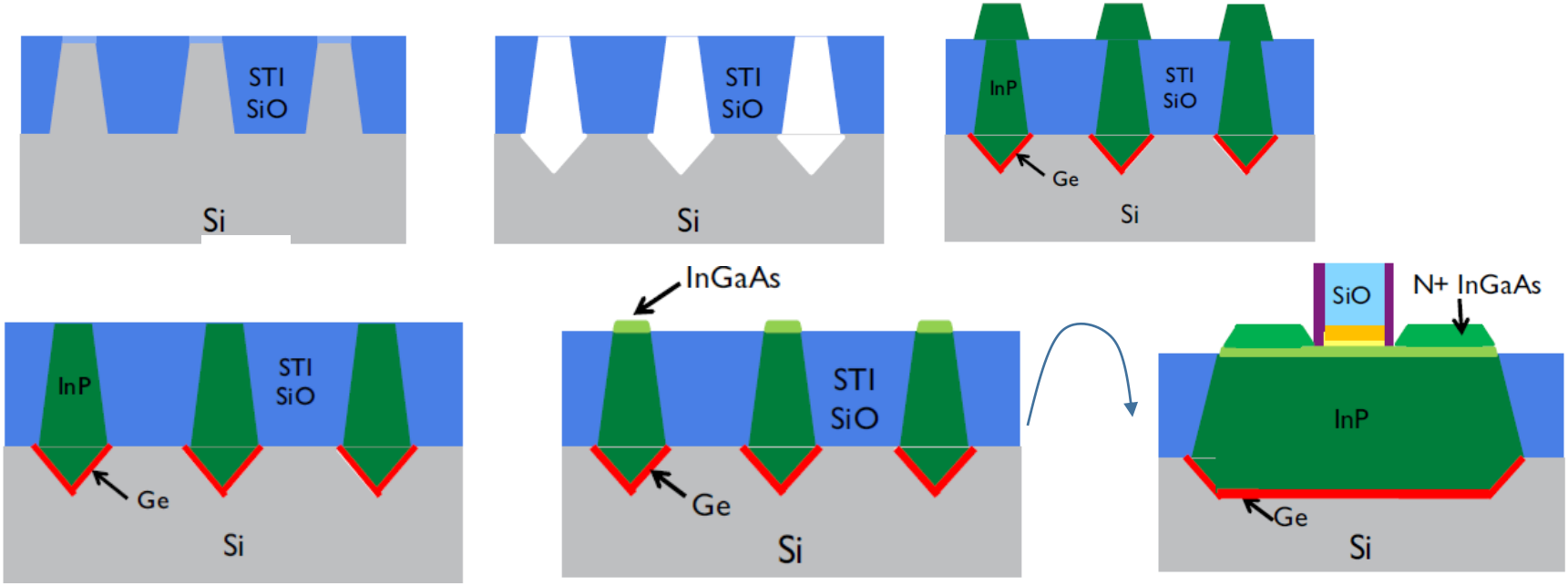
Epitaxial lateral overgrowth (ELO)



Buffer layer epitaxy

Aspect ratio trapping (ART)

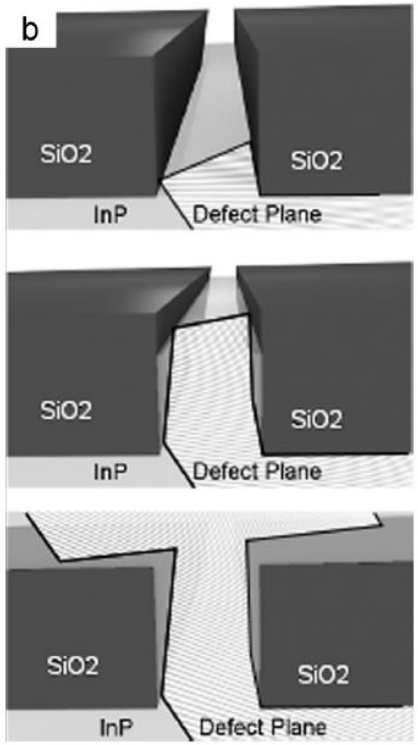
- Idea:
  - Based on ELO concept but no merging
  - High aspect ratio windows (trenches) to catch all defects
- Progress lead by IMEC, Sematech
- Completely compatible with Si CMOS fin processes (replacement fin)

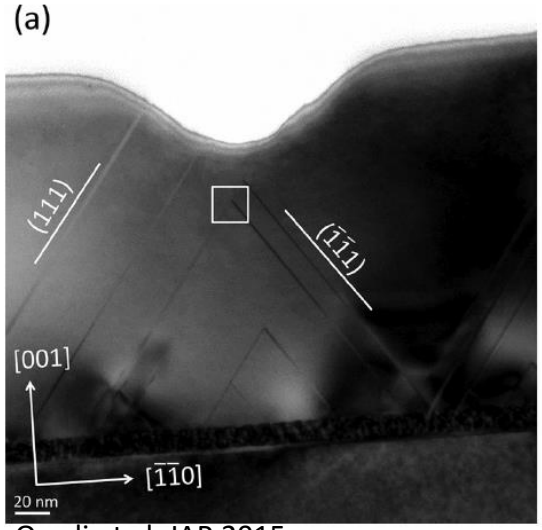


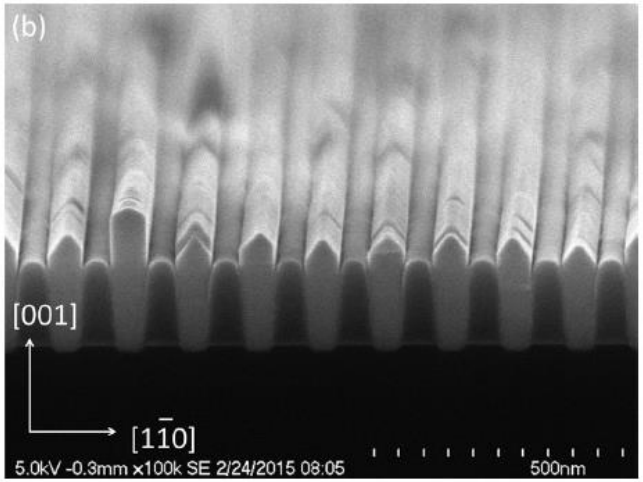
Defect ”trapping” in ART

- Defects (dislocation threading, twins, stacking faults) occur on (111) planes
- Defects across the trenches terminate on oxide
- Defects along the trench may not be trapped

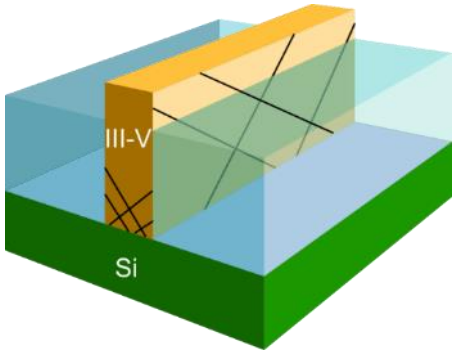
Julian et al JCG 2014





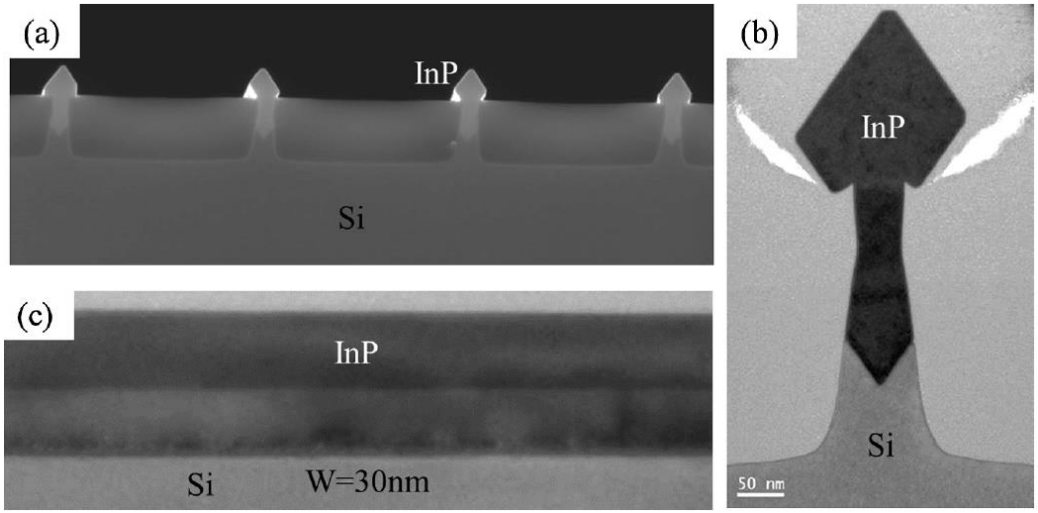


Orzali et al. JAP 2015

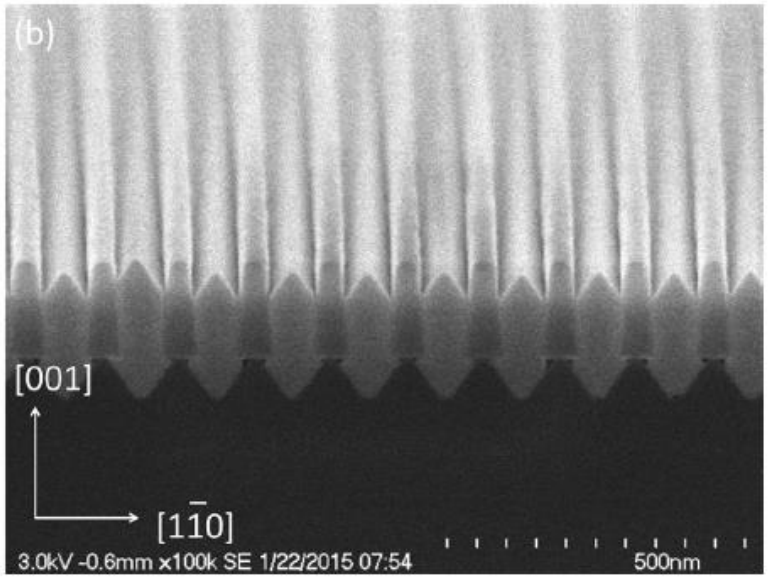


Latest status

- V-groove at bottom deemed crucial
- IMEC:
  - Two-step growth to create a dense twin network
  - Mg Counterdoping to increase resistivity in InP



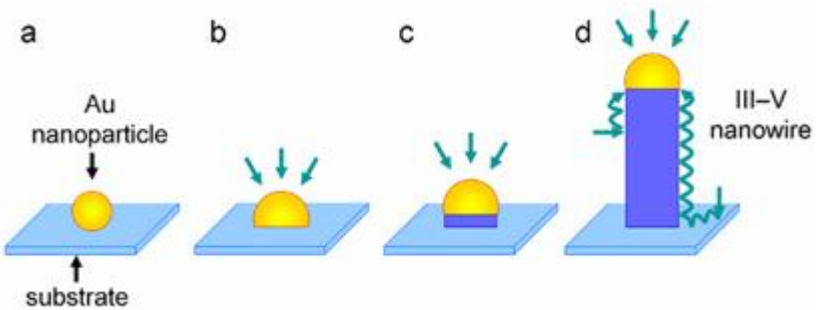
Waldron et al. SSE 2016 (IMEC)



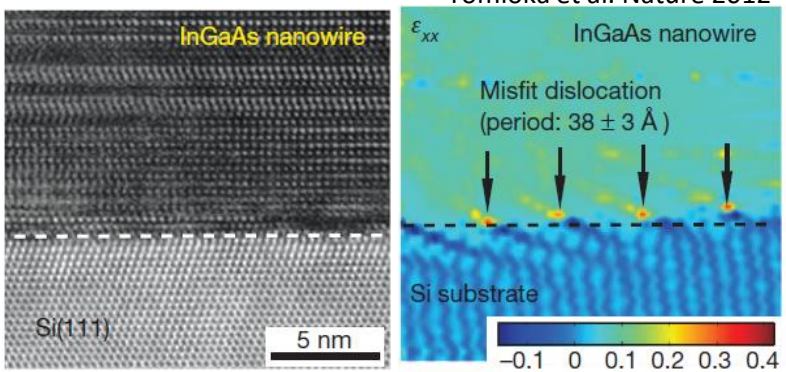
Orzali et al. JAP 2015 (SEMATECH)

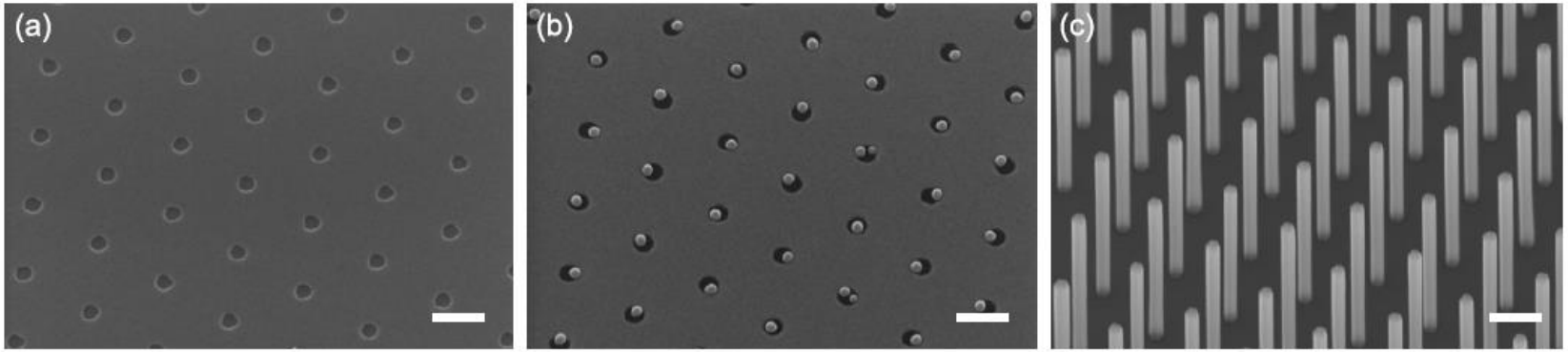
Nanowire epitaxy - VLS

- VLS – Vapour Liquid Solid
- Selective growth seeded by liquid particle
  - Extrinsic particle (Au, Ag, Al, Sn, ...)
  - Self-assisted (Ga → GaAs, In → InAs)
- Gives nanowire structures along [111]B (usually)
- Strain relaxation by
  - elastic relaxation at small dimensions (some claim)
  - Point contact to Si → Contained misfit dislocation network at heterojunction (observed)



Tomioka et al. Nature 2012

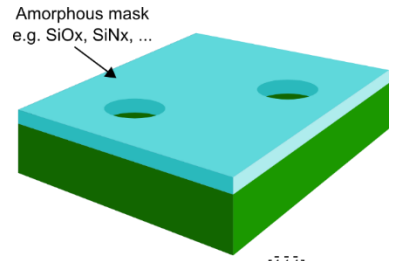


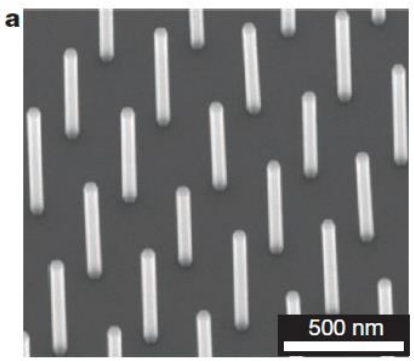


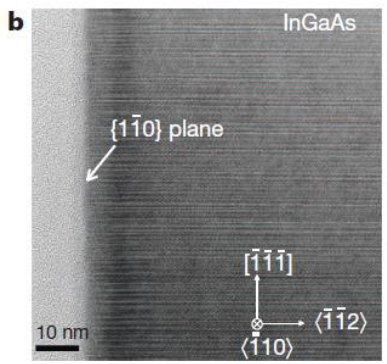
Plissard et al. Nanotechn. 2011

Nanowire epitaxy – Selective area

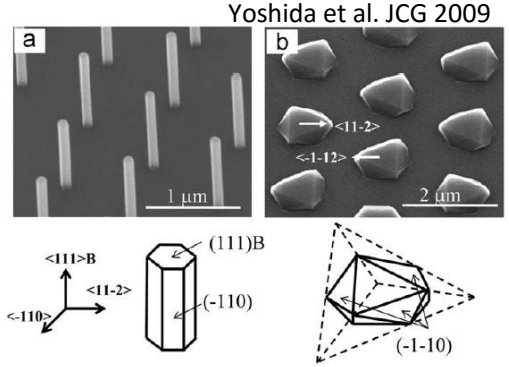
- No seed → abrupt junctions, CMOS compatible
- **Twin defects are necessary**!! → Prismatic crystal shape
  - (111)B top and {110} side facets
- Aspect rato given by growth rate anisotropy
- Excellent devices demonstrated by Hokkaido group

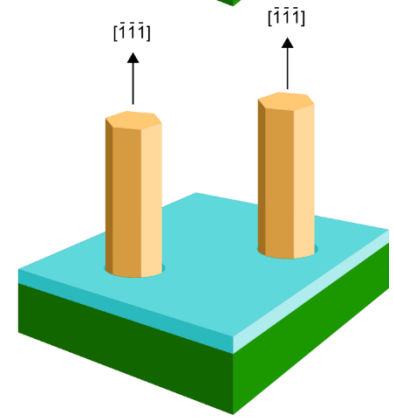


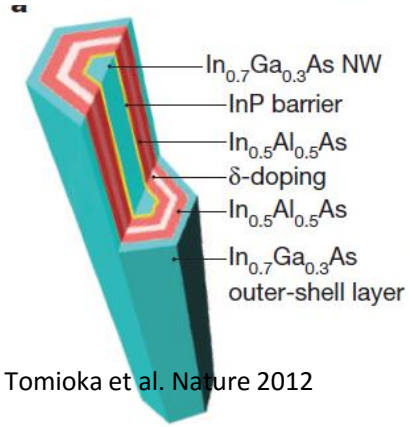




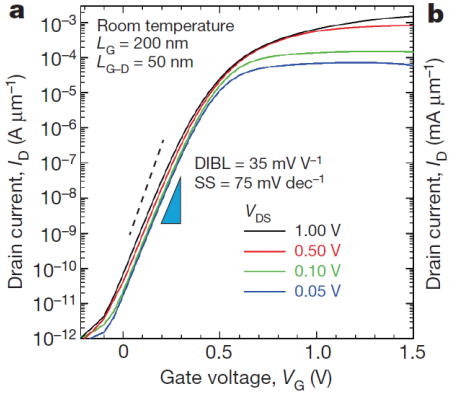
Yoshida et al. JCG 2009

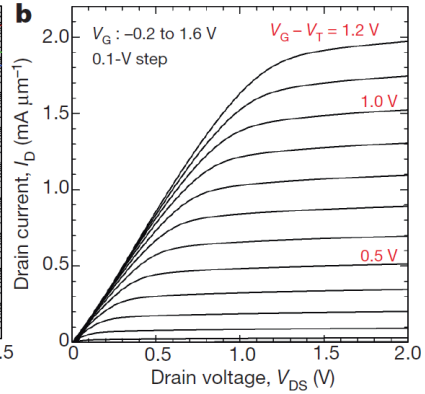


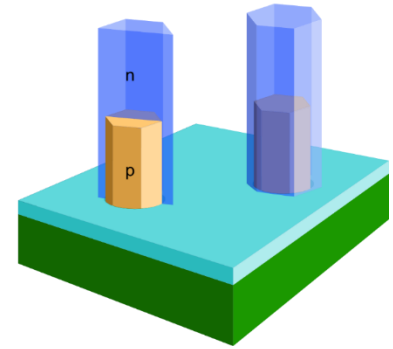




Tomioka et al. Nature 2012

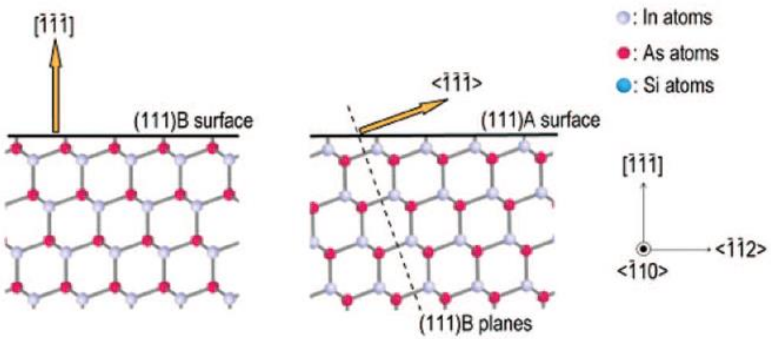


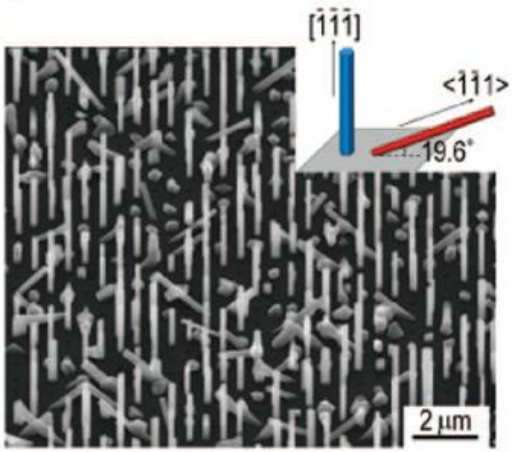




Limitations of nanowire epitaxy

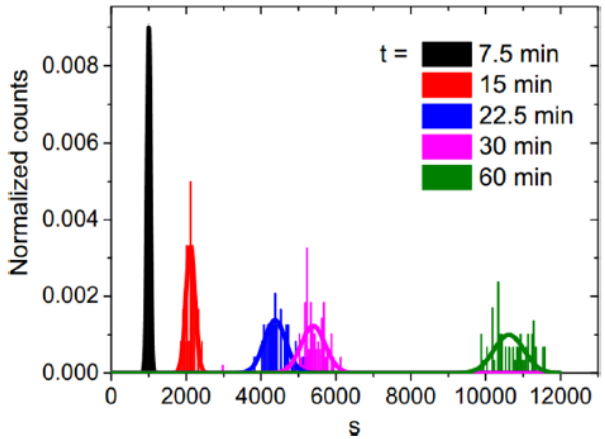
- Non-polarity of Si
  → Equivalent nucleation directions
- Vertical or inclined nanowire growth

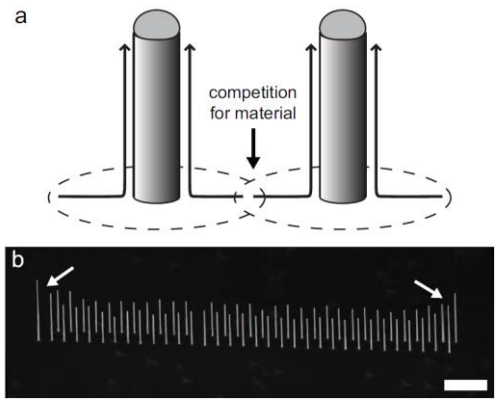




Tomioka et al. Nano Lett. 2008

Dubrovskii et al. CGD 2016



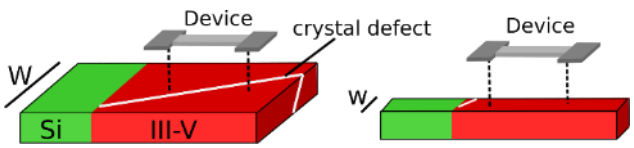


- Axial growth rate varies with
  - diameter
  - neighborhood
- Radial growth

→ Morphology variations

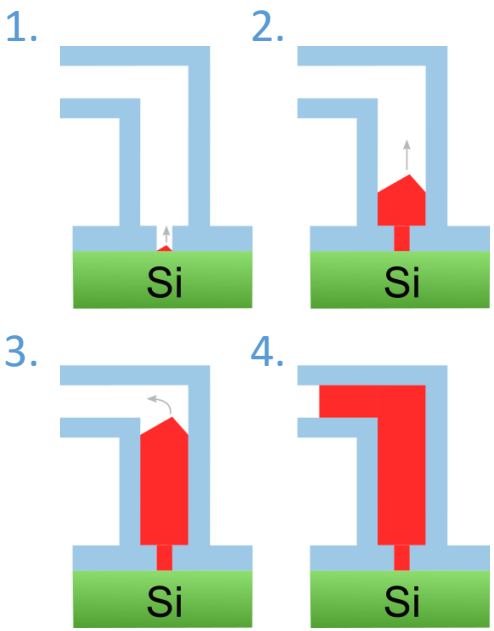
Template-Assisted Selective Epitaxy (TASE)

- **Developed by IBM**
- **Based on a combination of ELO, ART and nanowire concepts**



Key concepts:

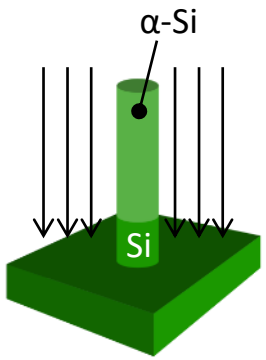
1. Limit epitaxy to start from a **single nucleation point**
2. Assist the crystal growth to desired shape by confining epitaxy within an **oxide template**.



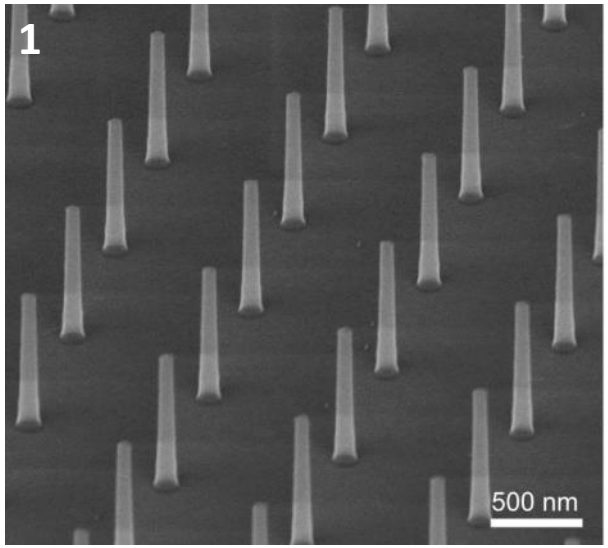
Benefits:

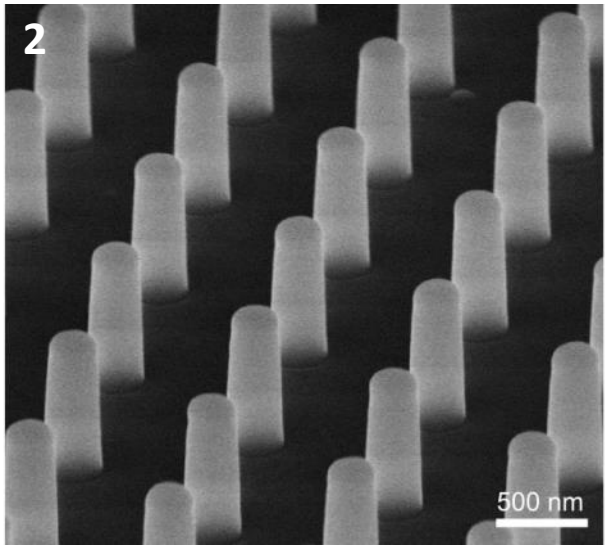
- **Avoids typical crystal defects** (anti-phase boundaries, dislocations)
- Allows for **precise control** of crystal morphology
- Allows for **in-plane heterostructures**, co-planar with Si
- **Wide range of materials** possible (arsenides, phosphides, nitrides, antimonides, ...)

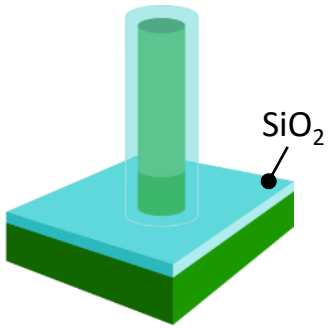
Vertical nanowire TASE process



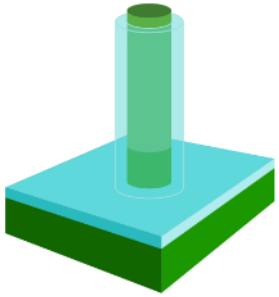
Etch out sacrificial NW



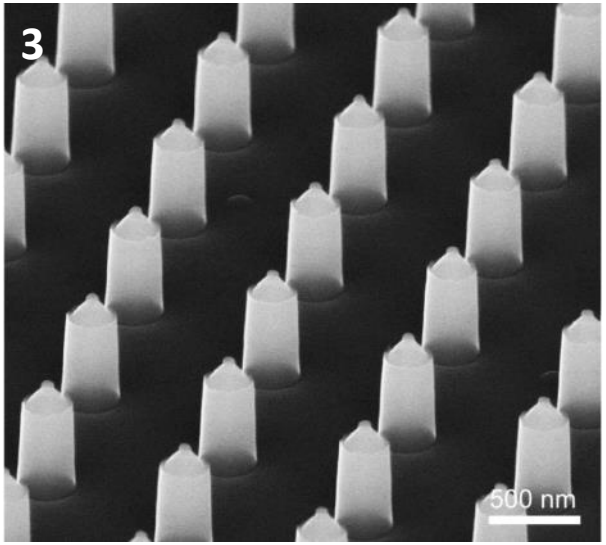


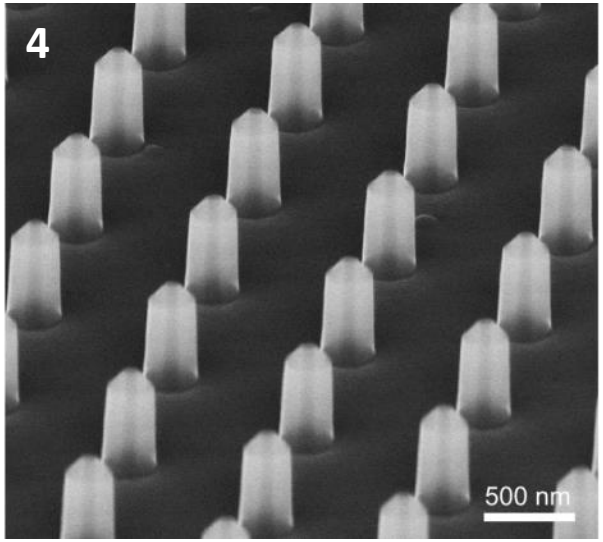


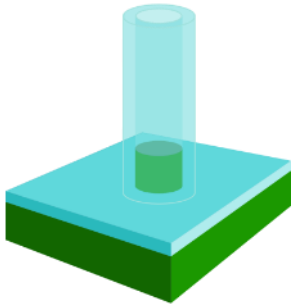
Deposit conformal SiO_2



Open template top

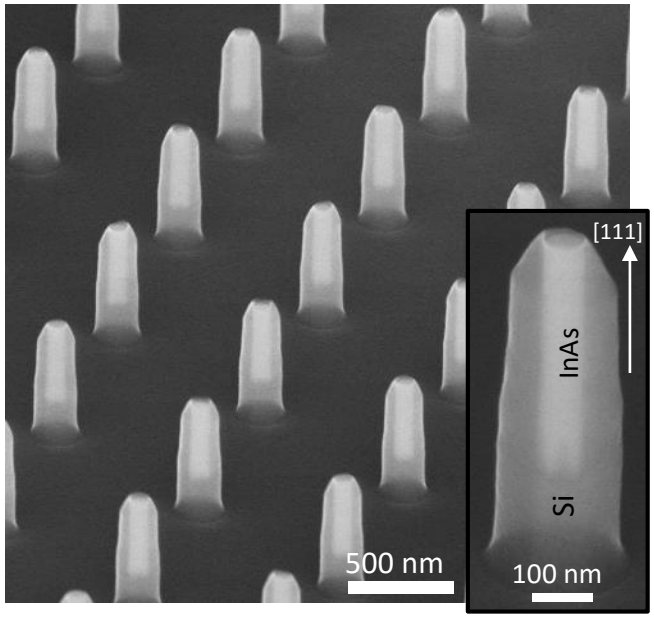




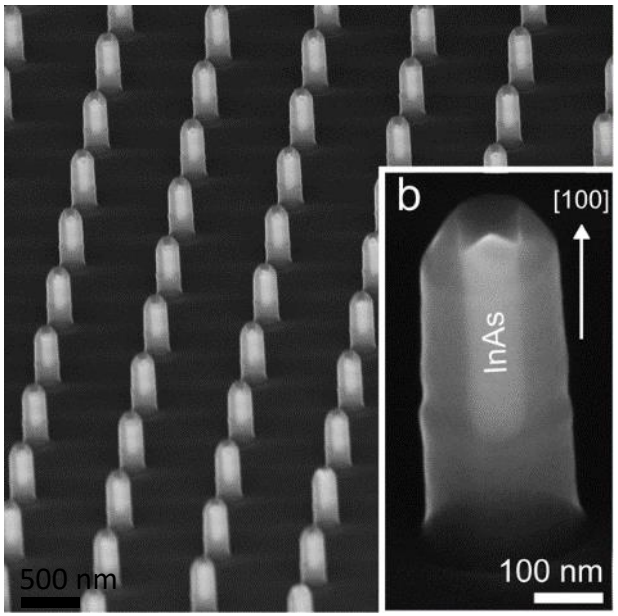


α-Si selective wet etch

InAs on Si(111)



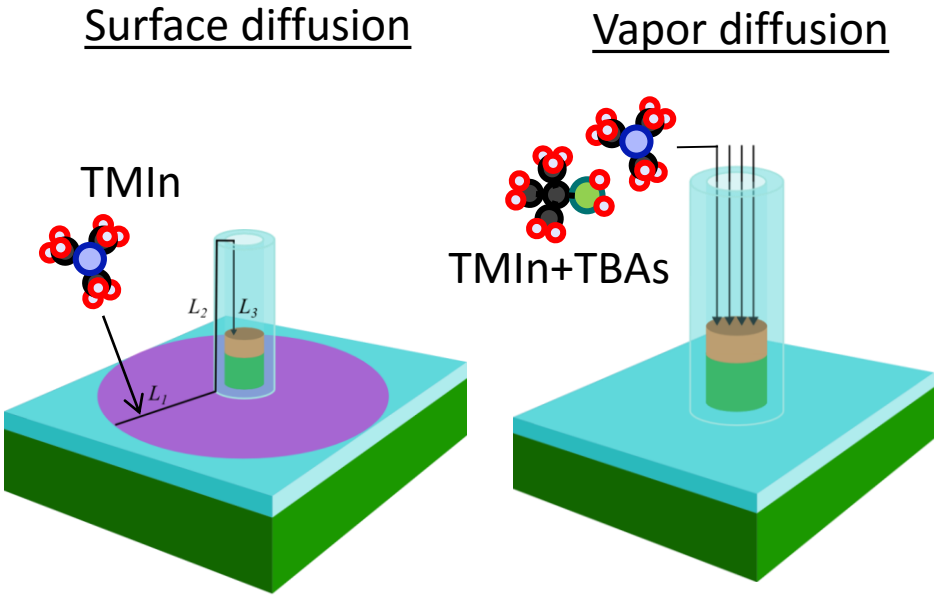
InAs on Si(001)

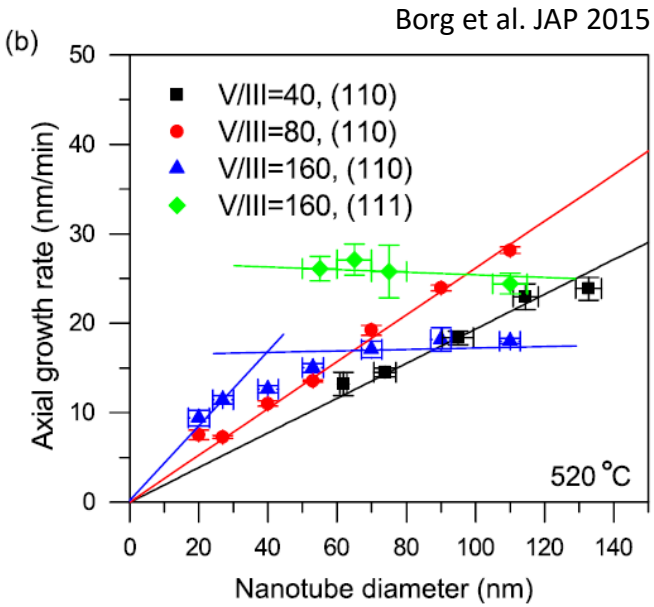


📖 Borg et al. Nano Lett. 2014

- **Selective** InAs growth on Si within nanotubes.
- Nanowire growth is **conformal** to template walls.
- **Vertical direction** independent on substrate orientation.

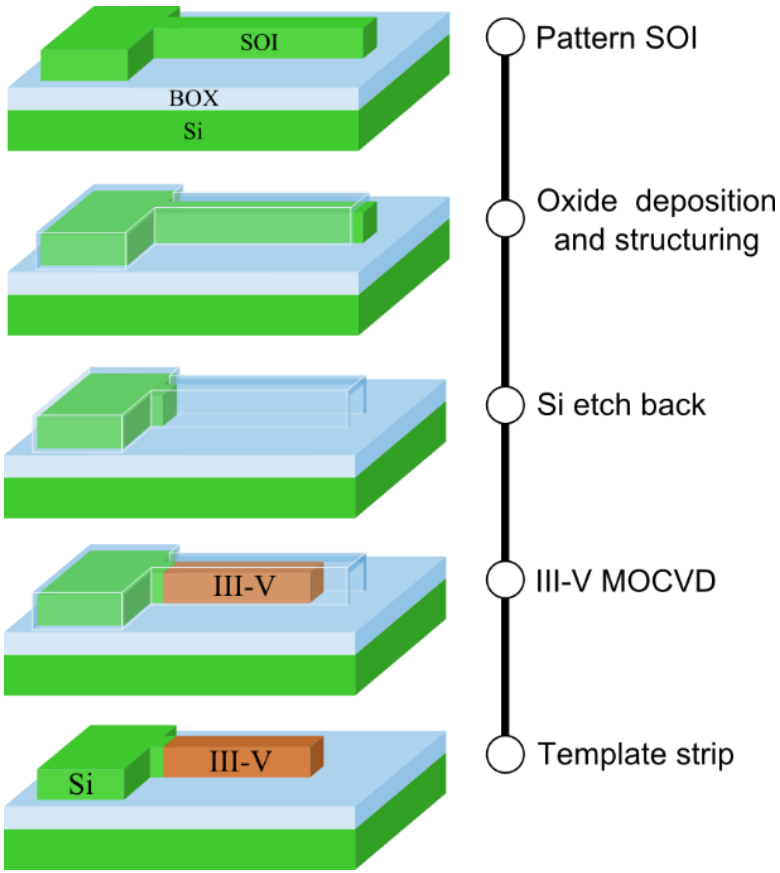
Effect of template on growth

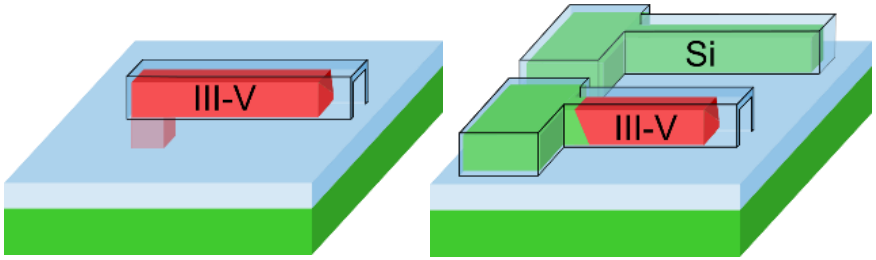




- Effectively lower As/In ratio in tubes
- Vapor diffusion less effective in smaller tubes
  → As/In reduces further in smaller tubes
  → Growth rate is affected

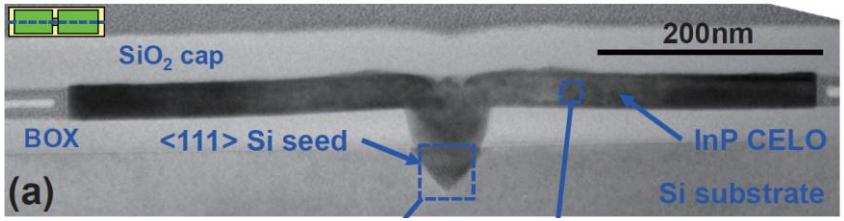
Horizontal TASE Process

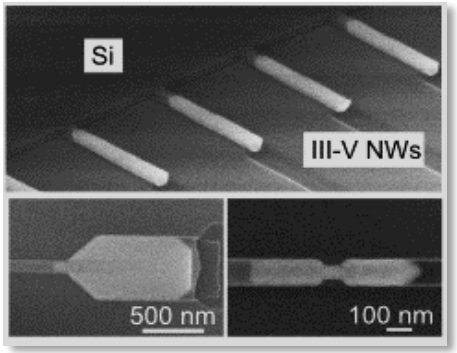


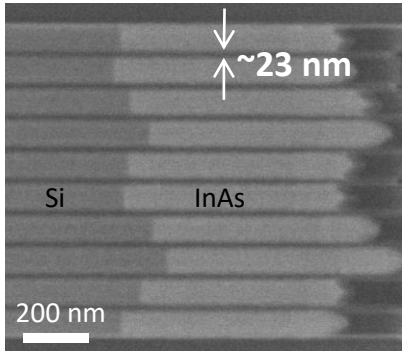


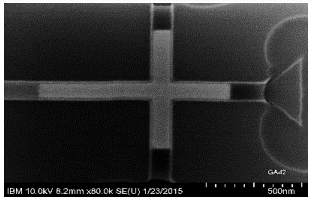
On bulk Si

Co-planar with Si





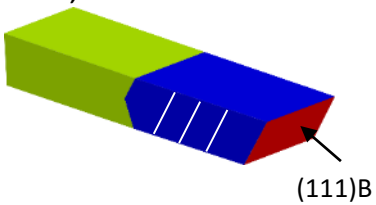




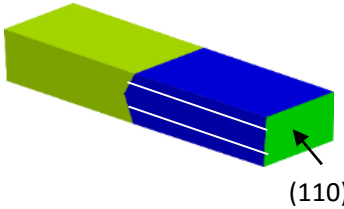
Material quality

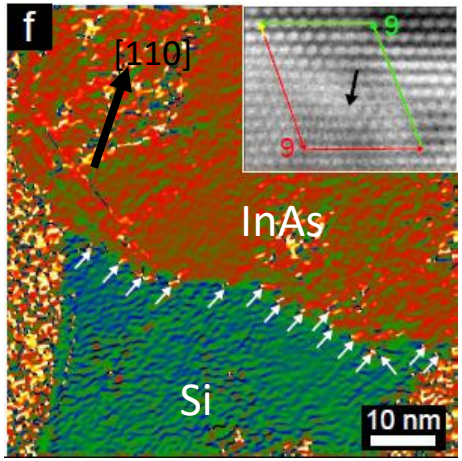
- Interface misfit dislocation network at Si/III-V junction.
  - Never have observed dislocation threading
- Crystal is predominately zinc-blende
- Twinning prominent in arsenides
  - Either across nanowire or along
  - Can be controlled by III-V ratio and T
- GaSb: Twin-free is possible

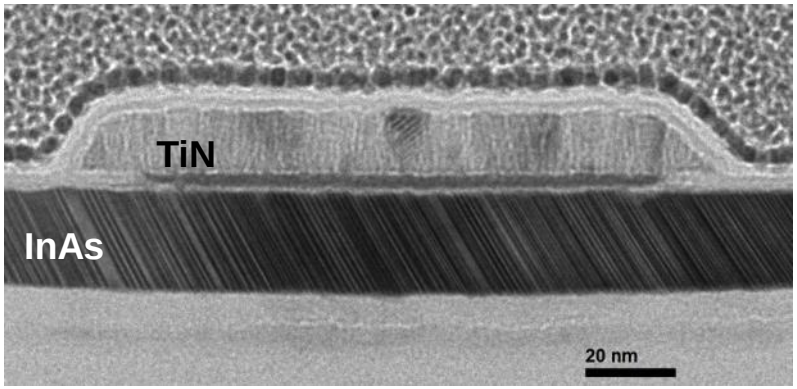
90%, twins across wire



10%, twins along wire







InAs finFET crossection

Schmid et al. APL. 2015, Schmid et al DRC 2015

Electrical quality

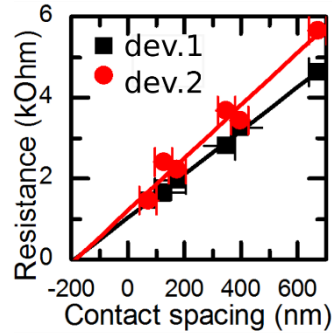
- TASE allows for growth of complex nanostructures
  → Ideal Hall devices are possible
- Electrical evaluation of 23 nm thick InAs nanostructures
  - Transmission line measurements and Van der Pauw/Hall
- Hall setup:
  - +/- 0.1 T (permanent magnet)
  - Pressure 5×10^{-4} mbar

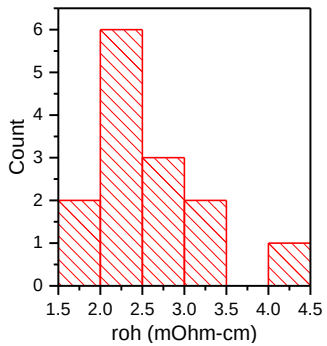
TLM

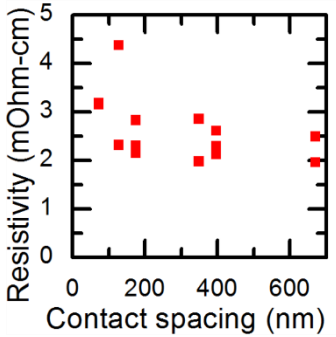
$\rho_c = 9.5\times10^{-8}$ Ohm·cm^2
$\langle\rho\rangle = 2.89$ mΩcm
$\langle R_{sheet}\rangle$ = 1257 Ohm/sq

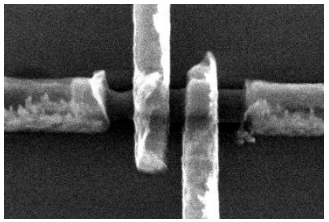
VDP → **R_{sheet} = 1281 Ohm/sq**
$V_H = -171$ µV → $n = 3.3\times10^{17}$ cm^{-3}
→ **μ_e ~ 5400 cm^2/Vs**

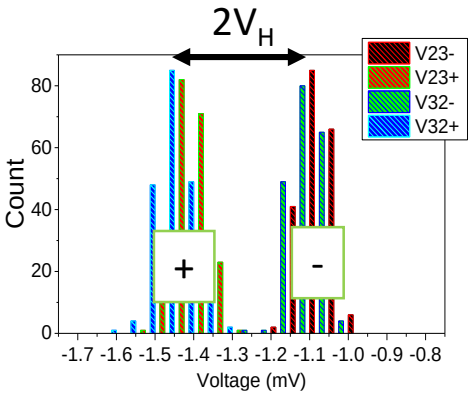
Compares well. Surface-limited

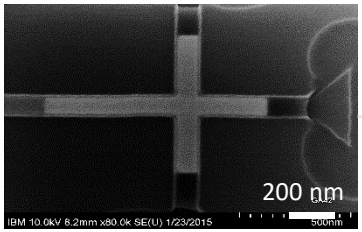


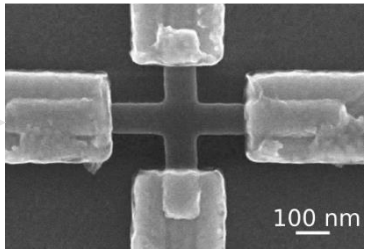






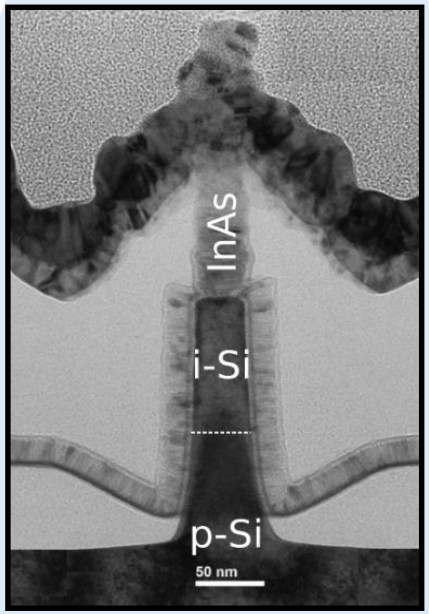


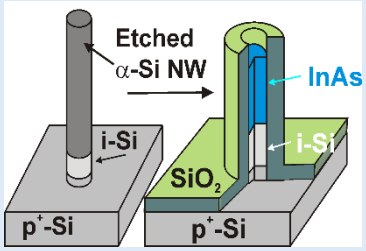


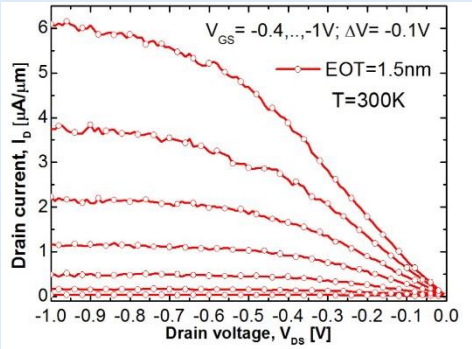


Device implementations

Vertical Tunnel Field effect-transistors





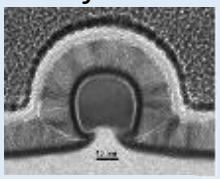


Cutaia et al. J-EDS 2015
Cutaia et al. ULIS 2015

- I_{on} = 50 μA/μm (V_{DS}=1 V)
- $I_{on}/I_{off} = 10^6$
- SS = 150 mV/dec

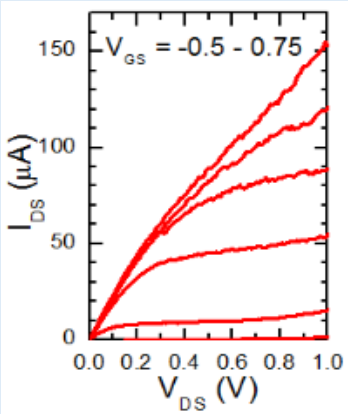
finFETs for III-V CMOS

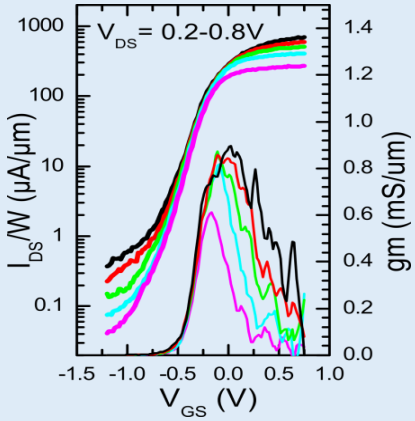
InAs fin



23x25 nm

- I_{on} = 480 μA/μm (V_{DS}=0.5V)
- g_m = 0.9 mS/μm (V_{DS}=0.5V)
- μ_{FE} ~ 500 cm^2/Vs
- SS = 250 mV/dec



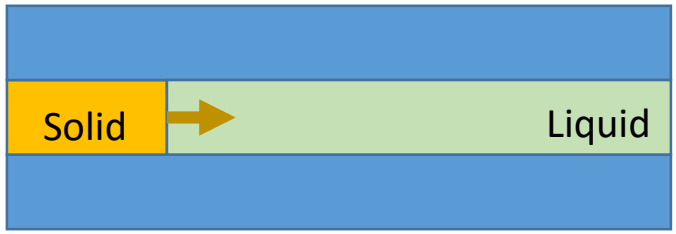


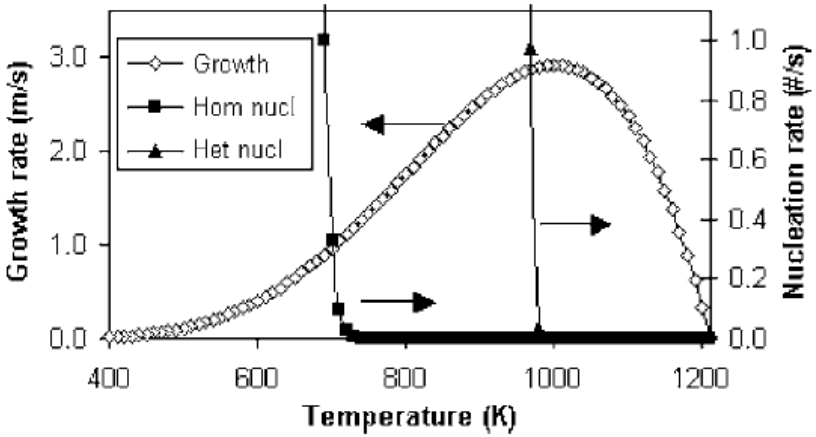
Schmid et al. APL 2015

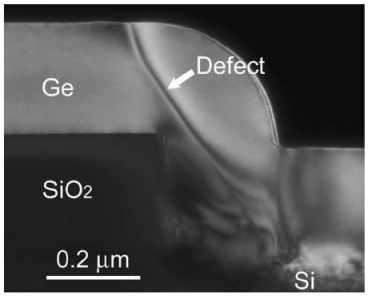
Performance at this point limited by device processing, not materials

Rapid Melt Epitaxy

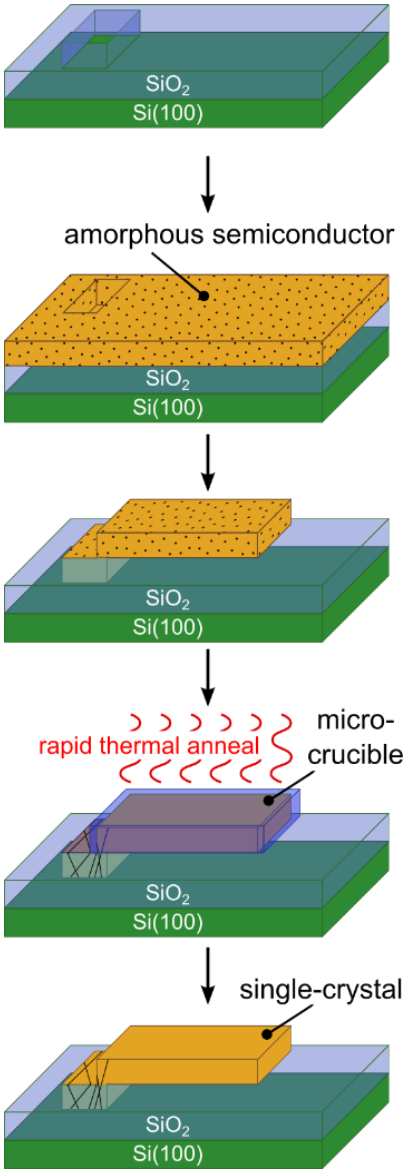
Pioneered by Stanford (Plummer group)



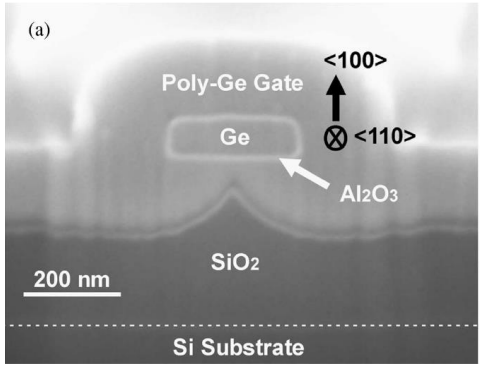




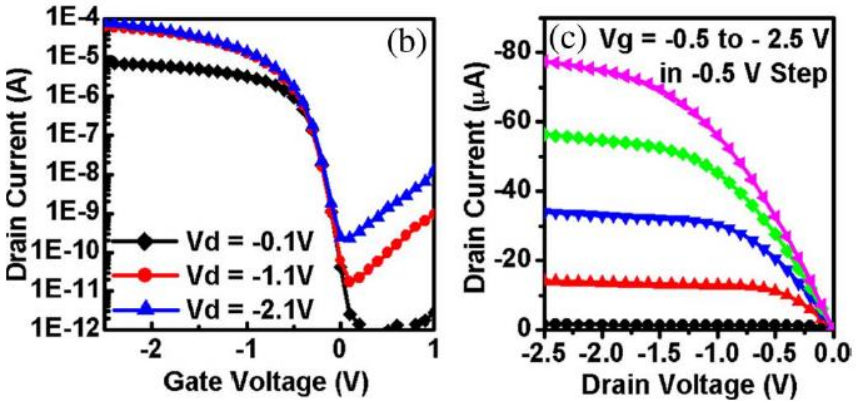
Feng EDL 2006

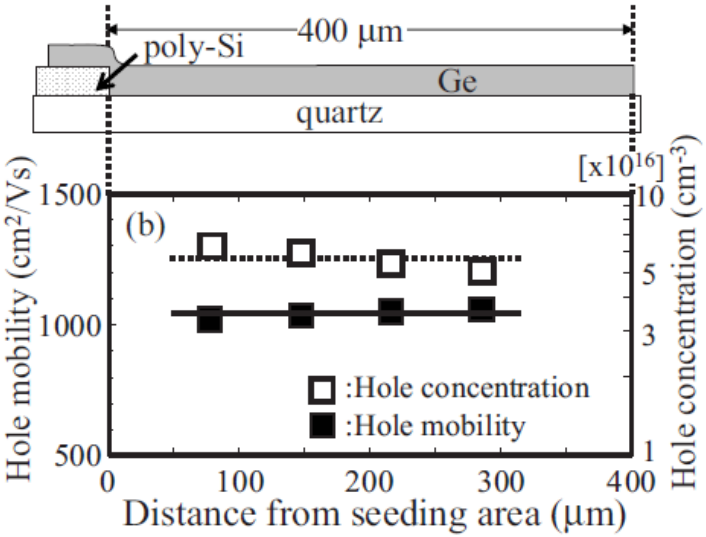


Ge Rapid Melt Epitaxy



Feng EDL 2008



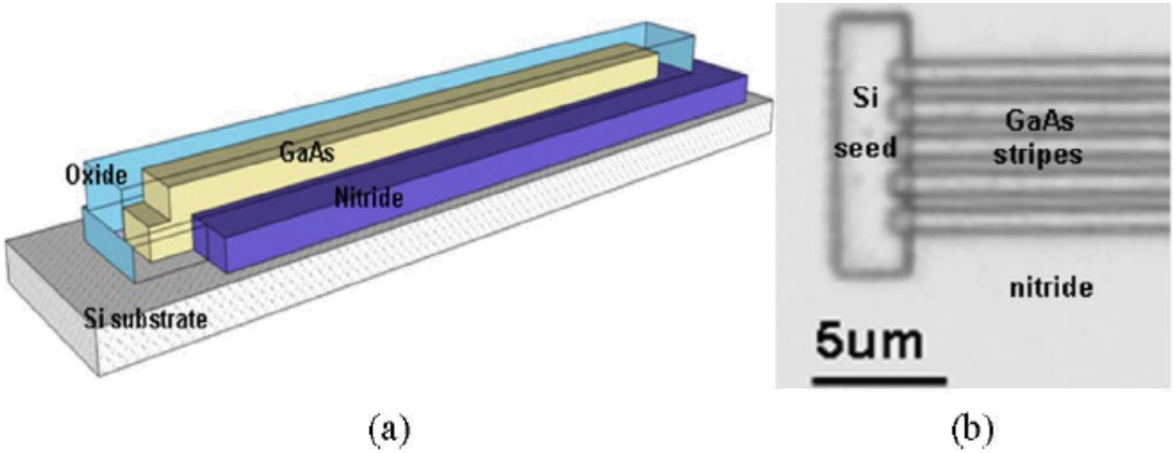


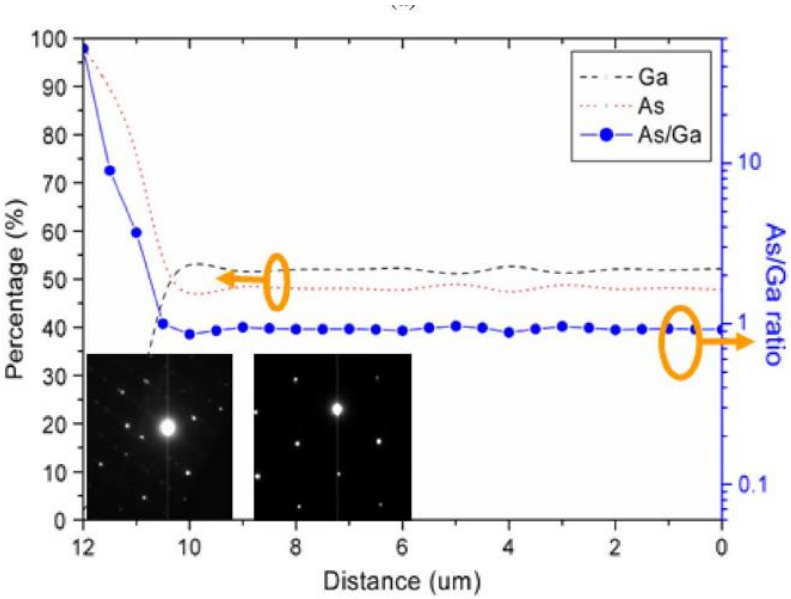
Miyao APL 2009

III-V RME

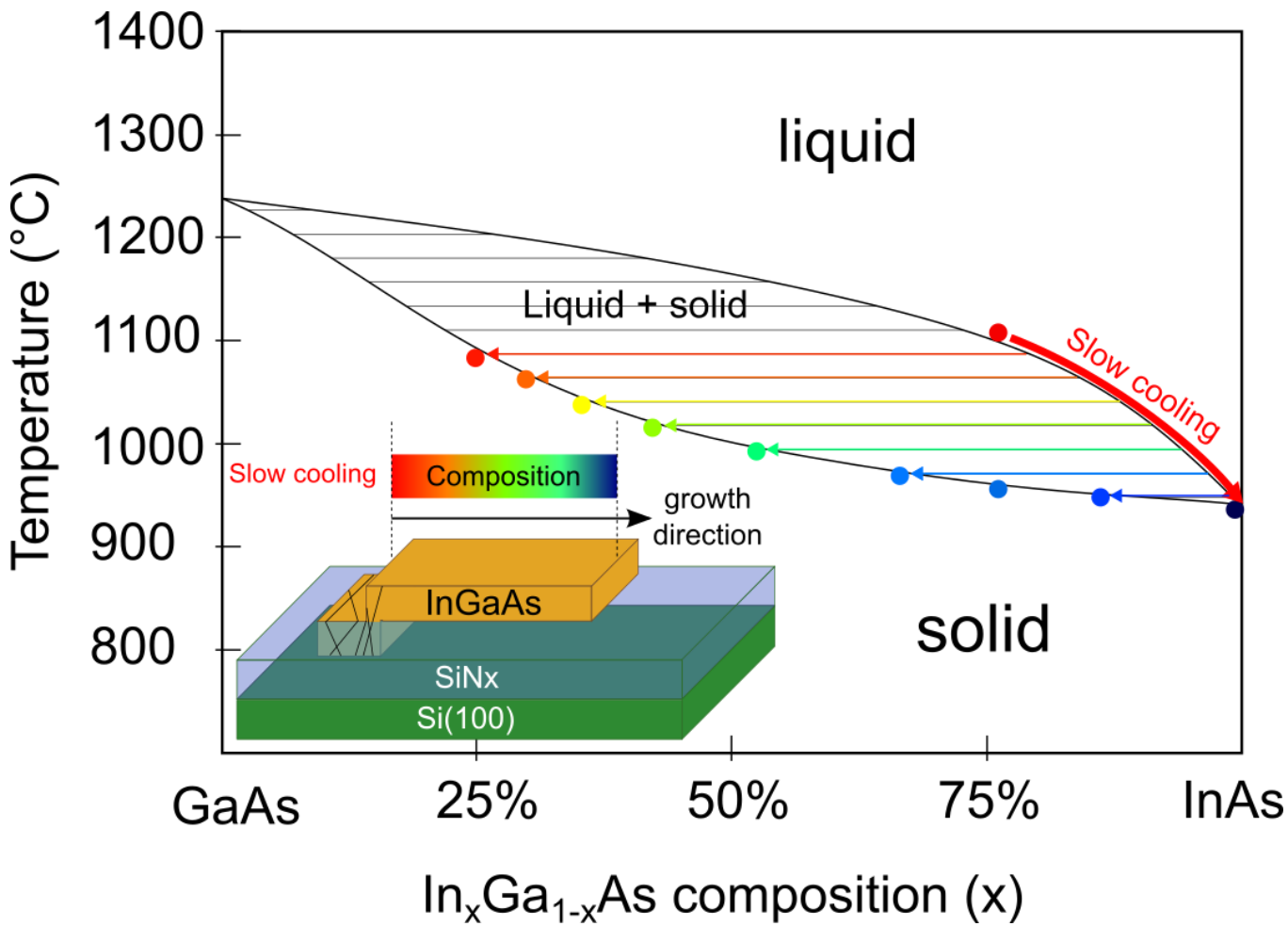
Chen (Plummer) EDL 2010

- Deposited Ga-As was As-rich
- After RME the material was stoichometric
- Excess As pushed to end
- ρ_{GaAs} = 20 mOhm-cm
  - i.e. Si background doping!



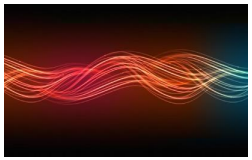


Ternaries in RME



The future

Integrated III-V Comm/Optical/Quantum technology



Si CMOS technology