Metal-oxide-semiconductor field effect transistors (2 lectures)

MOS physics (brief in book)

Current-voltage characteristics

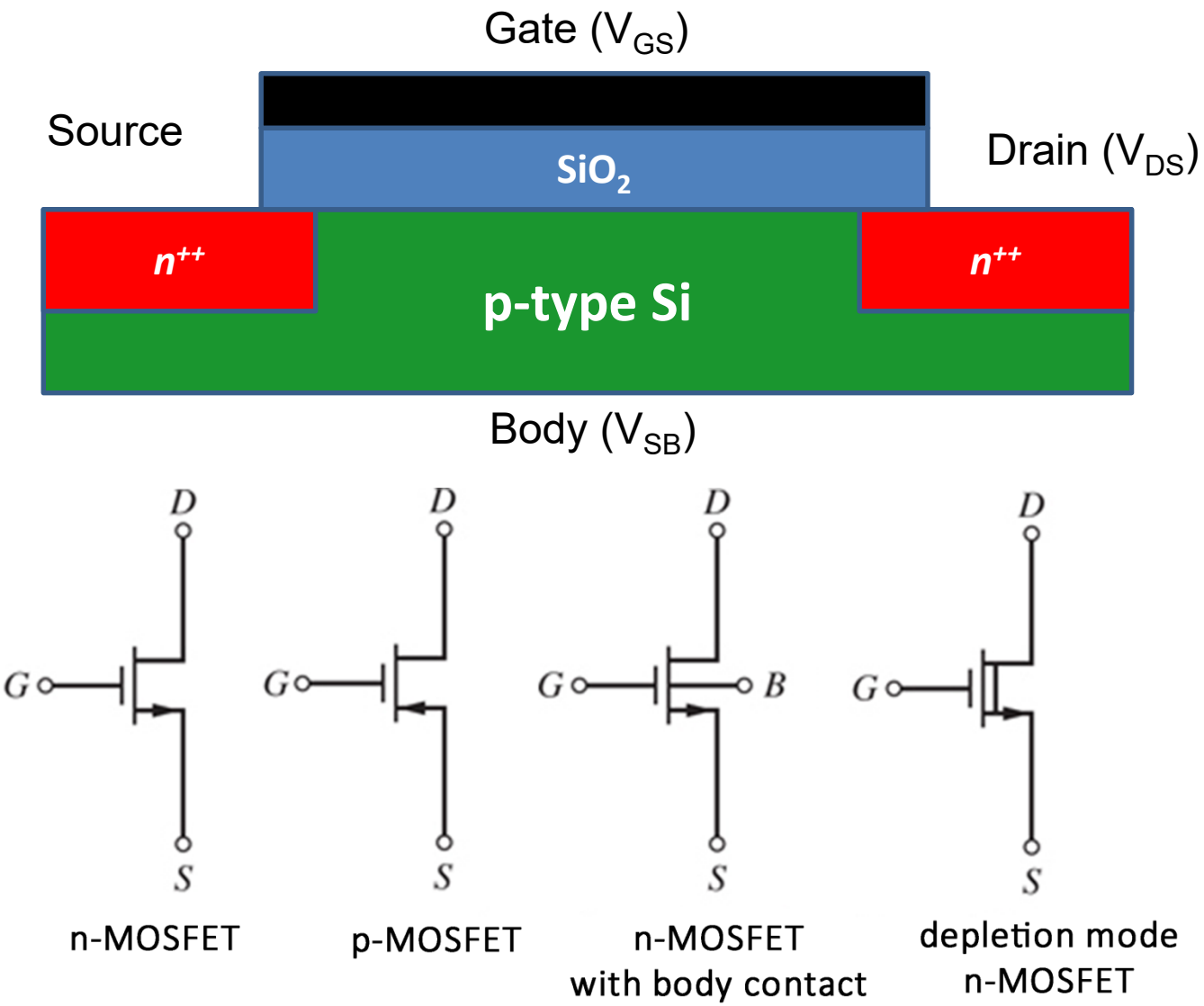
- **pinch-off / channel length modulation**
- **weak inversion**
- **velocity saturation**
- **metrics extraction**

Capacitances

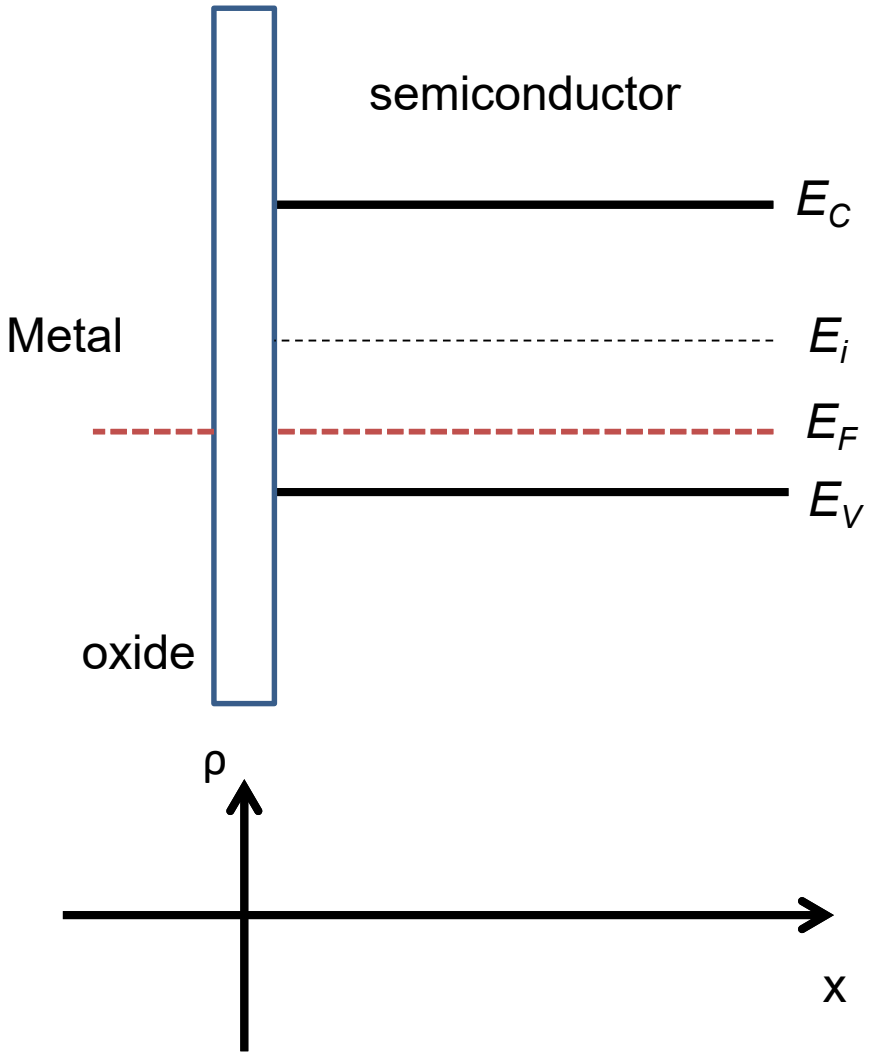
Small-signal model

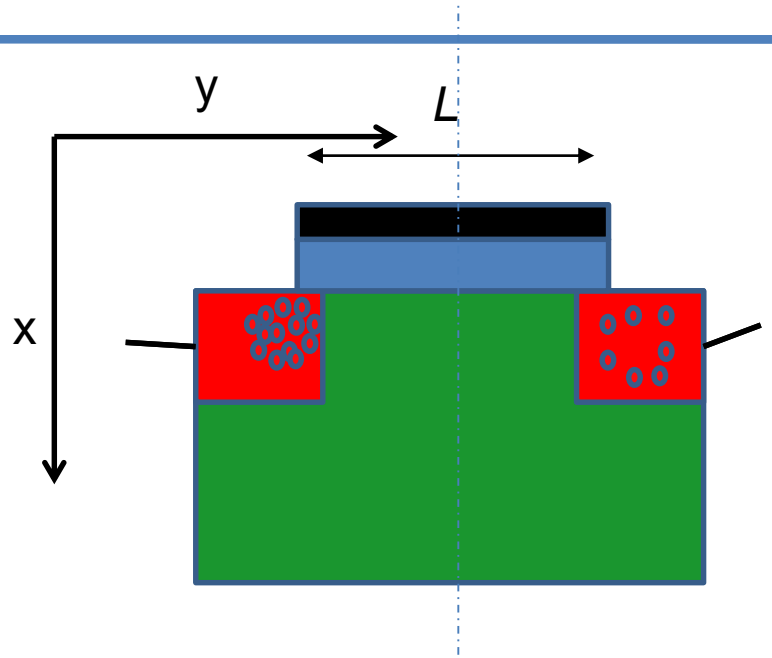
Reading: (Sedra, Smith, 7th edition)
5.1, 5.2, 5.3
5.4.3, 5.4.4
6.2.1 small signal model DC
9.2.1 small signal model AC

n-type MOSFET layout



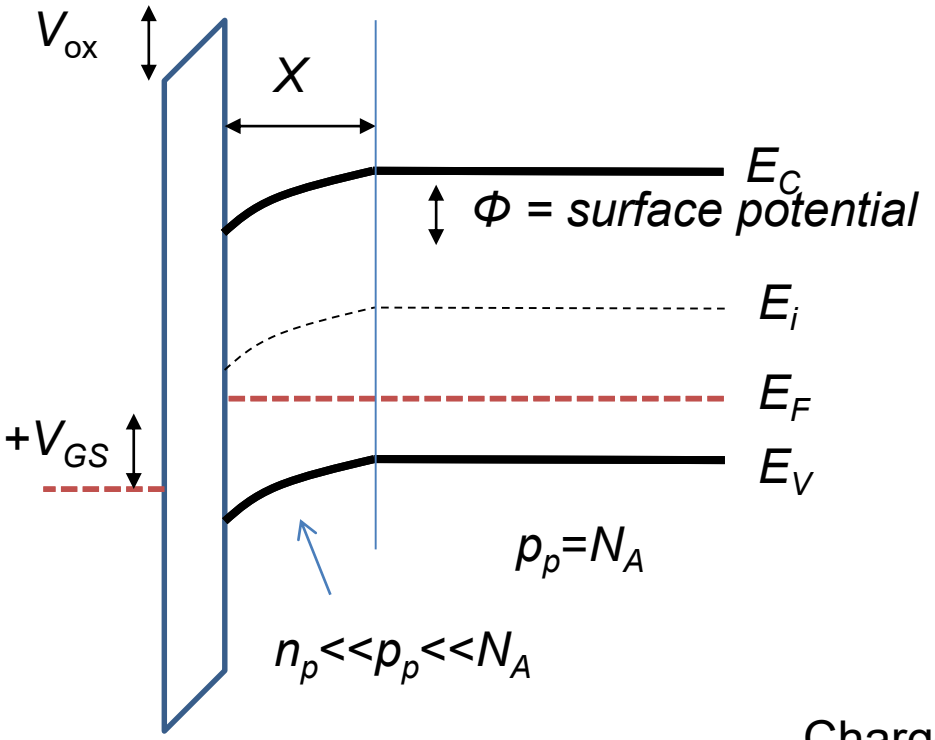
Energy bands 1 – flat band

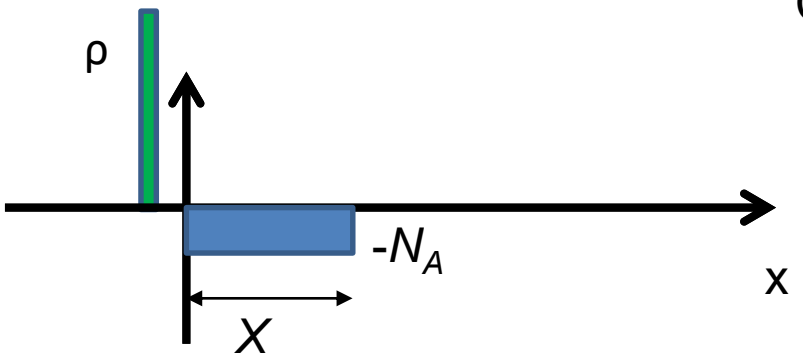


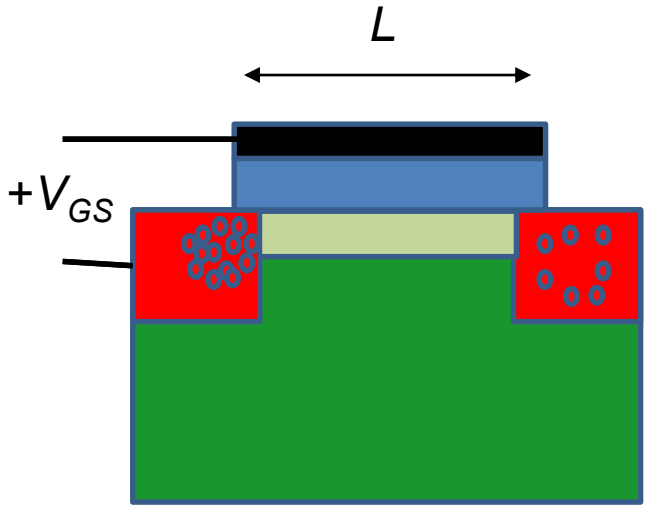


• Gate oxide has large band gap → no current. E_F constant in semiconductor

Energy bands 2 - depletion







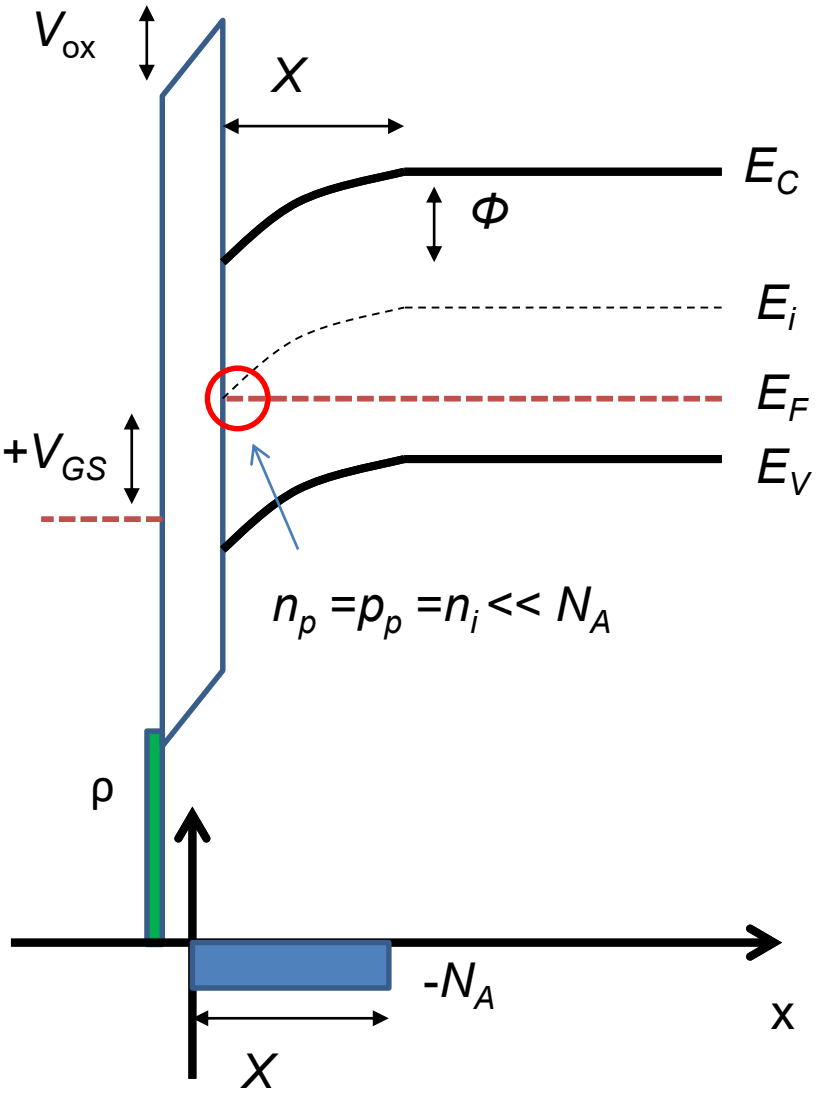
$$X = \sqrt{\frac{2 \cdot \varepsilon_s \cdot \varepsilon_0 \cdot \phi}{q \cdot N_A}}$$

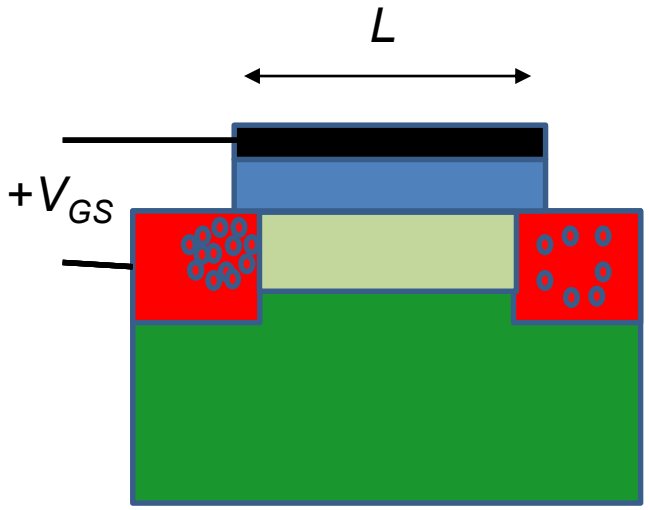
Charge per area: $Q = X \cdot N_A \cdot q$

$$V_{ox} = \frac{Q}{C_{ox}}$$

$$V_{GS} = V_{ox} + \phi$$

Energy bands 3 – intrinsic surface





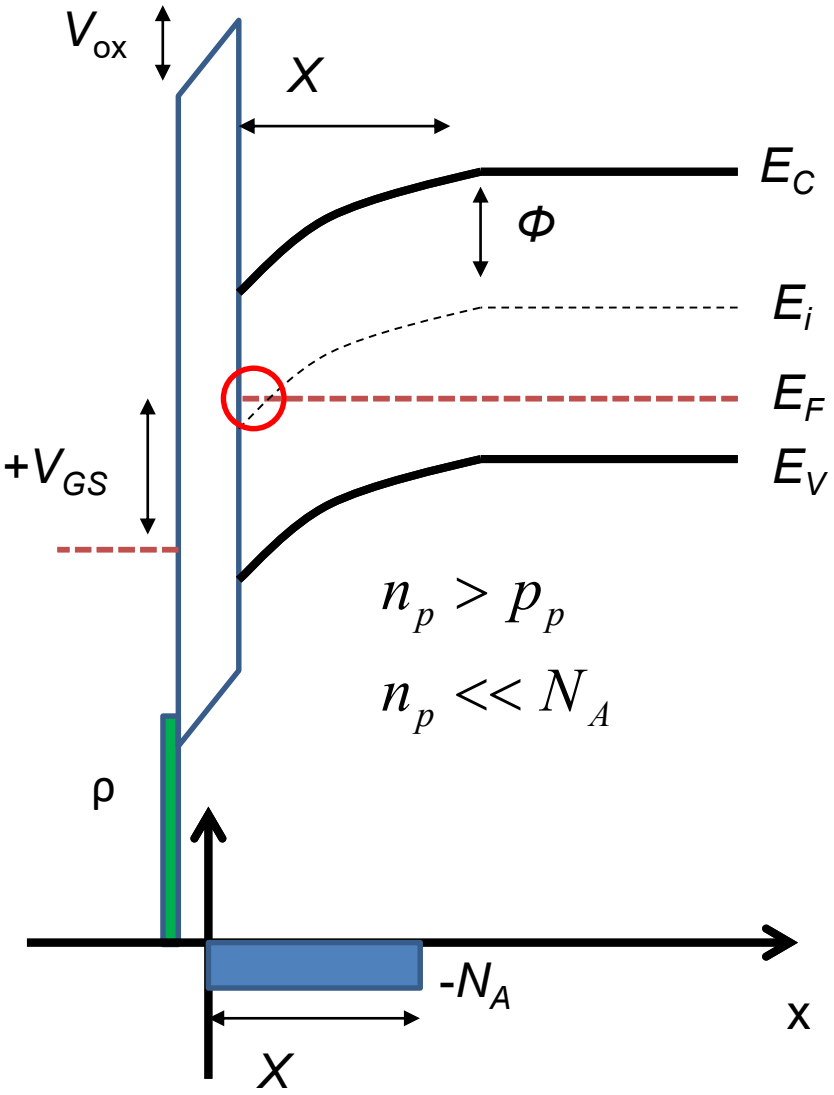
$$X = \sqrt{\frac{2 \cdot \varepsilon_s \cdot \varepsilon_0 \cdot \phi}{q \cdot N_A}}$$

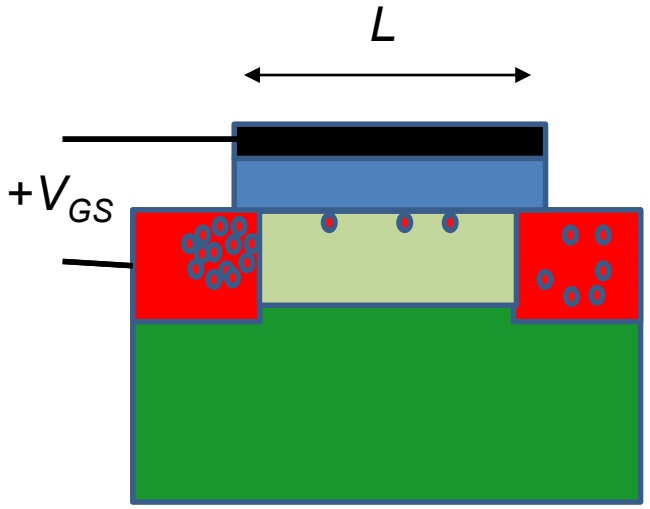
$$Q = X \cdot N_A \cdot q$$

$$V_{ox} = \frac{Q}{C_{ox}}$$

$$V_{GS} = V_{ox} + \phi$$

Energy bands 4 – weak inversion





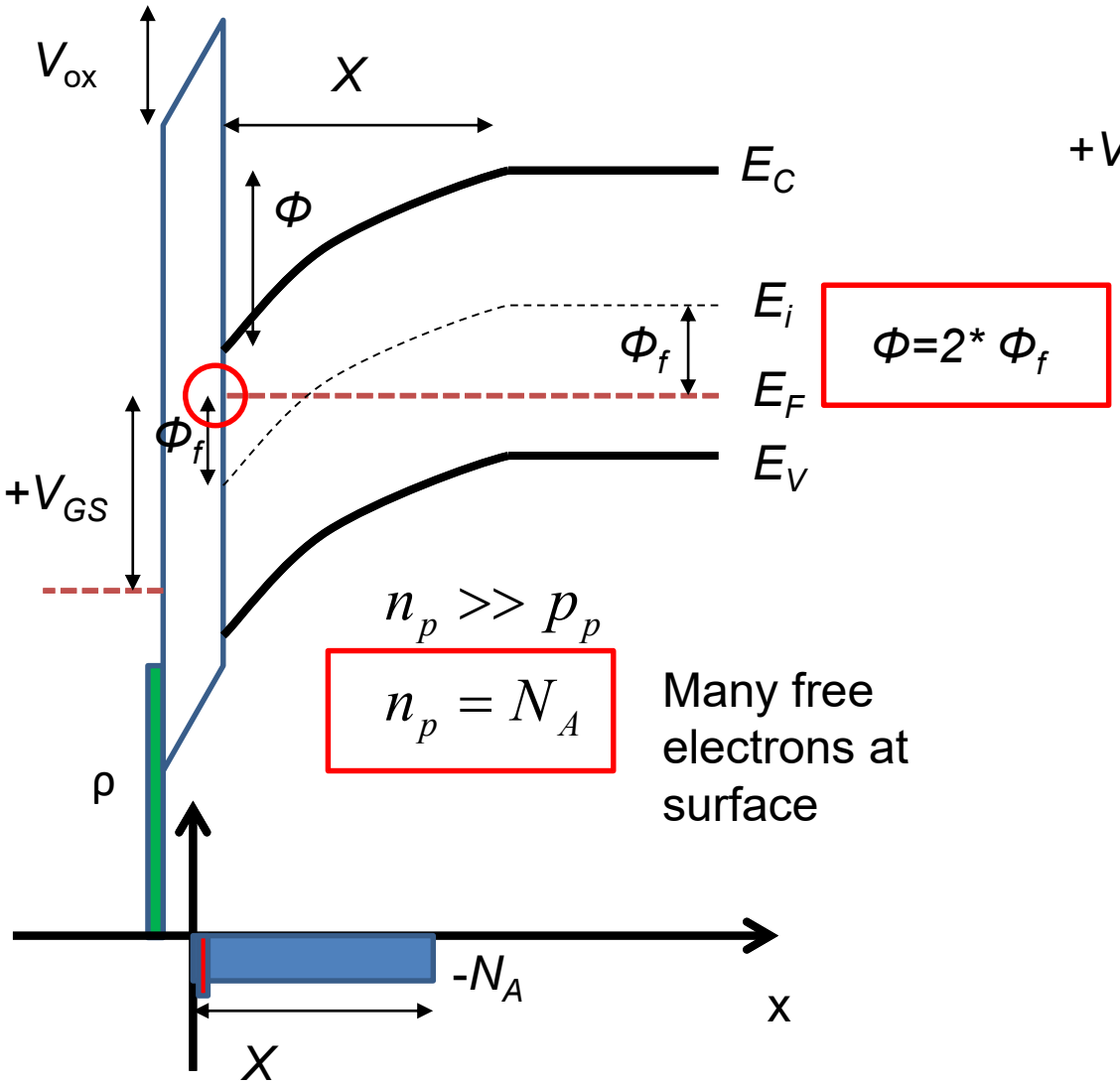
$$X = \sqrt{\frac{2 \cdot \varepsilon_s \cdot \varepsilon_0 \cdot \phi}{q \cdot N_A}}$$

$$Q = X \cdot N_A \cdot q$$

$$V_{ox} = \frac{Q}{C_{ox}}$$

$$V_{GS} = V_{ox} + \phi$$

Energy bands 5 – onset of strong inversion ($V_{GS}=V_t$)

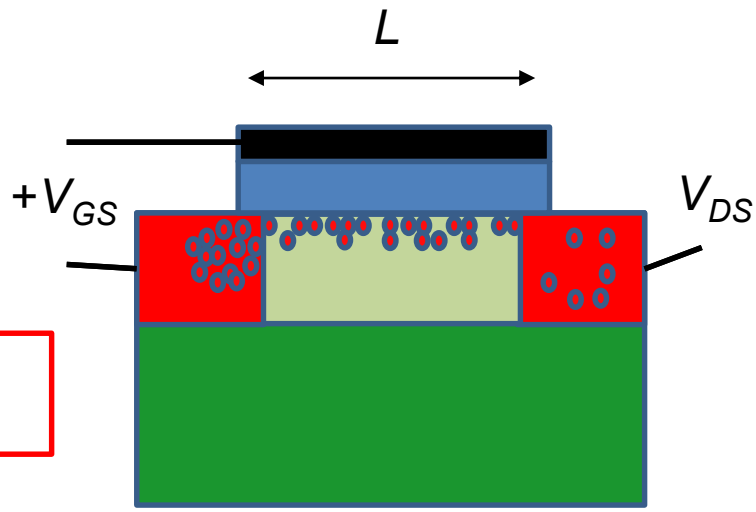


$\Phi=2^* \Phi_f$

$n_p >> p_p$

$n_p = N_A$

Many free electrons at surface



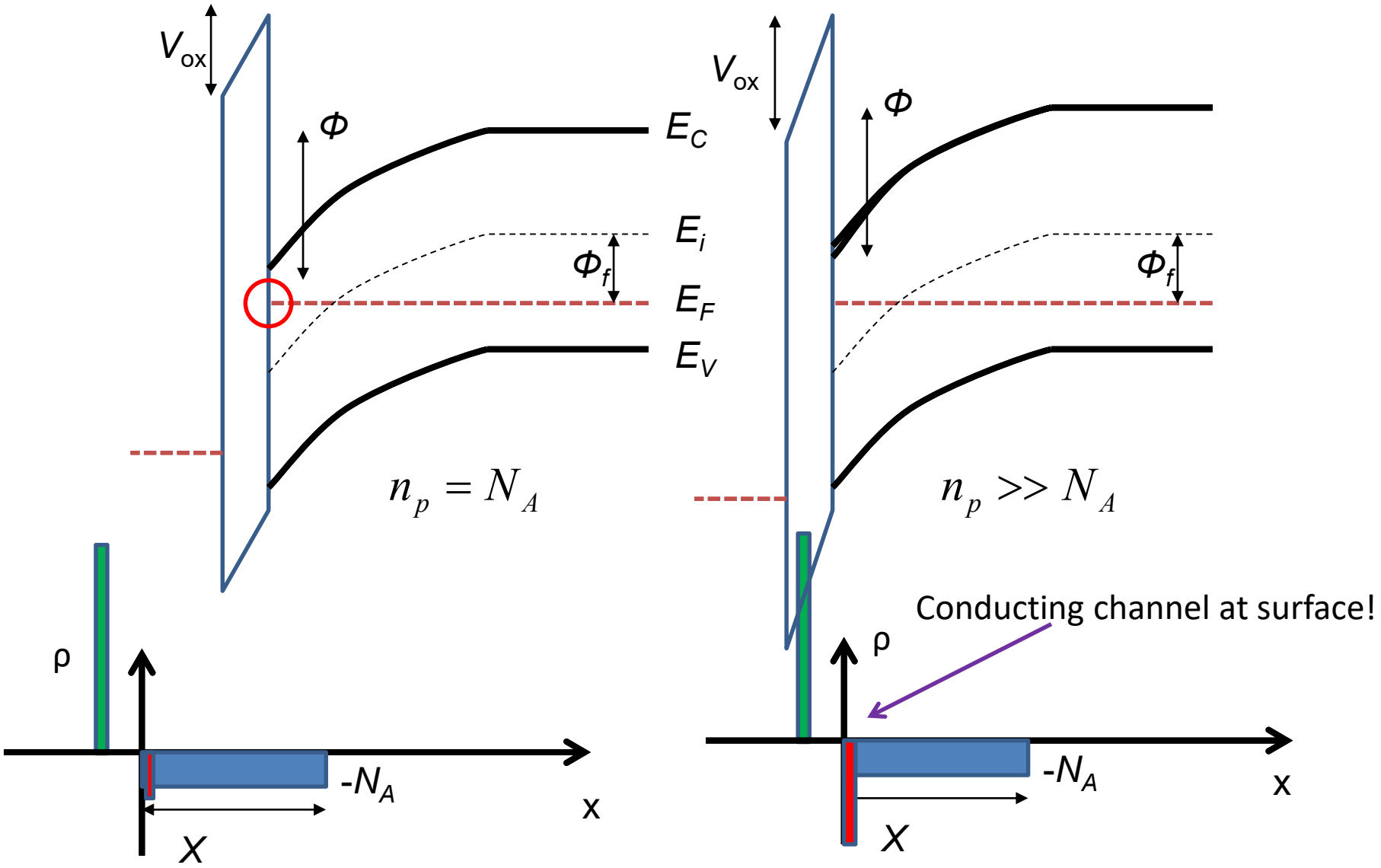
$$X = \sqrt{\frac{2 \cdot \varepsilon_s \cdot \varepsilon_0 \cdot \phi}{q \cdot N_A}}$$

$$Q = X \cdot N_A \cdot q$$

$$V_{ox} = \frac{Q}{C_{ox}}$$

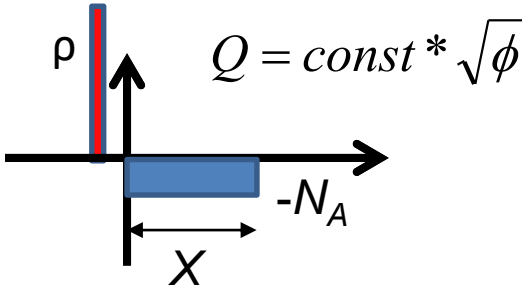
$$V_{GS} = V_{ox} + \phi$$

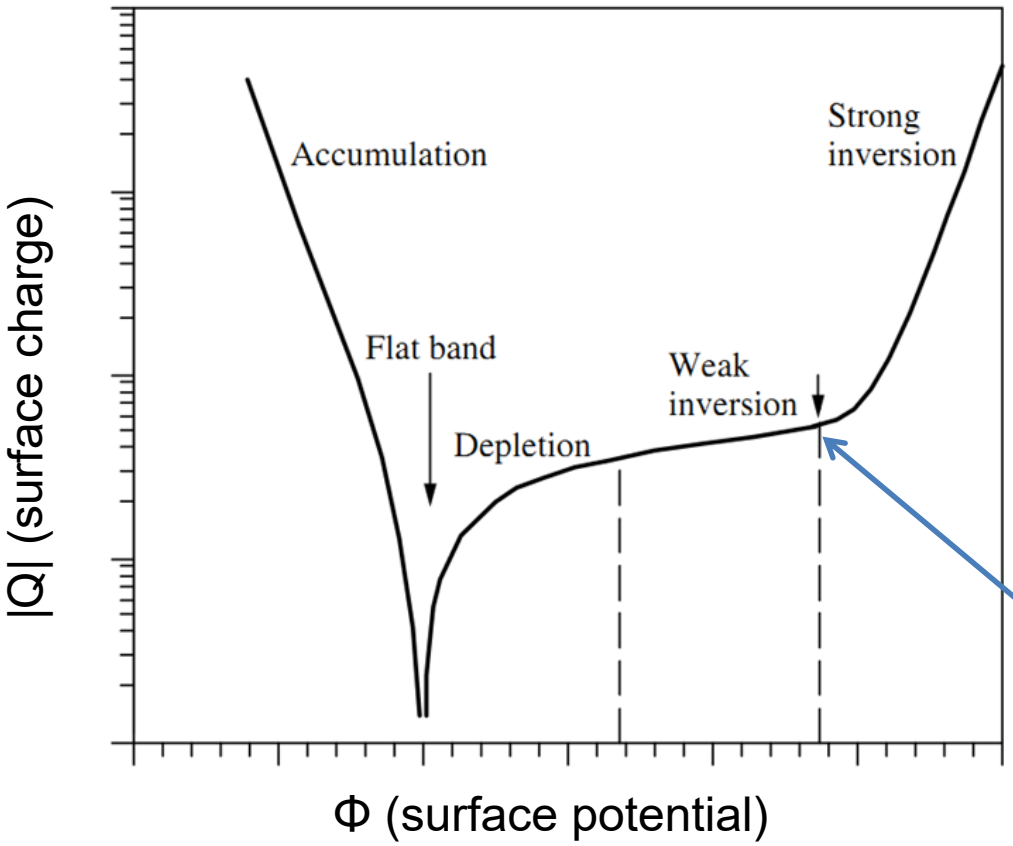
Strong inversion $V_{GS}>V_t$



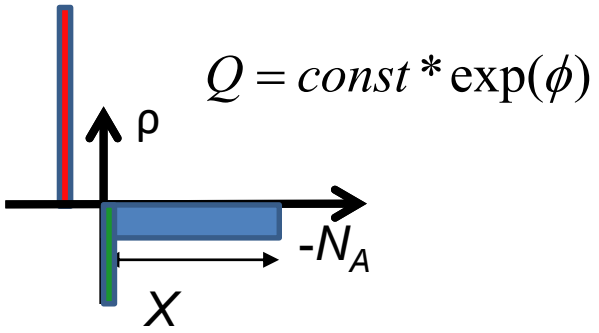
Charge vs surface potential

depletion / weak inversion
only acceptors contribute ->
slow increase in Q (increase X)





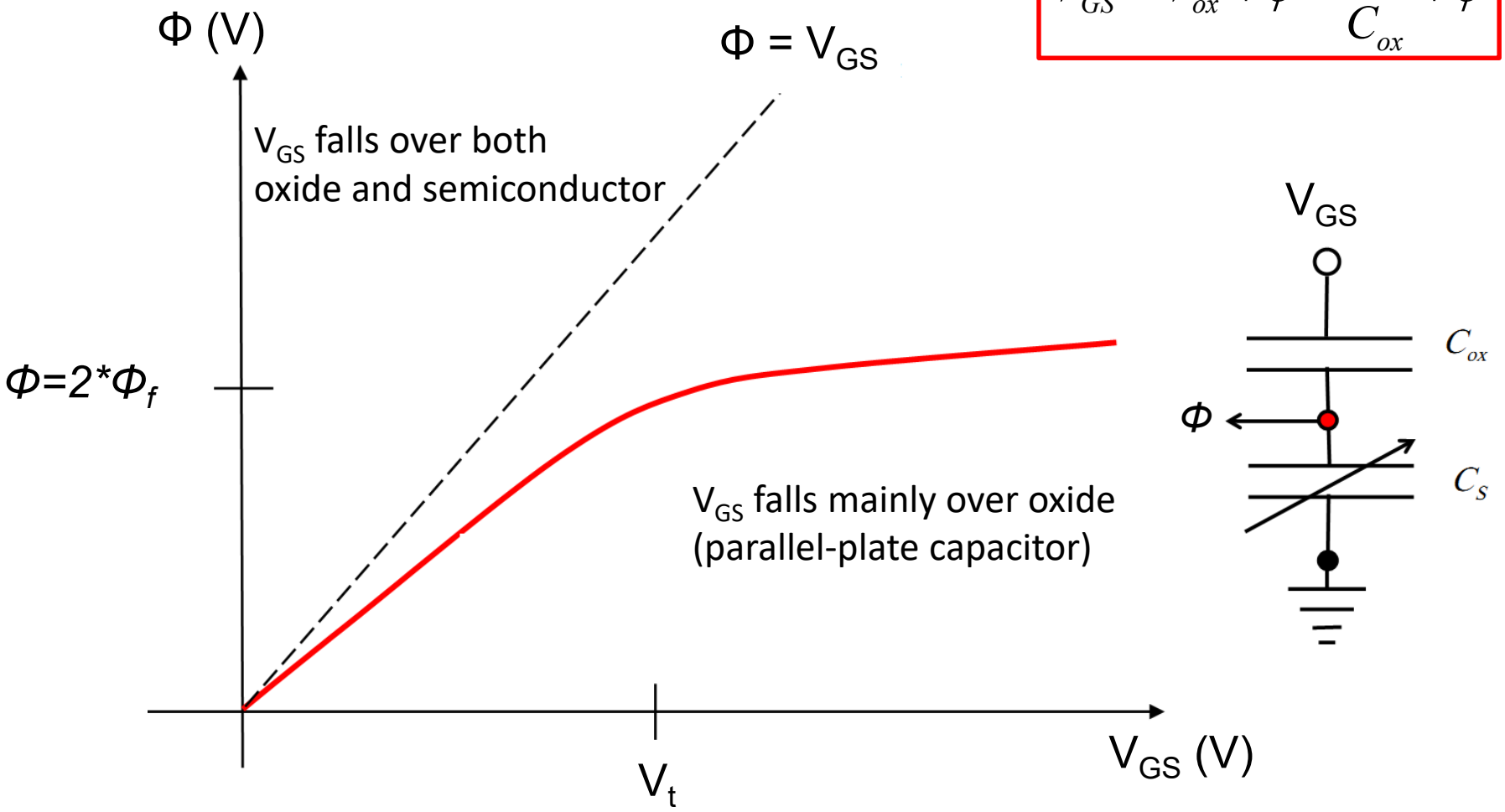
strong inversion
mainly electrons contribute ->
exponential increase in Q



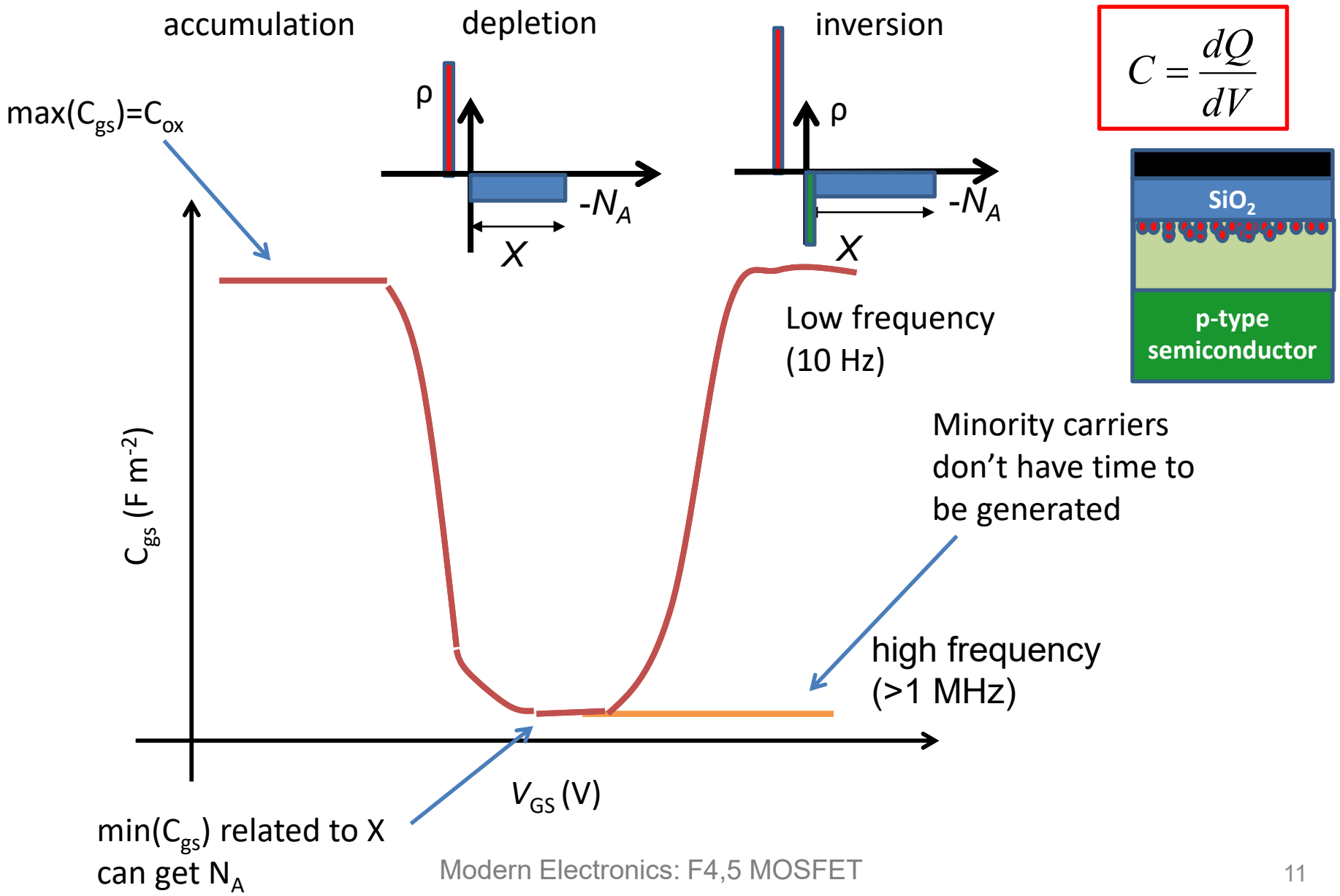
Threshold for
channel formation

Surface potential variation with gate voltage

$$V_{GS} = V_{ox} + \phi = \frac{Q}{C_{ox}} + \phi$$



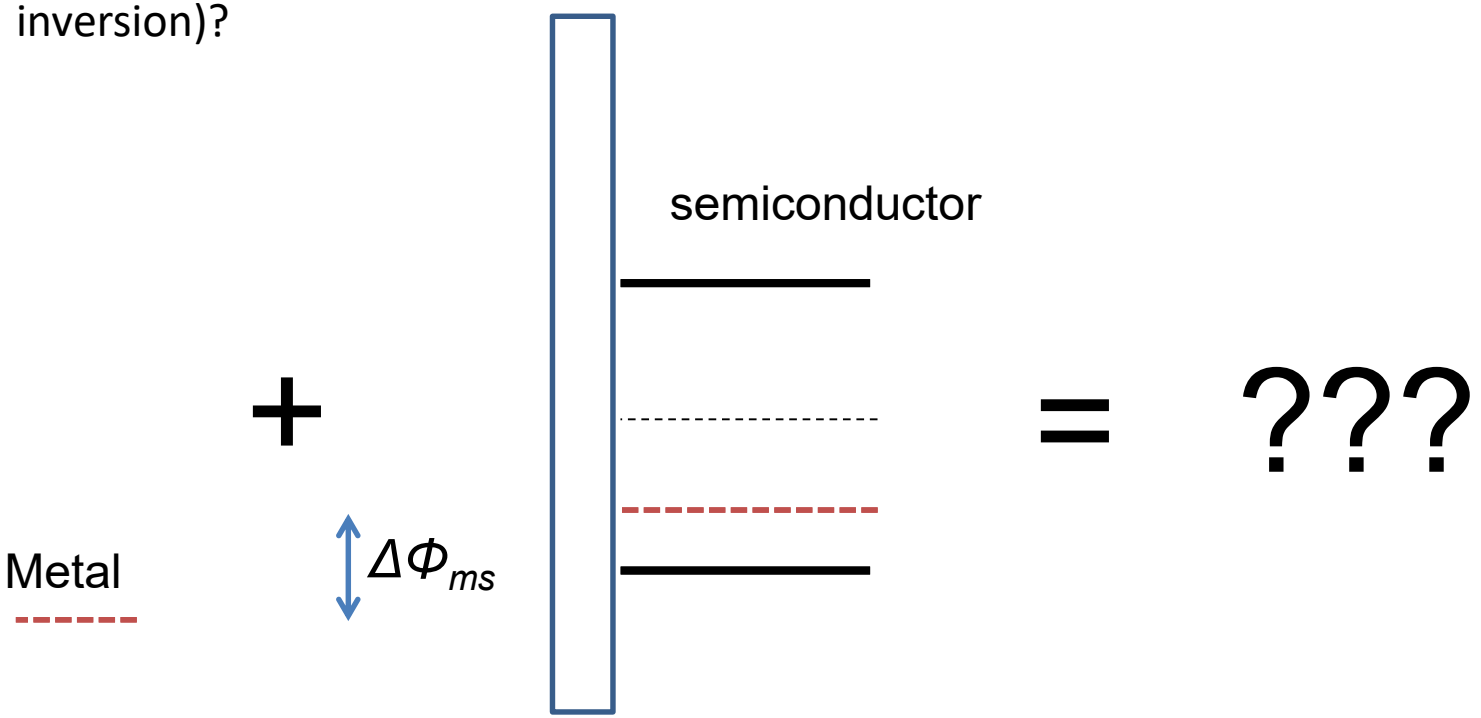
MOS physics: capacitance



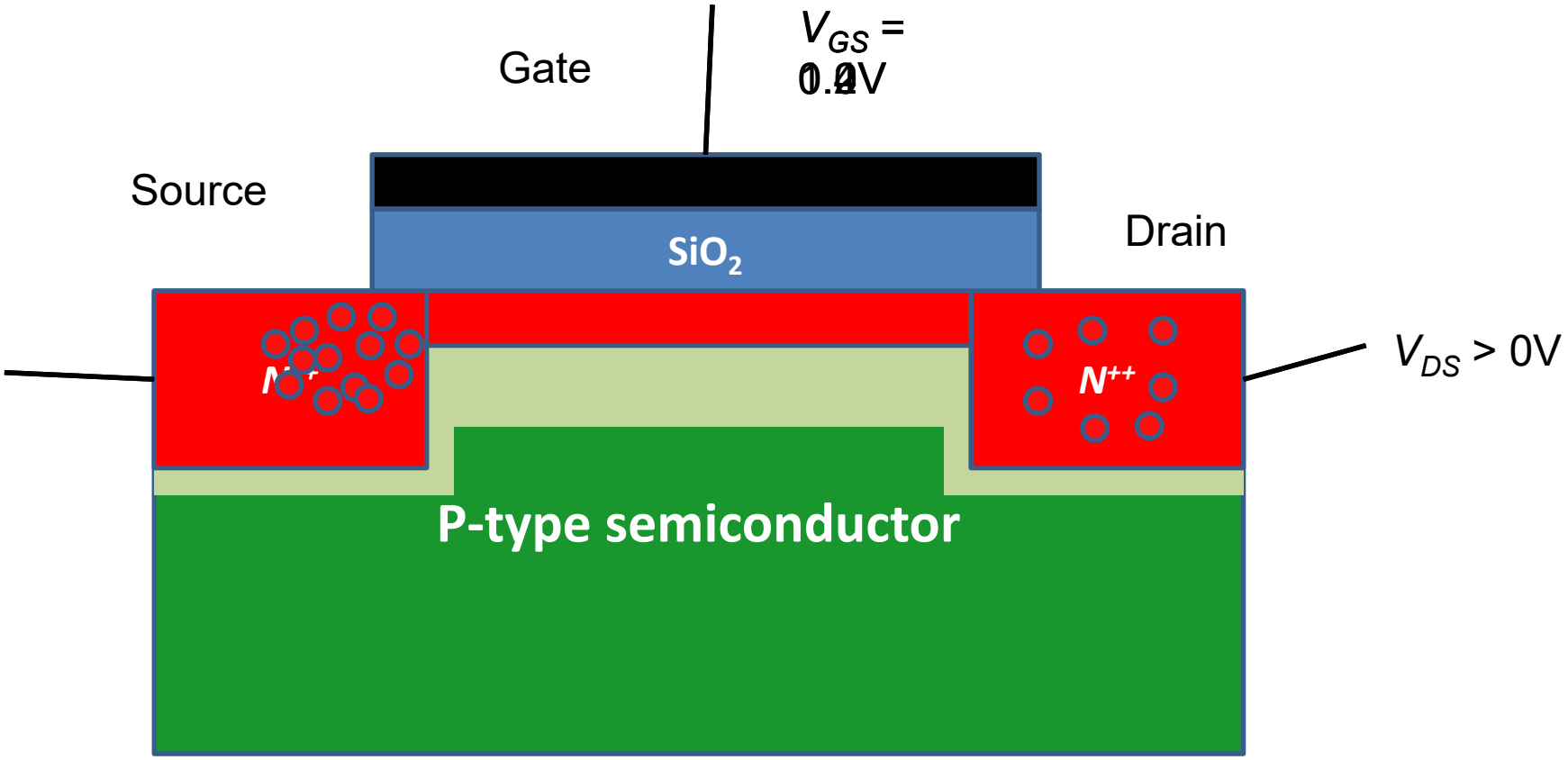
2 min exercise – metal work function variation

Metal and semiconductor work functions usually not the same (as we assumed before).

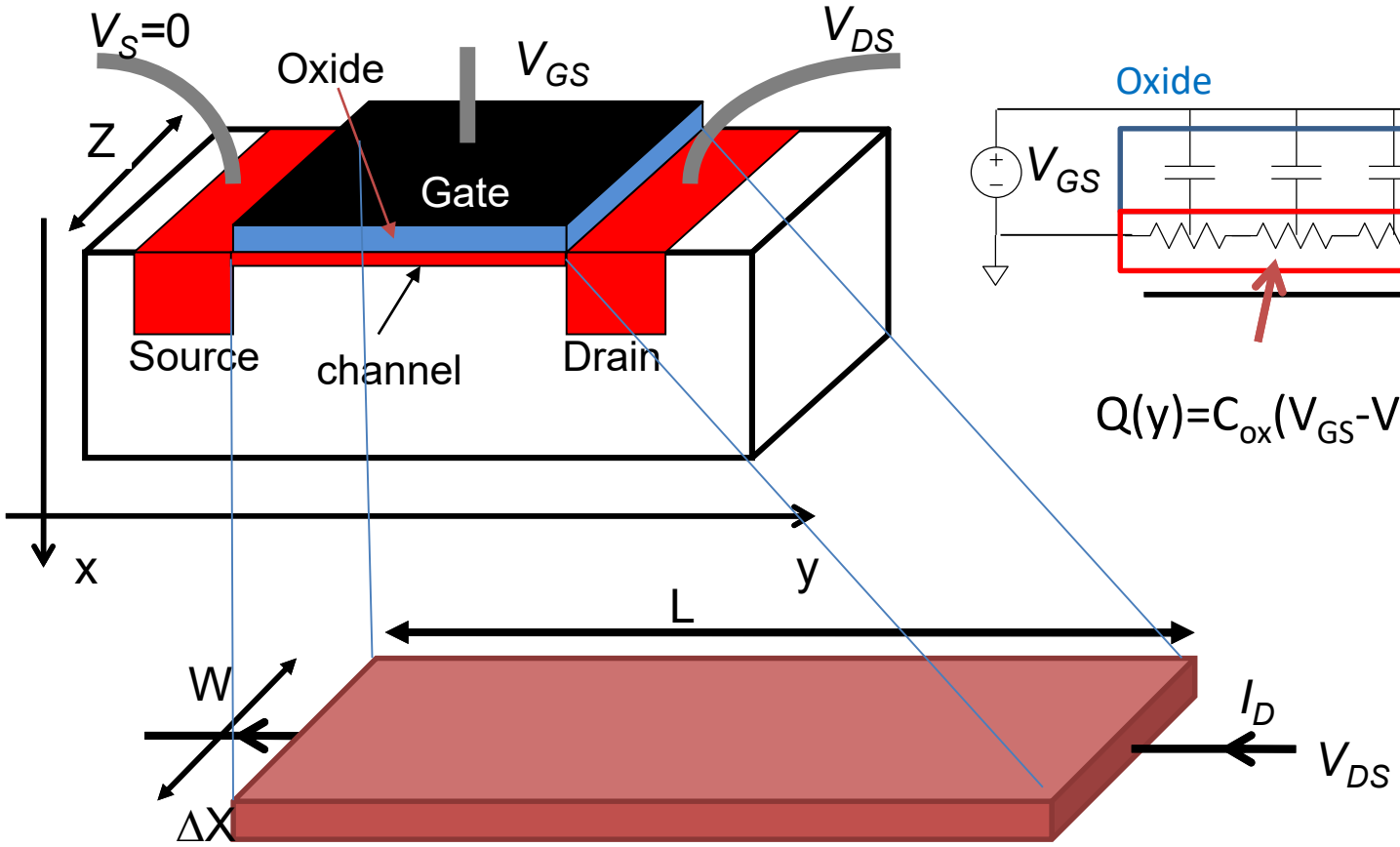
1. Sketch band diagram (without bias) for metal with higher work function in MOS.
2. How does the higher work function impact V_t (threshold voltage needed for strong inversion)?



Inversion layers creates channel in MOSFET



Geometry for drain current calculation (5.1.4 - 5.1.6)



$$Q(y)=C_{ox}(V_{GS}-V(y)-V_t)$$

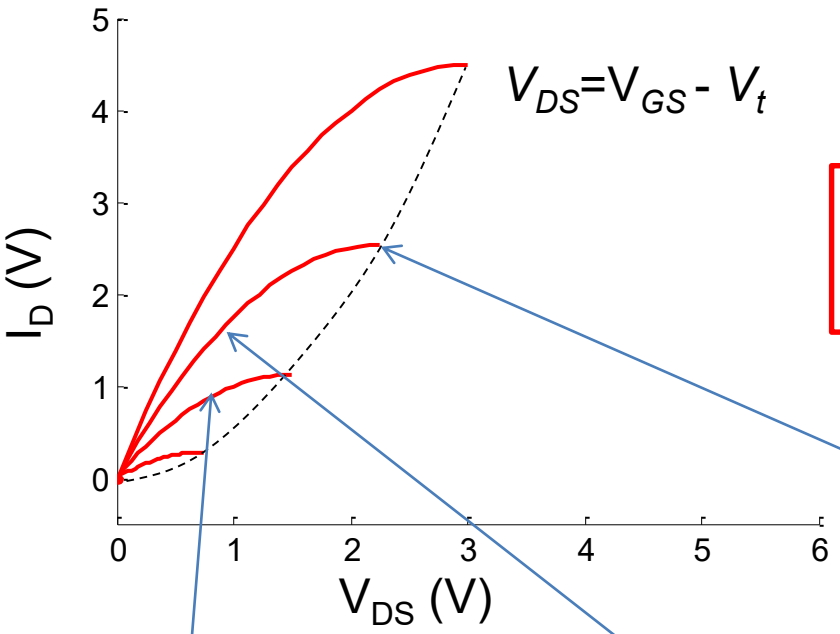
Q(y) = electrons per unit area at position y

V(y) = voltage at y w.r.t. source

V_{GS}-V(y) = gate-to-channel voltage at y

ε(y) = electric field at y

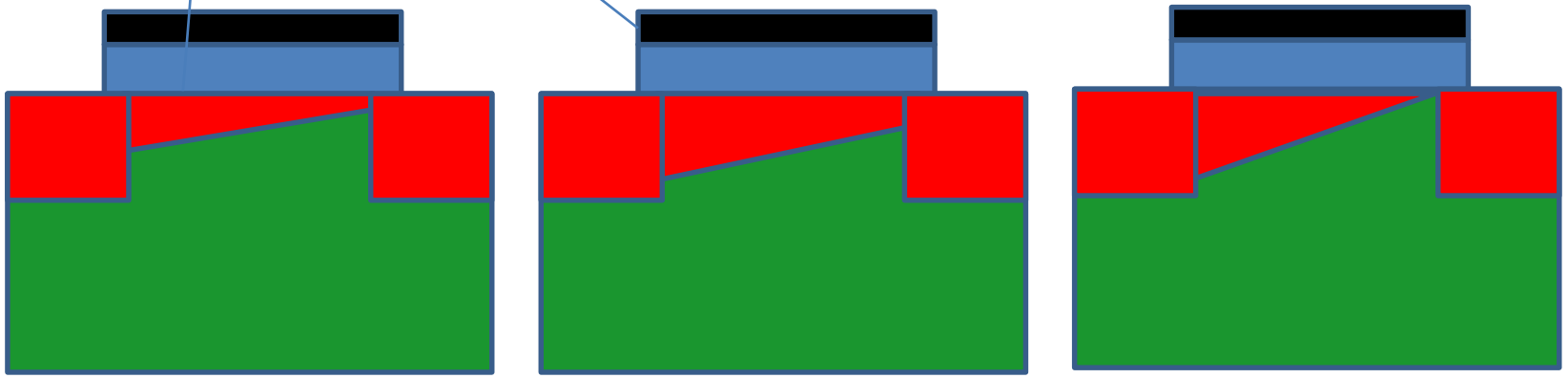
Current and channel shape – linear (triode) region



$$I_D = 0 \qquad V_{GS} < V_t$$

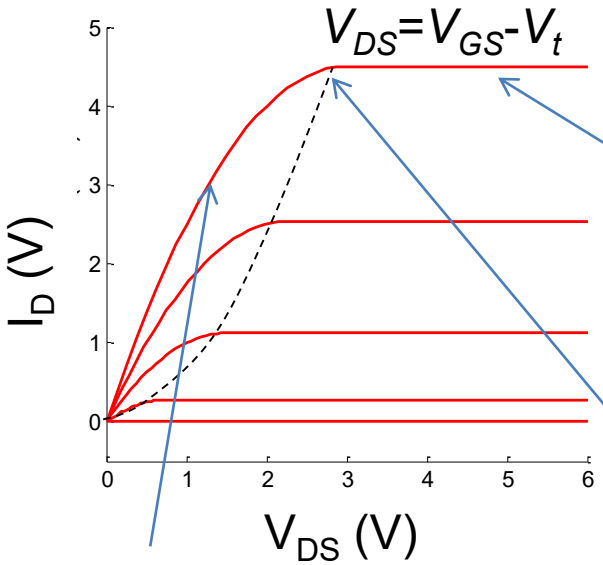
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_t)V_{DS} - V_{DS}^2\right]$$

$V_{GS} > V_t$
$V_{DS} < V_{GS} - V_t$



$$Q'(y) = C_{ox}\left(V_{GS} - V_t - V(y)\right)$$

Current and channel shape – saturation region (pinch-off)



$$I_{D,sat} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_t\right)^2$$

Pinch-off: I_D independent of V_{DS}

$V_{DS}<V_{GS}-V_t$

$$Q = C_{ox}\left(V_{GS}-V_t-V(y)\right)$$

$V_{DS}=V_{GS}-V_t$

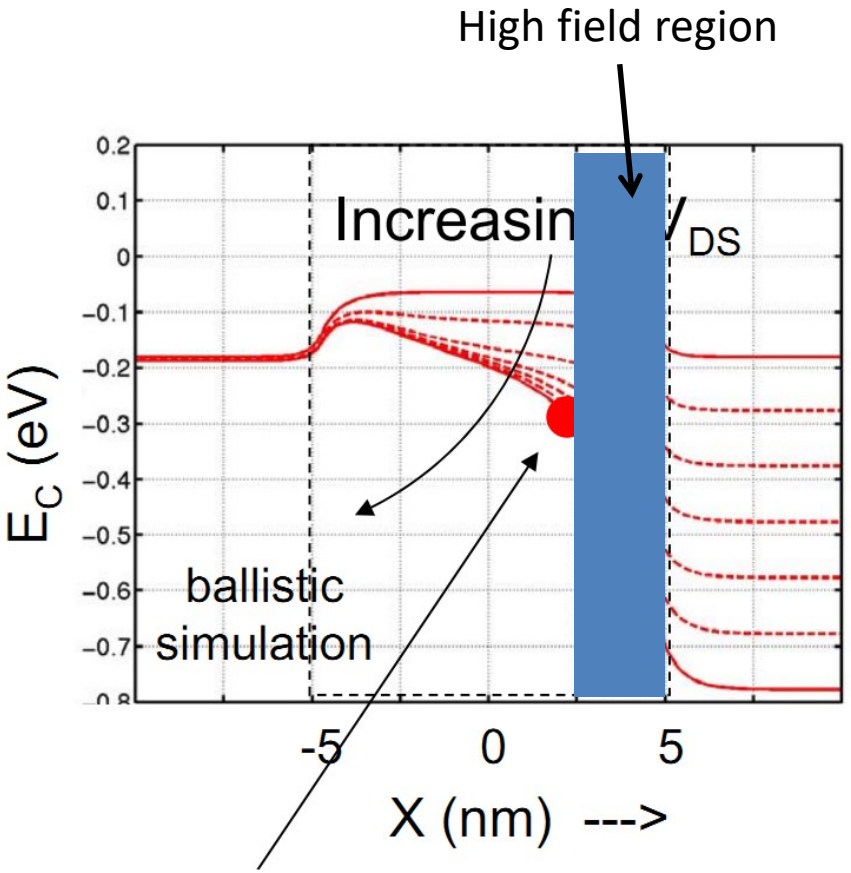
$$Q(0) = C_{ox}\left(V_{GS}-V_t\right) \qquad Q(L)\approx 0$$

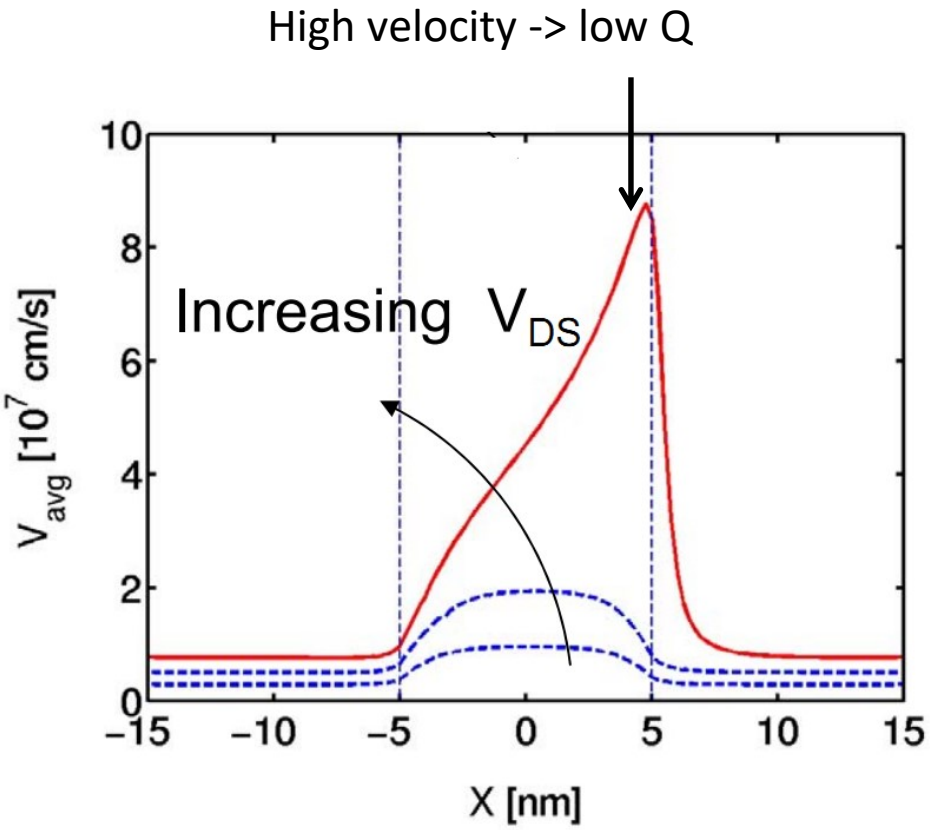
$V_{DS}>V_{GS}-V_t$

$$Q = C_{ox}\left(V_{GS}-V_t-V(y)\right)$$

$$Q(L)\approx 0$$

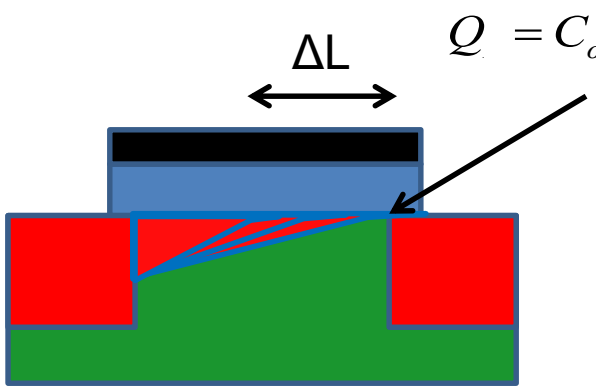
Pinch-off – band structure and electron velocity





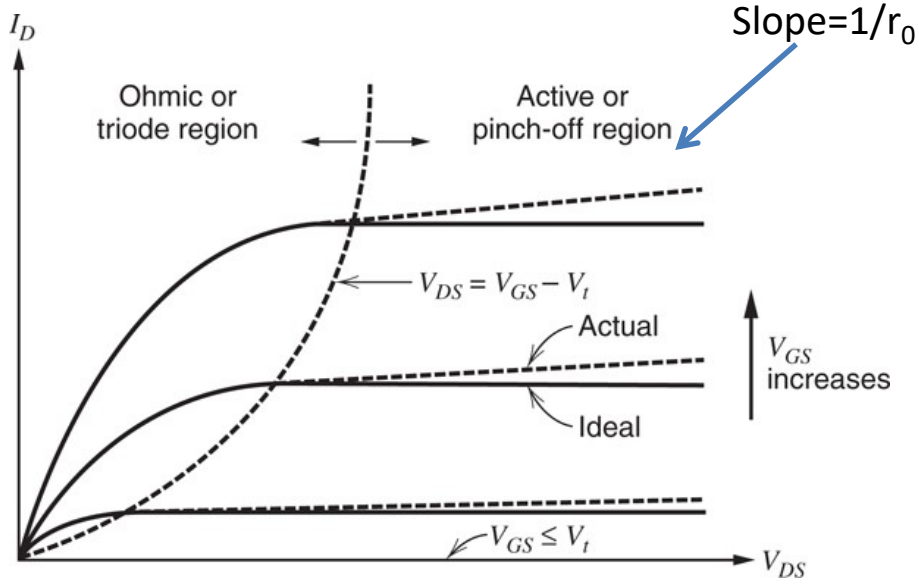
Pinch-off point:
Electrons swept into drain by E-field

Channel length modulation (5.2.4)



$$Q = C_{ox}\left(V_{GS} - V_t - V(y)\right)$$

$$I_{D,sat} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_t\right)^2\left(1 + \lambda V_{DS}\right)$$



- A non-inverted region is formed beyond pinch-off i.e. the channel length is reduced with V_{DS}
- Gives output resistance $r_0 = \left(\frac{dI_D}{dV_{DS}}\right)^{-1} = \frac{1}{\lambda I_D}$
- Output conductance $g_d = 1/r_0$
- $\lambda \approx 0.005\text{-}0.05\ V^{-1}$

1 min excercise

Which of these is correct for channel length modulation?

a) Stronger impact for longer channels
b) Lower impact for longer channels
c) No dependence on channel length

d) Stronger impact with higher channel doping
e) Lower impact with higher channel doping
f) No dependence on channel doping

Example: MOSFET with channel length modulation

V_t = 1.0 V
C_{ox} = 3 mF/m^2
μ_n = 0.135 m^2/Vs
L = 5 µm
W = 50 µm
λ = 0.02 V^{-1}

Calculate I_D for

1) V_{DS}= 0.5, 1, 2 & 3V if V_{GS} = 0 V

2) V_{DS}= 0.5, 1, 2 & 3V if V_{GS} = 2.5 V

Linear region

$$V_{DS} < V_{GS} - V_t$$

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_t)V_{DS} - V_{DS}^2\right]$$

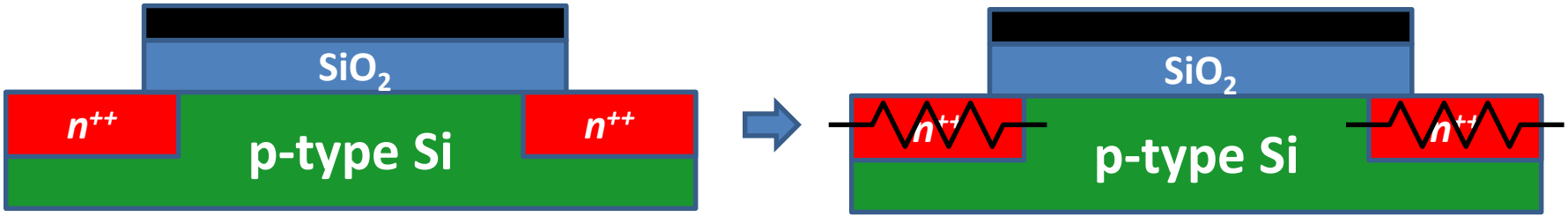
saturation

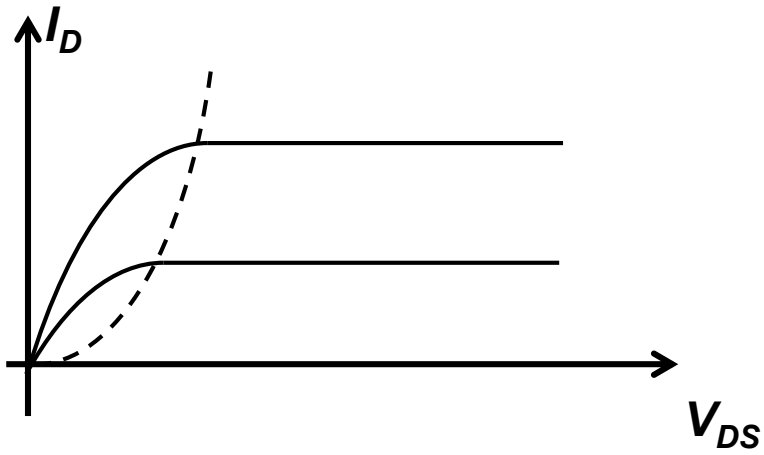
$$V_{DS} > V_{GS} - V_t$$

$$I_{D,sat} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$$

2 min exercise – source/drain resistance

In modern MOSFETs, resistance in the source/drain can not always be neglected. How does the output characteristics change if a significant source/drain resistance is added?



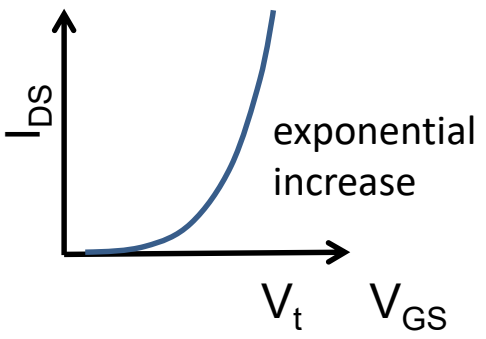


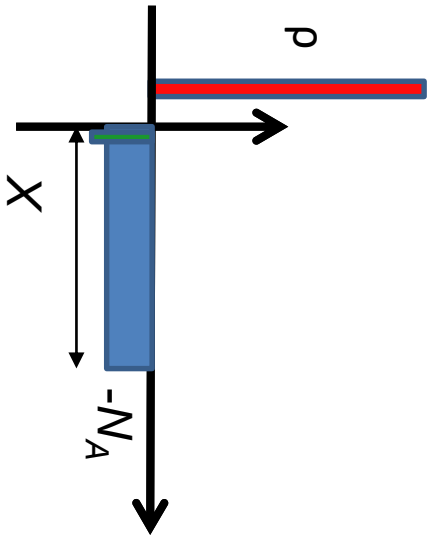
???

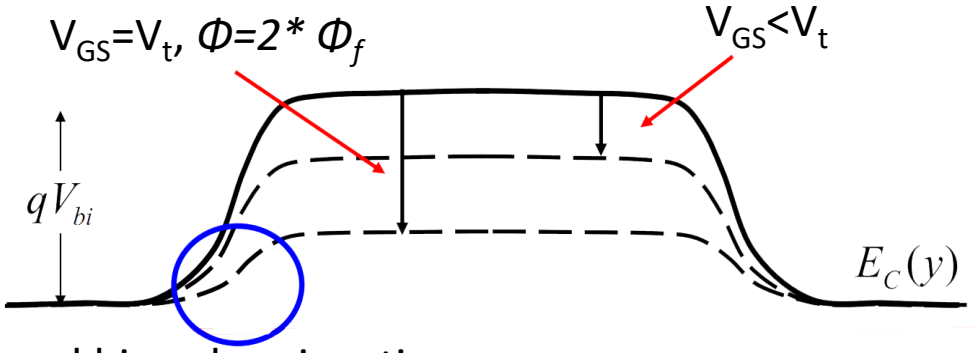
Subthreshold current (weak inversion) (not in book)

- For $V_{GS} < V_t$ (but high enough for weak inversion): channel charge << inversion charge
- Drift current is small, mainly diffusion current (as NPN BJT)
- Exponentially increasing injection over barrier with V_{GS}.

$$I_D \propto \exp\left(\frac{V_{GS}-V_t}{nV_T}\right)\cdot\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$





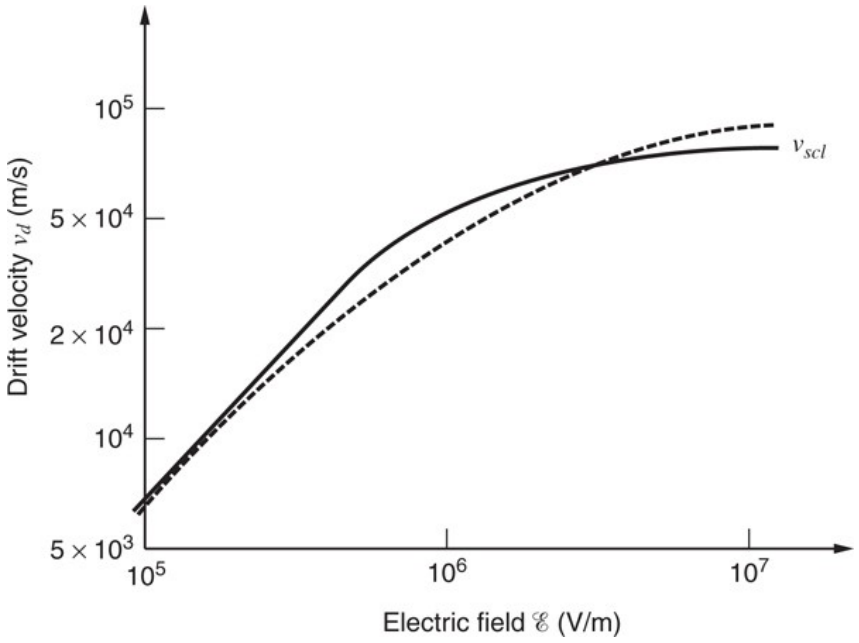


Forward biased np-junction

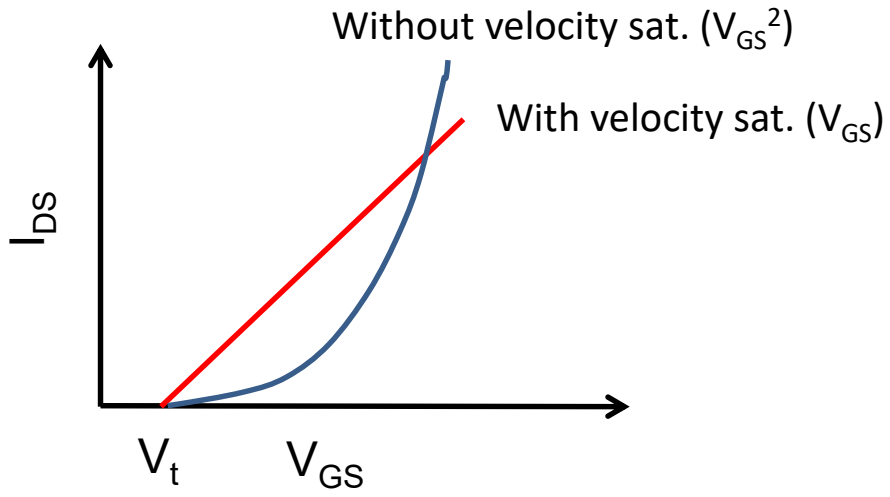
Velocity saturation in short-channel MOSFETs (5.4.4)

- Short channel length, high V_{DS} -> high electric field.
- At critical field ε_c ($1.5*10^6$ V/m) electron velocity saturates due to optical phonon emission.

$$v_d = \frac{\mu_n \varepsilon}{1 + \varepsilon / \varepsilon_c} \qquad \begin{cases} \varepsilon << \varepsilon_c \rightarrow v_d \approx \mu_n \varepsilon \\ \varepsilon >> \varepsilon_c \rightarrow v_d \approx \mu_n \varepsilon_c = v_{scl} \end{cases}$$

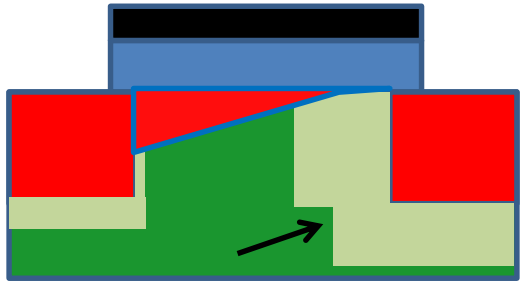


$$\lim_{E_C \to 0} I_D = WC_{ox}(V_{GS} - V_t)v_{scl}$$

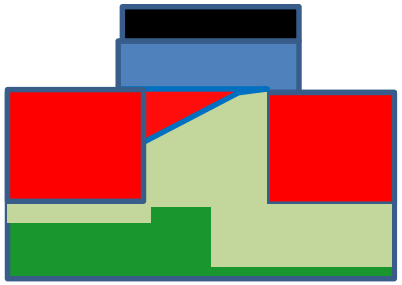


Detrimental effects

- **Junction breakdown** – For large V_{DS} of 20-150V (long channel) the drain-substrate pn-junction is reversed biased enough to cause avalanche breakdown.

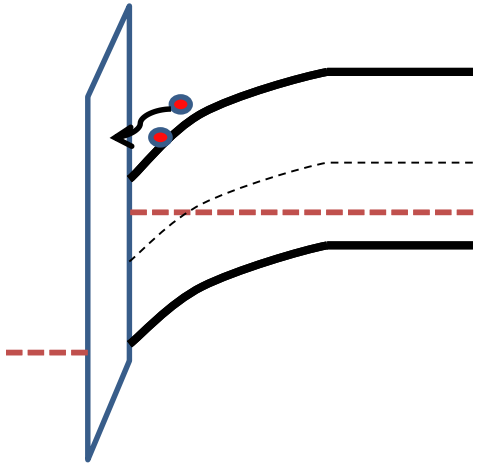


- **Punchthrough** – For large V_{DS} (short channel) the drain depletion region can touch the source depletion region. Slower current increase than junction breakdown. Increasing channel doping makes depletion regions thinner.



- **Hot carriers** – high electric fields give electrons enough energy to be injected into gate oxide. Can give higher gate current and/or shift the threshold voltage.

- **Oxide breakdown** – For high (> $6*10^6$ V/cm) vertical electric fields (from gate) the gate oxide may break.



Summary – MOSFET DC characteristics

- Linear (triode)
  $V_{DS} < V_{GS} - V_t$

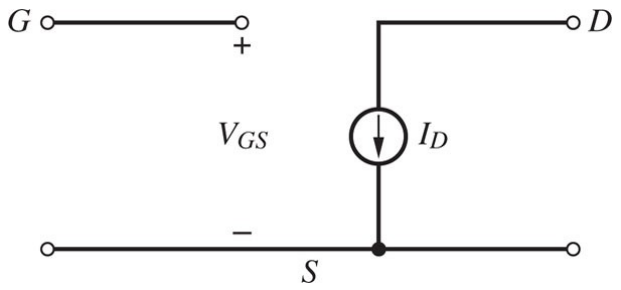
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_t)V_{DS} - V_{DS}^2\right]$$

- Saturation (active, pinch-off)
  $V_{DS} > V_{GS} - V_t$
  included channel length modulation

$$I_{D,sat} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$$

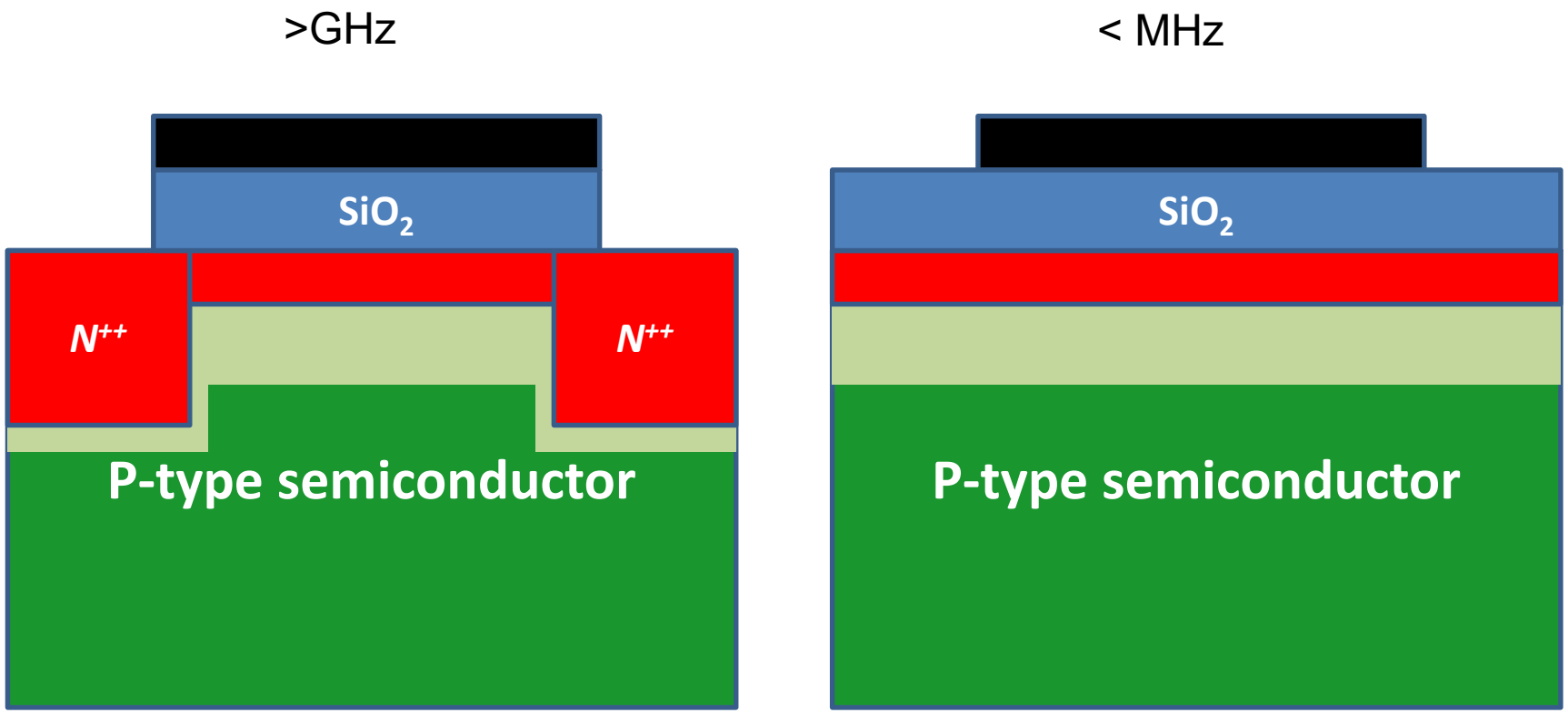
- Velocity saturation

$$\lim_{E_C \to 0} I_D = WC_{ox}(V_{GS} - V_t)v_{scl}$$

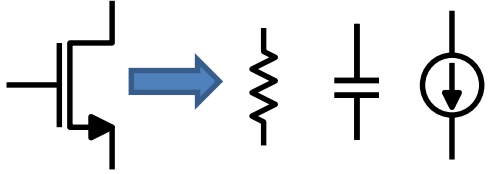


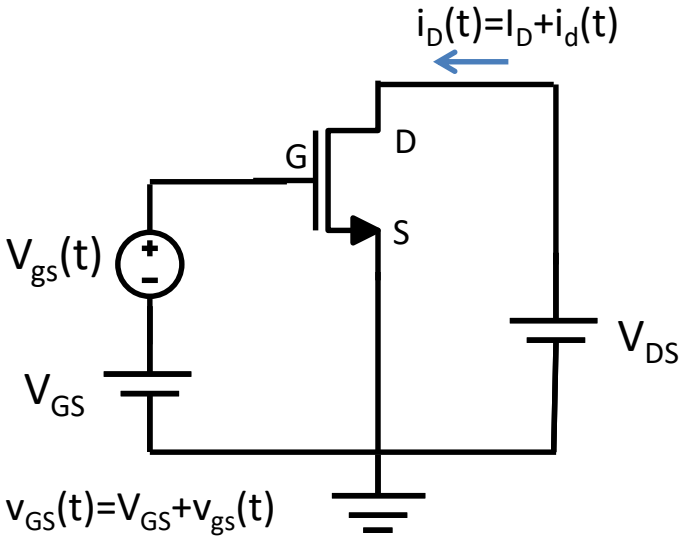
1 min excercise – MOSCAP vs MOSFET

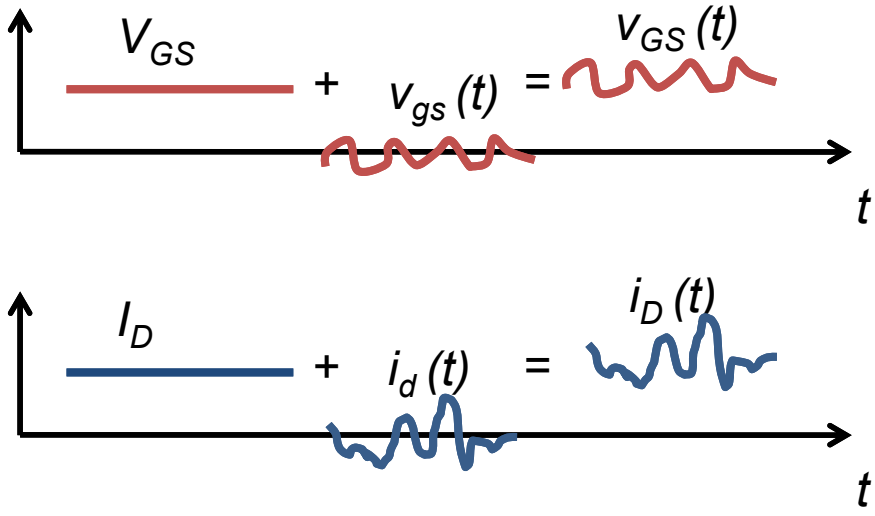
How can a MOSFET operate at GHz when MOSCAP only responds at frequencies < 1 MHz in inversion?

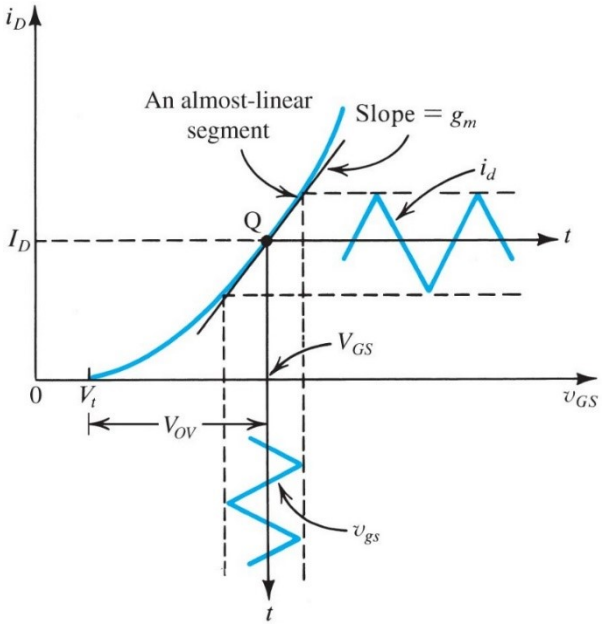


Small-signal model (6.2.1)









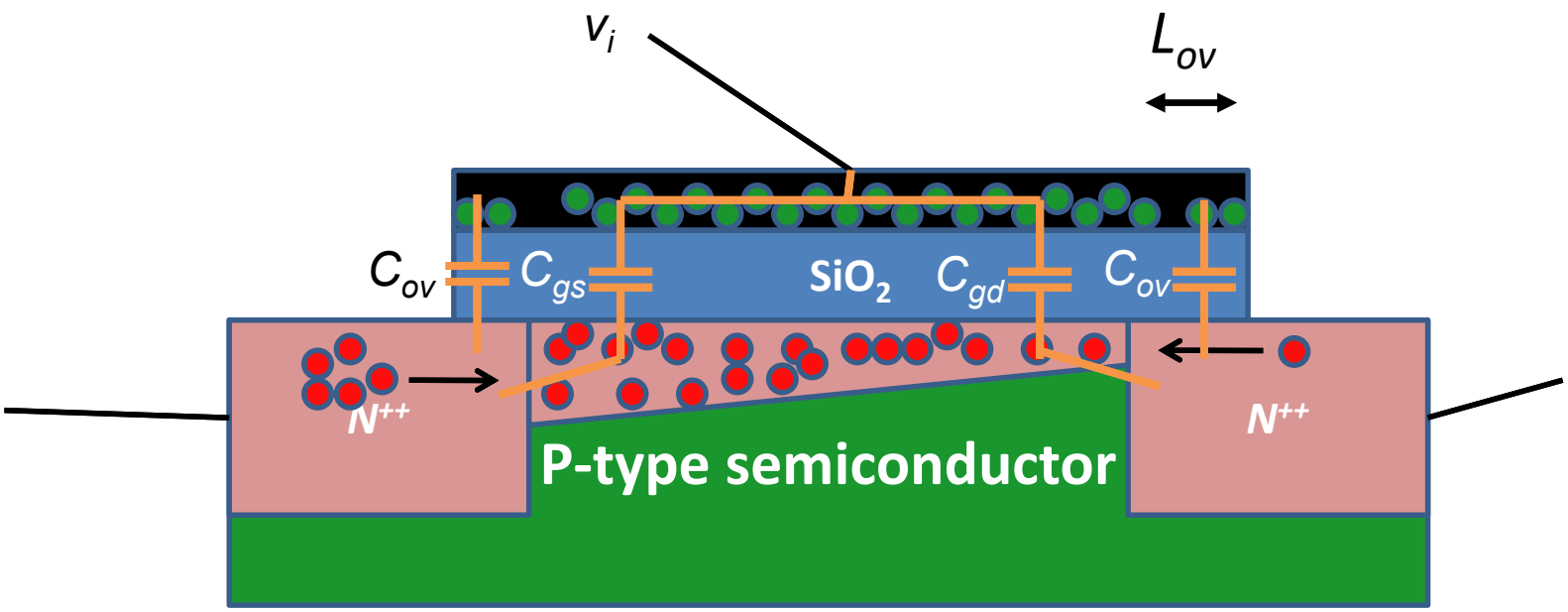
1st order Taylor expansion - linearization

$$f(x_0+\delta x) \approx f(x_0) + \left.\frac{df(x)}{dx}\right|_{x=x_0} \delta x + \ldots$$

$$i_D\left(V_{GS}+v_{gs}\right) \approx I_D\left(V_{GS}\right) + \frac{dI_D}{dV_{GS}} \cdot v_{gs} = I_D\left(V_{GS}\right) + g_m \cdot v_{gs}$$

$$i_D\left(V_{DS}+v_{ds}\right) \approx I_D\left(V_{DS}\right) + \frac{dI_D}{dV_{DS}} \cdot v_{ds} = I_D\left(V_{DS}\right) + \frac{1}{r_0} \cdot v_{ds}$$

Capacitances (9.2.1)



Linear region $C_{gs} = C_{gd} = \frac{1}{2} WLC_{ox}$ (C_{ox} [F/μm²])

Saturation region

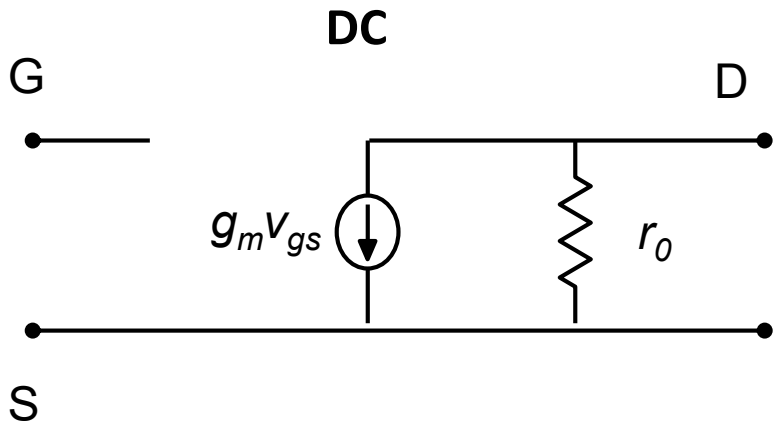
$$C_{gs} = \frac{2}{3} WLC_{ox}$$

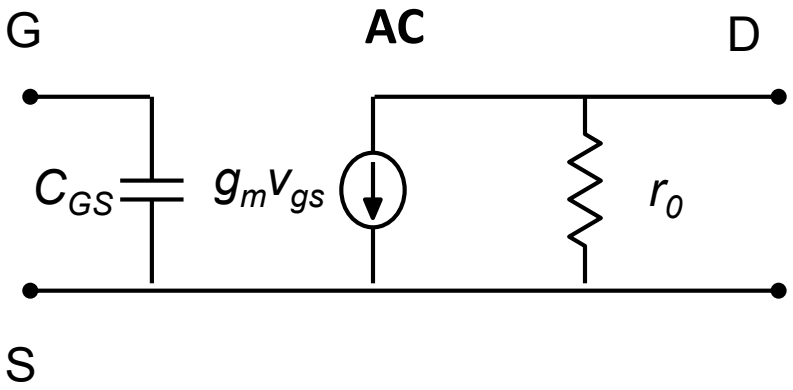
$$C_{gd} = 0$$

Overlap capacitance $C_{ov} = W L_{ov} C_{ox}$

source/drain-to-body capacitance ….

(simple) Small-signal model - saturation





- Transconductance – controls the current source

$$g_m = \sqrt{2 \cdot \mu_n \cdot C_{ox} \frac{W}{L} I_D}$$

- Output resistance – channel length modulation with increasing V_{DS}

$$r_o = \frac{1}{\lambda I_{DS}}$$

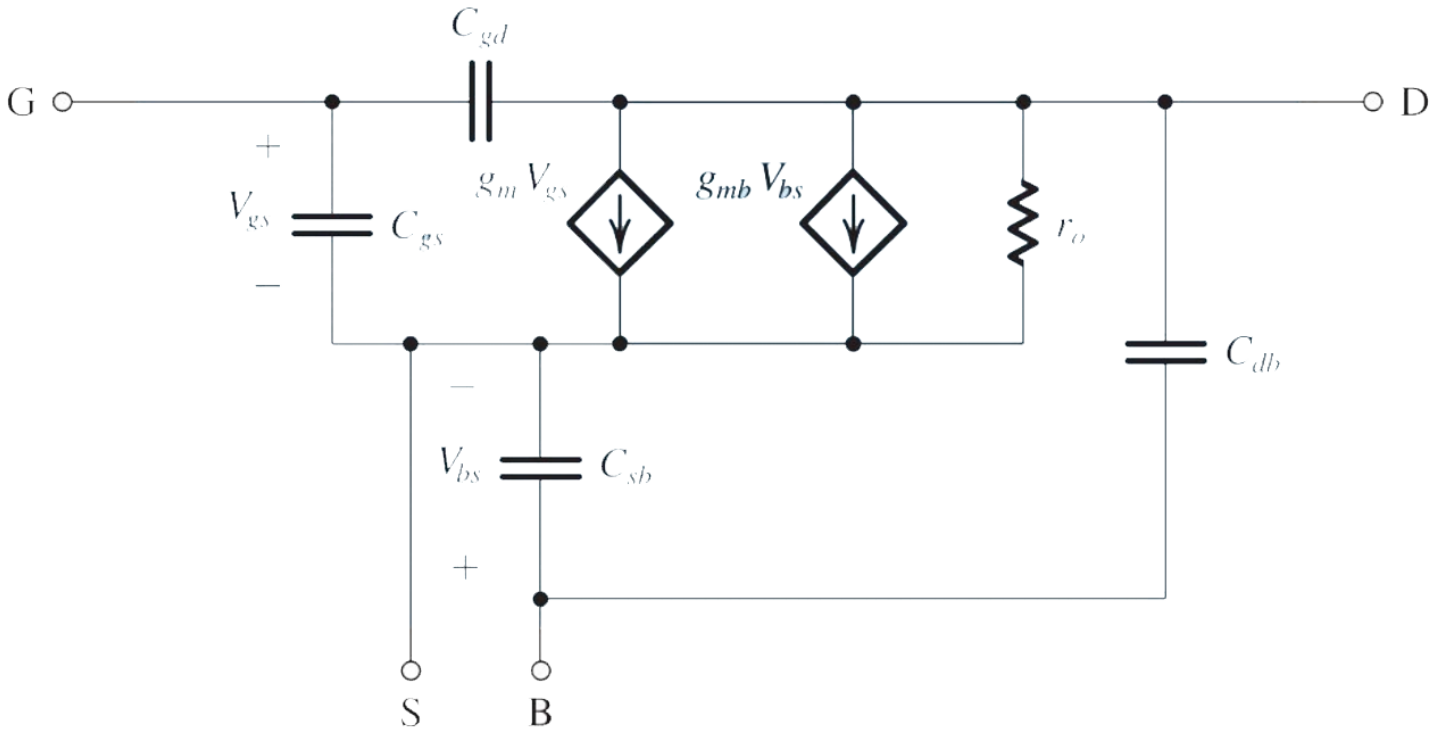
- gate-source capacitance

$$C_{GS} = \frac{2}{3} WLC_{ox}$$

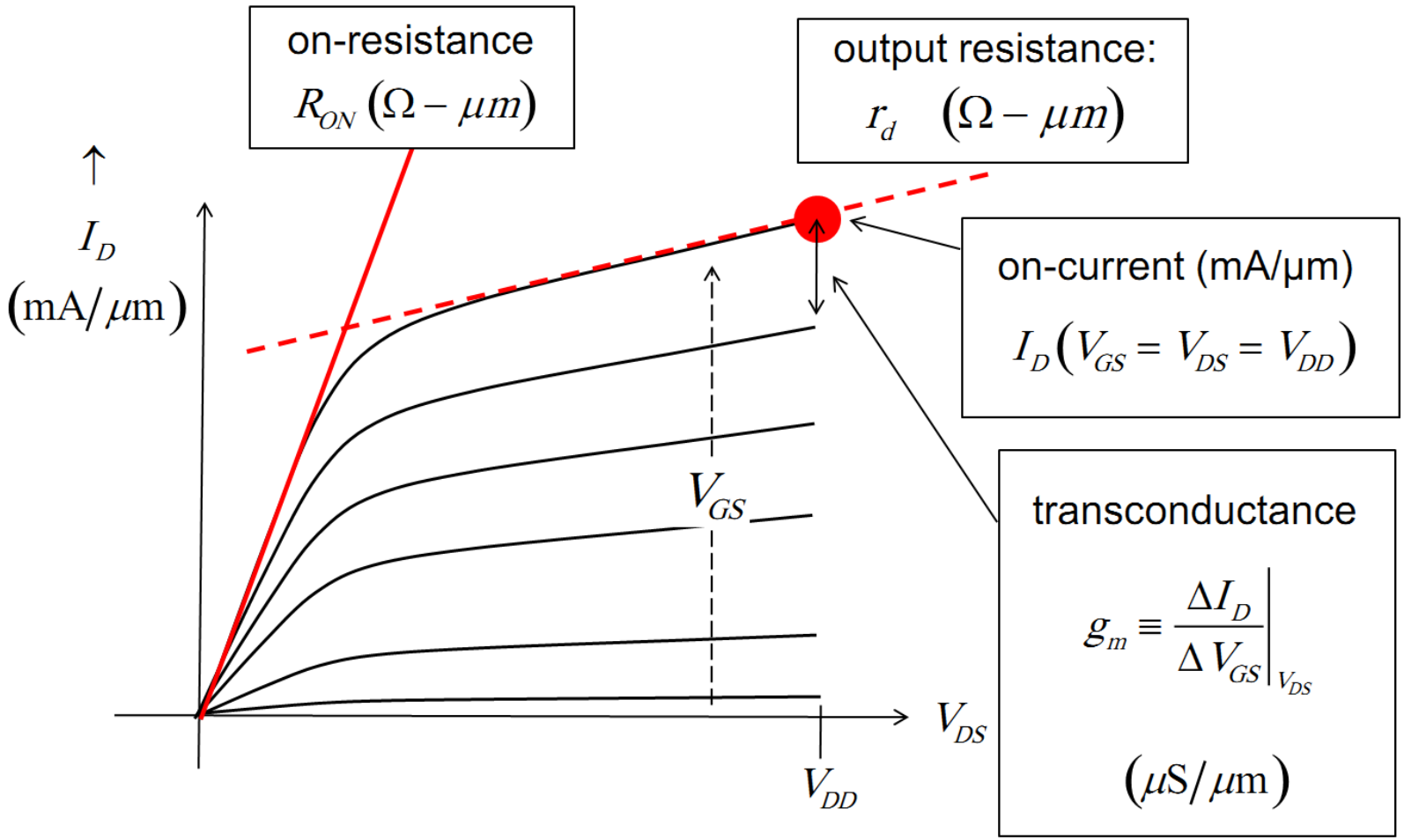
- Input resistance – infinite due to gate oxide

Small-signal model – more advanced

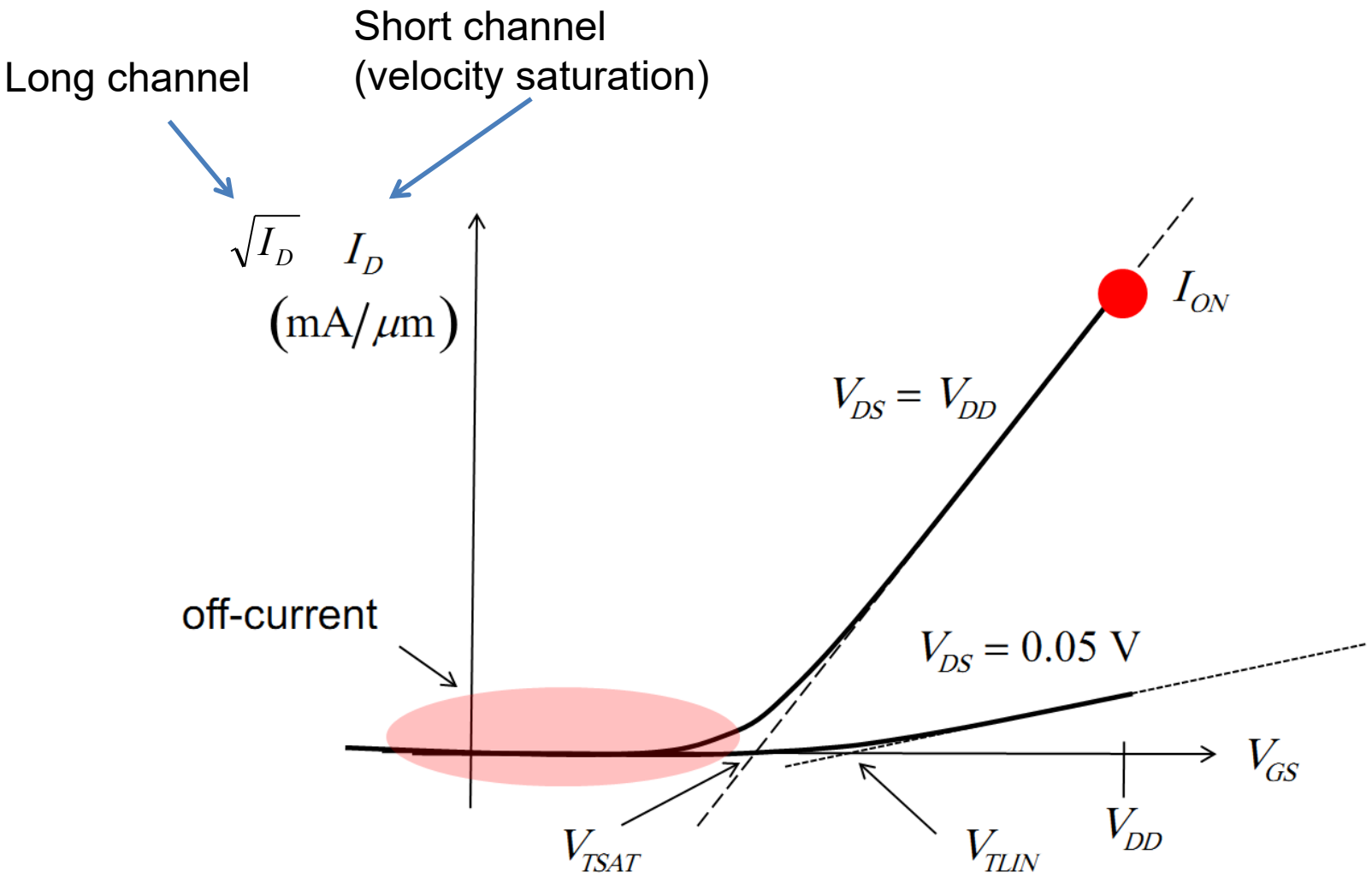
- drain-body / source-body capacitances (C_{db} /C_{sb}) – reversed biased pn-junctions
- gate overlap capacitances (C_{ov})
- gate-body capacitance - outside active device area
- body transconductance – acting as 2nd gate
- source/drain resistances – (not included here)



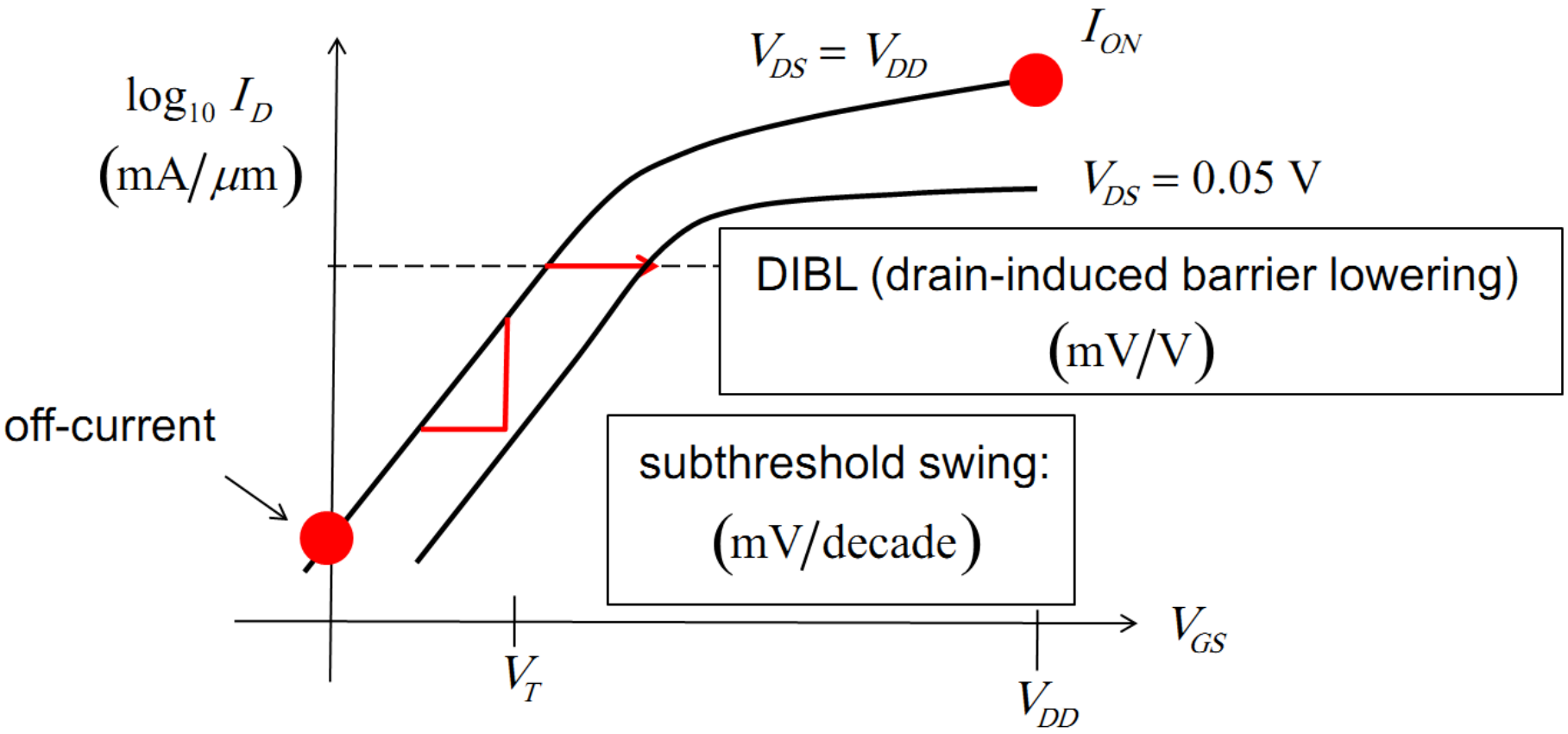
Parameter extraction from output characteristics



Parameter extraction from transfer characteristics



Parameter extraction from transfer characteristics (log)



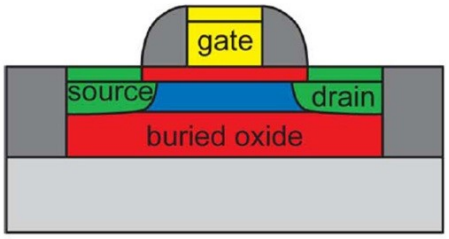
Summary - MOSFETs

- n-type (p-doped substrate) or p-type (n-doped substrate).
- Increasing V_{GS} voltage beyond V_t gives inversion layer (channel) under gate
  Linear (triode): I_D depends on both V_{GS} and V_{DS}.
  Saturation (active):I_D depends only on V_{GS} due to pinch-off of channel at drain.
- Channel length modulation: Increasing V_{DS} beyond pinch-off shortens channel. Increasing I_D with V_{DS}.
- Small signal model:
  - Infinite input resistance due to gate oxide.
  - Output resistance (r_0) due to channel length modulation.
  - Gate-source capacitance (C_{GS}) dominates
  - Can add more capacitances and resistances to get more accurate (and complicated) model.

Electrostatics

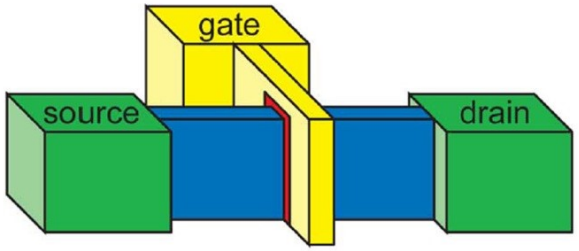
- λ = screening length, reduced by higher gate dielectric constant or thinner channel
- $L_g > 5\,\lambda$ to avoid short channel effects
- More ”wrapping” of the channel reduces λ -> enables L_g scaling
- Progession to FinFETs and Nanowire FETs

planar



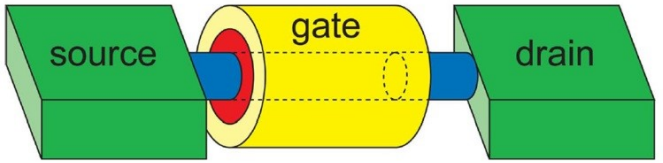
$$\lambda_1 \approx \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} t_{ox} t_{ch}}$$

trigate



$$\lambda \approx \sqrt{\frac{\varepsilon_{ch}}{2\varepsilon_{ox}} t_{ch} t_{ox} \left(1 + \frac{\varepsilon_{ox}}{4\varepsilon_{ch}} \frac{t_{ch}}{t_{ox}}\right)}$$

gate-all-around



$$\lambda \approx \sqrt{\frac{\varepsilon_{ch}}{4\varepsilon_{ox}} t_{ch} t_{ox} \left(1 + \frac{\varepsilon_{ox}}{4\varepsilon_{ch}} \frac{t_{ch}}{t_{ox}}\right)}$$

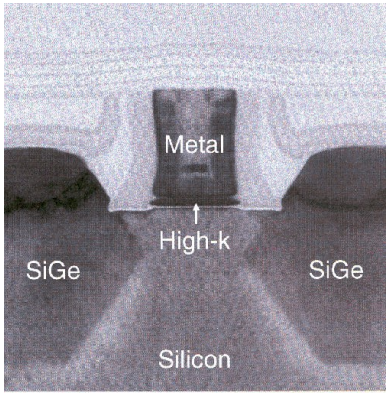
BJTs vs MOSFETs

	BJT	MOSFET
Terminals	Emitter, base, collector	Source, gate, drain, (body)
Symmetric	no (higher doping in emitter)	yes
Transport mechanism	Diffusion	Drift
Current formula (active region)	$I_C = I_S\left(1+\frac{V_{CE}}{V_A}\right)e^{\frac{V_{BE}}{V_T}}$	$I_{D,sat} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_t\right)^2\left(1+\lambda V_{DS}\right)$
Transconductance	$g_m = \frac{I_C}{V_T}$	$g_m = \sqrt{2\cdot\mu_n\cdot C_{ox}\frac{W}{L}I_D}$
Input resistance (r_0)	Finite due to base current	Infinite due to insulating gate oxide

Modern transistors

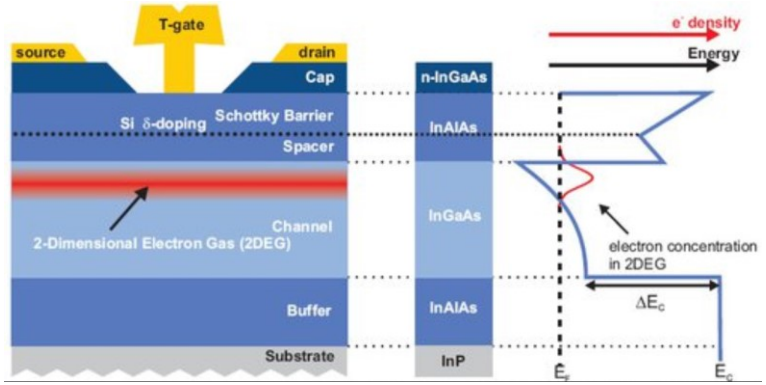
MOSFET

- Strain enhance mobility
- High-k gate dielectric gives higher C_{ox} without leakage current
- Tri-gate enables channel length reduction due to better electrostatic control (less short-channel effects)
- (III-V semiconductors would give higher mobility)



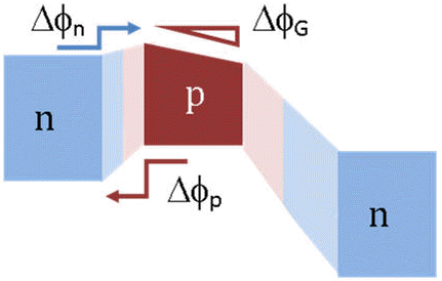
High electron mobility transistor (HEMT)

- III-V semiconductors to get high mobility
- Move doping away from channel to avoid scattering



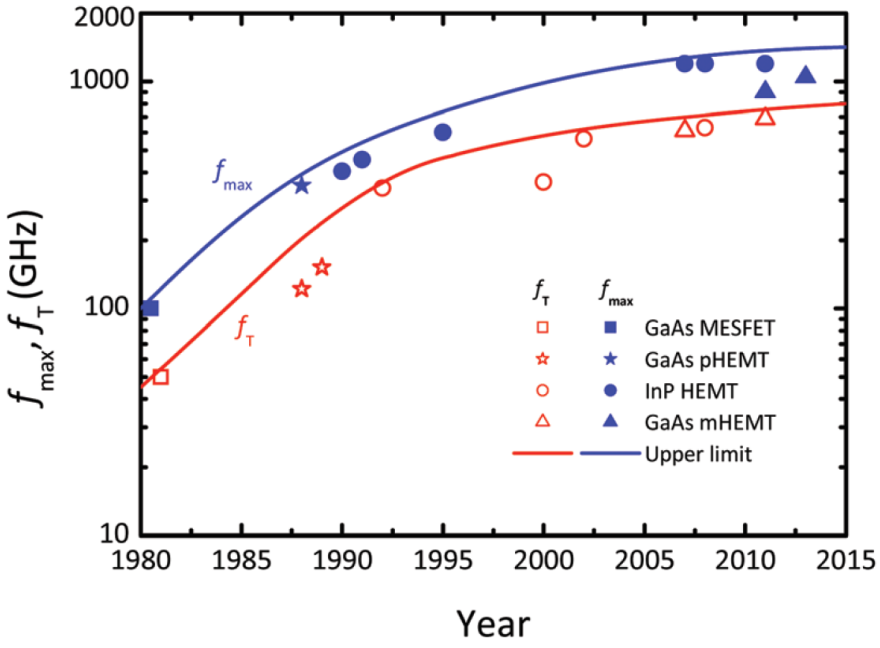
Heterojunction bipolar transistor (HBT)

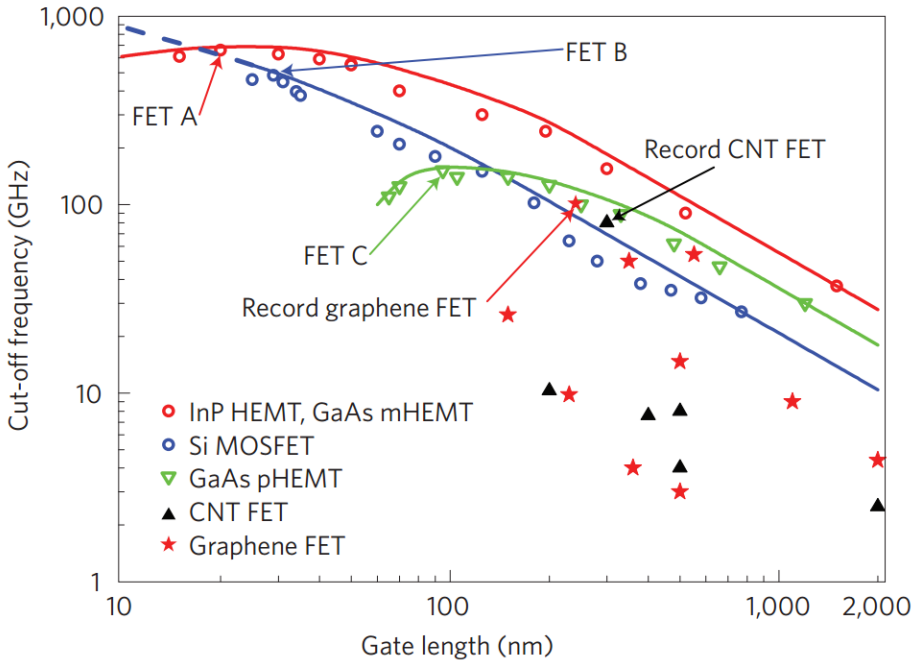
- Combine (III-V) semiconductors with different E_g. Valence band barrier gives less backinjection from base to emitter. Can increase base doping to lower base resistance but keep same gain.



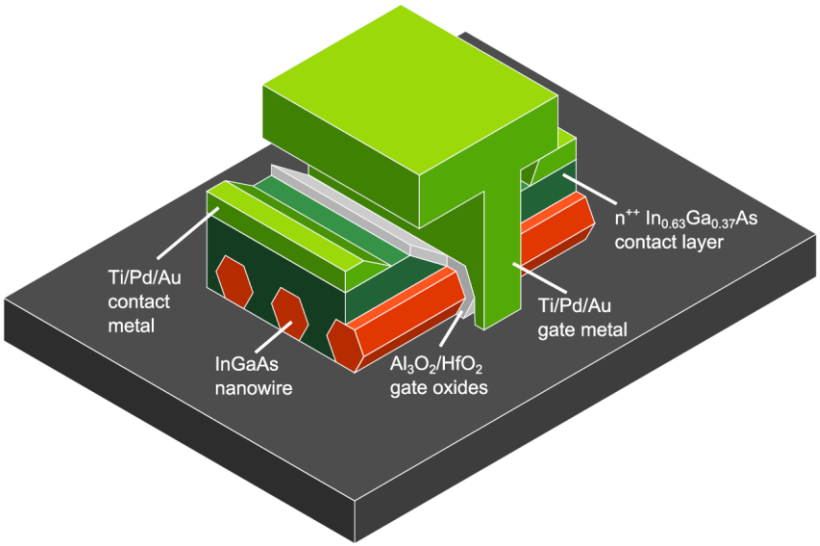
Analog electronics

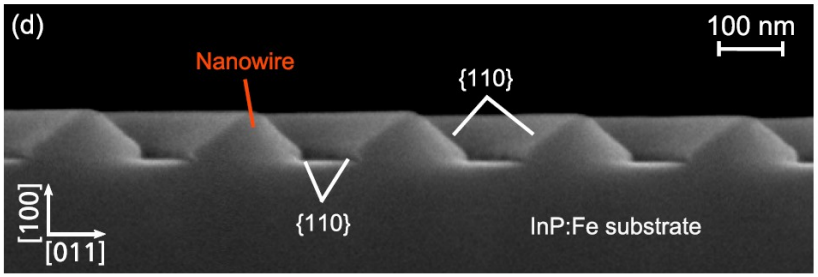
- HEMTs, Si MOSFETs, HBTs
- Improvement due to gate length scaling

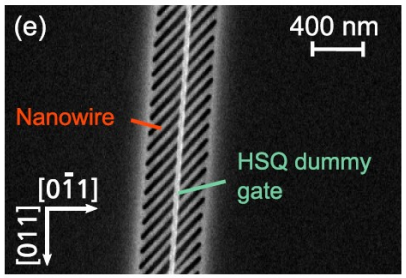


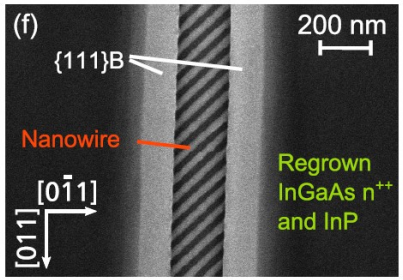


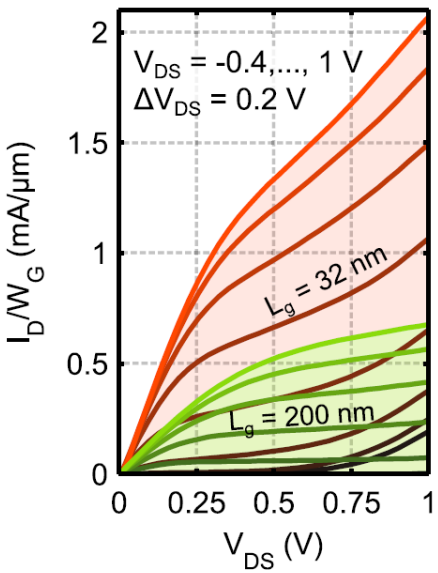
Modern MOSFET – (semi)ballistic III-V nanowires

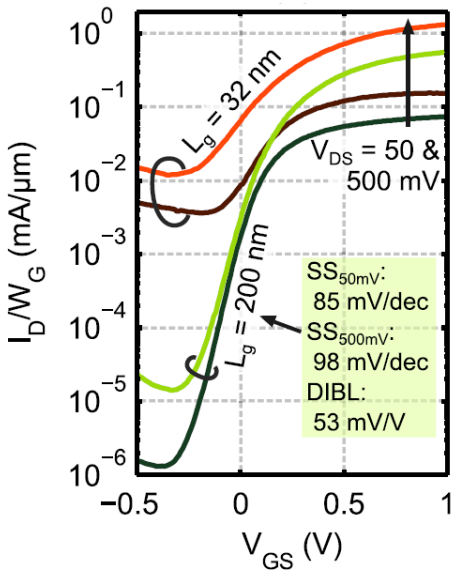












g_m = 3.3 mS/μm
f_T = 280 GHz
f_{max} = 312 GHz