F14 – Memory Circuits

Outline

- Combinatorial vs. sequential logic circuits
- Analogue multivibrator circuits
- Noise in digital circuits
- CMOS latch
- CMOS SR flip flop
- 6T SRAM cell
- 1T DRAM cell
- Memory column-row-block organisation
- Memory peripheral circuits
  - Sense amplifiers, (address decoders, clocks, etc.)

Reading Guide *Sedra/Smith 7ed int*

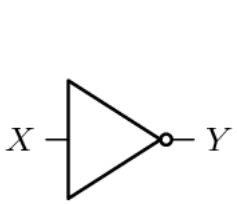
- Chapter 14.4 (bistable multivibrators)
- Chapter 17.1-17.4.1 memory cells
- (Chapter 17.4.2-17.6 (address decoders, ROM, image sensor))

Problems *Sedra/Smith 7ed int*

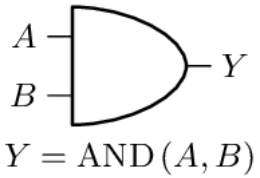
- P17.2, 17.4, 17.15, 17.19

Combinatorial vs. Sequential Logic Circuits

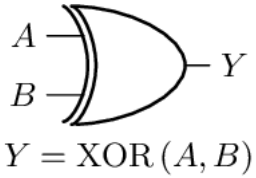
- Digital systems require logic gates and memory circuits
  - Perform logic operations and save the result
  - Store input data until needed in an operation
  - …



$Y = \mathrm{NOT}\,(X)$

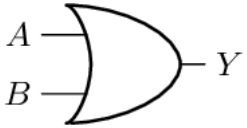


$Y = \mathrm{AND}\,(A, B)$



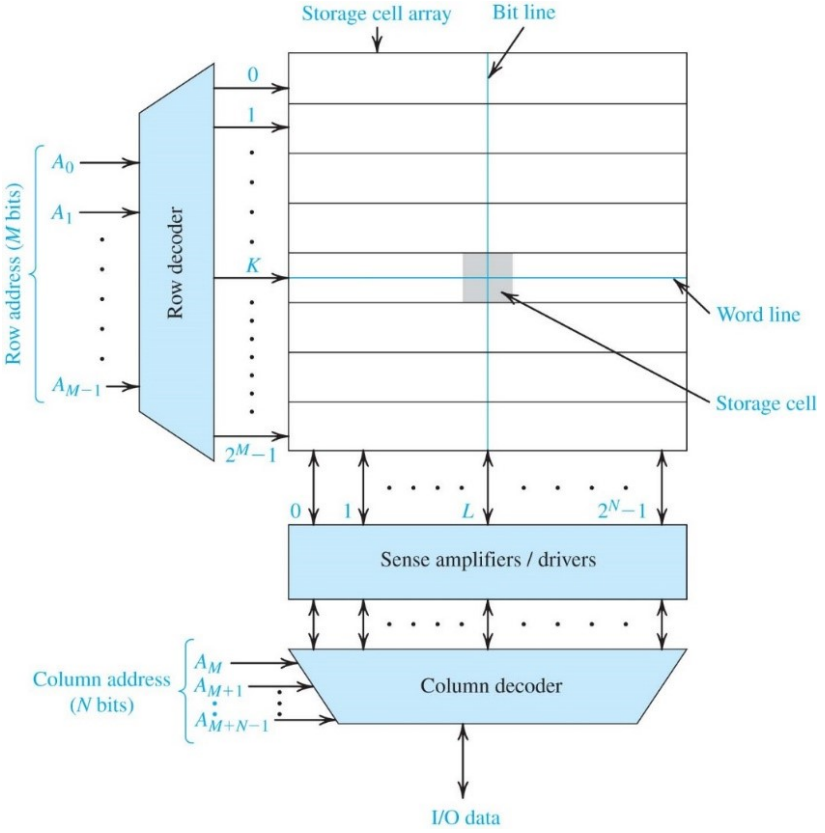
$Y = \mathrm{XOR}\,(A, B)$

- Combinatorial logic circuits (logic gates)
  - Given a specific input, output is always the same



$Y = \mathrm{OR}\,(A, B)$

- Sequential logic circuits (memory circuits)
  - Given a specific input, output may depend on history

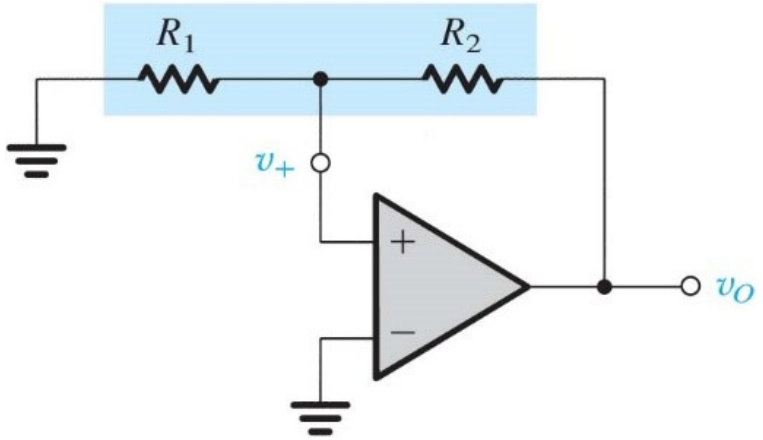


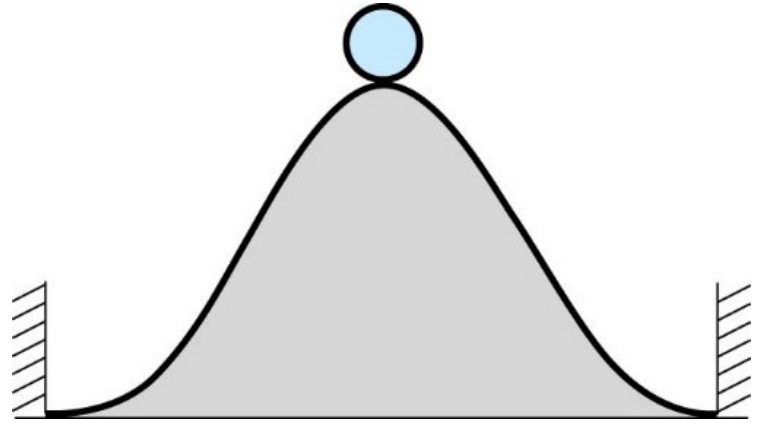
Analogue Multivibrator Circuits

- Bistable, a.k.a. latch
  - Retains its state until change is triggered
  - A circuit with two stable operating points, e.g. an op amp with positive feedback

- (Astable, a.k.a. function generator)
  - Switches states periodically
  - Self-triggered bistable multivibrator utilising an additional feedback circuit with delay

- (Monostable, a.k.a. pulse generator)
  - Switches state momentarily when triggered
  - A circuit with one stable state and one quasi-stable state that initiates self-triggering at predefined delay





Bistable circuits exhibit memory functionality, but analogue versions are large and power hungry.

Bistable Multivibrator Operation

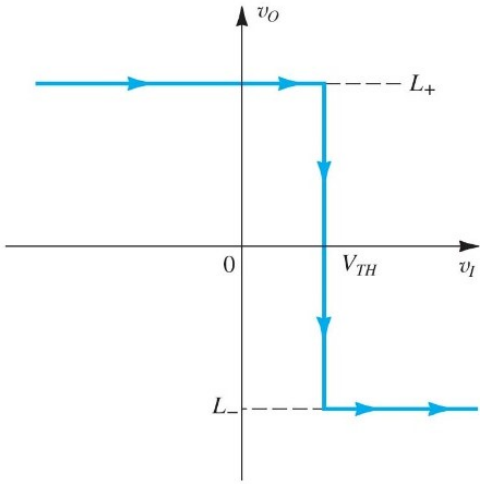
- Trigger input applied to either of “grounds” in bistable multivibrator circuit

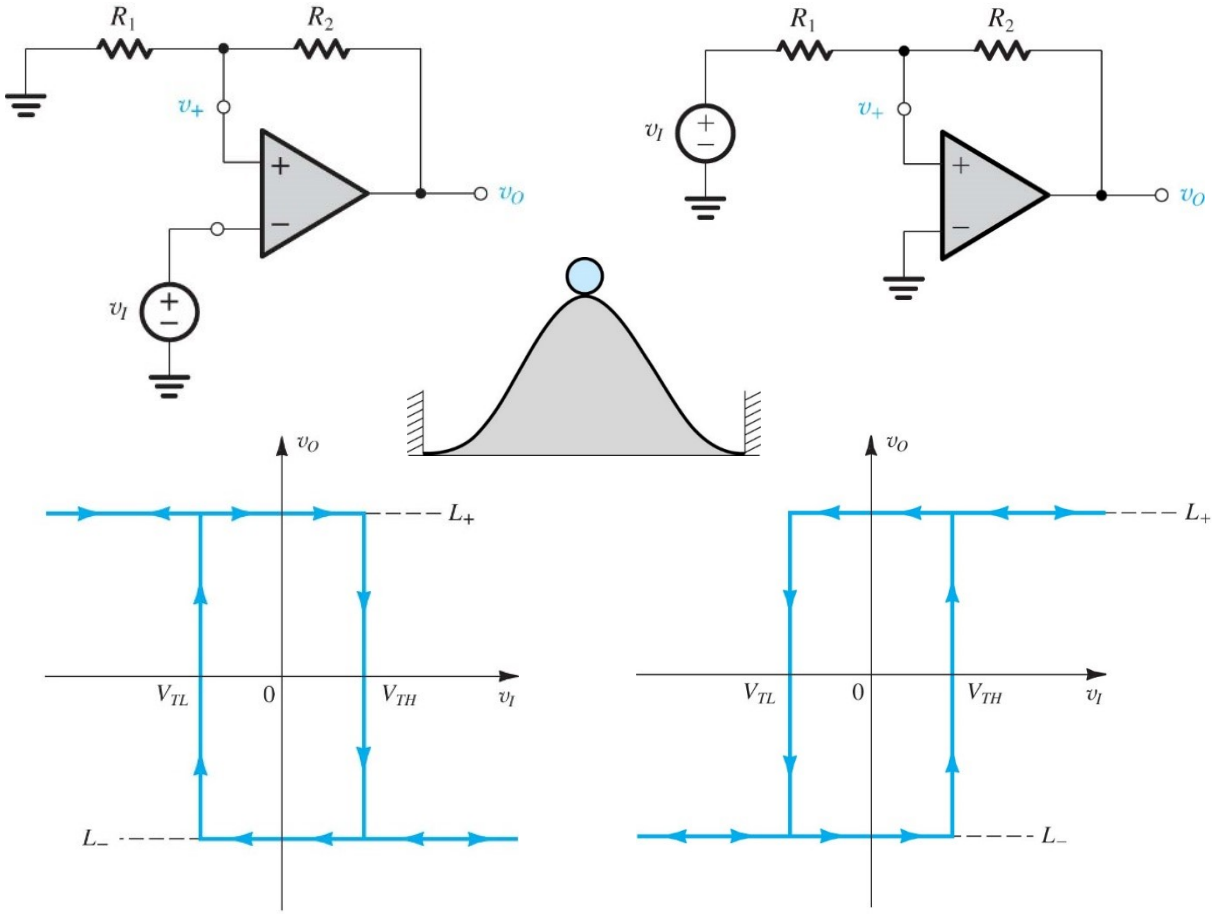
- Toggling output from high to low, using trigger at inverting input

$$v_+ = \beta v_O, \qquad v_O = A(v_+ - v_-) \rightarrow L_\pm$$

$$v_- = v_I < v_+, \qquad v_+ = \beta v_O = \beta A(v_+ - v_-) \rightarrow \beta L_+$$

$$v_I > \beta L_+ \Rightarrow v_+ - v_- < 0 \Rightarrow v_O = L_- \Rightarrow v_+ = \beta L_-$$

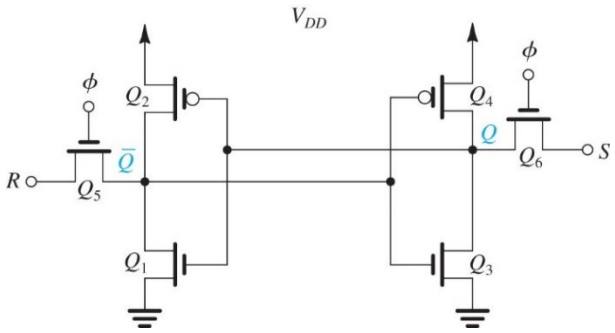




Trigger input point determines if characteristic is inverting or non-inverting.

Noise Sources

- Power supply noise due to switching logic gates, output stages, etc.



- Thermal noise(/ hot electron noise)
  - Carrier energy fluctuations due to temperature(/ apparent temperature)

$$S_{v,Thermal}(\omega) = \frac{\overline{v^2}}{\Delta f} = 4kTR \Leftrightarrow S_{v,Thermal}(\omega) = \frac{\overline{i^2}}{\Delta f} = 4kTG$$

- Shot noise
  - Carrier fluctuations due to MOSFET gate tunnelling

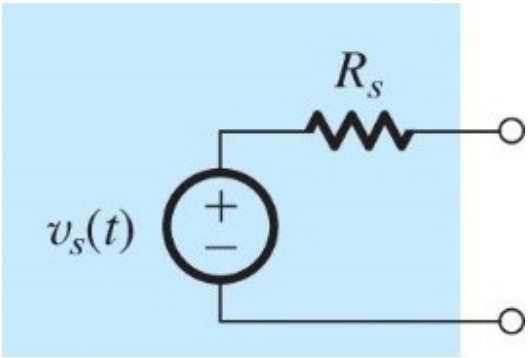
$$S_{i,Shot}(\omega) = \frac{\overline{i^2}}{\Delta f} = 2qI_G$$

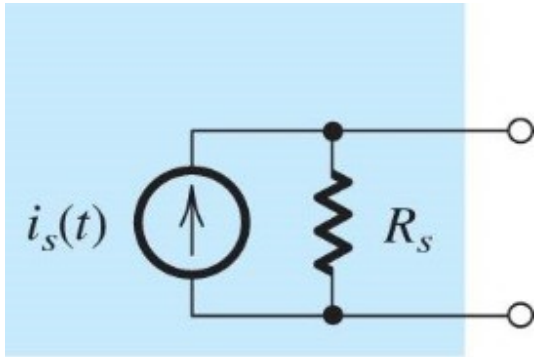
- Burst noise
  - Carrier fluctuations due to MOSFET channel interaction with a trap with a time constant

$$S_{i,Burst}(\omega) = \frac{\overline{i^2}}{\Delta f} = k_{Burst}\frac{I_D}{1+(\omega\tau)^2}$$

- Flicker noise
  - Carrier fluctuations due to MOSFET channel interaction with multiple traps with evenly distributed time constants

$$S_{i,Flicker}(\omega) = \frac{\overline{i^2}}{\Delta f} = k_{Flicker}\frac{I_D}{f}$$

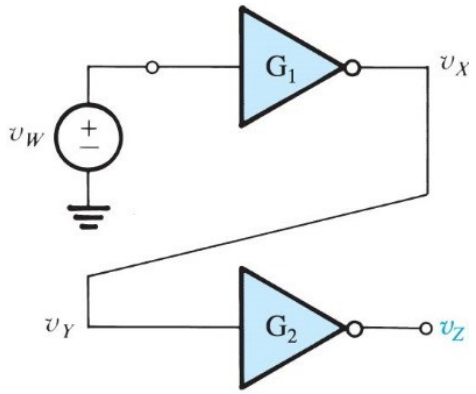


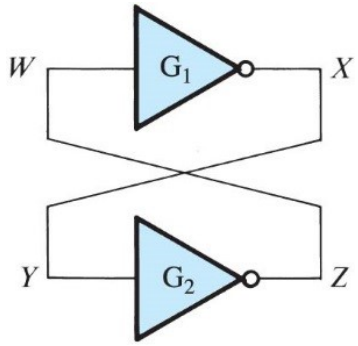


Basic CMOS Latch

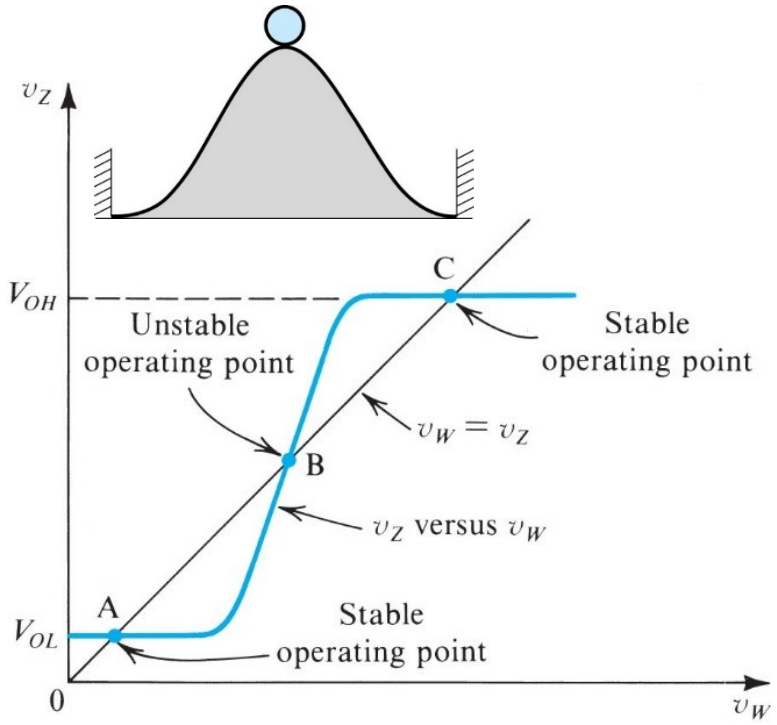
- Latch (bistable multivibrator) circuit
  - Retains its own output signal by means of positive feedback

- Basic CMOS latch
  - Two inverters in positive feedback loop
  - Inverted output fed back to input of the same inverter
  - Three possible operating points
    - Low/ high
    - Midpoint
    - High/ low





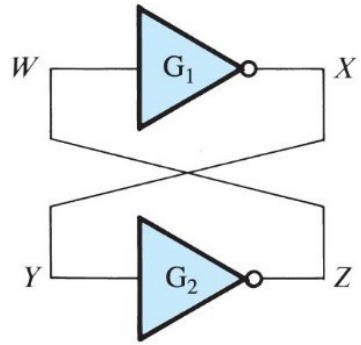
W	$X = Y$	Z
0	1	0
1	0	1

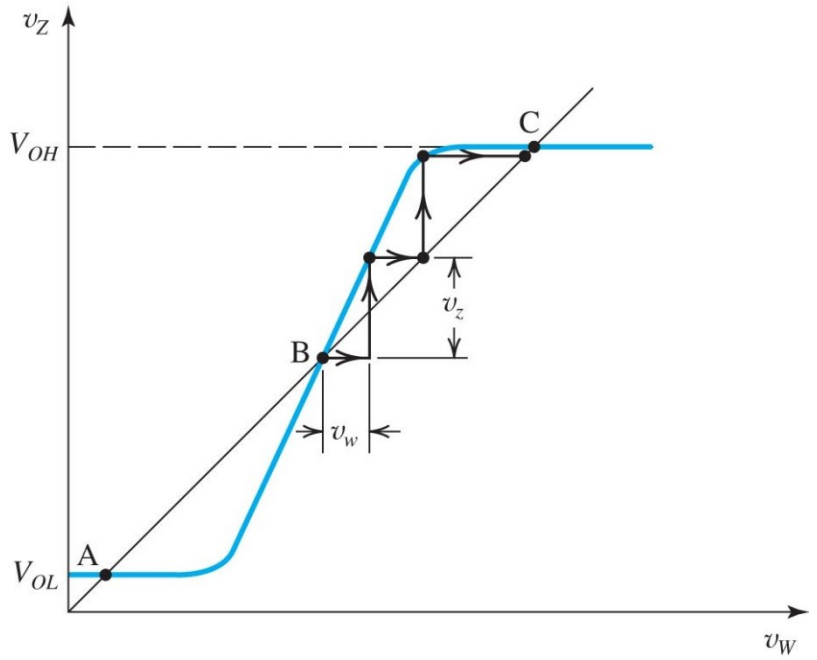


Latch provides volatile memory, requiring power supply for data storage, at minimal static power.

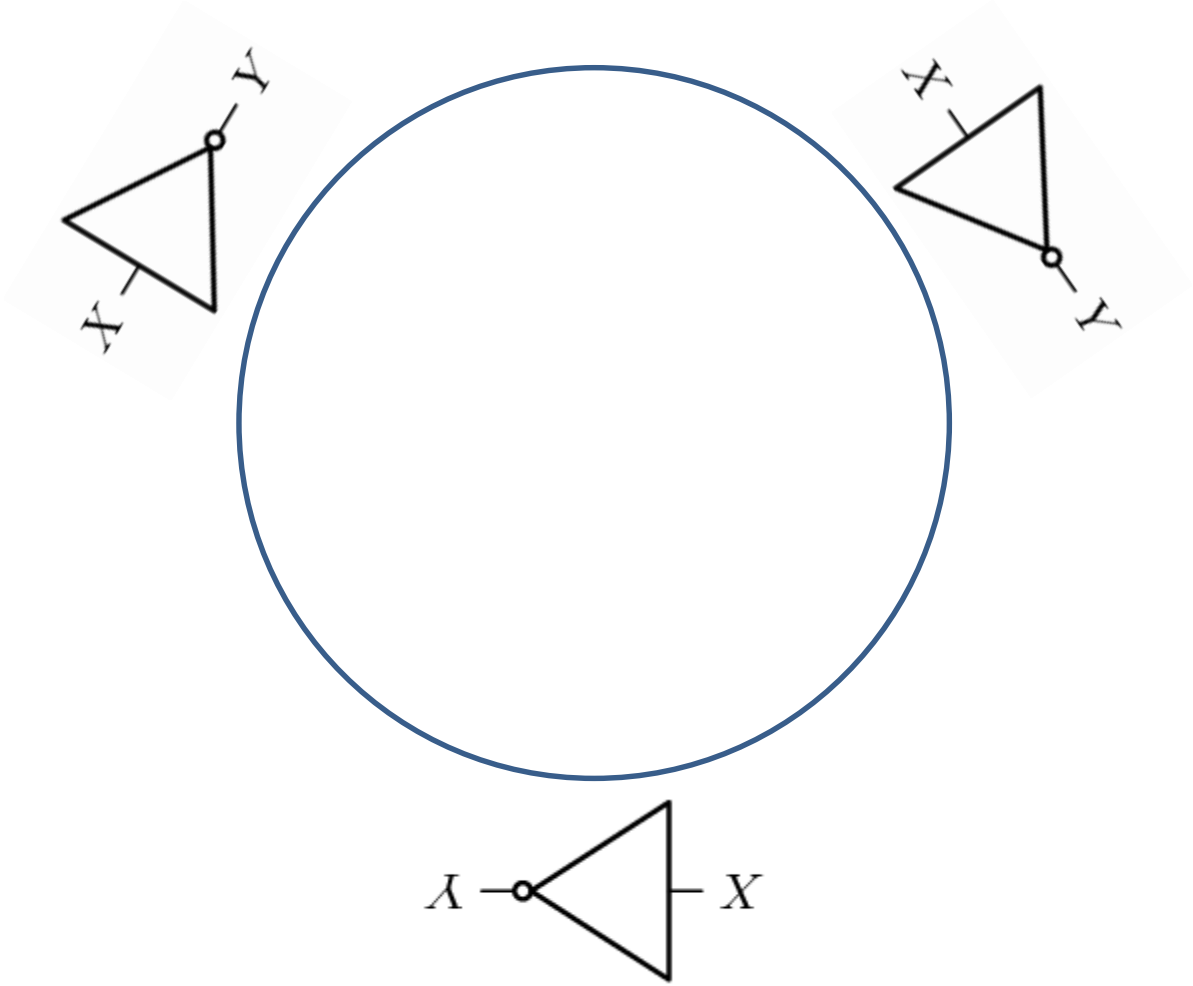
Basic Latch Operation

- Three possible operating points
  - A: Low/ high
  - B: Midpoint (unstable)
  - C: High/ low
- Operation at slight offset above(/ below) B will initiate regenerative latch process towards A(/ C)
- Inverter butterfly diagram can be used to illustrate operation points and noise margins





Two inverters in a loop yields latched output, but what about three inverters?



Two Input NOR Gate (recap)

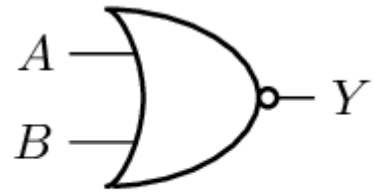
- Logic (boolean) NOT-OR compound function
  - Inputs, $\{A, B\}$

    $A, B \in \{0, 1\}$

  - Output, Y

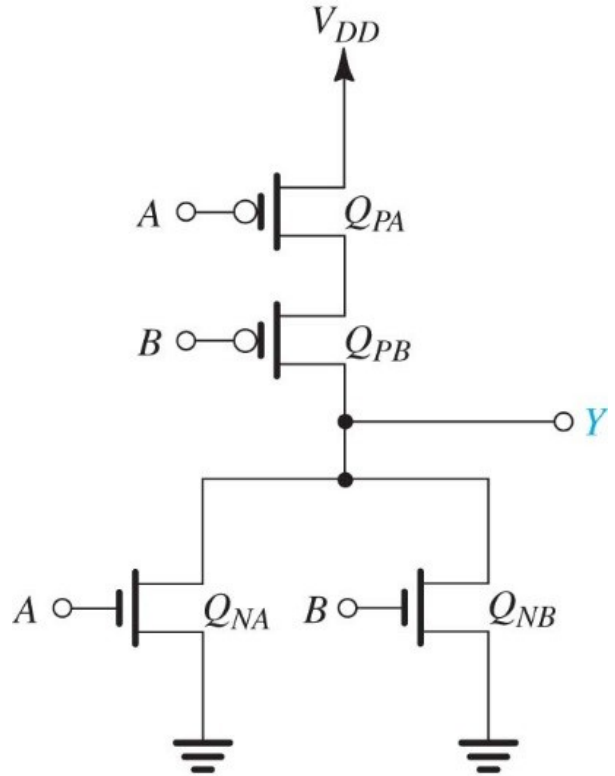
    $$Y = \overline{A + B} = \bar{A}\bar{B} = \begin{cases} 1, & (A = 0, B = 0) \\ 0, & \text{otherwise} \end{cases}$$

- CMOS NOR gate
  - PUN, $Y = \bar{A}\bar{B}$
    - One series branch with all inputs
  - PDN, $\bar{Y} = A + B$
    - One parallel branch for each input



$Y = \text{NOR}(A, B)$

A	B	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0



$Y = \overline{A + B}$

Inclusive OR function, dissimilar from exclusive XOR function.

Set/ Reset (SR) Flip Flop

- SR flip flop: latch with trigger inputs
  - Two NOR gates in latch configuration allow set/ reset trigger operations

- Storage mode
  - R and S low, i.e. $\bar{R}\bar{S}$, preserves latched output

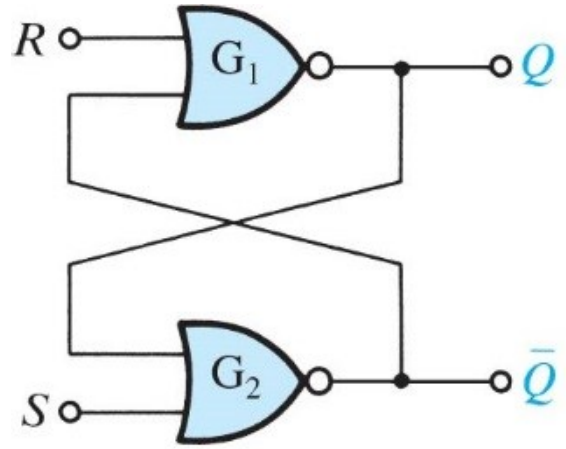
$$Q_{n+1} = \mathrm{NOR}(\bar{R}, \overline{Q_n}) = Q_n, \qquad \overline{Q_{n+1}} = \mathrm{NOR}(\bar{S}, Q_n) = \overline{Q_n}$$

- Set operation
  - R low, S high yields Q forced high

$$\overline{Q_{n+1}} = \mathrm{NOR}(S, Q_n) = 0 \Rightarrow Q_{n+1} = 1$$

- Reset operation
  - R high, S low yields Q forced low

$$Q_{n+1} = \mathrm{NOR}(R, \overline{Q_n}) = 0$$



R	S	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	Q_n	$\overline{Q_n}$
0	1	1	0
1	0	0	1
1	1	Not used	Not used

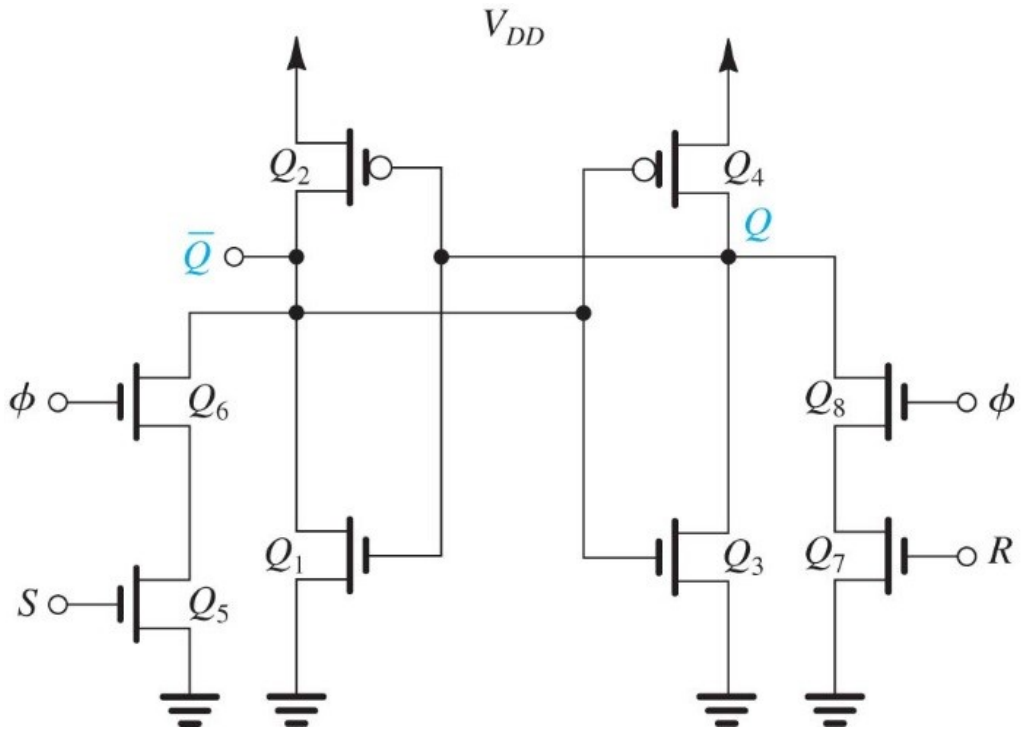
Complementary SR flip flop using NAND gates is also possible, etc.

Clocked SR Flip Flop

- Inverter latch with clocked set/ reset inputs
  - Clock, ϕ, form AND functions with respective trigger inputs, S and R
    - Trigger inputs ignored when clock is low, $\bar{\phi}$
  - Clock and trigger inputs use NMOS transistors only

- Requirements for set operation
  - Q5-Q6 sink enough current to pull $\bar{Q}$ below threshold of Q3-Q4 inverter
  - Set signal remains high long enough to cause regeneration to take over the switching process

- Requirements for reset (parallels set due to symmetry)
  - Q7-Q8 sink … Q below threshold… Q1-Q2 inverter
  - Reset signal remains high…



Superior functionality at same transistor count as SR flip flop: clock low enforces storage mode.

Set Operation on Clocked SR Flip Flop: Part I

- Set operation on clocked SR flip flop in reset storage mode

$$v_\phi = V_{DD}, \qquad v_S = V_{DD}, \qquad v_R = 0\ \text{V}$$

$$Q_n = 0, \qquad \overline{Q_n} = 1, \qquad \phi S\bar{R} = 1$$
$$\Rightarrow Q_{n+1} = 1, \qquad \overline{Q_{n+1}} = 0$$

- Part I: Q5-Q6 must pull $\overline{Q_{n+1}}$ down past midpoint…

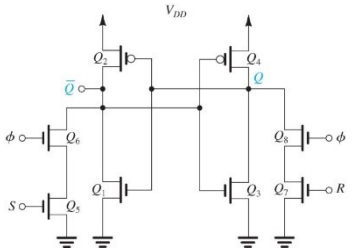
$$v_Q = 0, \qquad v_{\bar{Q}} < \frac{V_{DD}}{2} \Rightarrow I_{D2} < I_{D5} = I_{D6} \approx I_{Deq}\Big|_{\frac{1}{2}\left(\frac{W}{L}\right)_{5,6}}$$

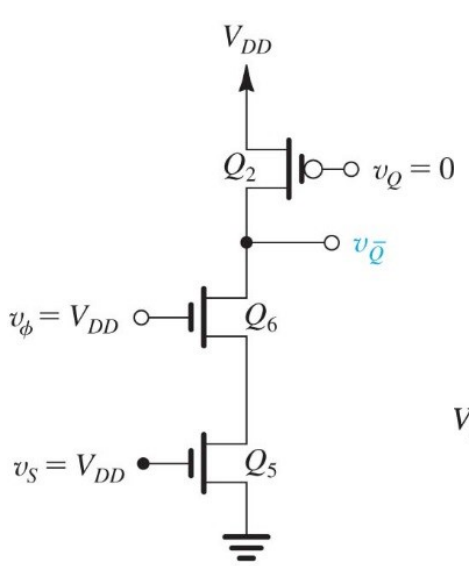
$$I_{D2} = I_{Deq} = i_{Dx}\left(|V_{GS}| = V_{DD}, |V_{DS}| = \frac{V_{DD}}{2}\right)$$

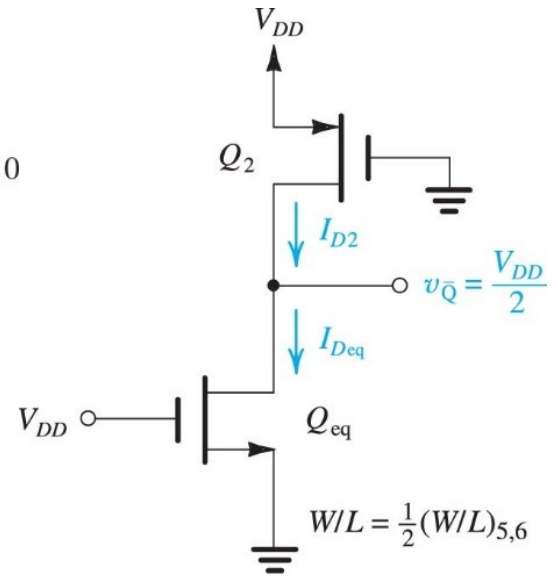
$$i_{Dx} = k'_x\left(\frac{W}{L}\right)_x\left[V_{DD} - V_{tx} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)\right]\left(\frac{V_{DD}}{2}\right)$$

$$\Rightarrow \left(\frac{W}{L}\right)_{5,6} > 2\frac{k'_p}{k'_n}\left(\frac{W}{L}\right)_2$$

- Part II: … and hold at least until latch responds







Reset operation parallels that of set operation.

Set Operation on Clocked SR Flip Flop: Part II

- Set operation on clocked SR flip flop in reset storage mode

  $v_\phi = V_{DD}, \quad v_S = V_{DD}, \quad v_R = 0\ \text{V}$

  $Q_n = 0, \quad \overline{Q_n} = 1, \quad \phi S\bar{R} = 1$
  $\Rightarrow Q_{n+1} = 1, \quad \overline{Q_{n+1}} = 0$

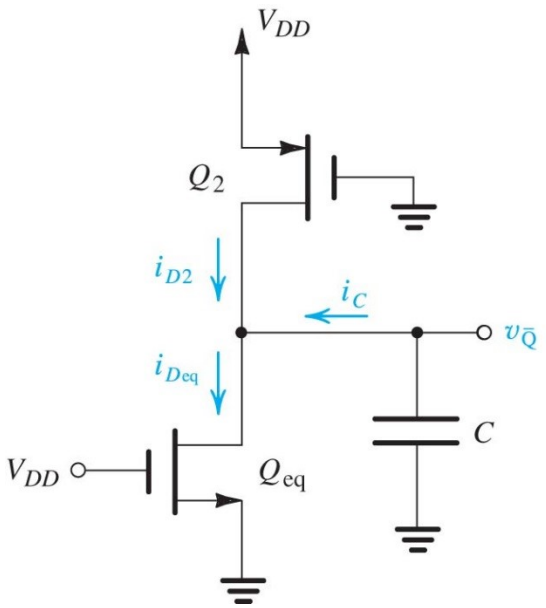
- Part I: Q5-Q6 must pull $\overline{Q_{n+1}}$ down past midpoint…

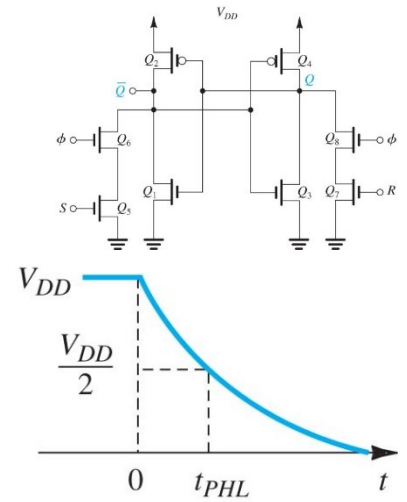
- Part II: … and hold at least until latch responds
  - Flip…

    $v_Q = 0, \quad v_{\bar{Q}} = V_{DD} \rightarrow \frac{V_{DD}}{2} \Rightarrow t_{PHL}(\text{Qeq}-\text{Q2}) = \frac{CV_{DD}}{2I_{PHL}}$

  - … flop

    $v_{\bar{Q}} \approx 0, \quad v_Q = V_{DD} \rightarrow \frac{V_{DD}}{2} \Rightarrow t_{PLH}(\text{Q3}-\text{Q4}) = \frac{CV_{DD}}{2I_{PLH}}$





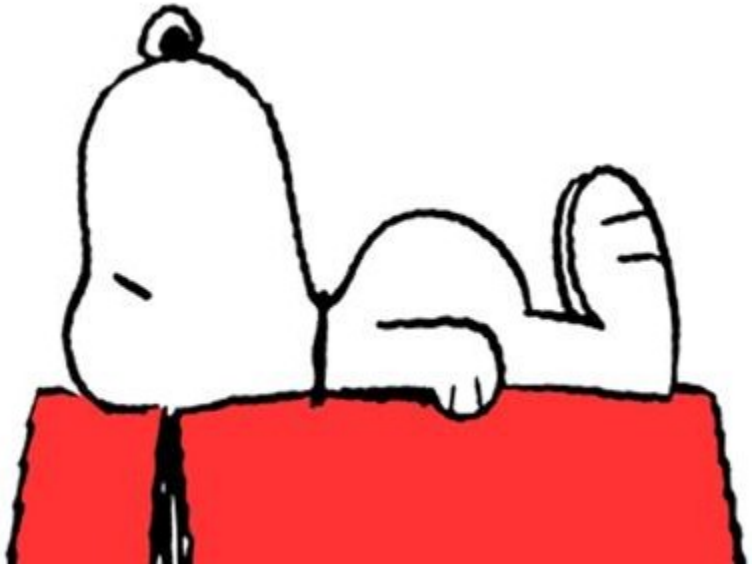
$$T_{min} = t_{PHL}(\text{Qeq}-\text{Q2}) + t_{PLH}(\text{Q3}-\text{Q4})$$

$$I_{PHL} \approx i_{Deq}\Big|_{t=0} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_{eq}(V_{DD} - V_{tn})^2$$

$$I_{PLH} \approx i_{D4}\Big|_{t=t_{PHL}} = \frac{1}{2}k_p'\left(\frac{W}{L}\right)_4(V_{DD} - |V_{tp}|)^2$$

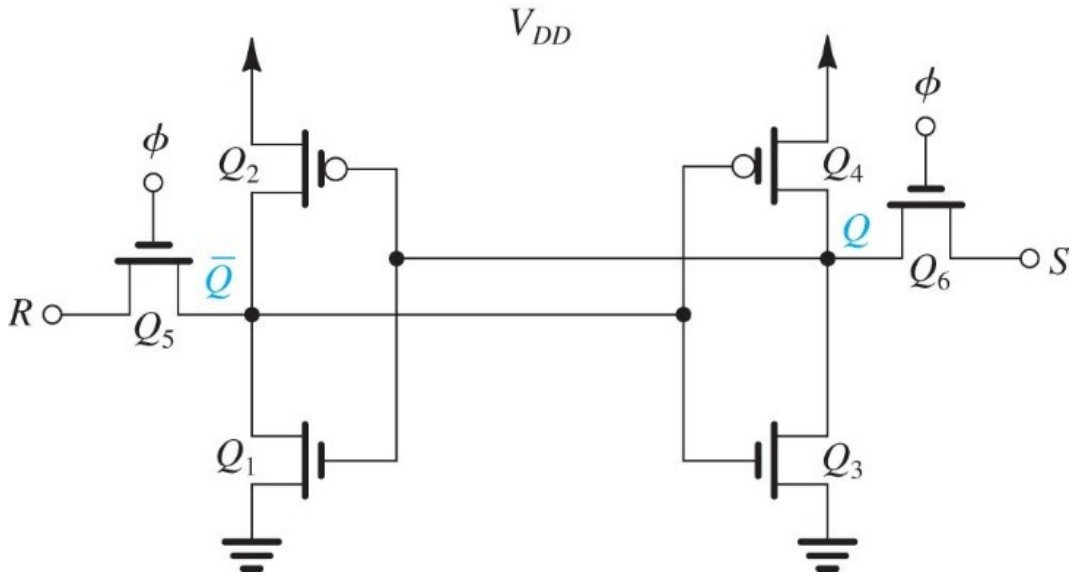
Reset operation parallels that of set operation.

BREAK



6T Static Random Access Memory (SRAM) Cell

- Simplified implementation of the CMOS clocked SR flip flop
  - CMOS inverter latch
    - Q1-Q2 and Q3-Q4
  - Set/ reset and output are all provided through clocked access transistors (cf. pass transistor logic)
    - Q5 and Q6
- Storage mode, $\bar{\phi}$
- Reset operation, $\phi\bar{S}R$
- Set operation, $\phi S\bar{R}$
- Read operation, ϕ
  - Must be controlled to not accidentally set or reset the 6T cell

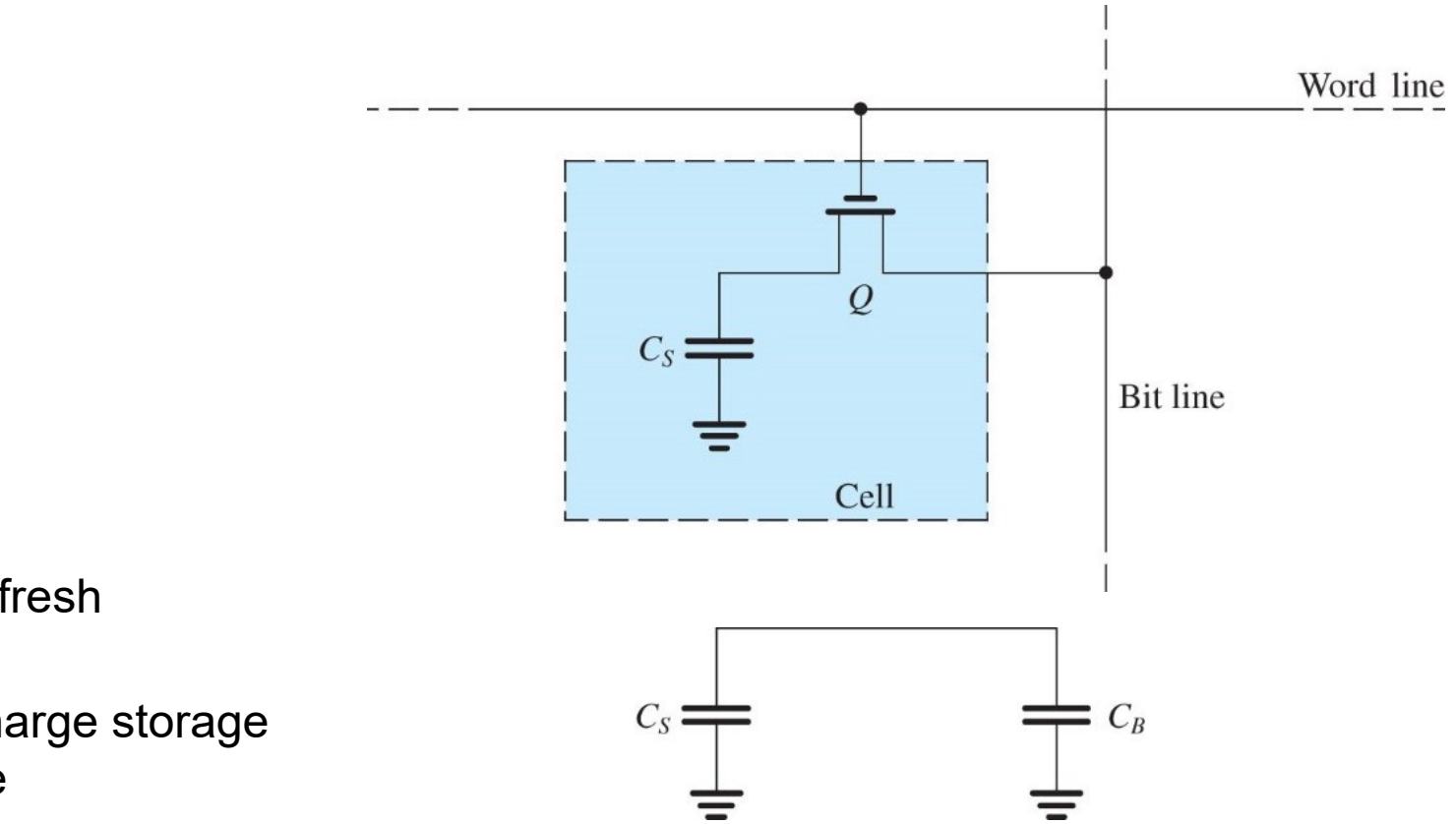


This is the industry standard volatile static memory cell.

1T Dynamic RAM (DRAM) Cell

- One single access transistor
- Storage capacitor
  - Logic 0: not charged
  - Logic 1: charged
- Read operation exchanges charges with bit line
- Leakage demands periodic refresh
- Word line boost required to charge storage capacitor to full supply voltage

$$v_{OV} = v_W - v_{C_S} - V_{tn} \Rightarrow v_w = V_{DD} + V_{tn}$$

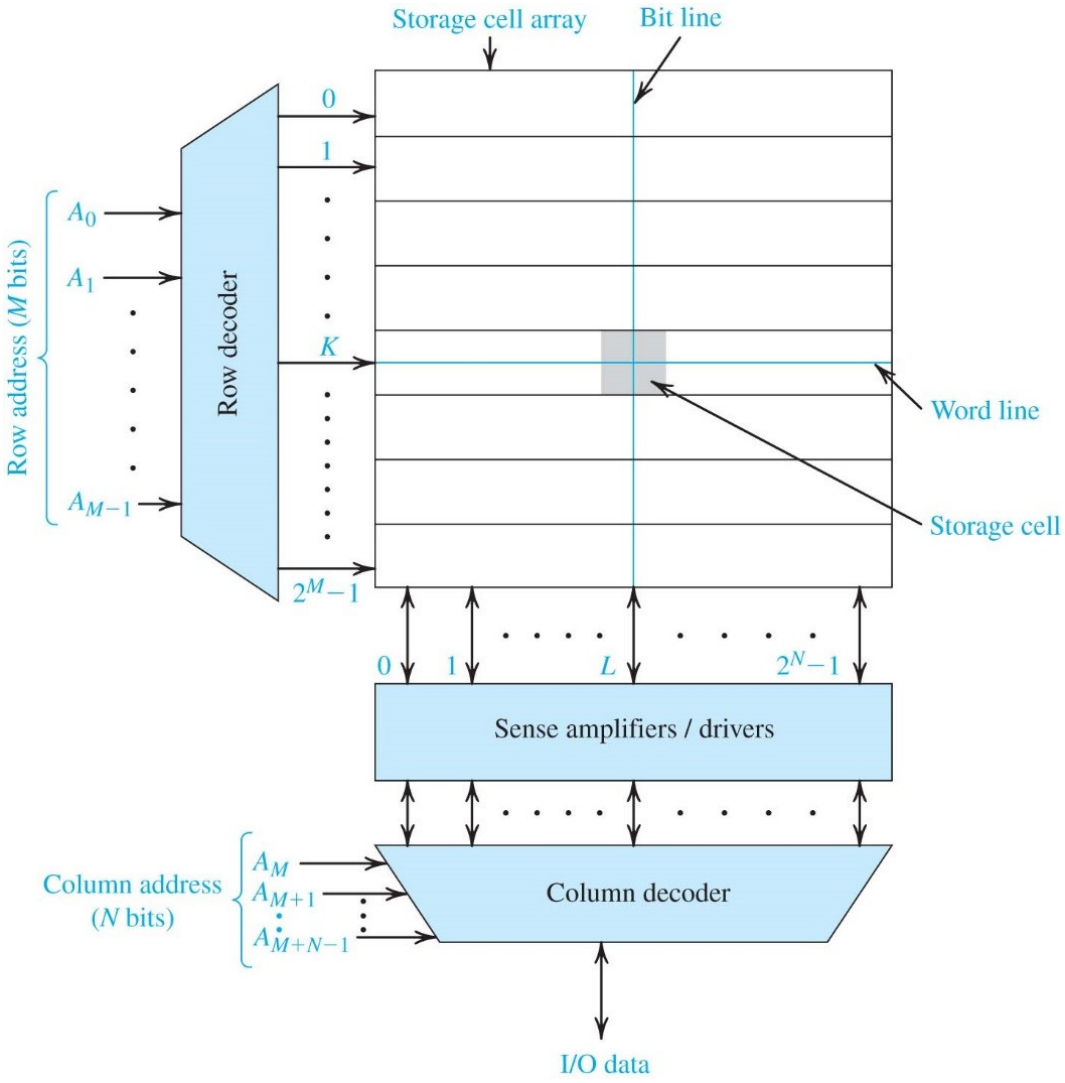


1T is dynamic, requiring periodic refresh on millisecond time scale.

Memory Chip Column-Row-Block Organisation

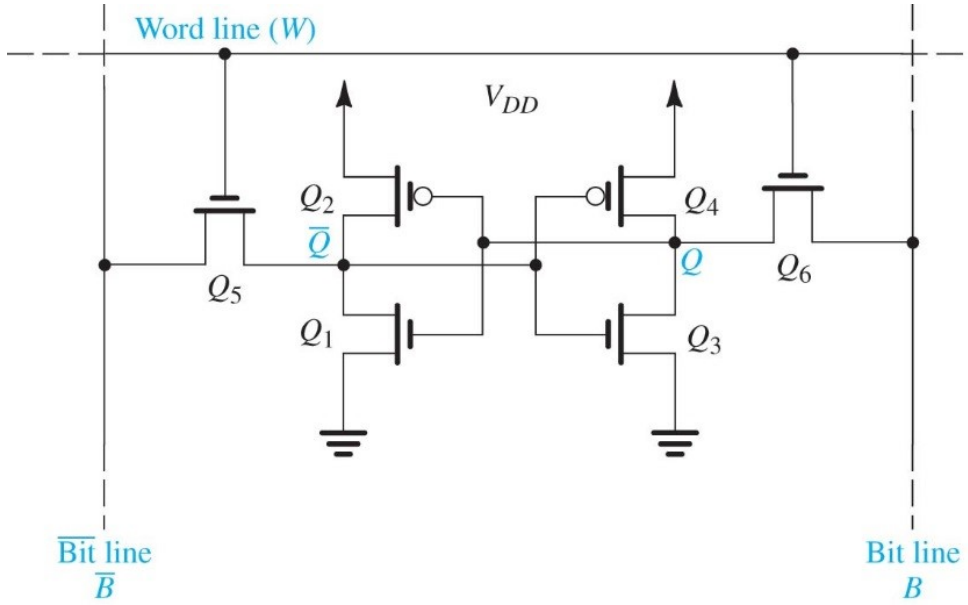
- Memory organisation needed to (time/ energy) efficiently read or write data in a controlled fashion
  - Matrix minimizes bit and word line RC time constant
    - Bits stored in columns
    - Words in rows (across columns)
  - Several blocks required for large memories

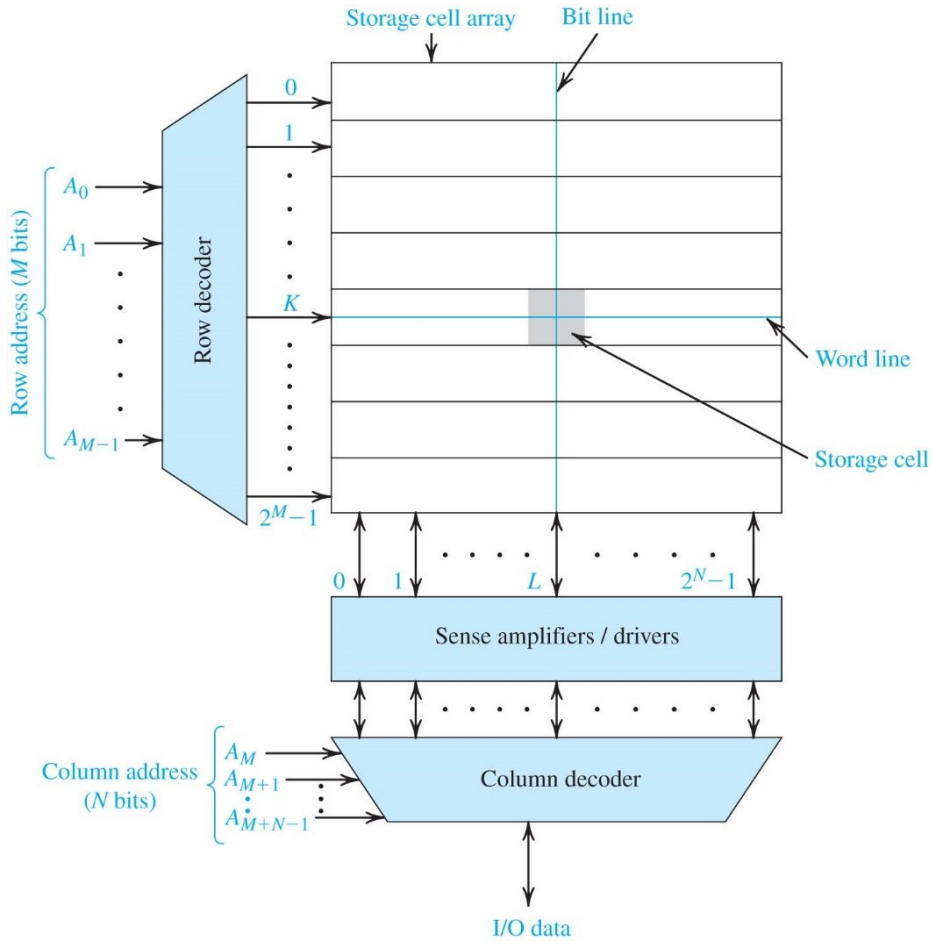
- Memory peripheral circuits
  - Row and column address decoders, built from combinatorial logic circuits
  - Precharge and equalisation for differential bit line preconditioning
  - Sense amplifiers read data from memory cells
  - Drivers write data into memory cells



6T SRAM Cells in a Memory Block

- Row address lets row decoder activate all access transistors in a specific row
- Column address lets column decoder operate on a pair of complementary bit lines
  - Read to or write from I/O data bus

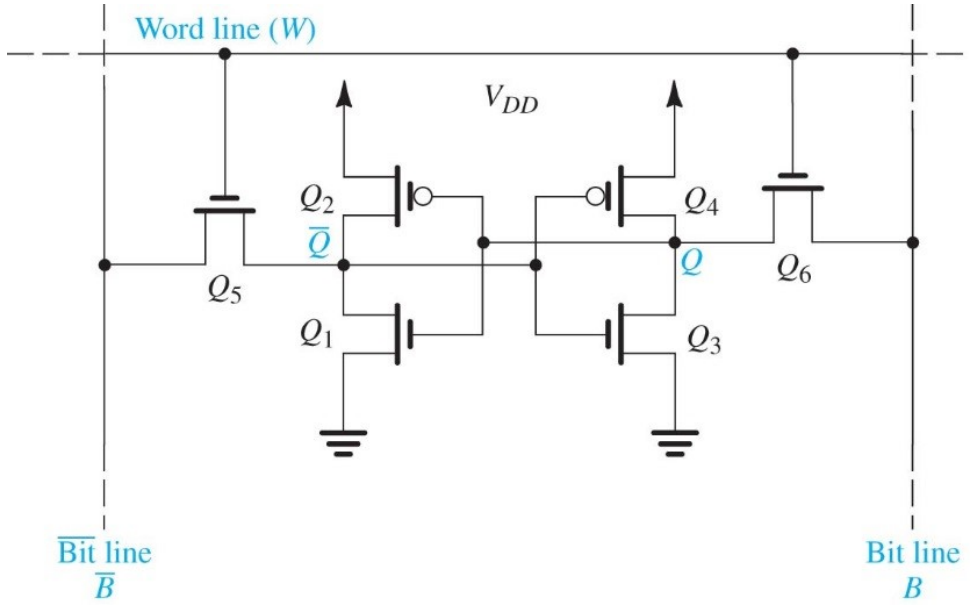


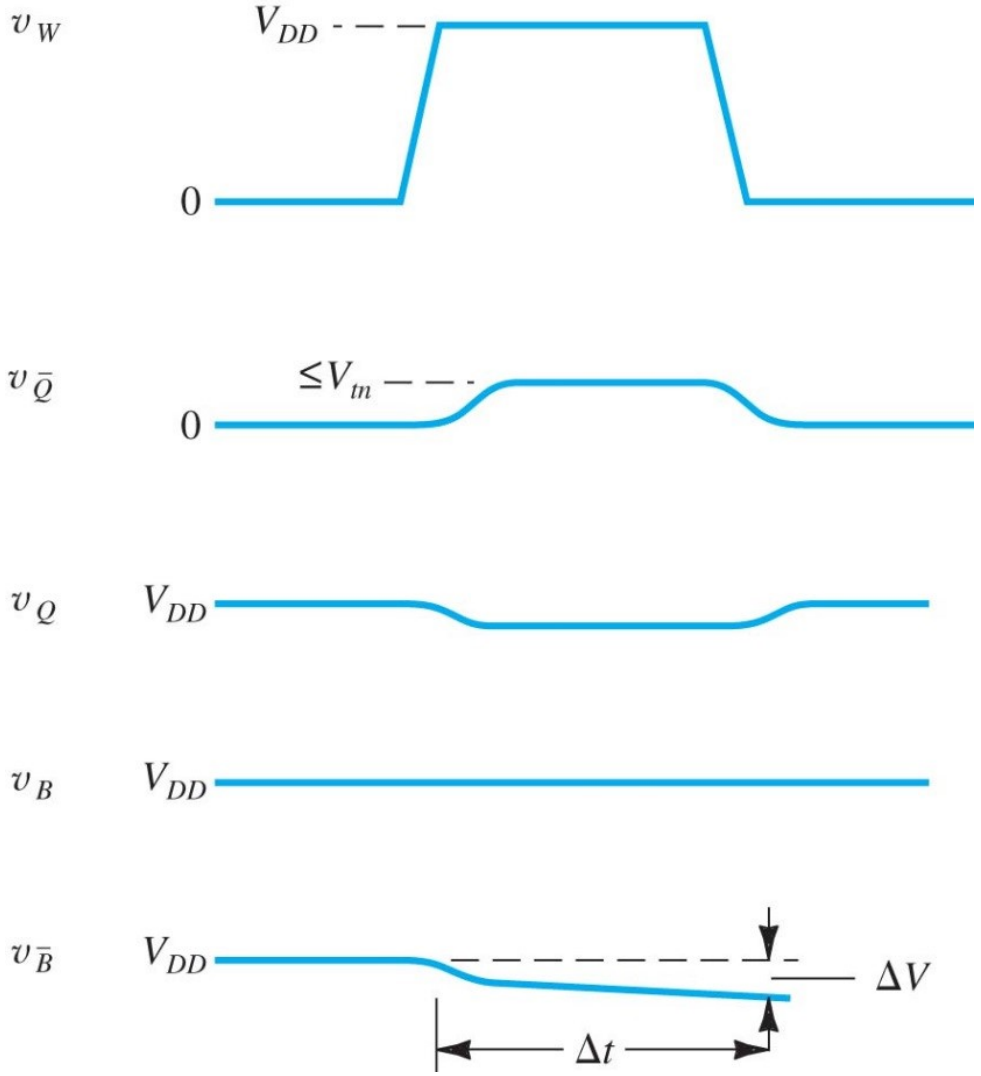


Memory cycle time is on nanosecond time scale, limited by word line RC and sense response.

6T SRAM Cell Operation Conditions

- Read and write functionality through access transistors
- Read operation must not shift the logic level more than a threshold voltage from stored value
- Write operation must toggle the logic level to within a threshold voltage of new value





6T SRAM Cell: Reading a Stored Logic 1

- Initial data and bit lines precharged to supply voltage

$$V_{\overline{Q_n}} = 0\ \text{V}, \qquad V_{Q_n} = V_{DD}, \qquad v_{\bar{B}}\Big|_{t=0} = V_{DD}, \qquad v_B\Big|_{t=0} = V_{DD}$$

- Non-destructive read 1 operation

$$v_{\bar{Q}} < V_{\overline{Q_n}} + V_{tn} = V_{tn}$$

$$I_5 = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_5\left(V_{DD} - V_{\bar{Q}} - V_{tn}\right)^2$$

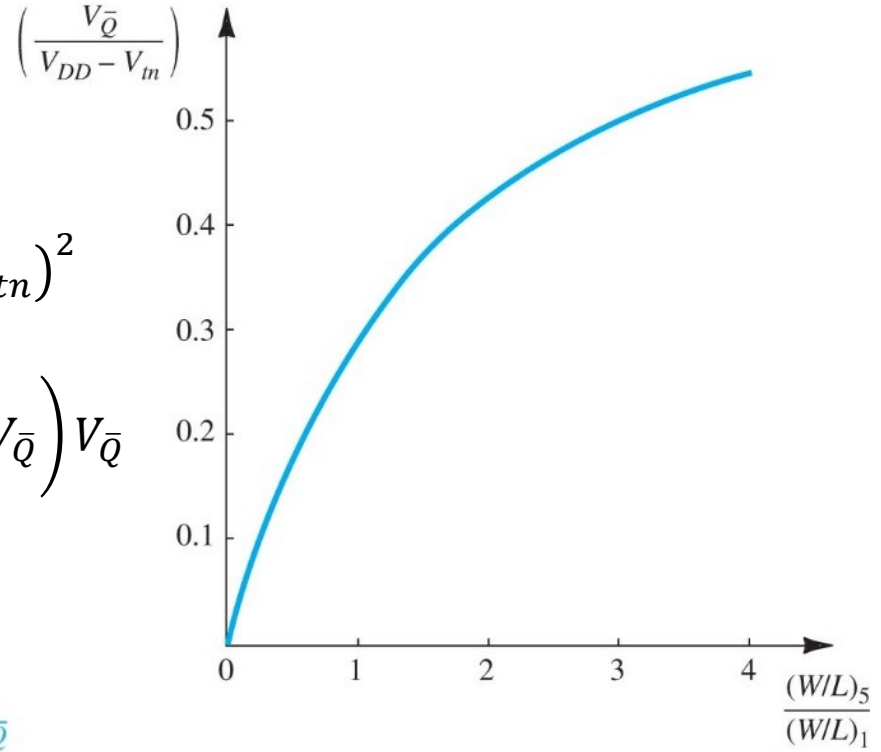
$$I_1 = k_n'\left(\frac{W}{L}\right)_1\left(V_{DD} - V_{tn} - \frac{1}{2}V_{\bar{Q}}\right)V_{\bar{Q}}$$

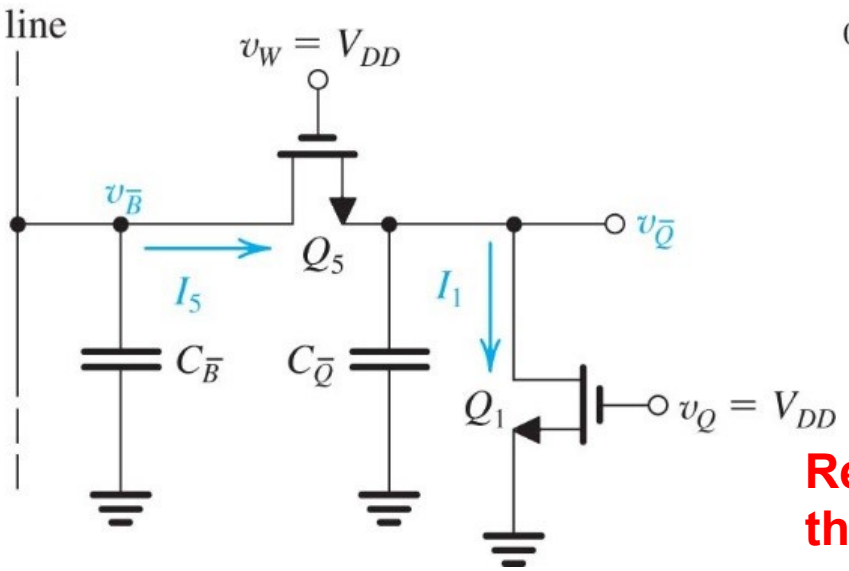
$$\frac{V_{\bar{Q}}}{V_{DD} - V_{tn}} = 1 - 1\Big/\sqrt{1 + \frac{(W/L)_5}{(W/L)_1}}$$

$$\frac{(W/L)_{a:5}}{(W/L)_{n:1}} < 1\Big/\left(\frac{V_{tn}}{V_{DD} - V_{tn}}\right)^2 - 1$$

$$\Delta Q = I_5\Delta t = C_{\bar{B}}\Delta V \qquad C_{\bar{B}} \gg C_{\bar{Q}}$$
$$\Rightarrow v_{\bar{B}} = V_{DD} - \Delta\text{V}$$

$$\Delta V = \frac{I_5\Delta t}{C_{\bar{B}}} \Leftrightarrow \Delta t = \frac{C_{\bar{B}}\Delta V}{I_5}$$





Read must not shift data more than a threshold voltage.

6T SRAM Cell: Writing a Logic 0 Over a Logic 1

- Initial data and bit lines precharged to new data

$$V_{\overline{Q_n}} = 0\ \text{V}, \qquad V_{Q_n} = V_{DD}, \qquad v_{\bar{B}}\Big|_{t=0} = V_{DD}, \qquad v_B\Big|_{t=0} = 0\ \text{V}$$

- Successful 1 through 0 toggling

$$v_Q < V_{Q_{n+1}} + V_{tn} = V_{tn}$$

$$I_4 = \frac{1}{2}k_p'\left(\frac{W}{L}\right)_4\left(V_{DD} - |V_{tp}|\right)^2$$

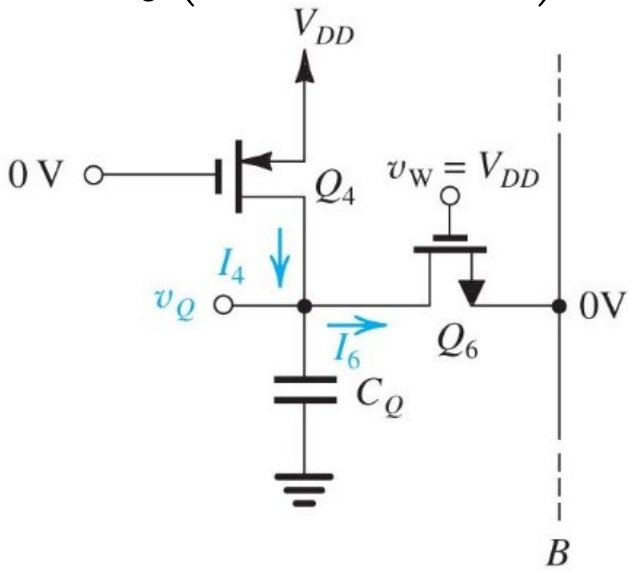
$$I_6 = k_n'\left(\frac{W}{L}\right)_6\left(V_{DD} - V_{tn} - \frac{1}{2}V_Q\right)V_Q$$

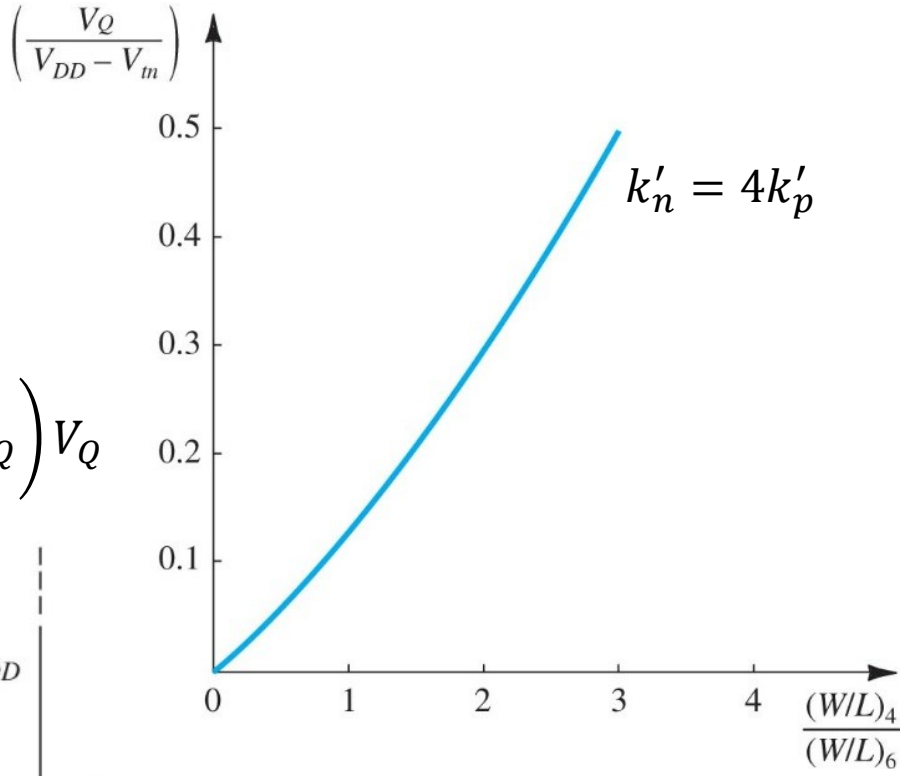
$$\frac{V_Q}{V_{DD} - V_{tn}} = 1 - \sqrt{1 + \frac{k_p'(W/L)_4}{k_n'(W/L)_6}}$$

$$\frac{(W/L)_{p:4}}{(W/L)_{a:6}} < \frac{k_n'}{k_p'}\left[1 - \left(1 - \frac{V_{tx}}{V_{DD} - V_{tx}}\right)^2\right]$$

$$\Delta Q = I_6\Delta t = C_Q\Delta V \qquad C_B \gg C_Q$$
$$\Rightarrow v_Q = V_{DD} - \Delta\text{V}$$

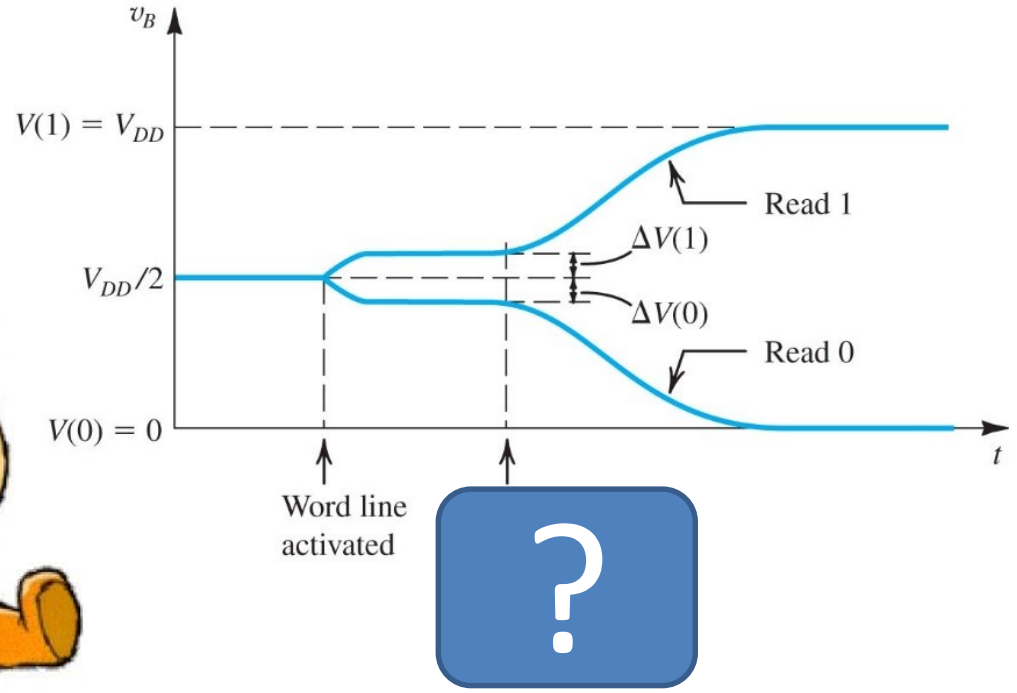
$$\Delta V = \frac{I_6\Delta t}{C_Q} \Leftrightarrow \Delta t = \frac{C_Q\Delta V}{I_6}$$

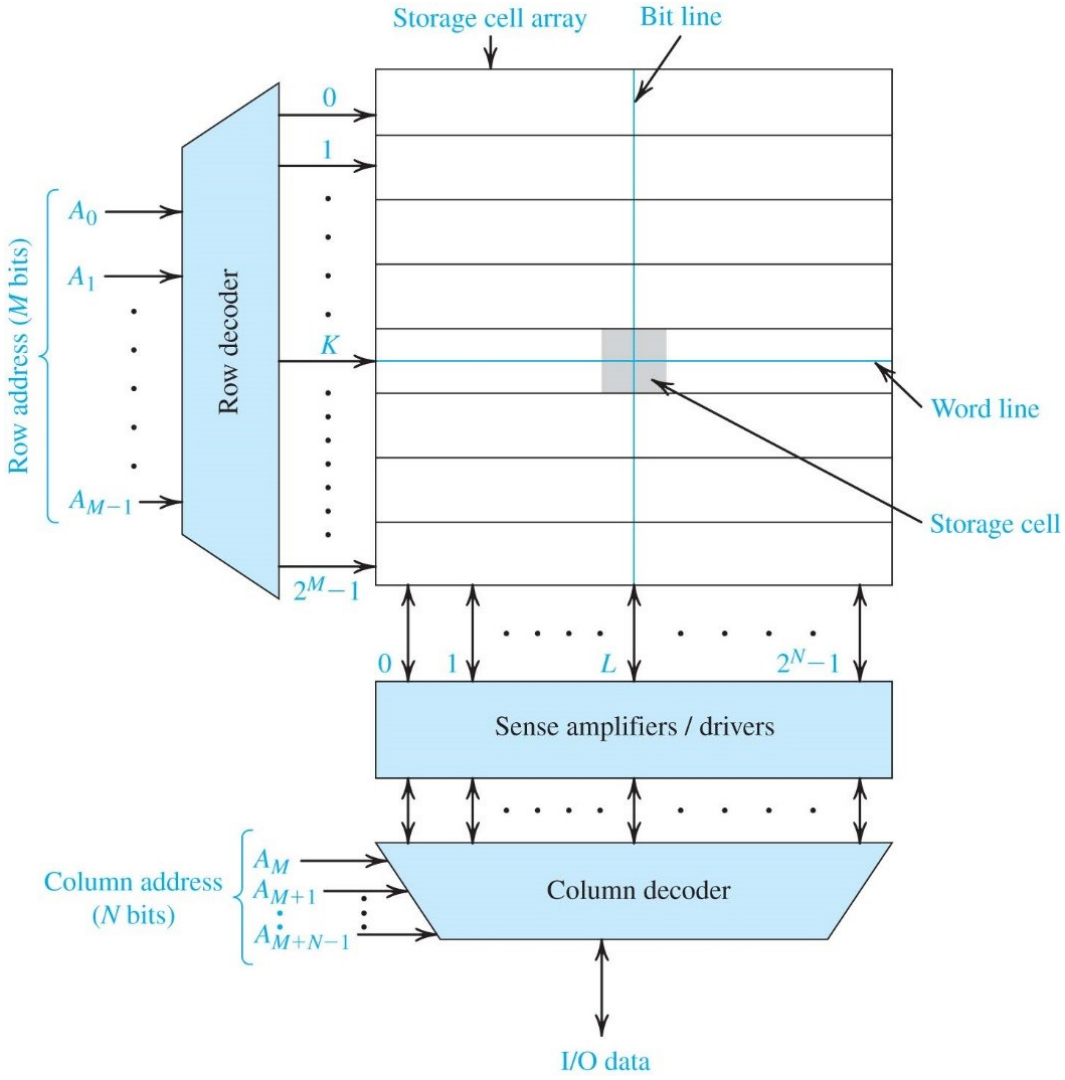




Write must toggle data to within a threshold voltage.

How to boost small differential signal from memory cell to logic levels?

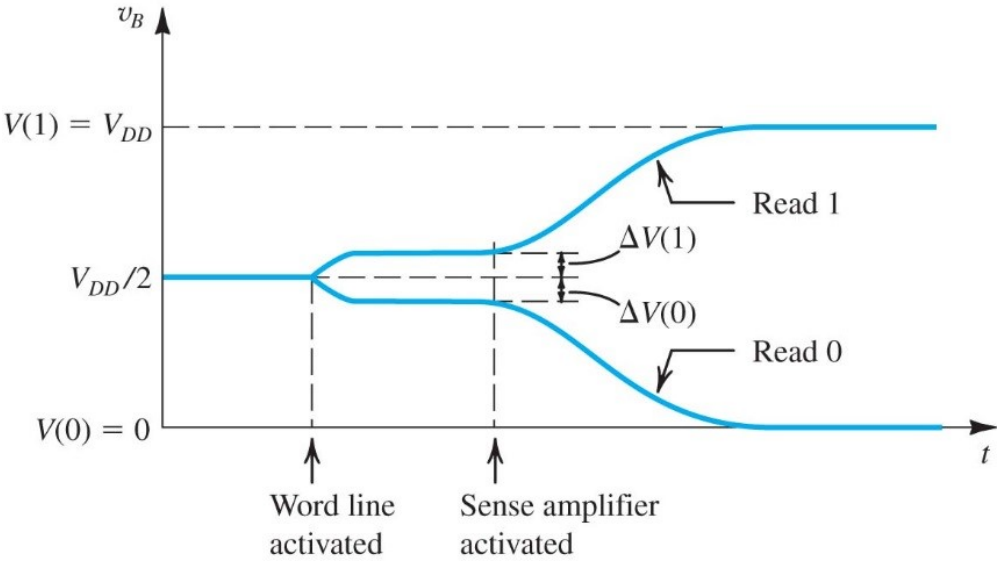


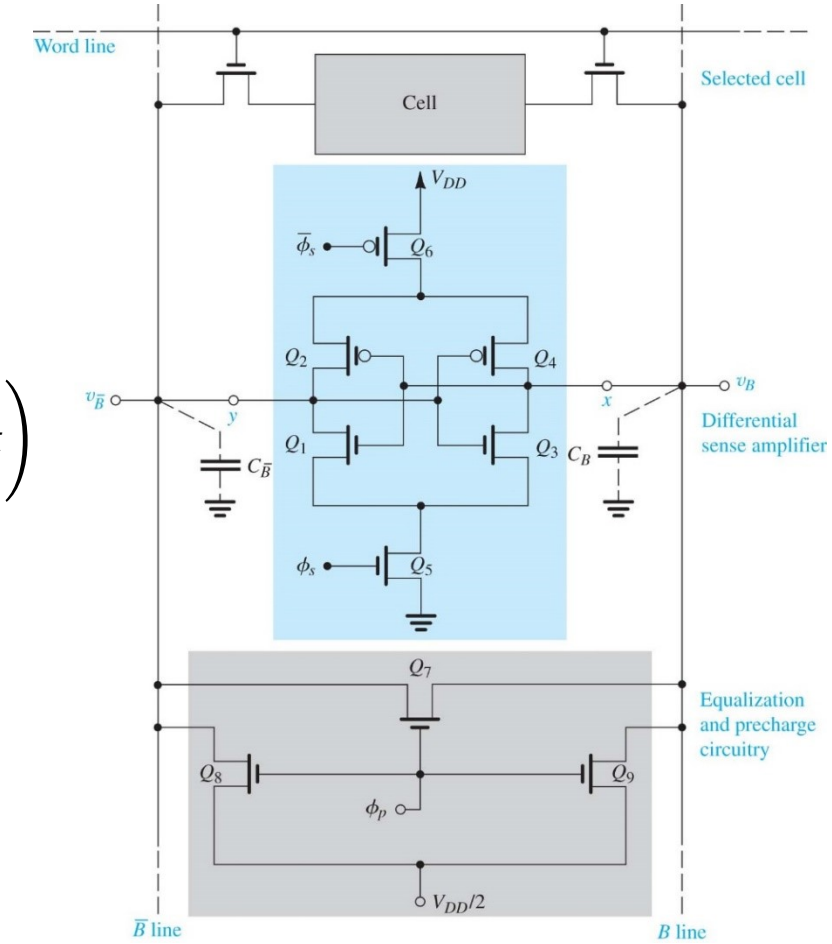


Clocked Latch as a Differential Sense Amplifier

- Latch with clocked bias between bit lines
  - First, bit lines are precharged/ equalised
  - Then, word line with addressed memory cell is activated
  - Finally, sense amplifier is activated, latching the detected difference towards full logic levels

$$v_B\Big|_{0<v_B<V_{DD}} \approx \frac{V_{DD}}{2} \pm \Delta V \exp\left(\frac{G_m}{C_B}t\right) = \frac{V_{DD}}{2} \pm \Delta V \exp\left(\frac{g_{mn}+g_{mp}}{C_B}t\right)$$

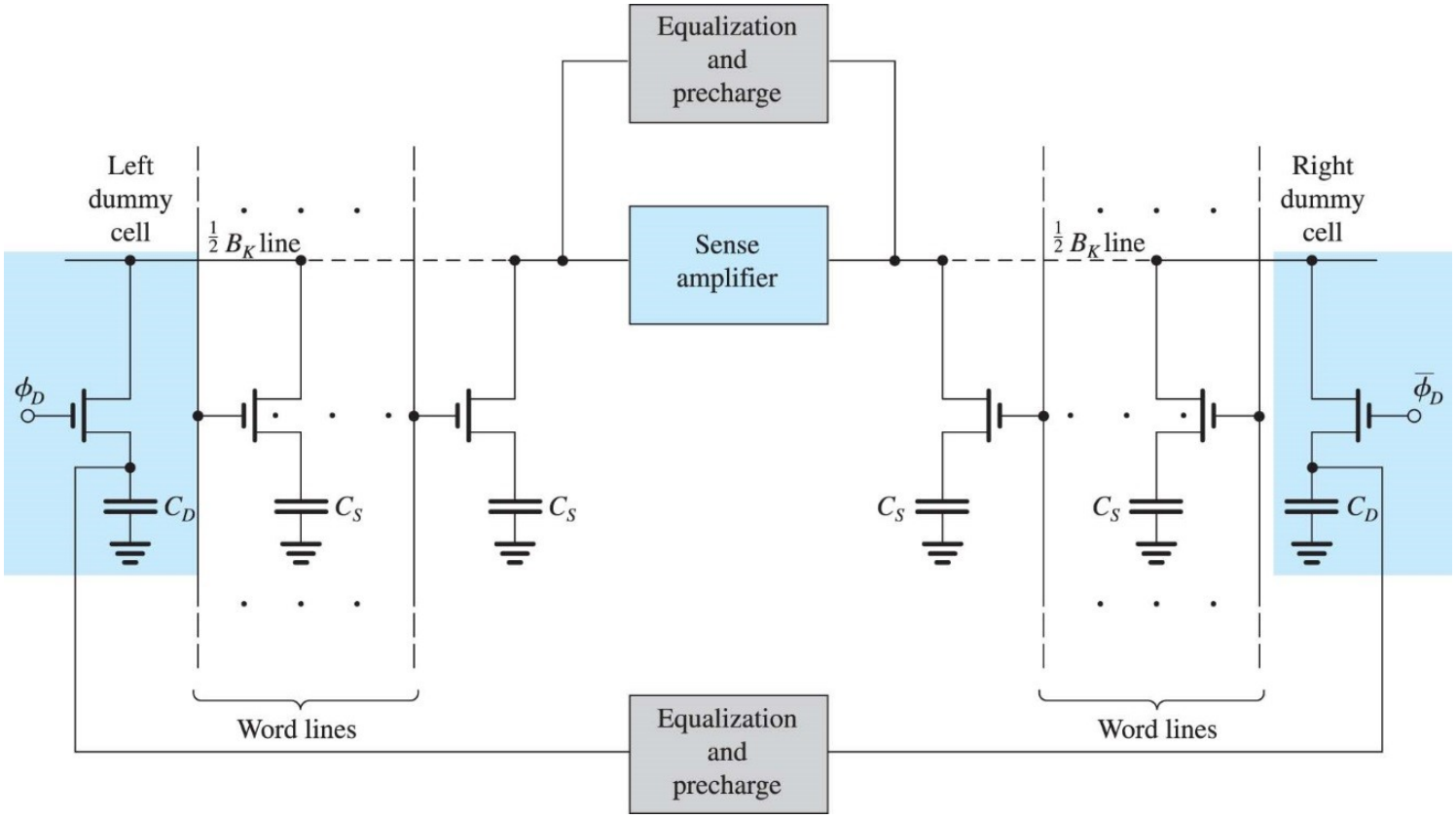




Exponential time response, set by latch transistors and bit line parasitics.

Dummy Cells for Differential DRAM Operation

- DRAM cells yield single ended output, not compatible with differential sense amplifier/ driver
- Dummy cells at memory block edge used to simulate differential characteristics



MOS Differential Amplifier as a Sense Amplifier

- MOS differential pair w/ current mirror load
  - Sufficient differential input switches bias current, I, to one branch

$$\Delta V > \sqrt{2}V_{OV} = \sqrt{\frac{2I}{k_n'\left(\frac{W}{L}\right)_{1,2}}}$$

  - Current mirror forces current to/ from output, charging/ discharging its voltage to either logic level within Δt

$$\Delta t = \frac{CV_{DD}}{I}$$

  - Increased speed costs static power dissipation

$$P = V_{DD}I$$