F13 – Digital Logic

Outline

- Digital logic
- CMOS complementary switches
- CMOS logic gate circuits
- CMOS inverter
  - Static operation
  - Dynamic operation
  - Power dissipation
  - Power-delay product
  - Energy-delay product

Reading Guide *Sedra/Smith 7ed int*

- Chapter 15.1-4, 15.6
- (Chapter 15.5 (transistor sizing))
- (Chapter 16 (logic families))

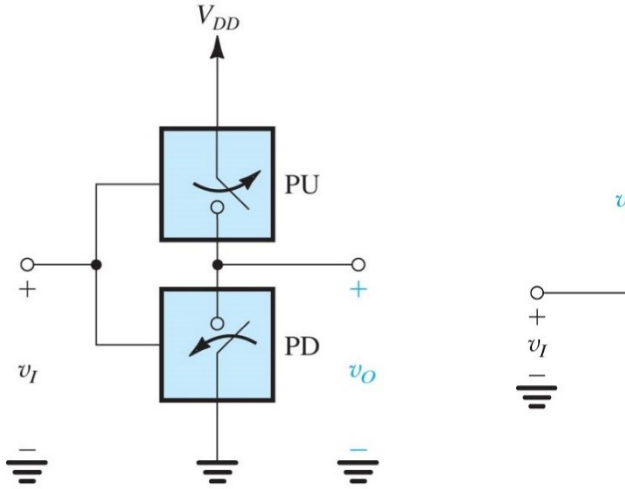
Problems *Sedra/Smith 7ed int*

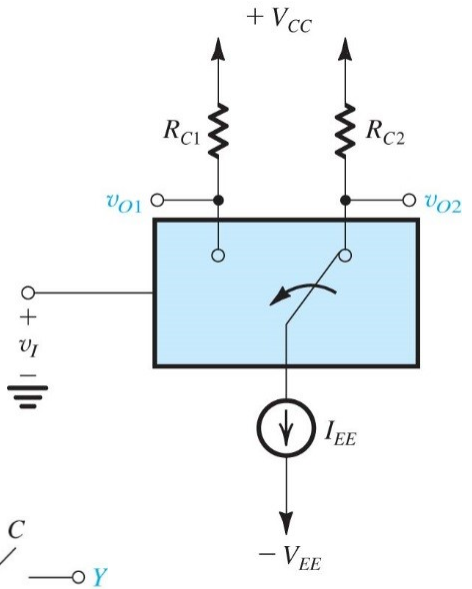
- P15.3, 15.4, 15.33, 15.34, 15.57, 15.60

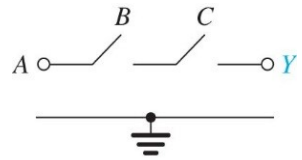
Digital Logic Families

- Complementary MOS (CMOS) digital logic
  - Complementary common source devices
  - Low static power dissipation but high dynamic

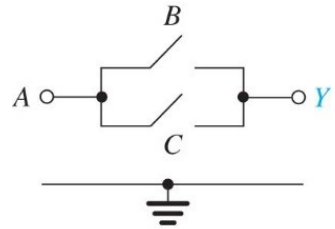
- Current-steering logic (CSL)/ emitter coupled logic (ECL)
  - Differential pair + followers for level shift
  - Naturally produces complementary output variables
  - Fast operation and approximately constant supply current







- Pass transistor logic (PTL) and complementary pass transistor logic (CPL)
  - PTL: CMOS transmission gates, typically requiring some complementary input variables
  - CPL: Zero threshold NMOS (or PMOS) only, demanding complementary input variables
  - Slow operation, susceptible to noise, and poor 1 logic level, but can be area efficient

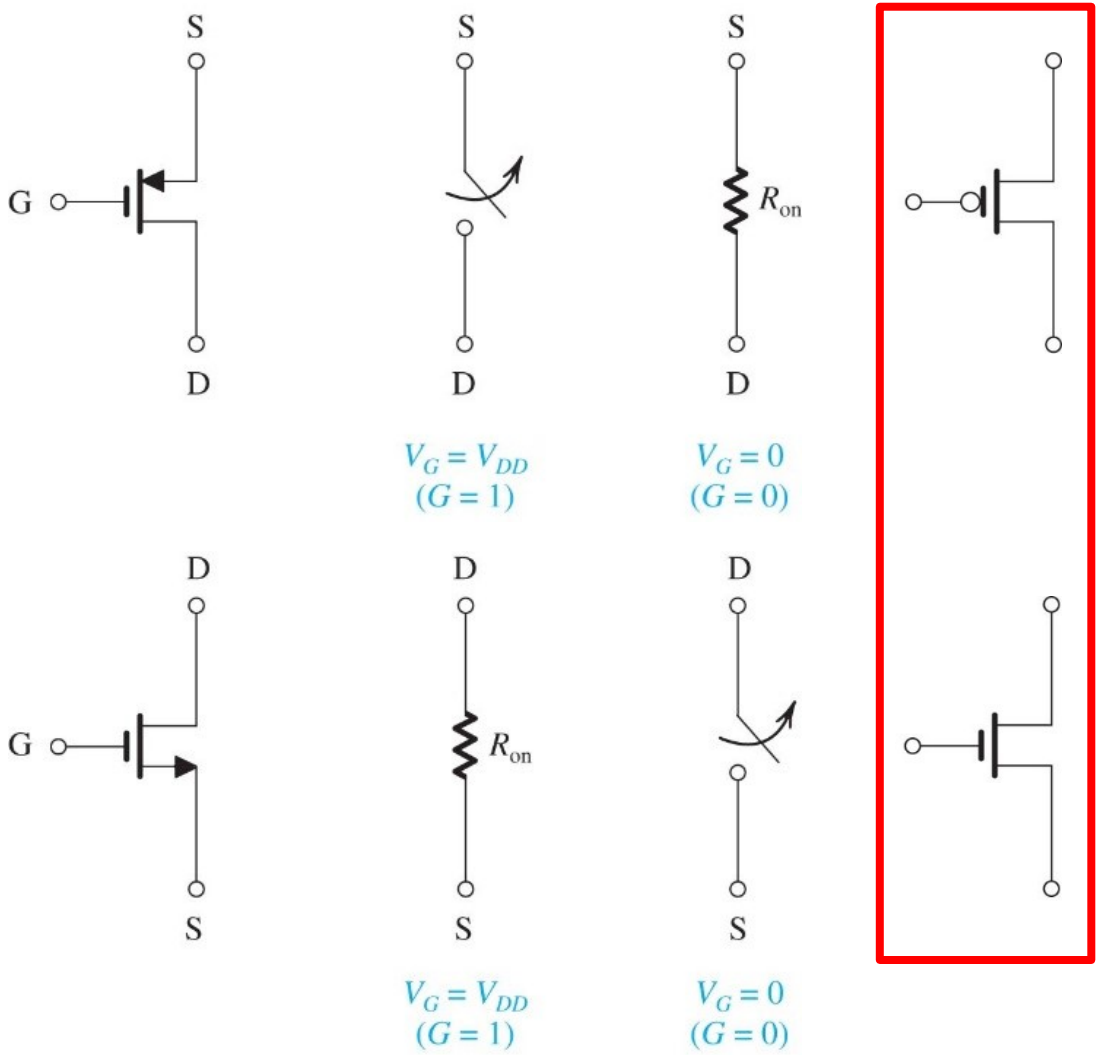


- … and many other digital logic families

Every logic family has its pros and cons, but CMOS logic is economic, versatile, and low static power.

CMOS: Complementary MOS Devices Operated as Switches

- Switch level transistor models utilised in function design
- CMOS logic levels
  - Logic 0: Ground level (low), i.e. $0 \leftrightarrow V_{"0"} = 0\ \mathrm{V}$
  - Logic 1: Positive supply (high), i.e. $1 \leftrightarrow V_{"1"} = V_{DD}$
- PMOS w/ source connected towards supply: active low
  - Gate high: cut off, i.e. open switch
  - Gate low: saturation, i.e. closed switch, with a small resistance
- NMOS w/ source connected towards ground: active high
  - Gate high: saturation, i.e. closed switch, with a small resistance
  - Gate low: cut off, i.e. open switch



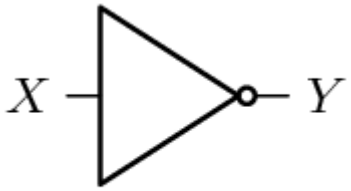
NOT Gate a.k.a. Inverter

- Logic (boolean) NOT function
  - Input, X

    $X \in \{0, 1\}$

  - Output, Y

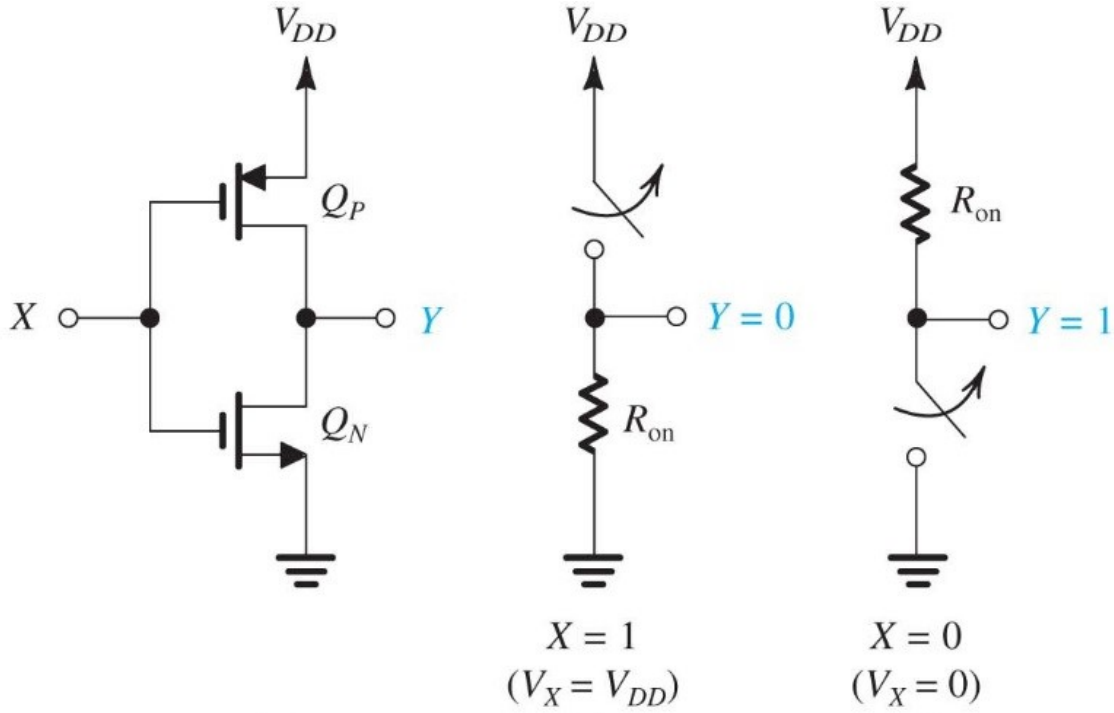
    $$Y = \bar{X} = \begin{cases} 1, & X = 0 \\ 0, & X = 1 \end{cases}$$



$Y = \text{NOT}\,(X)$

X	$Y = \bar{X}$
0	1
1	0

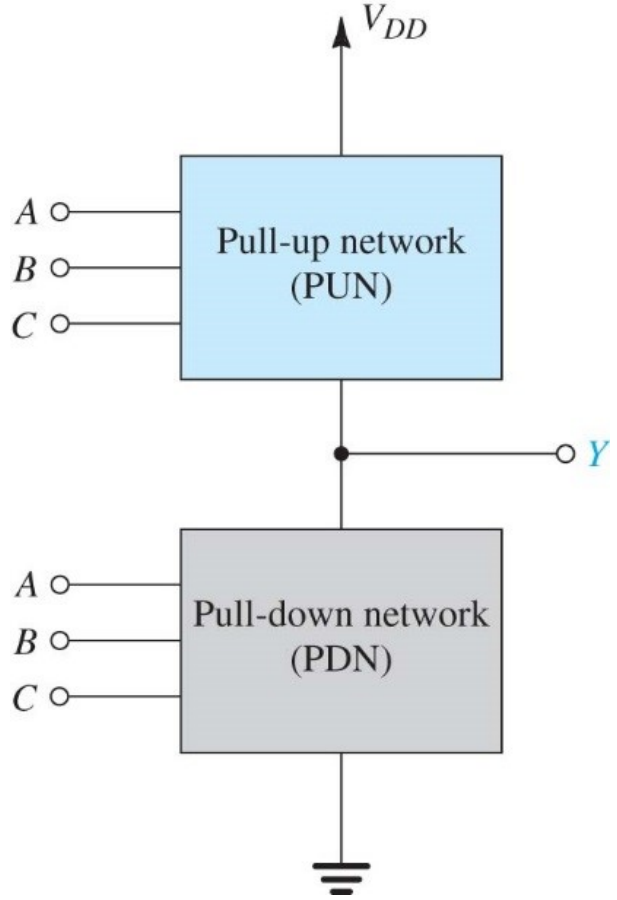
- CMOS inverter (i.e. NOT gate)
  - Pull up transistor QP, $Y = \bar{X}$
    - Connects output towards supply if input is low, otherwise isolates
  - Pull down transistor QN, $\bar{Y} = X$
    - Connects output towards ground if input is high, otherwise isolates



Digital logic gate circuits perform logic (boolean) functions.

CMOS Logic Gates

- Input nodes
  - Gate nodes of various NMOS and PMOS transistors
- Output node
  - Routed either to supply or ground, depending on input levels
- Pull up network (PUN), $Y = f_{PUN}(\bar{A}, \bar{B}, \bar{C}, \dots)$
  - PMOS connects output node towards supply for low input
- Pull down network (PDN), $\bar{Y} = f_{PDN}(A, B, C, \dots)$
  - NMOS connects output node towards ground for high input
- Complementary PUN and PDN device operation
  - Input variables $(A, B, C, \dots)$ connect to both PUN and PDN
  - Per input variable, PUN PMOS does opposite of PDN NMOS



Boolean logic requires three basic operations: NOT, IF and AND.

Two Input NOR Gate

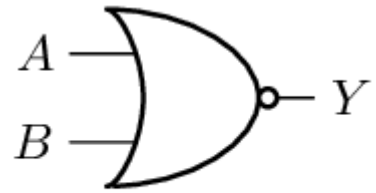
- Logic (boolean) NOT-OR compound function
  - Inputs, $\{A, B\}$

    $A, B \in \{0, 1\}$

  - Output, Y

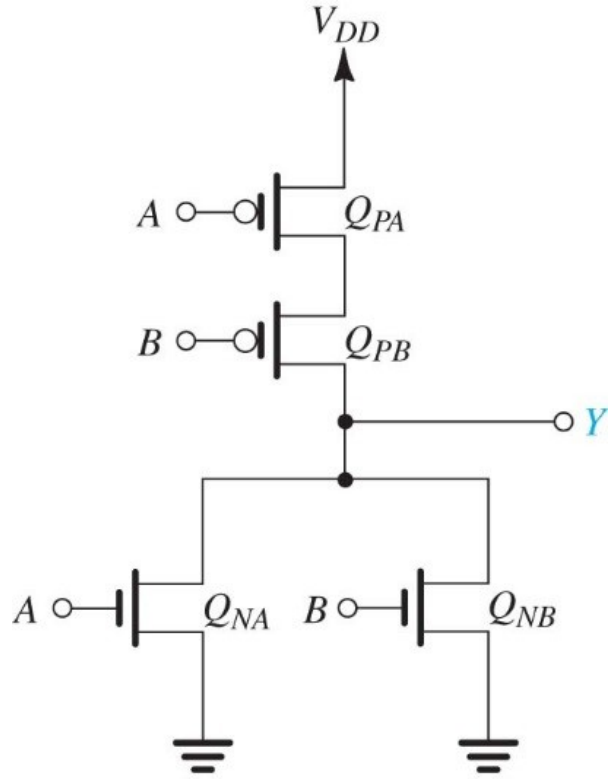
    $$Y = \overline{A + B} = \bar{A}\bar{B} = \begin{cases} 1, & (A = 0, B = 0) \\ 0, & \text{otherwise} \end{cases}$$

- CMOS NOR gate
  - PUN, $Y = \bar{A}\bar{B}$
    - One series branch with all inputs
  - PDN, $\bar{Y} = A + B$
    - One parallel branch for each input



$Y = \text{NOR}(A, B)$

A	B	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0



$Y = \overline{A + B}$

Inclusive OR function, dissimilar from exclusive XOR function.

Two Input NAND Gate

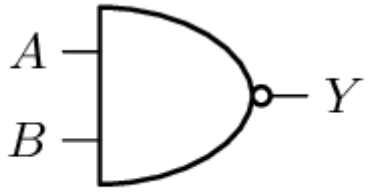
- Logic (boolean) NOT-AND compound function
  - Inputs, $\{A, B\}$

    $A, B \in \{0, 1\}$

  - Output, Y

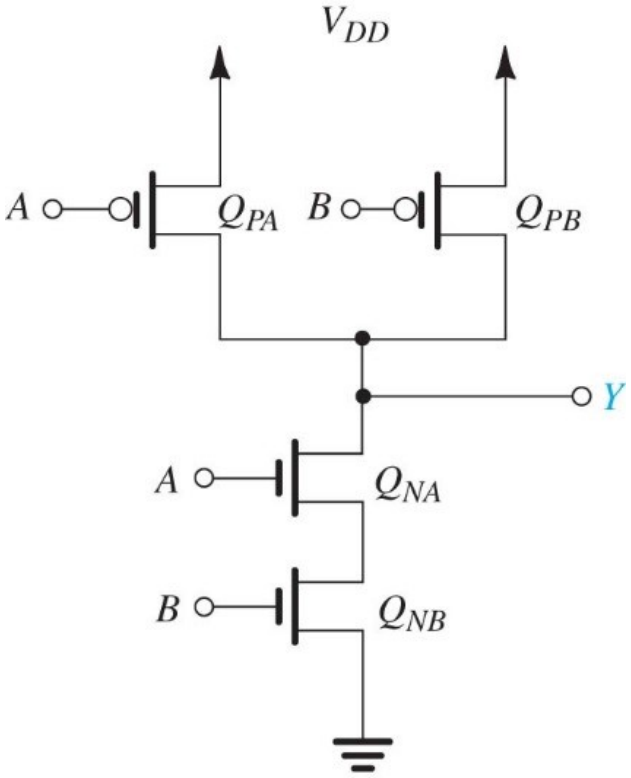
    $$Y = \overline{AB} = \bar{A} + \bar{B} = \begin{cases} 0, & (A = 1, B = 1) \\ 1, & \text{otherwise} \end{cases}$$

- CMOS NAND gate
  - PUN, $Y = \bar{A} + \bar{B}$
    - One parallel branch for each input
  - PDN, $\bar{Y} = AB$
    - One series branch with all inputs



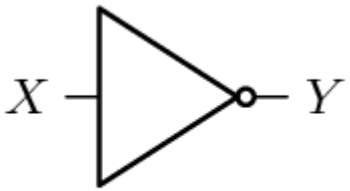
$Y = \text{NAND}\,(A, B)$

A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

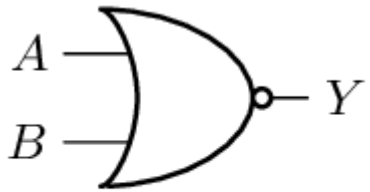


$Y = \overline{AB}$

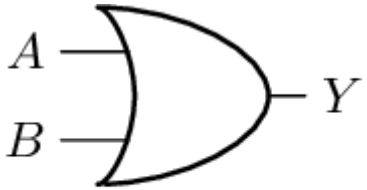
How can OR and AND gates be implemented?



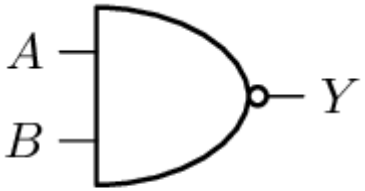
$Y = \mathrm{NOT}\,(X)$



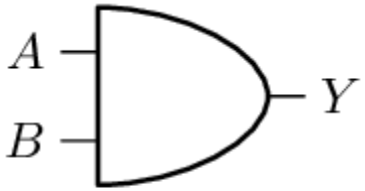
$Y = \mathrm{NOR}\,(A, B)$



$Y = \mathrm{OR}\,(A, B)$



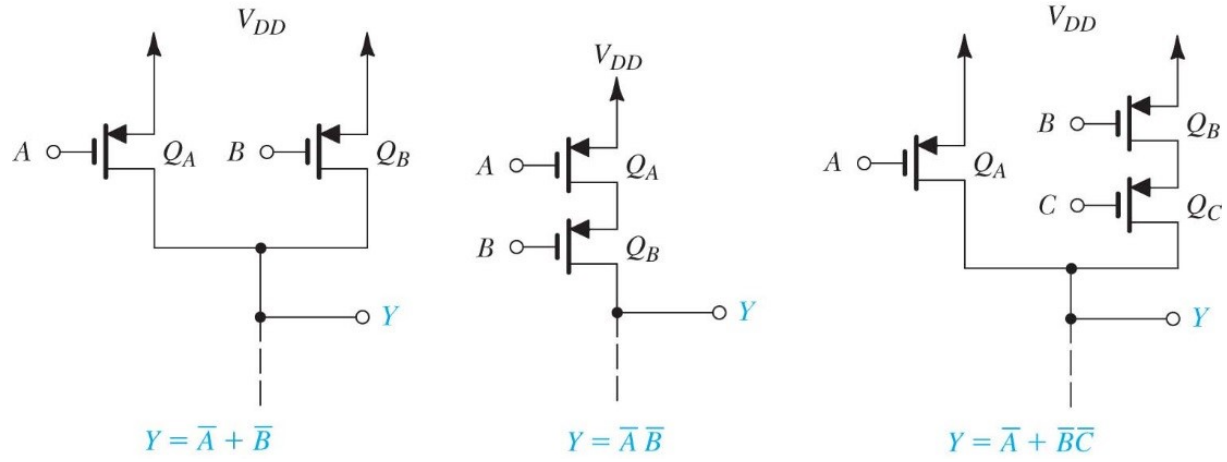
$Y = \mathrm{NAND}\,(A, B)$



$Y = \mathrm{AND}\,(A, B)$

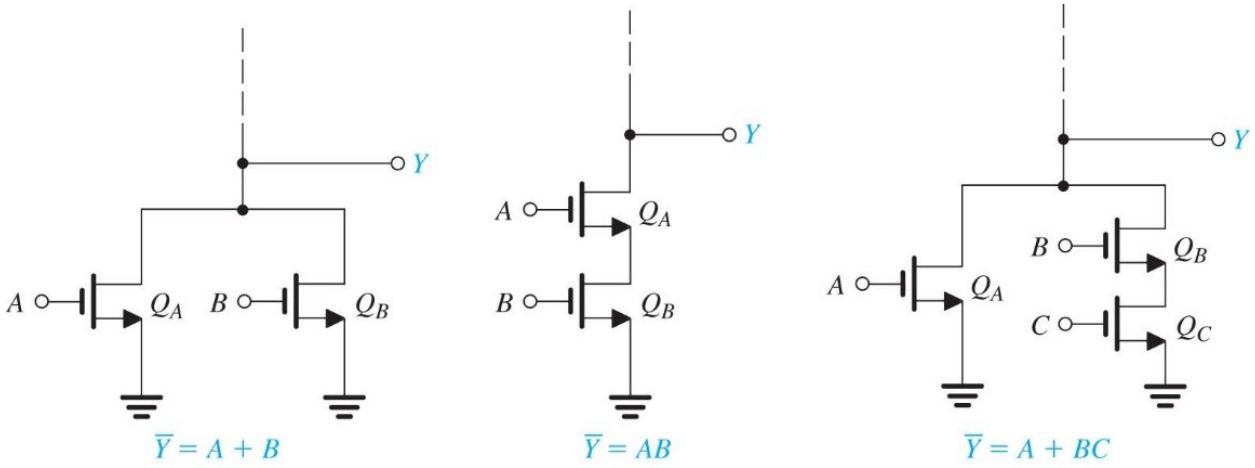
CMOS Pull Up Networks (PUNs)

- PUNs consist of active low PMOS transistors only
- PMOS w/ source towards supply
  - Active when gate input is low (0)
  - Not active if gate input is high (1)
- Parallel connection: NAND
  - At least one low yields conductive path towards supply
- Series connection: NOR
  - All, and only all, low yields conductive path towards supply
- Scalable to arbitrary number of devices in series/ parallel branches



CMOS Pull Down Networks (PDNs)

- PDNs consist of active high NMOS transistors only
- NMOS w/ source towards ground
  - Not active if gate input is low (0)
  - Active when gate input is high (1)
- Parallel connection: NOR
  - At least one high yields conductive path towards ground
- Series connection: NAND
  - All, and only all, high yields conductive path towards ground
- Scalable to arbitrary number of devices in series/ parallel branches



Complex Gates: Duality, Boolean Algebra, and De Morgan's Law

- PUN-PDN duality between series and parallel connections

- Basic operators in boolean algebra/ set theory/ digital logic
  - Disjunction/ union/ OR

$$A \vee B \Leftrightarrow A \cup B \Leftrightarrow \mathrm{OR}(A,B) \sim \max(A,B) = A + B - AB$$

  - Conjunction/ intersection/ AND

$$A \wedge B \Leftrightarrow A \cap B \Leftrightarrow \mathrm{AND}(A,B) \sim \min(A,B) = AB$$

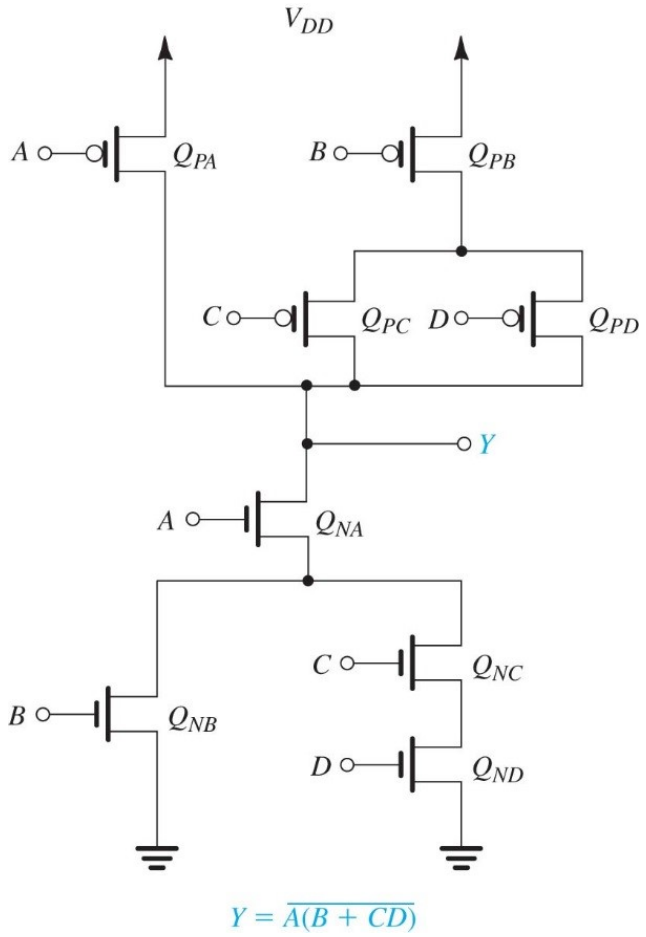
  - Negation/ complement/ NOT

$$\neg \Leftrightarrow \bar{X} \Leftrightarrow \mathrm{NOT}(X) \sim 1 - X$$

- De Morgan's law
  - Negation of disjunction is equivalent to conjunction of negations, and vice versa

$$\neg(A \vee B) = (\neg A) \wedge (\neg B) \Leftrightarrow \overline{A \cup B} = \bar{A} \cap \bar{B} \Leftrightarrow \overline{A + B} = \bar{A}\bar{B}$$

$$\neg(A \wedge B) = (\neg A) \vee (\neg B) \Leftrightarrow \overline{A \cap B} = \bar{A} \cup \bar{B} \Leftrightarrow \overline{AB} = \bar{A} + \bar{B}$$



De Morgan's law: "break the line, change the sign".

Synthesis by Duality: Two Input XOR Gate

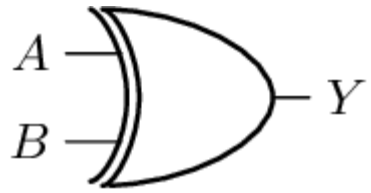
- Logic (boolean) XOR function
  - Inputs, $\{A, B\}$

    $A, B \in \{0, 1\}$

  - Output, Y

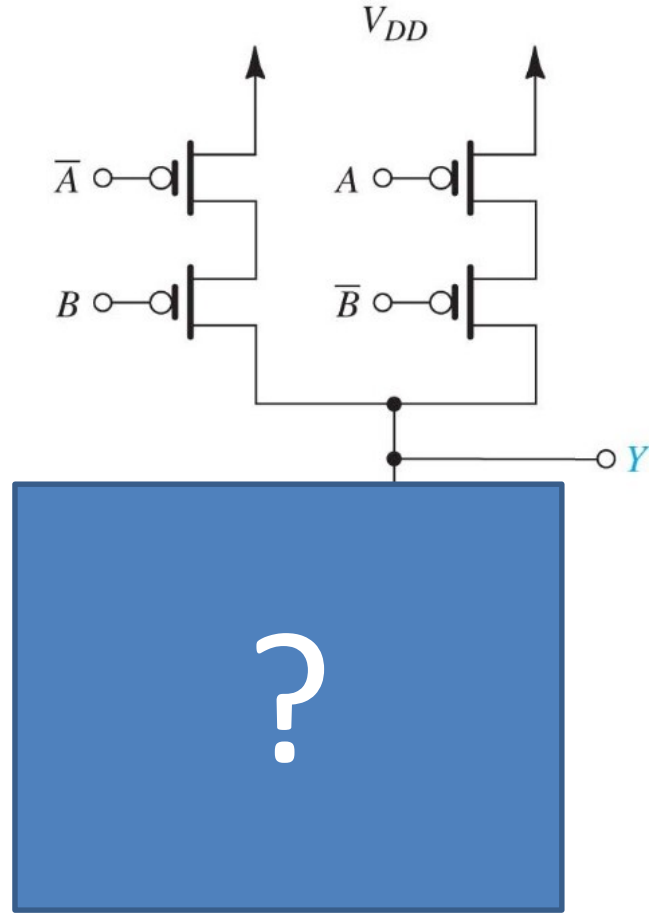
    $$Y = A\bar{B} + \bar{A}B = \begin{cases} 1, & (A \neq B) \\ 0, & \text{otherwise} \end{cases}$$

- CMOS XOR gate
  - PUN, $Y = A\bar{B} + \bar{A}B$
    - Parallel branches with series devices
  - PDN
    - Series branch with parallel devices
  - Auxiliary logic
    - Inverters for complemented variables



$$Y = \text{XOR}(A, B)$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



Two-input inclusive $\text{OR}(A, B) \sim \max(A, B)$, whereas exclusive $\text{XOR}(A, B) \sim \text{mod}(A + B, 2)$.

Synthesis by Complementary Expressions: Two Input XOR Gate

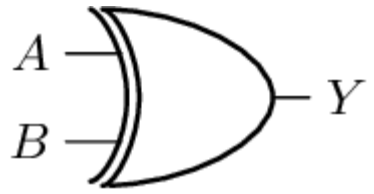
- Logic (boolean) XOR function
  - Inputs, $\{A, B\}$

    $A, B \in \{0, 1\}$

  - Output, Y

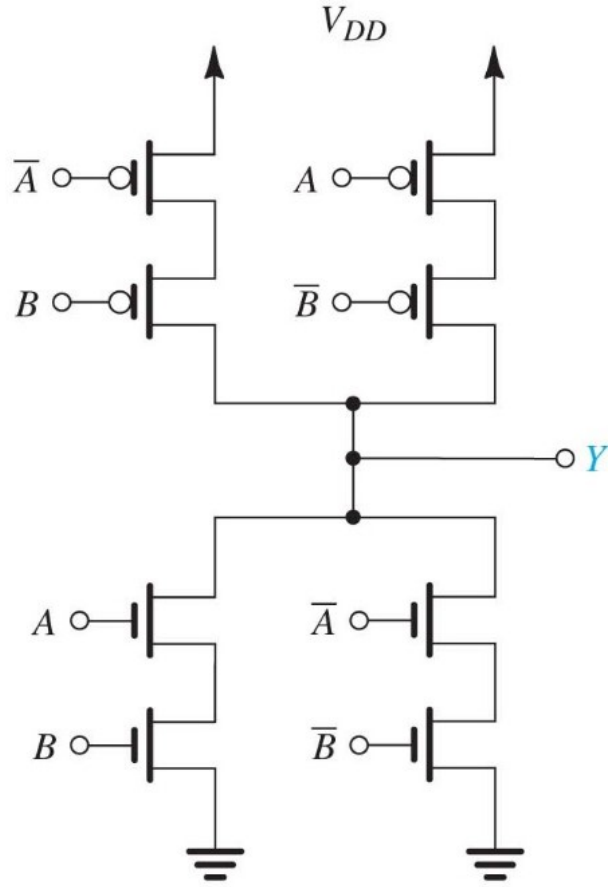
$$Y = A\bar{B} + \bar{A}B = AB + \bar{A}\bar{B} = \begin{cases} 1, & (A \neq B) \\ 0, & \text{otherwise} \end{cases}$$

- CMOS XOR gate
  - PUN, $Y = A\bar{B} + \bar{A}B$
    - Parallel branches with series devices
  - PDN, $\bar{Y} = AB + \bar{A}\bar{B}$
    - Parallel branches with series devices
  - Auxiliary logic
    - Inverters for complemented variables



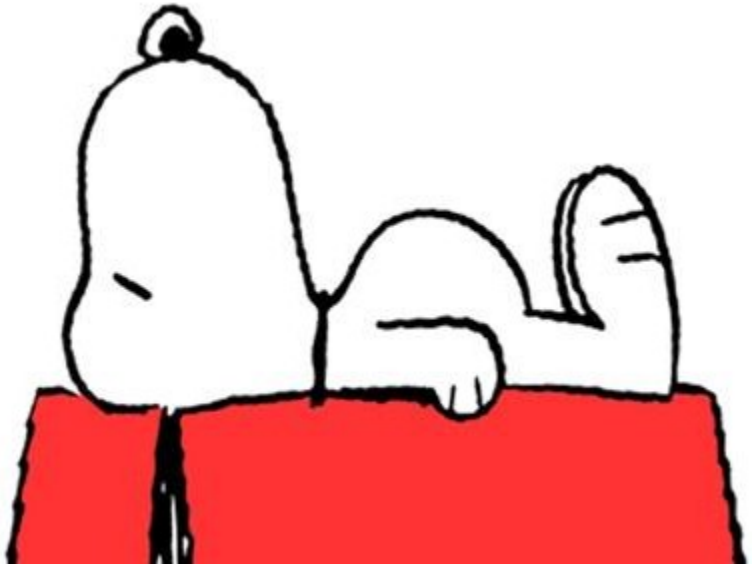
$$Y = \text{XOR}(A, B)$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



PDN is not the dual of the PUN; gate design is not unique.

BREAK



CMOS Inverter

- Two complementary MOS switches between ground and supply
  - High off resistance (open switch)
  - Small on resistance (closed switch)

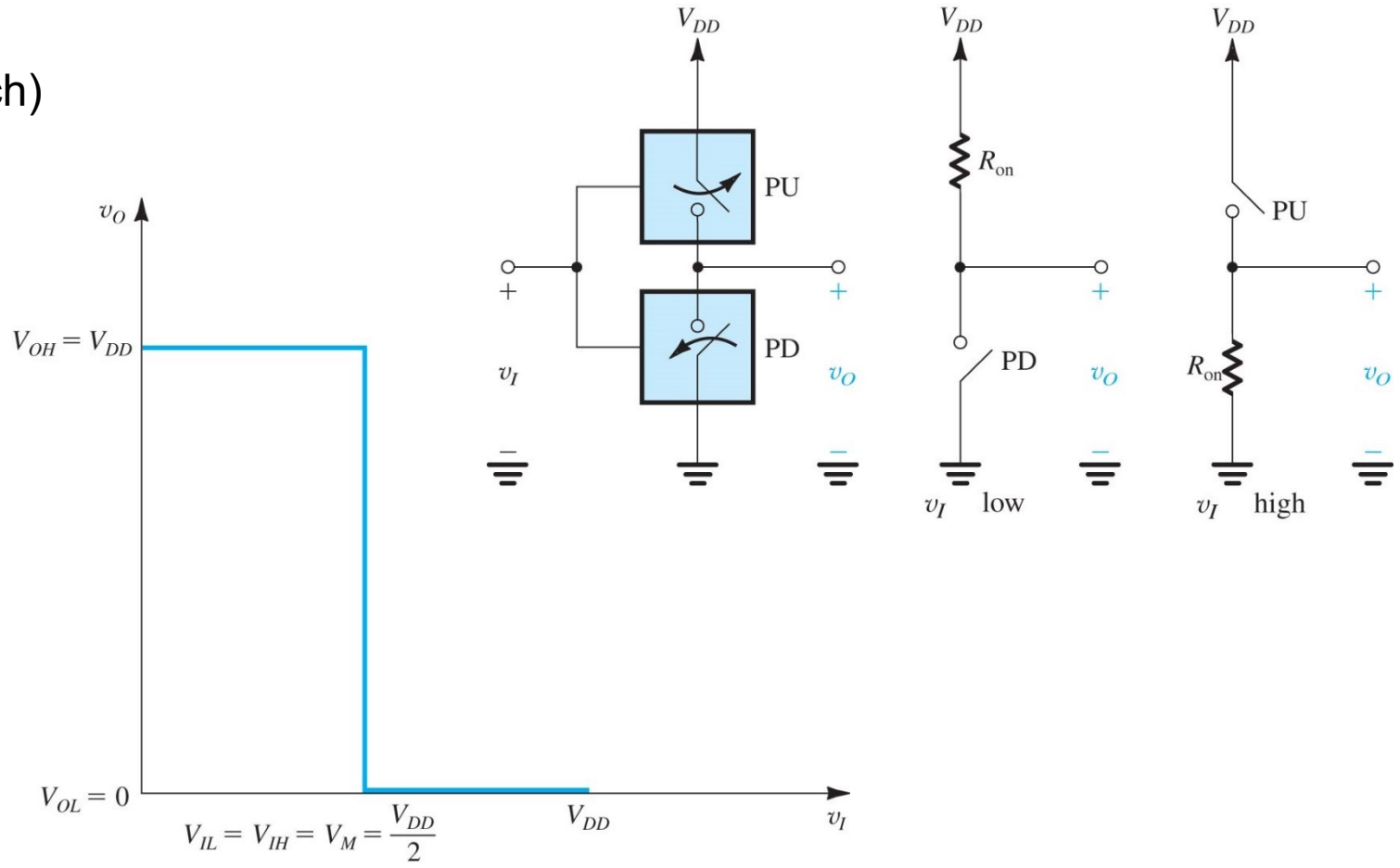
- Ideal characteristics
  - Full range output swing

    $0 = V_{OL} < v_O < V_{OH} = V_{DD}$
  - Discrete switch at midpoint

    $$V_{IL} = V_{IH} = V_M = \frac{V_{DD}}{2}$$
  - High output for low input level

    $v_I < V_{IL} \Rightarrow v_O = V_{OH} = V_{DD}$
  - Low output for high input level

    $v_I > V_{IH} \Rightarrow v_O = V_{OL} = 0$



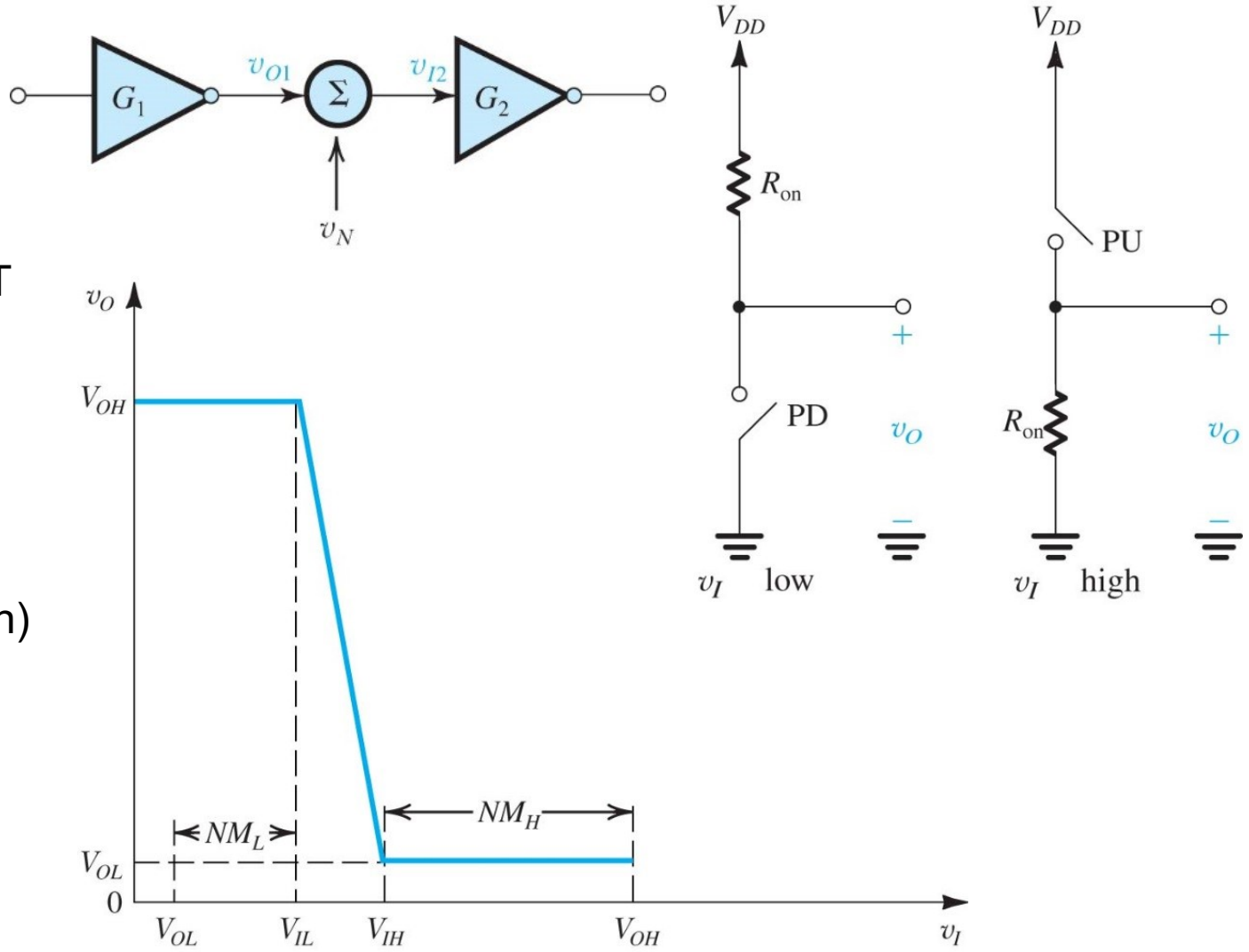
Inverter VTC

- Simplified characteristics
  - Reduced output range
    - Off state leakage
  - Midpoint smeared
    - Output resistance due to MOSFET channel length modulation
    - PUN triode operation just below output midpoint
    - PDN triode operation just above output midpoint
- Noise margins (to intrinsic switching region)
  - High output state

$$NM_H = V_{OH} - V_{IH}$$

  - Low output state

$$NM_L = V_{IL} - V_{OL}$$



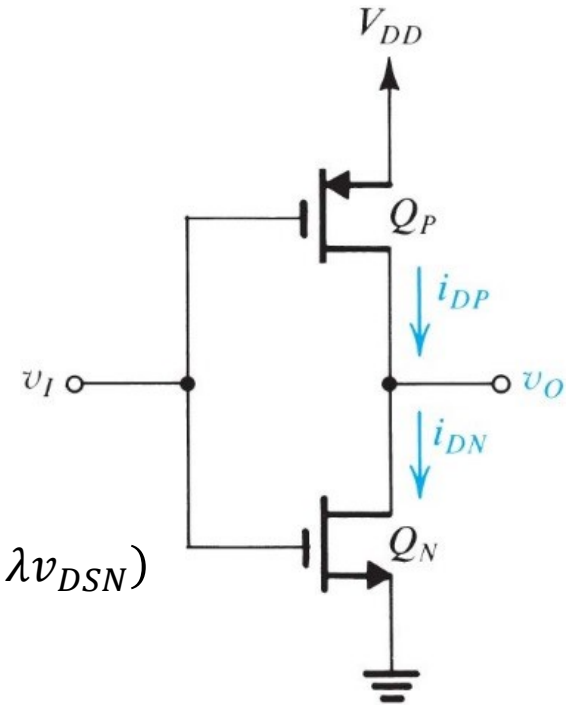
CMOS Inverter: High Input

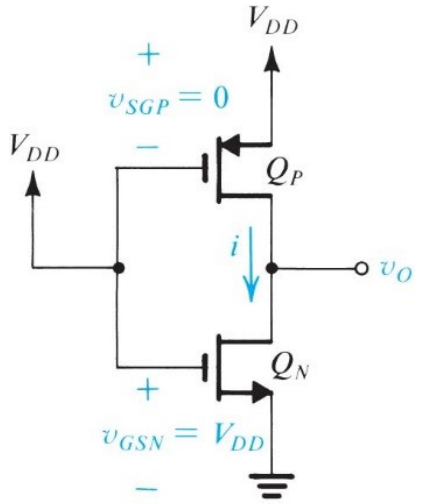
- Inverter with high input voltage, investigated through “load line”
  - QN triode, QP cutoff
  - Low output voltage
- QP resistance, $R_P = r_{OP} \approx \infty$
- QN resistance, $R_N = r_{DSN}$

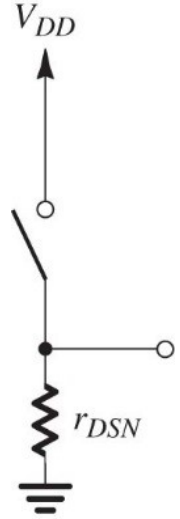
$$i_{DN} = k_n' \left(\frac{W}{L}\right)_n \left(v_{OV} - \frac{1}{2} v_{DSN}\right) v_{DSN}(1 + \lambda v_{DSN})$$

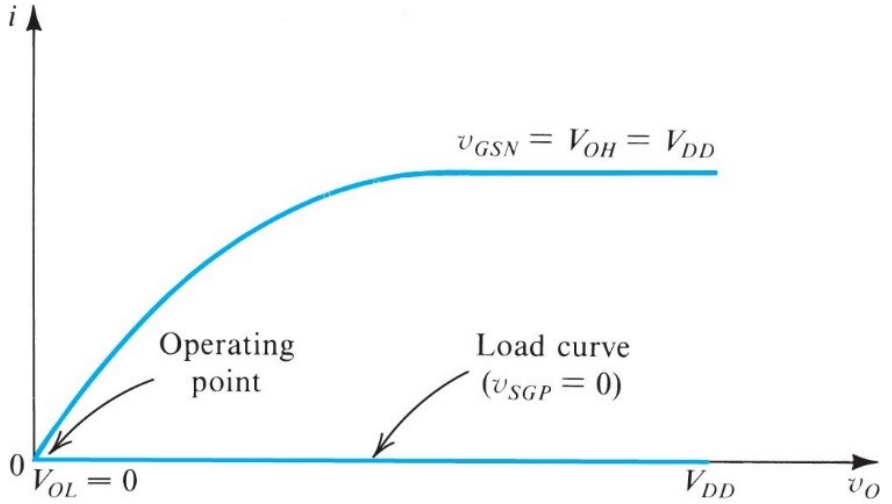
$$\approx \{v_{DSN} \ll 2v_{OV}\} \approx k_n' \left(\frac{W}{L}\right)_n v_{OV} v_{DSN}$$

$$\Rightarrow r_{DSN} = \frac{\partial v_{DSN}}{\partial i_{DN}} \approx 1/k_n' \left(\frac{W}{L}\right)_n v_{OV}$$









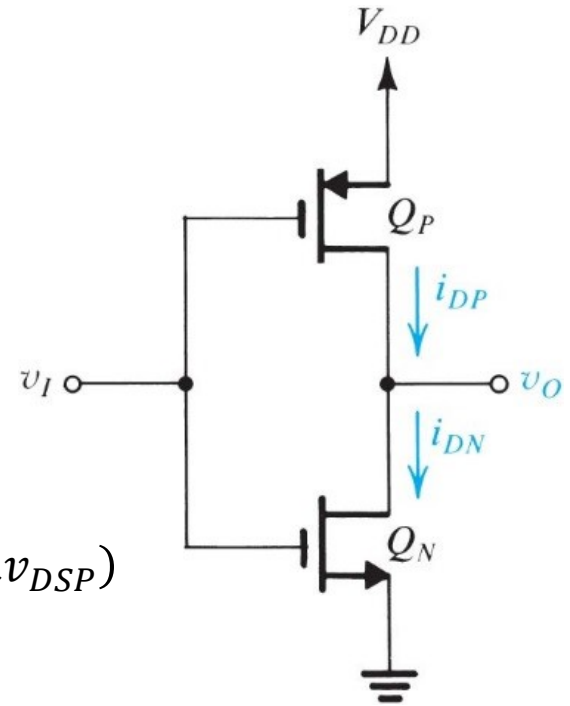
CMOS Inverter: Low Input

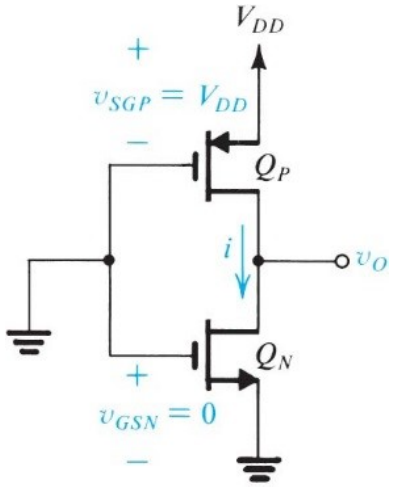
- Inverter with low input voltage, investigated through “load line”
  - QN cutoff, QP triode
  - High output voltage
- QN resistance, $R_N = r_{ON} \approx \infty$
- QP resistance, $R_P = r_{DSP}$

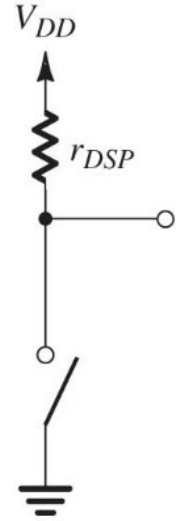
$$i_{DP} = k'_p \left(\frac{W}{L}\right)_p \left(v_{OV} - \frac{1}{2} v_{DSP}\right) v_{DSP}(1 + \lambda v_{DSP})$$

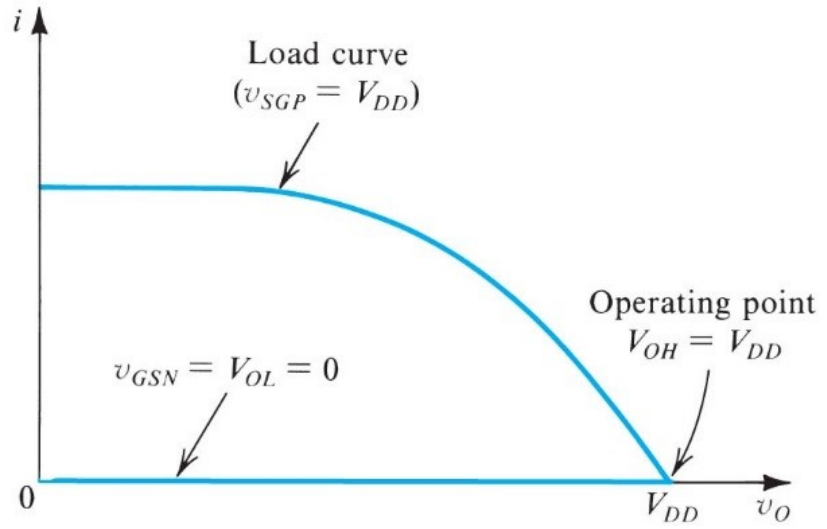
$$\approx \{v_{DSP} \ll 2v_{OV}\} \approx k'_p \left(\frac{W}{L}\right)_p v_{OV} v_{DSP}$$

$$\Rightarrow r_{DSP} = \frac{\partial v_{DSP}}{\partial i_{DP}} \approx 1/k'_p \left(\frac{W}{L}\right)_p v_{OV}$$



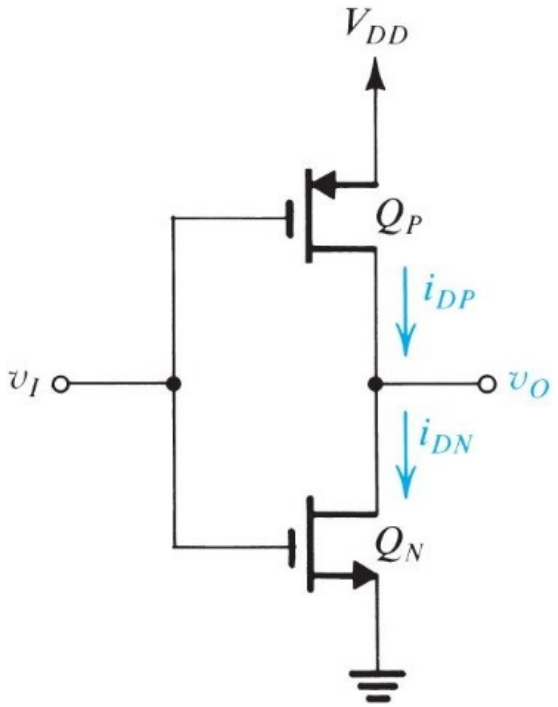


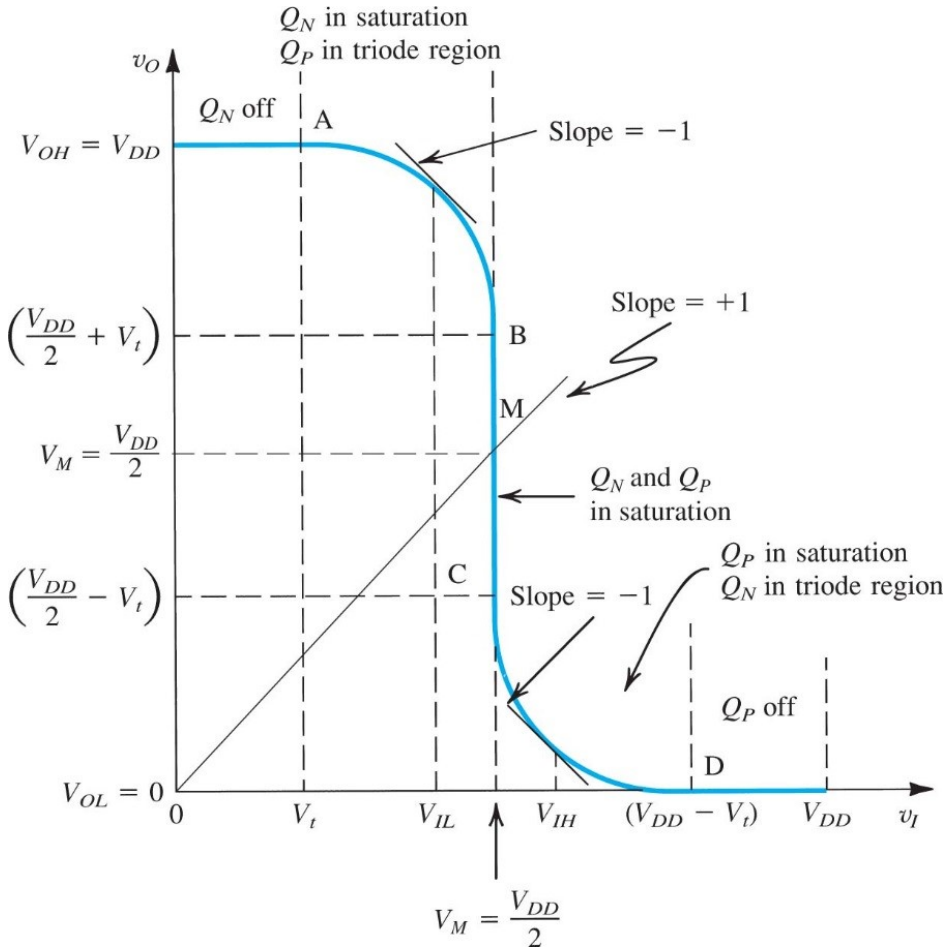




Detailed CMOS Inverter VTC for Matched Devices

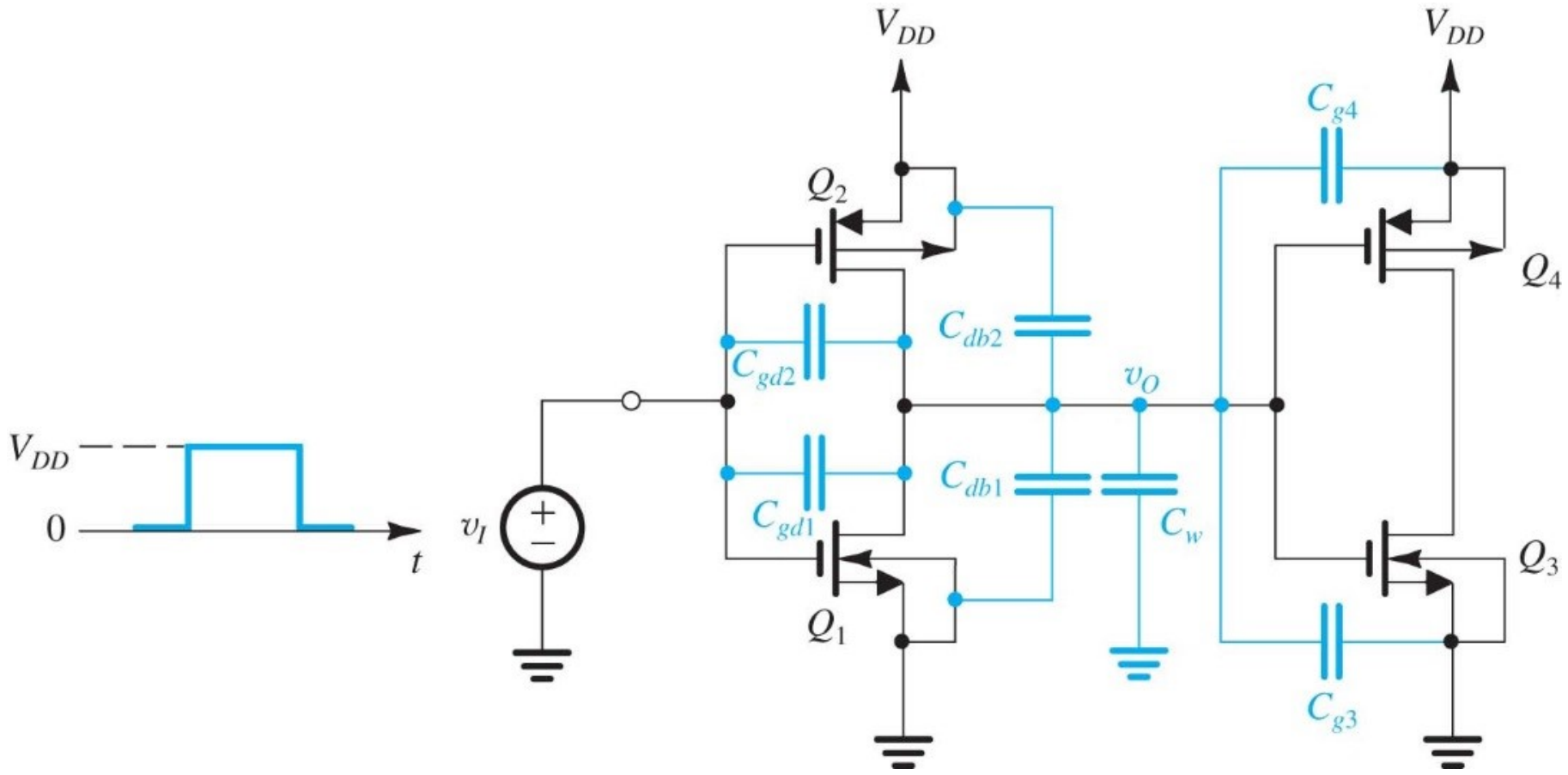
- Voltage transfer characteristics for input starting low, going high
  - Low input/ high output
    - QN cutoff, QP zero bias
  - Passing threshold for QN
    - QN saturation, QP triode
  - Steep drop at midpoint
    - QN and QP saturation, (neglecting channel length modulation)
  - Passing midpoint
    - QN triode, QP saturation
  - Passing threshold for QP
    - QN zero bias, QP cutoff
  - High input/ low output





Matched devices assumed, i.e. equivalent NMOS and PMOS characteristics.

What is the effect of circuit capacitance on the inverter step response?



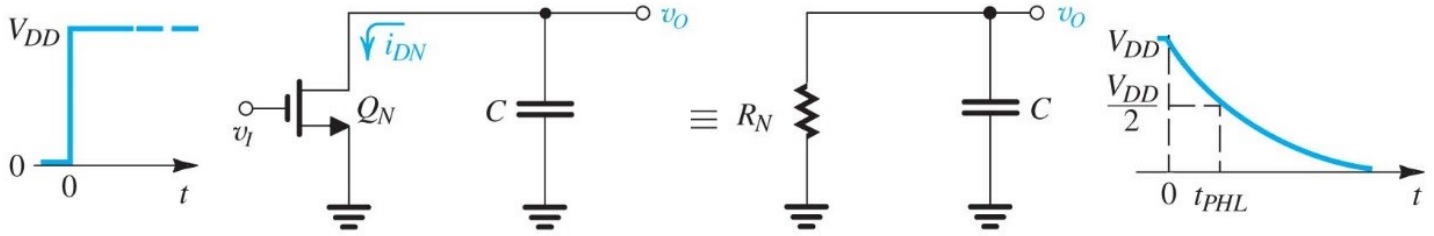
Propagation Delay: Equivalent Circuits

- Effective capacitance at output node, C, and equivalent MOSFET resistance, R, sourcing/ sinking current I

- Input low, going high
  - Output capacitance discharges from high to low through QN

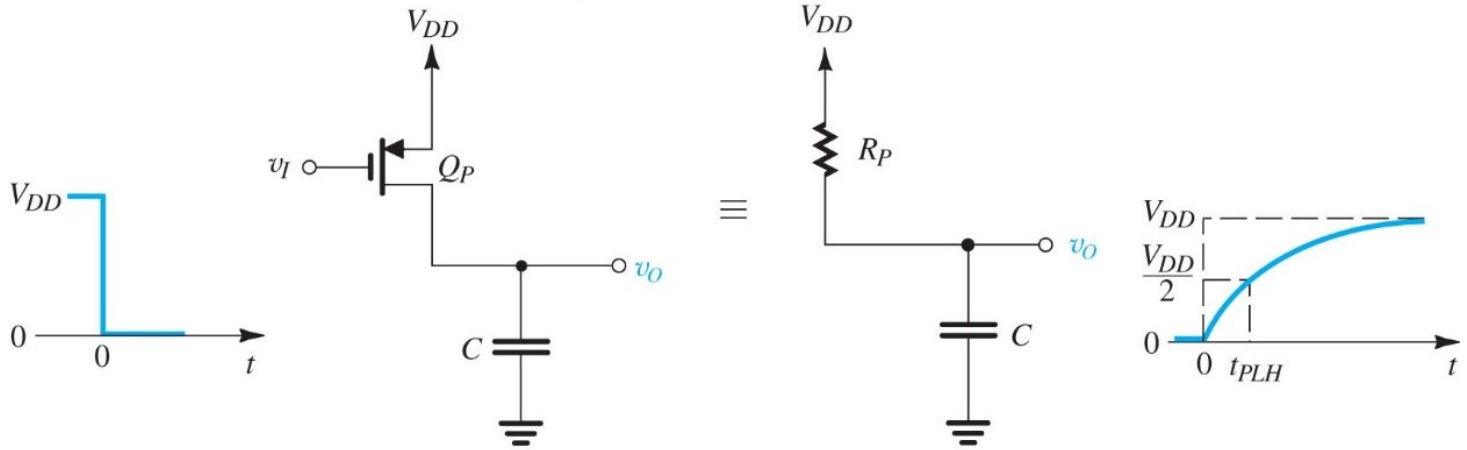
- Input high, going low
  - Output capacitance charges from low to high through QP

- Generalised step response of single time constant (STC) network



$$I\Delta t = \Delta Q = C\Delta V$$

$$y(t) = Y_\infty - (Y_\infty - Y_{0+})\exp\left(-\frac{t}{\tau}\right), \qquad \tau = RC$$



Propagation Delay and Maximum Switching Frequency

- Effective inverter transition time constant, τ

  $\tau = RC$

- Propagation delay, t_P

  $$t_P = \frac{1}{2}(t_{PLH} + t_{PHL}) = \frac{\ln 2}{2}(\tau_{PLH} + \tau_{PLH})$$

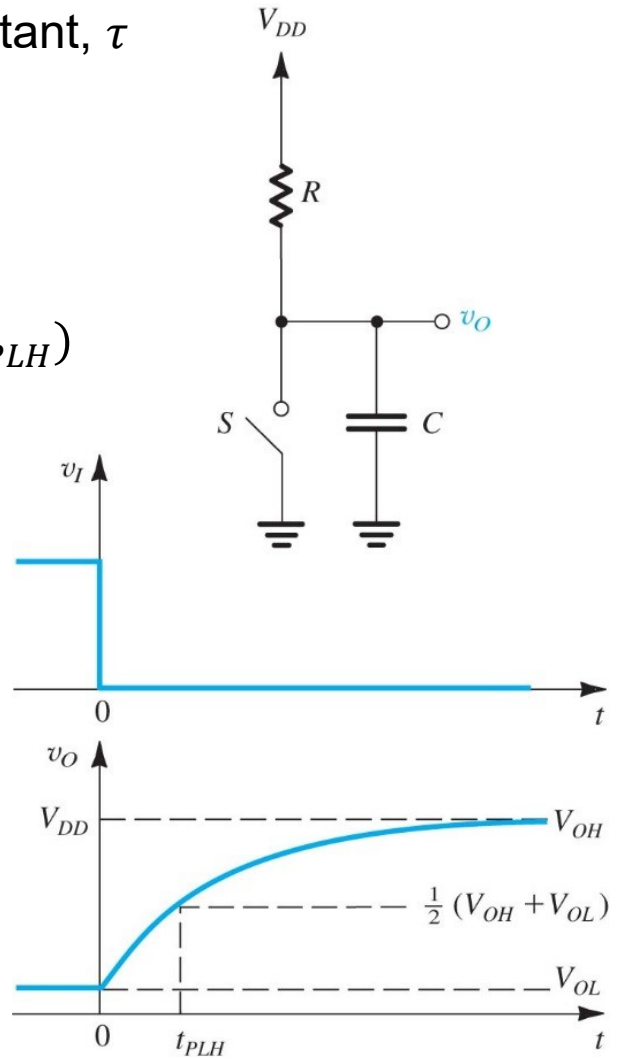
  $$t_{PHL} \approx \frac{CV_{DD}}{2i_{DN}}, \qquad t_{PLH} \approx \frac{CV_{DD}}{2i_{DP}}$$

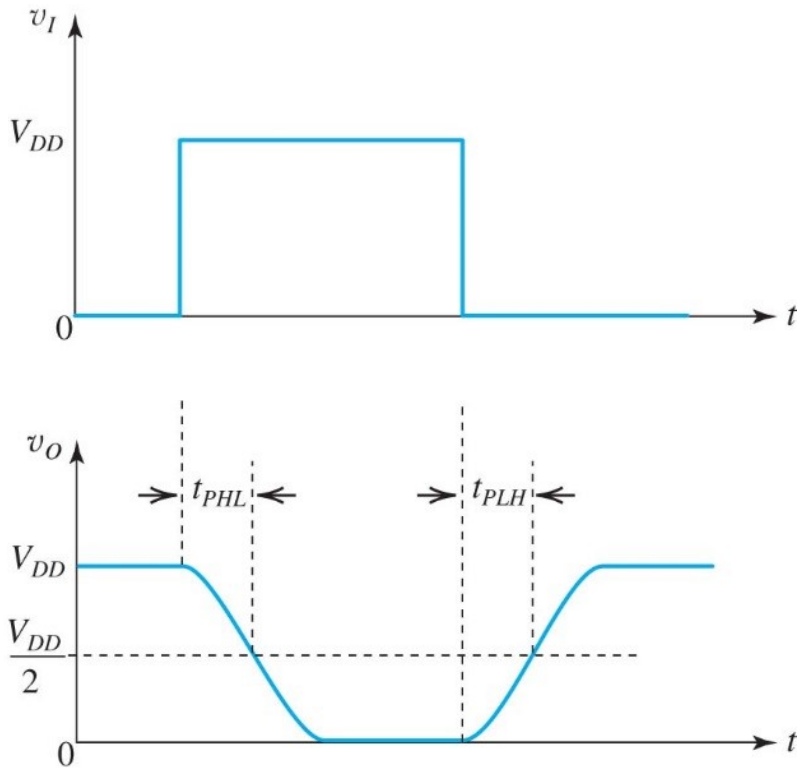
- Minimum switching period, $T_{\min}$

  $T_{min} = t_{PLH} + t_{PHL} = 2t_P$

- Maximum switching frequency, $f_{\max}$

  $$f_{max} = \frac{1}{T_{min}} = \frac{1}{2t_P}$$





Propagation delay defined from start to output midpoint.

Equivalent Capacitance at Inverter Output

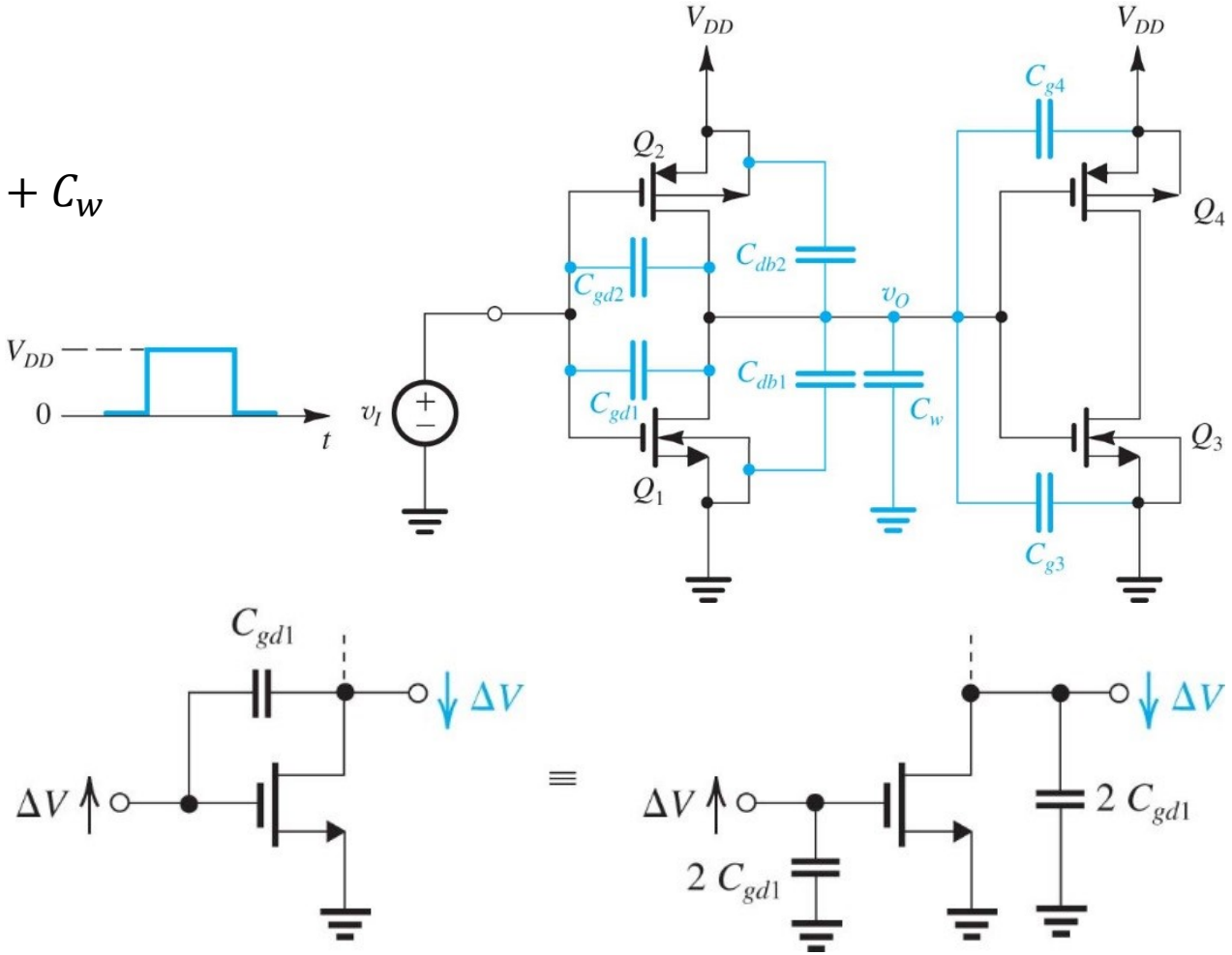
- Large signal equivalent capacitance at output, C
  - Contributions from input and load inverter

    $C \approx 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$

- Gate-drain capacitance of input stage, C_{gdx}
  - Miller feedback

    $\Delta v_O = K\Delta v_I = -1\Delta v_I \Rightarrow (1-K) = 2$

- Drain-body capacitance of input stage, C_{dbx}
- Wiring capacitance between stages, C_w
- Gate capacitance of load stage, C_{gx}



Static and Dynamic Power Dissipation

- Static power dissipation, P_{static}
  - No connection between supply and ground
  - No (or quite small) static power dissipation

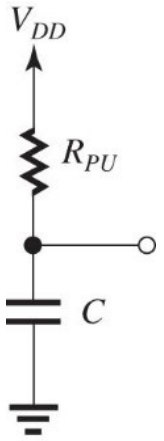
$$P_{static} = V_{DD} i_{static} \approx 0$$

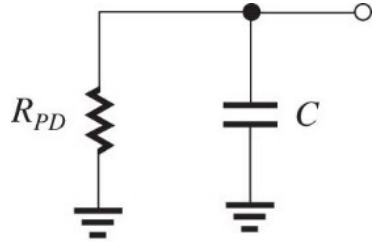
- Dynamic power dissipation, $P_D = P_{dynamic} + P_{leakage}$
  - Repeated output node charge/ discharge cycles through PUN/ PDN equivalent resistances

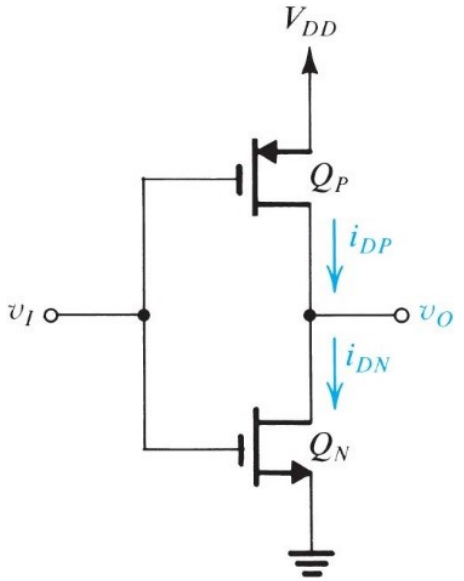
$$P_{dynamic} = f(E_{PLH} + E_{PHL}) = fCV_{DD}^2 = f\left(\frac{1}{2}CV_{DD}^2 + \frac{1}{2}CV_{DD}^2\right)$$

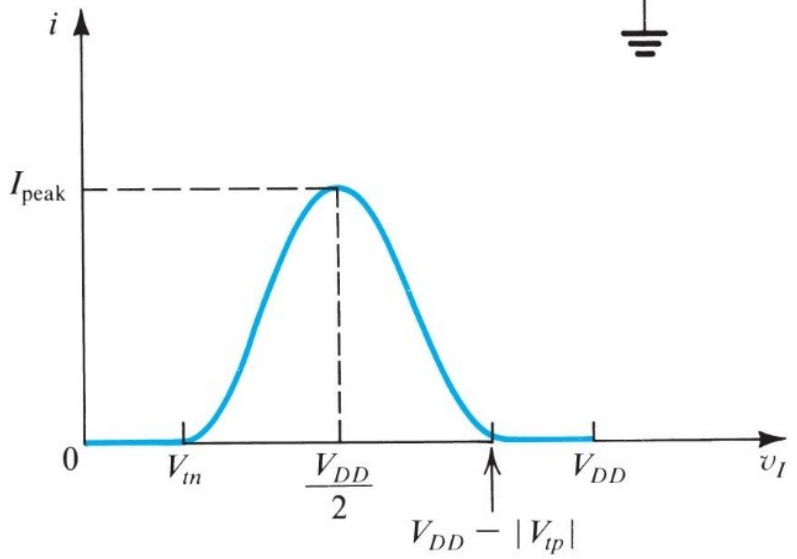
  - Small direct leakage current from supply to ground through PUN and PDN, peaking at midpoint (often negligible)

$$P_{leakage} = f\int_0^T V_{DD} i_{leakage}(t)\,\partial t \ll P_{dyn}, \qquad T = \frac{1}{f}$$









Power Delay Product and Energy Delay Product

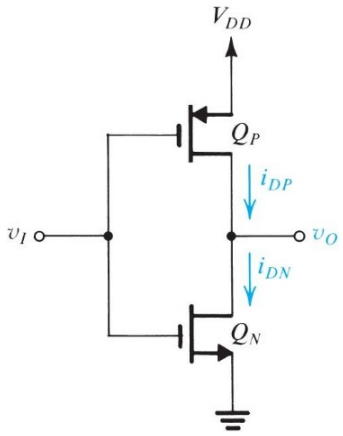
- Dynamic power, P_D, of inverter operated at frequency, f

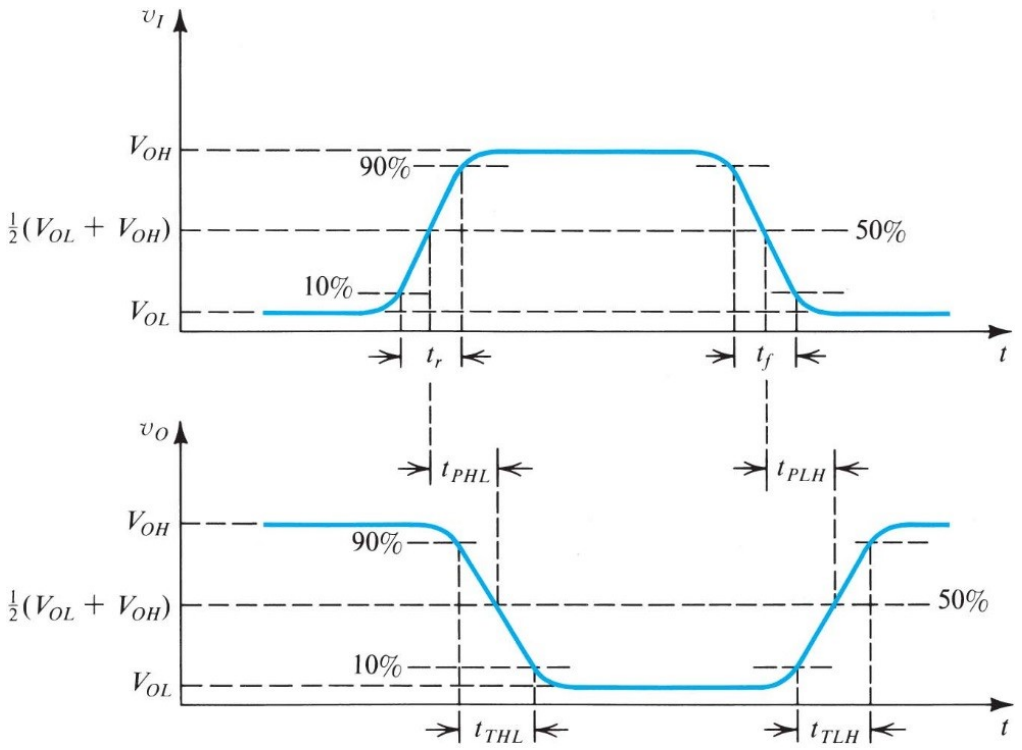
  $P_D \approx fCV_{DD}^2$
- Propagation delay, t_P, at frequency, f

  $t_P \approx \frac{1}{2f}$
- Power delay product, PDP, is a logic technology figure of merit (should be small)

  $PDP = R_D t_P \approx \frac{1}{2} CV_{DD}^2$
- Energy delay product, EDP, is a logic design figure of merit (should be small)

  $EDP = \{\text{energy} \times \text{time per transition}\} = PDP \times t_P$





Power delay product can be physically interpreted as average energy dissipation per inverter transition.