F12 – Output Stages

Outline

- Classification of output stages
  - Class A
  - Class B
  - Class AB
  - Class C
  - Class D
- Operation and power efficiency of class A, B, and AB
- CMOS implementation of class AB output stage
- Power transistors

Reading Guide *Sedra/Smith 7ed int*

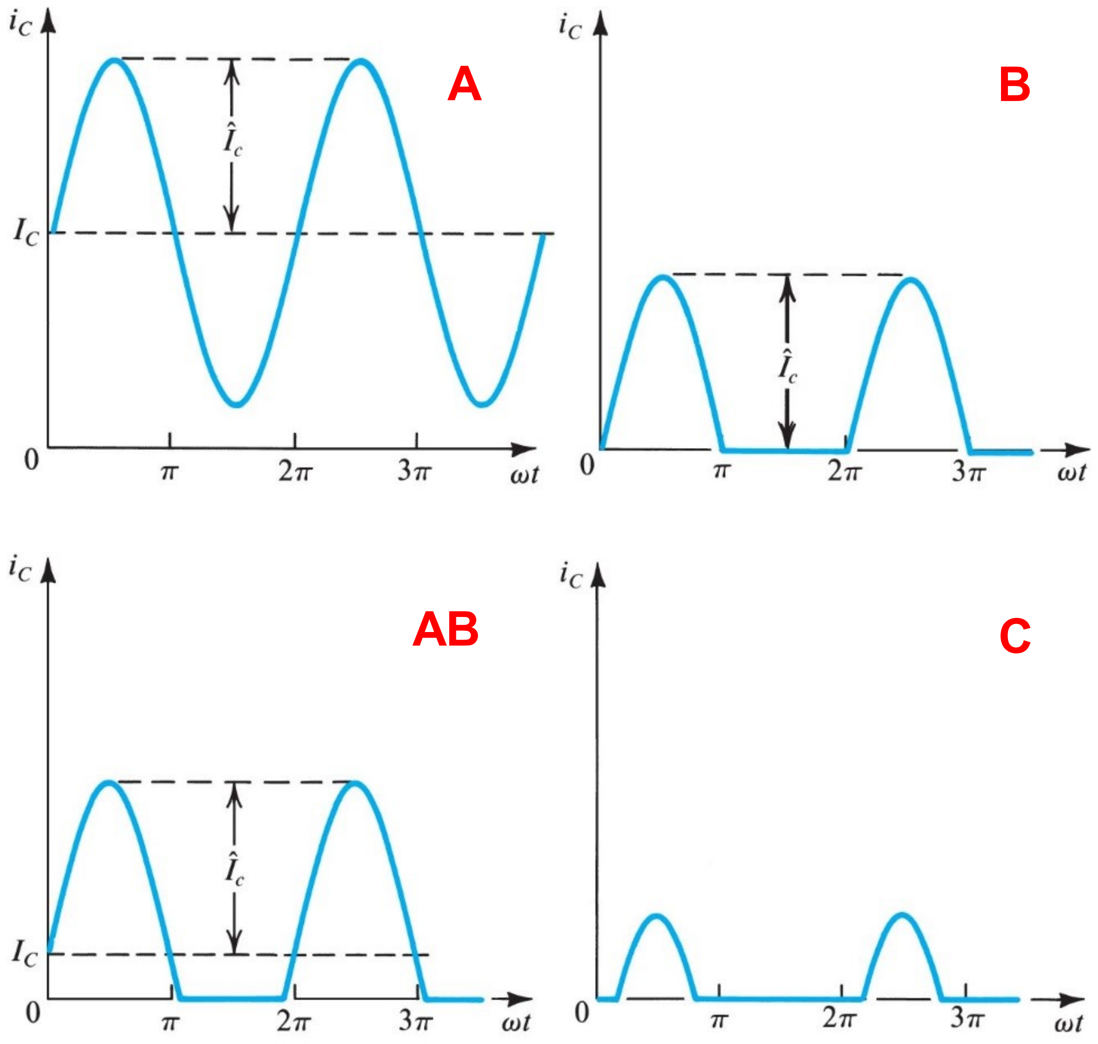
- Chapter 11.1-5 (output stages)
- (Chapter 11.6 (variations))
- Chapter 11.7 (CMOS AB stage)
- (Chapter 11.8-10 (PAs, power devices))

Problems *Sedra/Smith 7ed int*

- P11.2, 11.11, 11.19(a-b), 11.56

Classification of Output Stages

- Output stages are primarily classified by their periodic active angle, θ
- Linear and "quasi-linear complementary" amplifiers
  - Class A: $\theta = 360°$
  - Class B: $\theta = 180°$
  - Class AB: $180° < \theta \ll 360°$
- Small angle (tuned resonator) amplifiers
  - Class C: $0° < \theta < 180°$
- Pulse width modulated (switching) amplifiers
  - Class D: $\theta = 360°$ non-linear
- … and more sophisticated classes (E, F, G, H, etc.)



Source(/ Emitter) Follower as an Output Stage

- Common drain(/ collector) a.k.a. source(/ emitter) follower
  - High input resistance

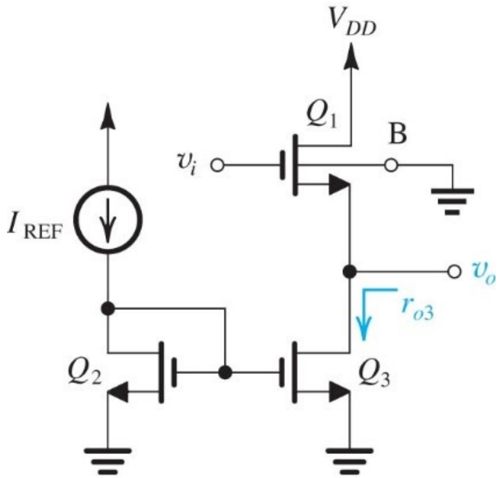
    $$R_i = \infty$$

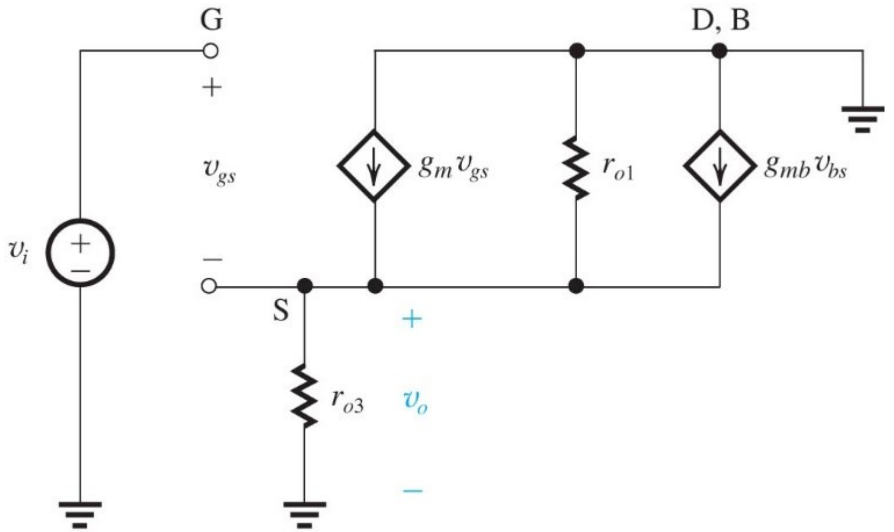
  - Voltage buffer

    $$A_{vo} \approx \frac{1}{1+\chi}$$

  - Low output resistance

    $$R_o \approx \frac{1}{g_m(1+\chi)}$$





Ideal input/ output resistance for a voltage amplifier, but gain must be provided by previous stages.

Class A

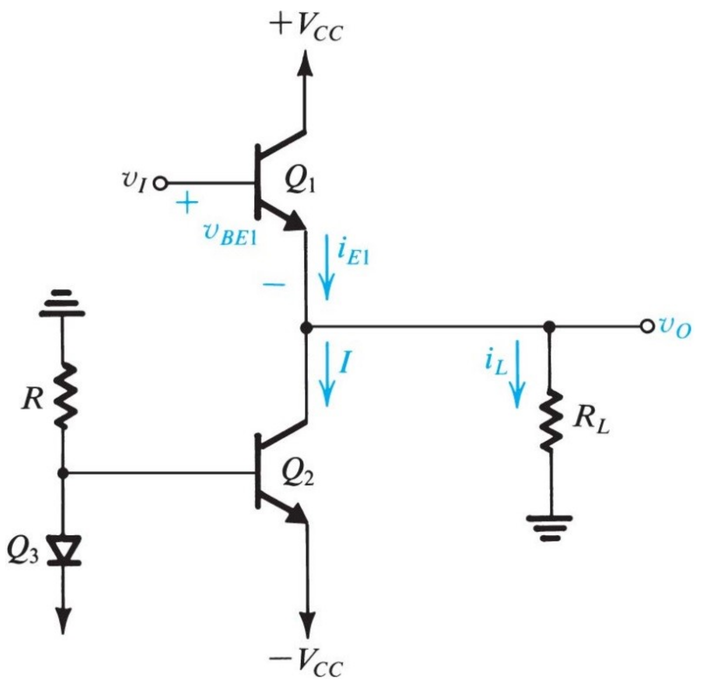
- Common drain(/ emitter), Q1, with active load, Q2

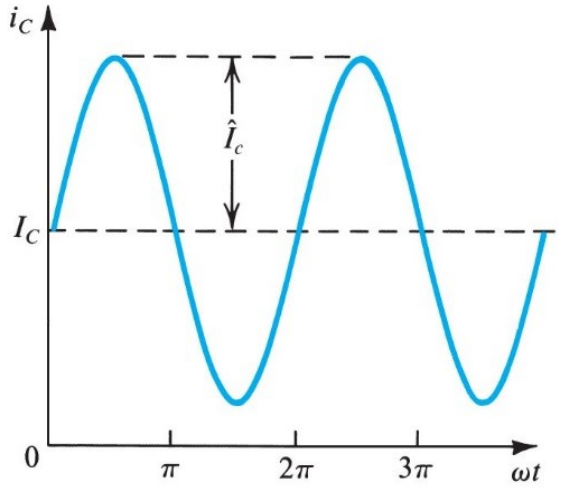
- Balanced supplies ($\pm V_{CC}$) allow load to ground

  $$V_{EE} = -V_{CC}$$

- Bias/ load should be designed to support rail-to-rail signal operation
  - Positive output: Q1 on
  - Negative output: Q1 off

$$v_O = -IR_L \leq -V_{CC}$$
$$\Leftrightarrow$$
$$R_L \geq \frac{V_{CC}}{I}$$





Class A: Large Signal Operation

- Non-inverting operation centred on $i_{E1} = I$ and $v_O = 0$
  - Rail-to-rail operation (neglecting Q1 and Q2 v_{CEsat})

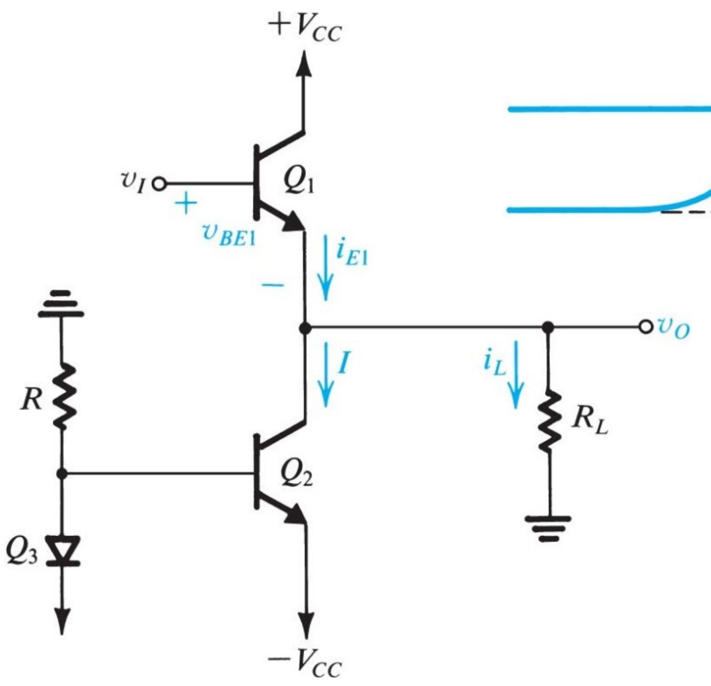
$$R_L \geq \frac{V_{CC}}{I} \quad \Rightarrow \quad -V_{CC} < v_O < V_{CC}$$

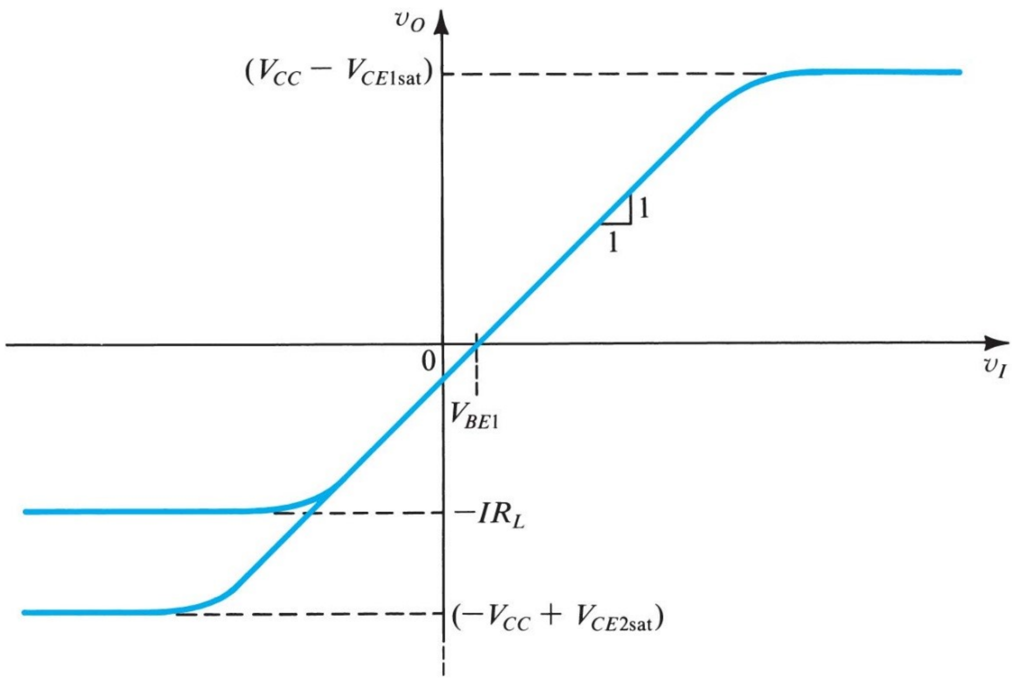
  - High output (Q1 on)

$$v_O = V_{CC}, \qquad i_{E1} = 2I$$
$$\Leftrightarrow$$
$$i_L = i_{E1} - I = I$$

  - Low output (Q1 off)

$$v_O = -V_{CC}, \qquad i_{E1} = 0$$
$$\Leftrightarrow$$
$$i_L = i_{E1} - I = -I$$





Class A: Signal Waveforms

- Rail-to-rail output voltage swing (neglecting v_{CEsat})
  - Load resistance selected to support rail-to-rail operation

    $$R_L = \frac{V_{CC}}{I}$$

  - Collector-emitter voltage shifted and inverted w.r.t output

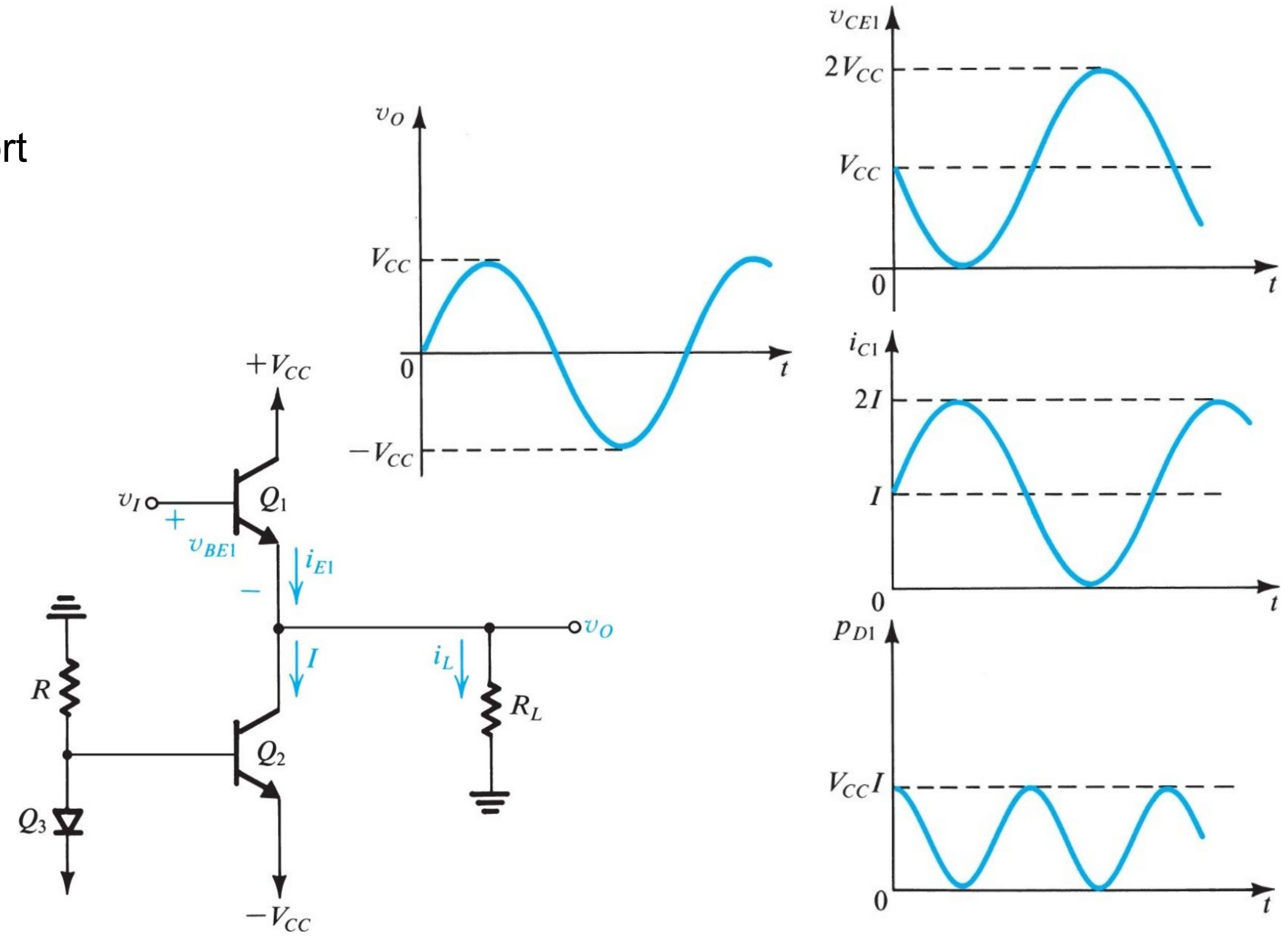
    $$-V_{CC} < v_{CE1} = V_{CC} - v_O < V_{CC}$$

  - Current swing

    $$0 < i_{C1} \approx I + v_O R_L < 2I$$

  - Power dissipated in Q1

    $$0 < p_{D1} = v_{CE1} i_{C1} < V_{CC} I$$



Class A: Power Efficiency

- Power efficiency
  - Ratio of load power, P_L, to supply power, P_S

$$\eta = \frac{P_L}{P_S} = \frac{1}{4}\left(\frac{\hat{V}_o}{IR_L}\right)\left(\frac{\hat{V}_o}{V_{CC}}\right) \leq 25\%$$

$$10\% < \eta_{typical} < 20\%$$

- Harmonic output assumed

$$v_O = \hat{V}_o \sin(\omega t) = \hat{V}_o \sin\left(\frac{2\pi}{T}t\right)$$

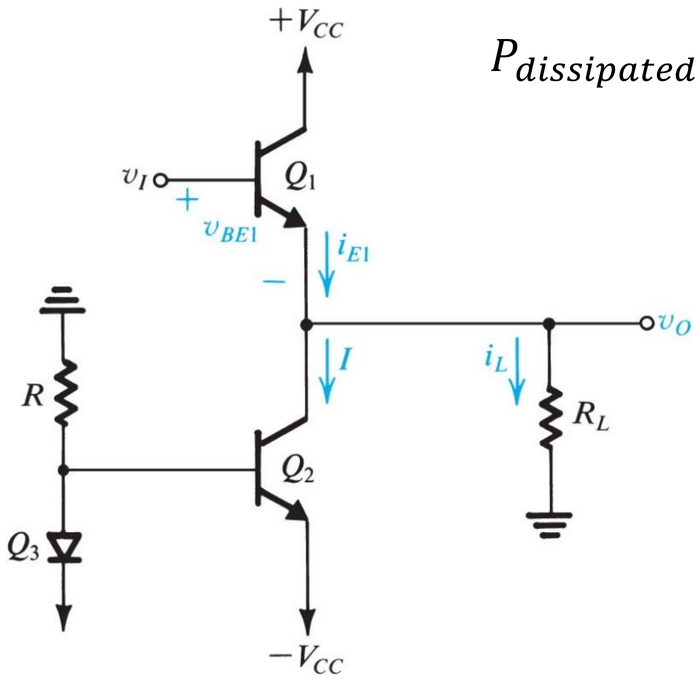
- Load power

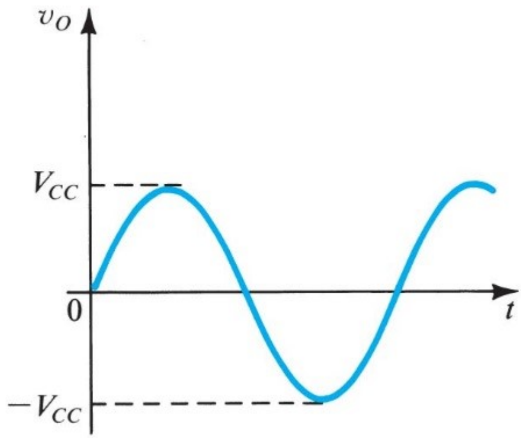
$$P_L = \frac{v_O^2}{R_L} = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

- Supply power

$$P_S = P_{S+} + P_{S-} = 2V_{CC}I$$

$$P_{dissipated} = P_L - P_S = 2V_{CC}I - \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

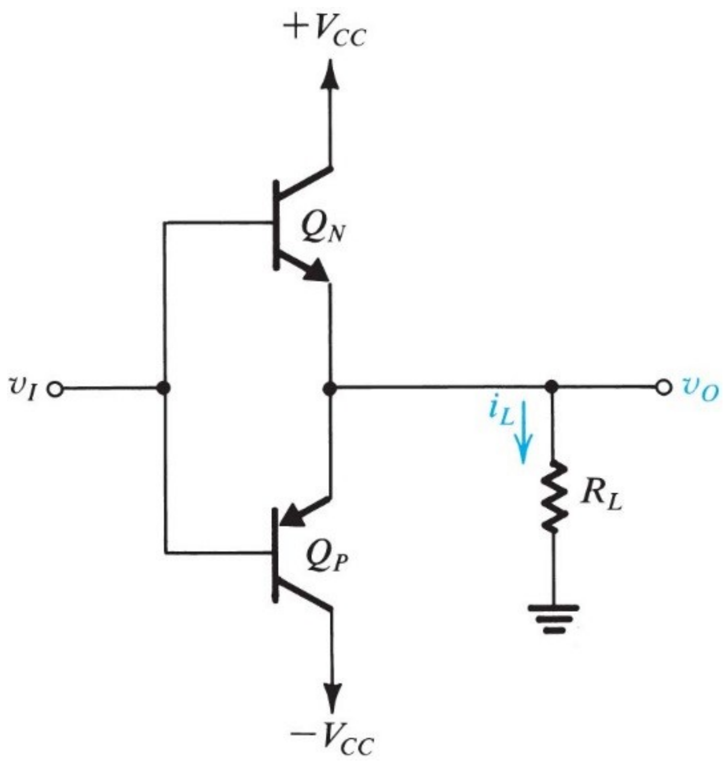


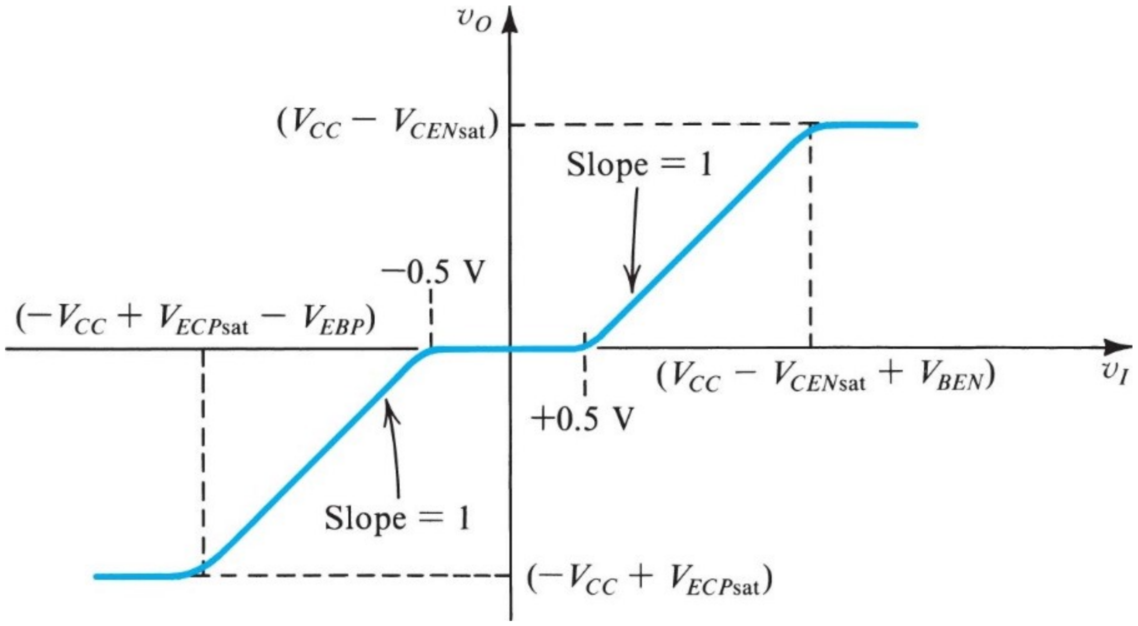


Power dissipation monotonically reduced with output voltage level, but high quiescent value and low maximum efficiency.

Complementary Emitter(/ Source) Follower as an Output Stage

- Complementary push-pull configuration
  - One transistor active
  - One transistor cutoff

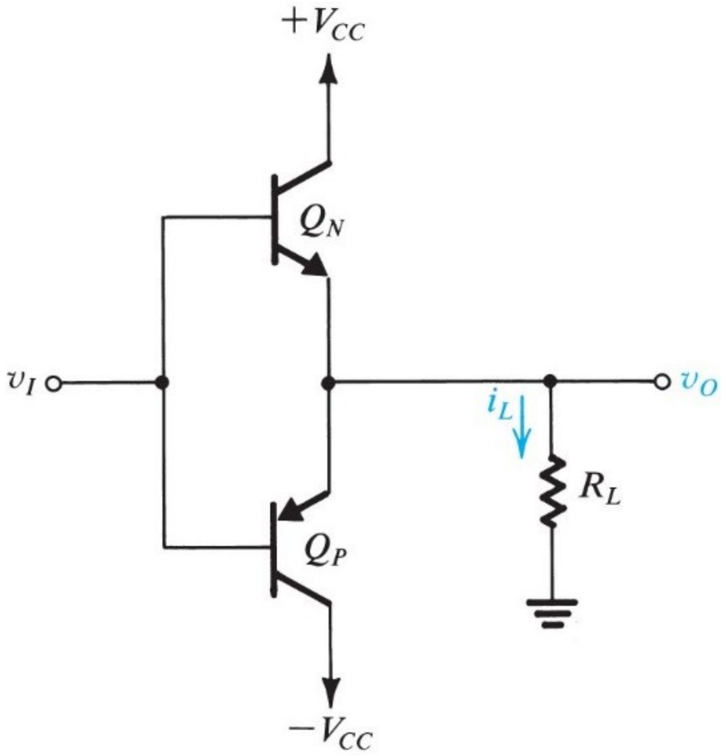


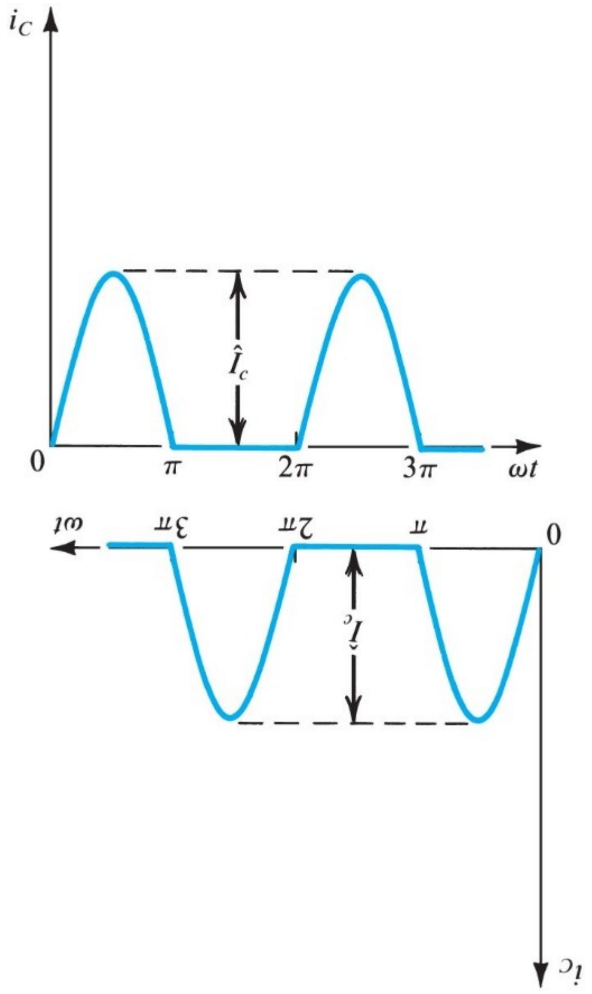


Q1 sources (pushes) load current,
Q2 sinks (pulls) load current.

Class B

- Complementary push-pull configuration
- Balanced supplies ($\pm V_{CC}$) allow load to ground
- Supports rail-to-rail operation (within v_{CEsat})
  - Positive output: QN on, QP off
  - Negative output:QP on, QN off
- Dead band about zero input
  - Both QN and QP cutoff



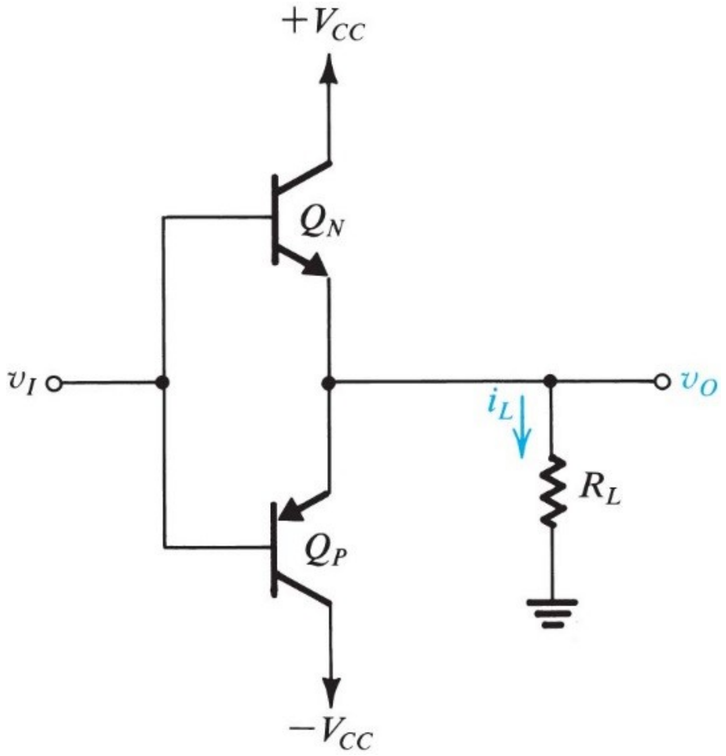


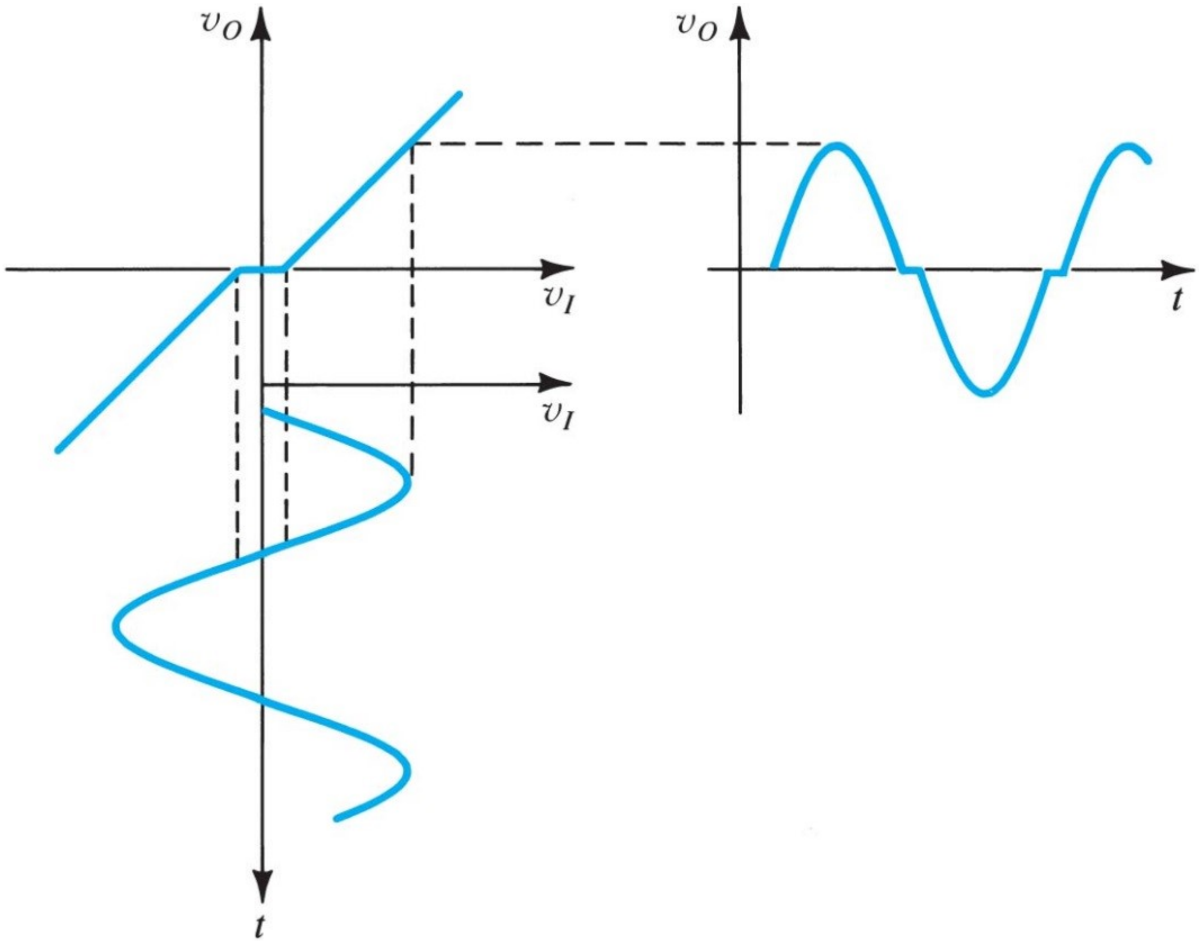
Class B: Crossover Distortion

- Dead band due to conduction threshold voltage

  $|v_I| < v_{BEactive} \Rightarrow v_O \approx 0$

- Signal distortion at zero-crossing





Crossover distortion can be circumvented through use of clever biasing.

Class B: Power Efficiency

- Power efficiency
  - Ratio of load power, P_L, to supply power, P_S

$$\eta = \frac{P_L}{P_S} = \frac{\pi}{4}\left(\frac{\hat{V}_o}{V_{CC}}\right) \leq 78.5\%$$

$$40\% < \eta_{typical} < 60\%$$

- Harmonic output assumed

$$v_O = \hat{V}_o \sin(\omega t) = \hat{V}_o \sin\left(\frac{2\pi}{T}t\right)$$

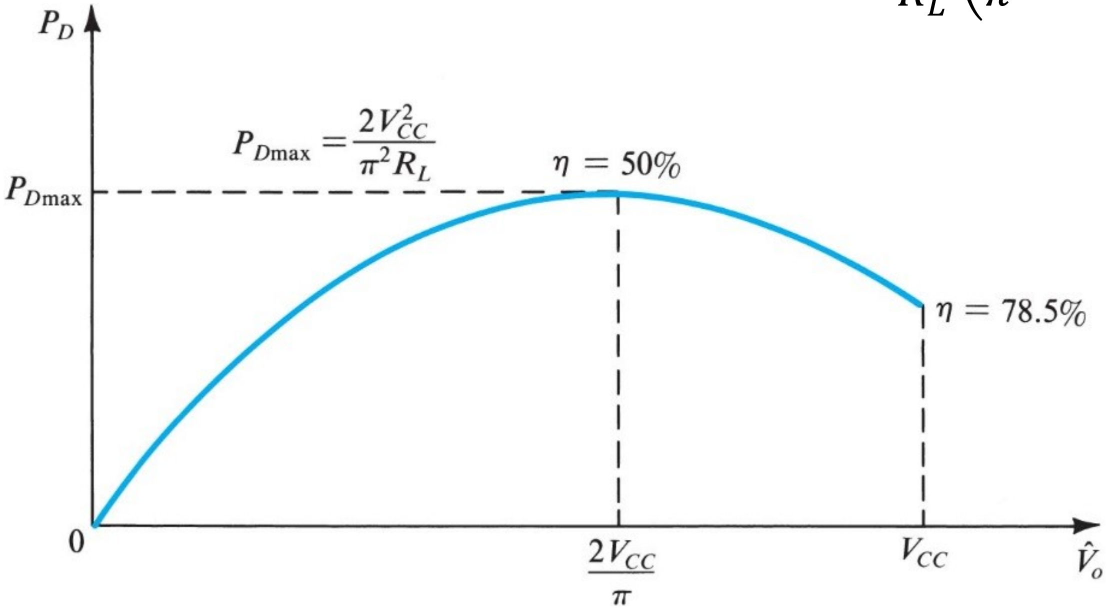
- Load power

$$P_L = \frac{v_O^2}{R_L} = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

- Supply power

$$P_S = P_{S+} + P_{S-} = \frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC}$$

$$P_D = P_{dissipated} = P_L - P_S = \frac{\hat{V}_o}{R_L}\left(\frac{2}{\pi}V_{CC} - \frac{1}{2}\hat{V}_o\right)$$



Power dissipation low for low and high output voltage, and quite good maximum efficiency.

Class B: Single Supply

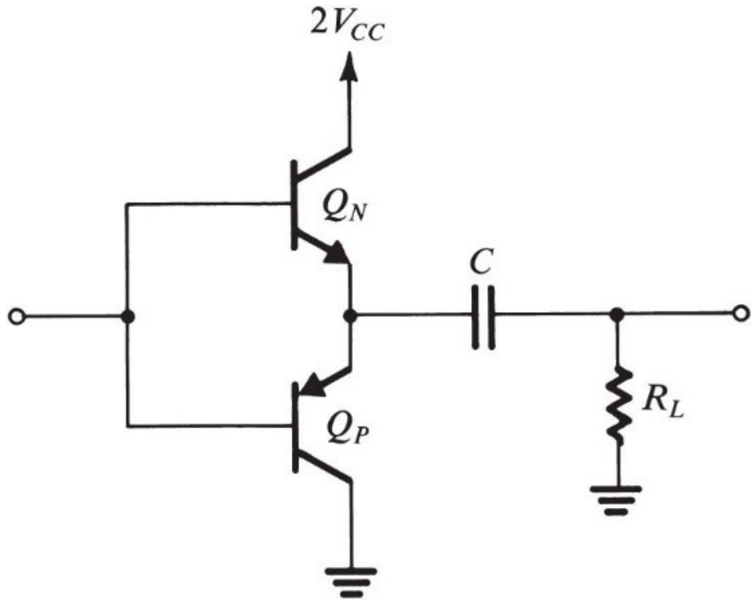
- Shifted positive supply

$$V'_{CC} = V_{CC} + V_{EE} = \{V_{EE} = V_{CC}\} = 2V_{CC}$$

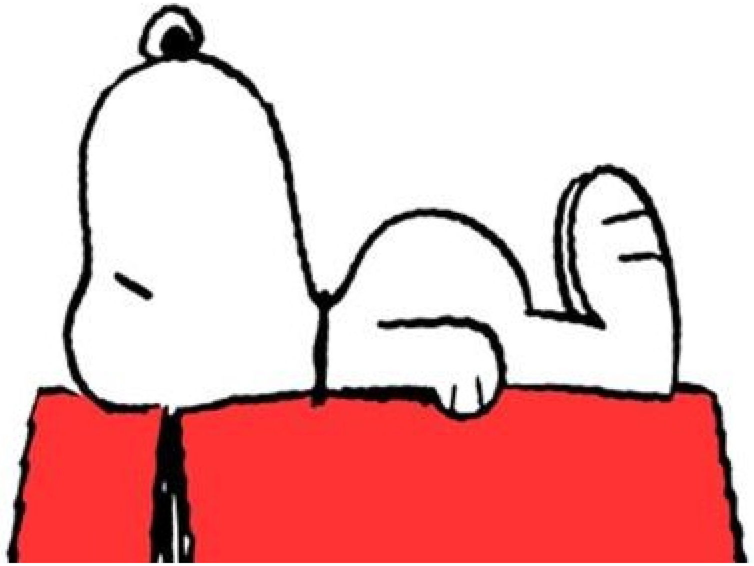
- Grounded current sink

$$V'_{EE} = -V_{EE} + V_{EE} = 0$$

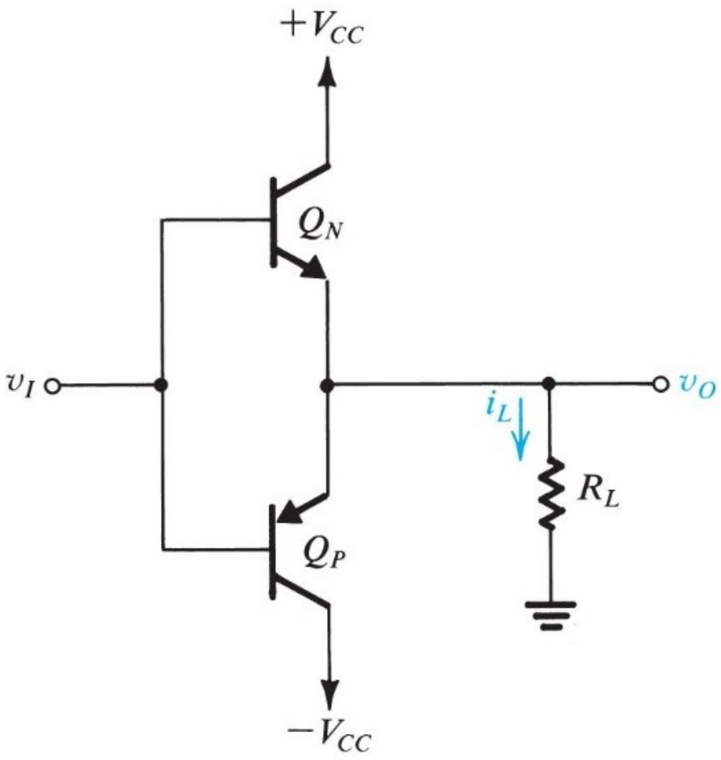
- Capacitively coupled load to ground
    - Separates dc from signal

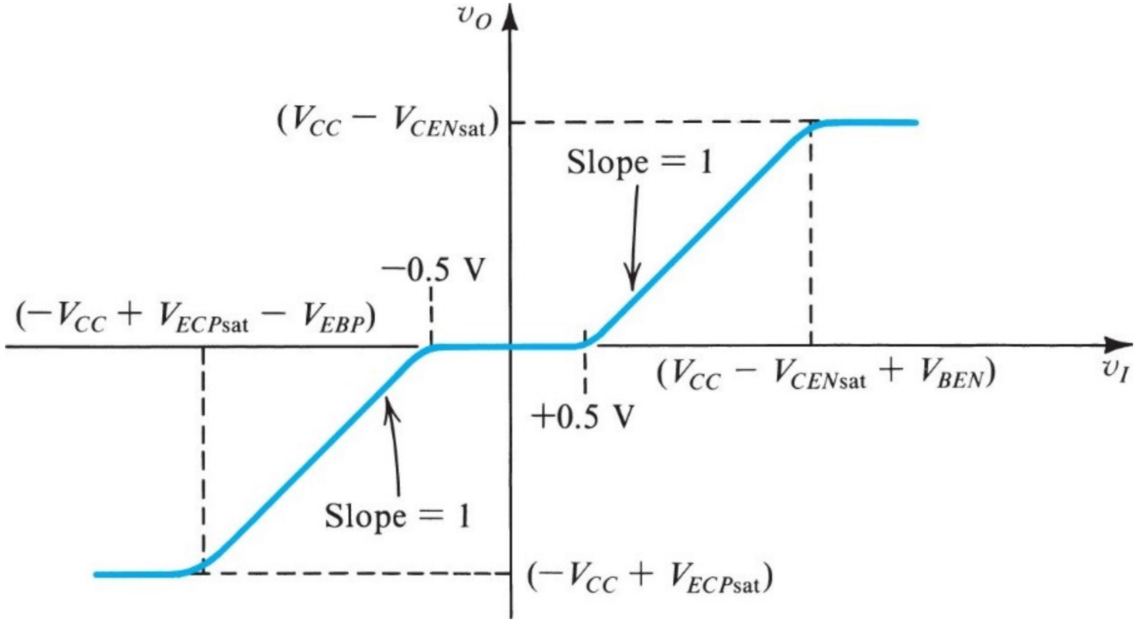


BREAK



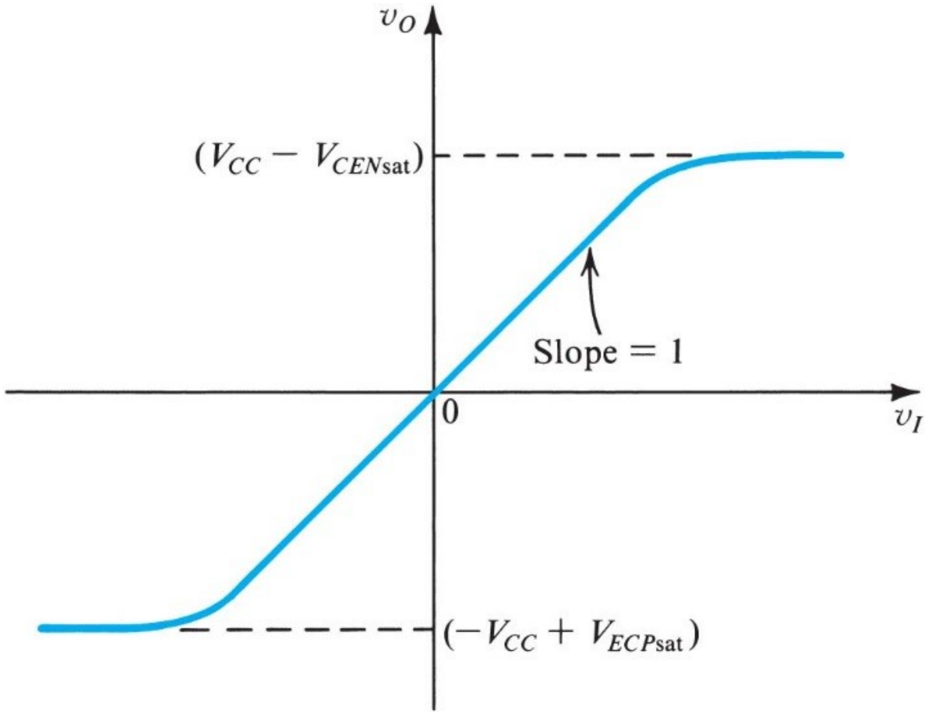
Attractive to eliminate class B conduction threshold; why and how?

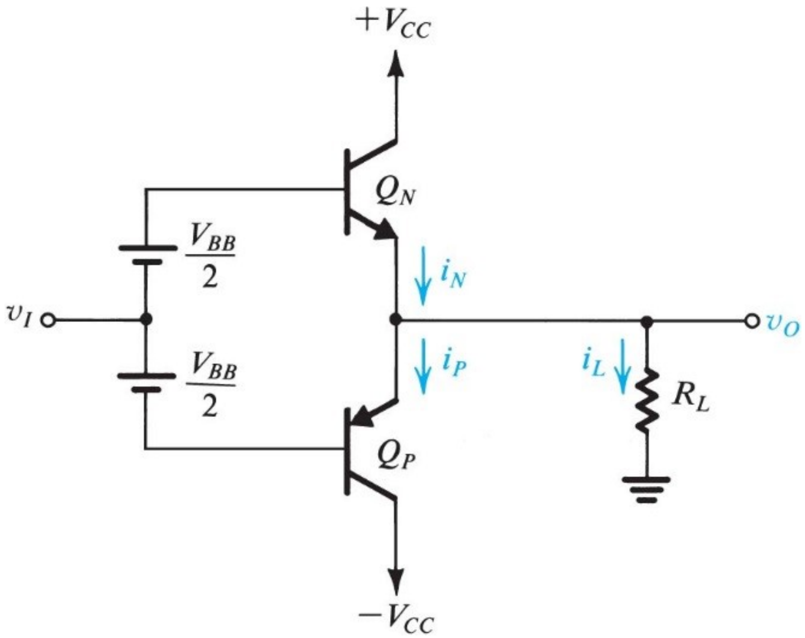


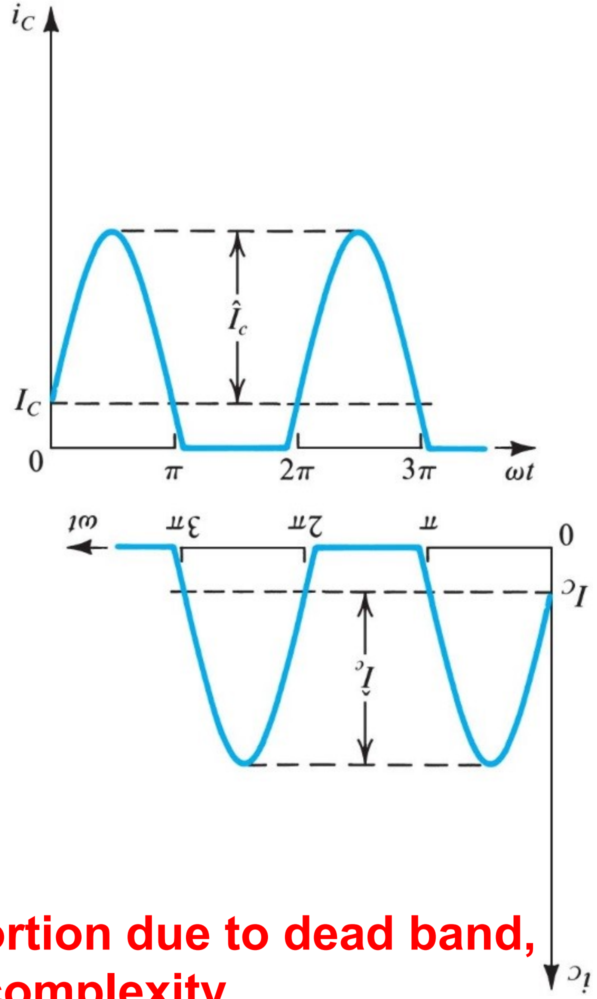


Class AB

- Class A at very low bias, or bias on a class B stage
  - Removes conduction threshold, no crossover distortion
  - Small quiescent power dissipation







Elimination of harmonic distortion due to dead band, at the cost of efficiency and complexity.

Class AB: Quiescent Current and Large Signal Operation

- Input bias generates quiescent current

$$i_N\Big|_{v_O=0} = i_P\Big|_{v_O=0} = I_Q = I_S \exp\left(\frac{V_{BB}}{2V_T}\right)$$

- Positive output voltage (negative just opposite)
  - Output follows input

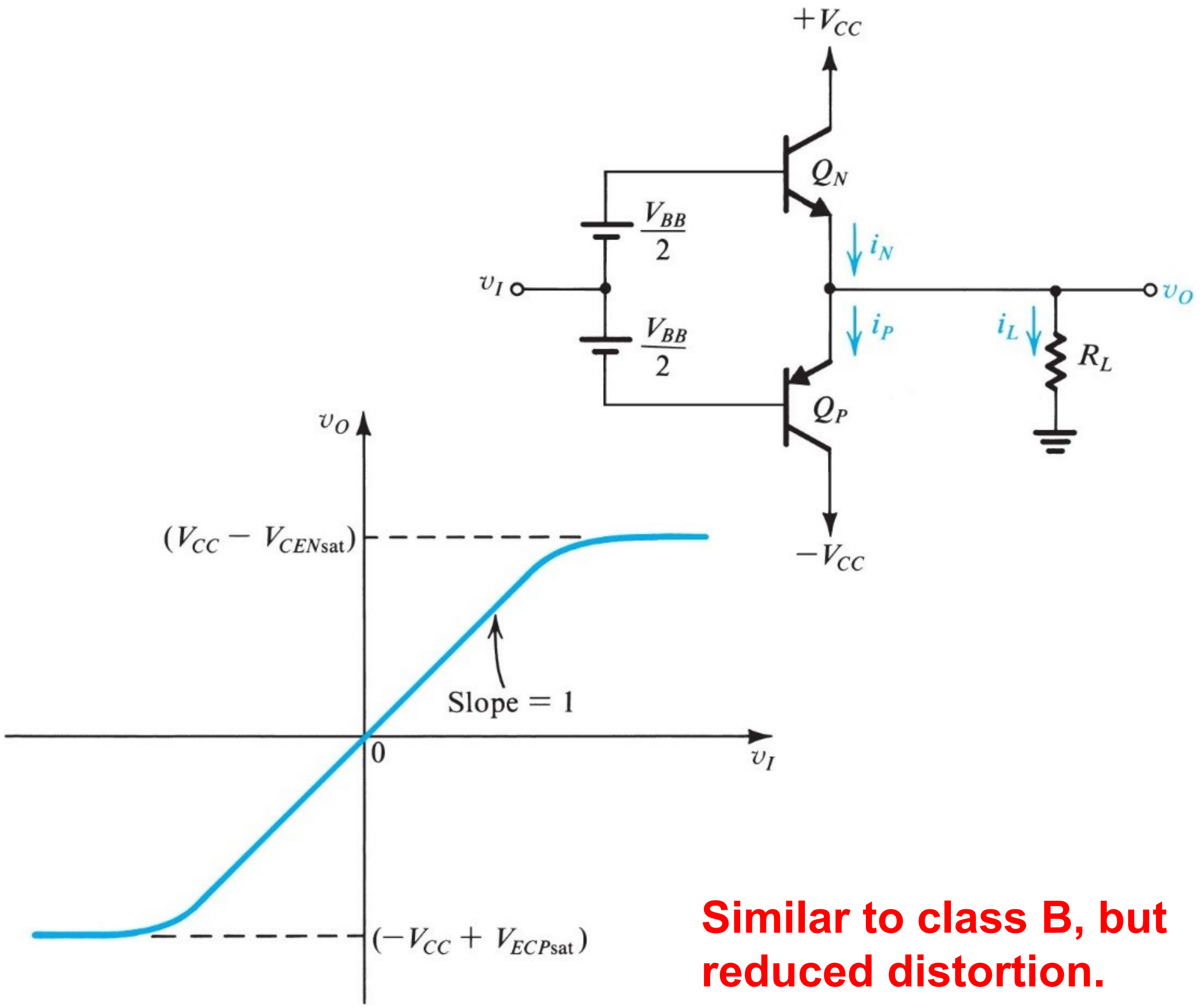
$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN}, \qquad i_L = \frac{v_O}{R_L}$$

  - Incremental load current supplied by QN, which requires increased QN base drive

$$i_N = i_P + i_L, \qquad v_{BEN} + v_{EBP} = V_{BB}$$

  - Product of device currents remain constant

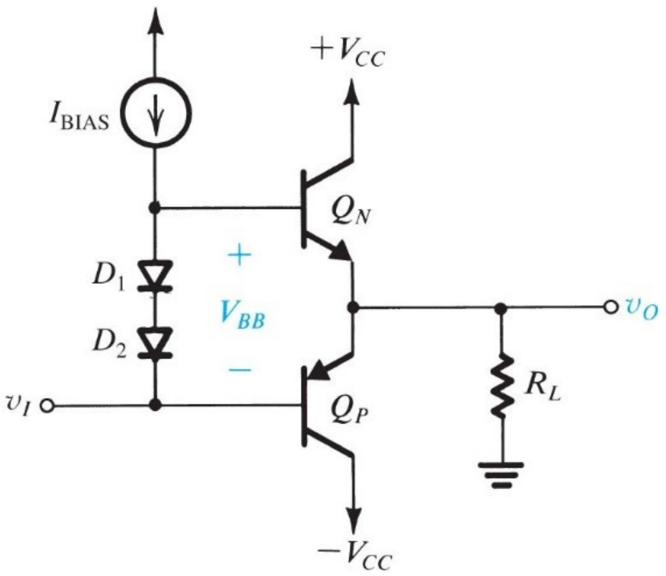
$$i_N i_P = I_Q^2 \quad \Rightarrow \quad i_N^2 - i_L i_N - I_Q^2 = 0$$



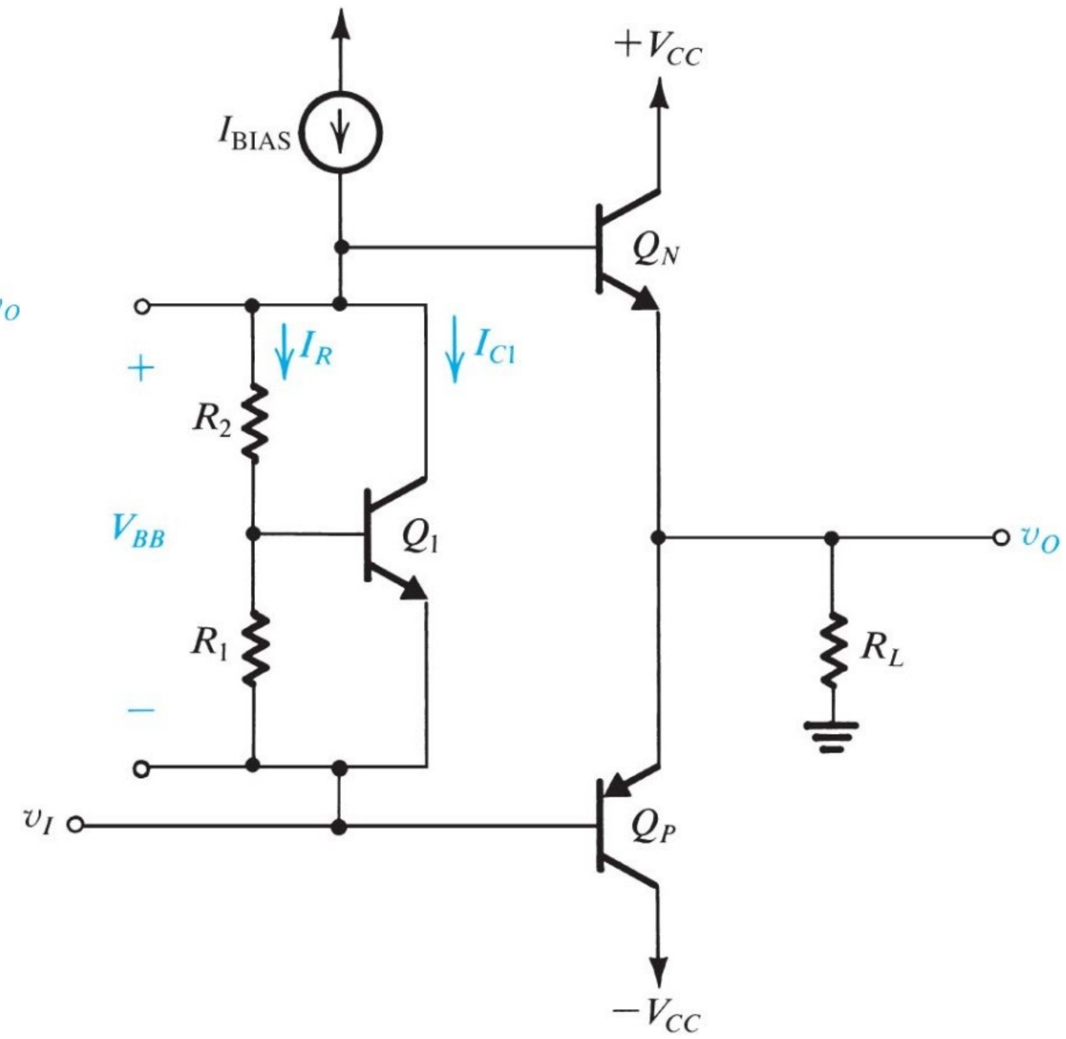
Similar to class B, but reduced distortion.

Biasing the BJT Class AB Input

- Diodes
  - Simple but primitive



- Base-emitter multiplier
  - Design ratio using resistances



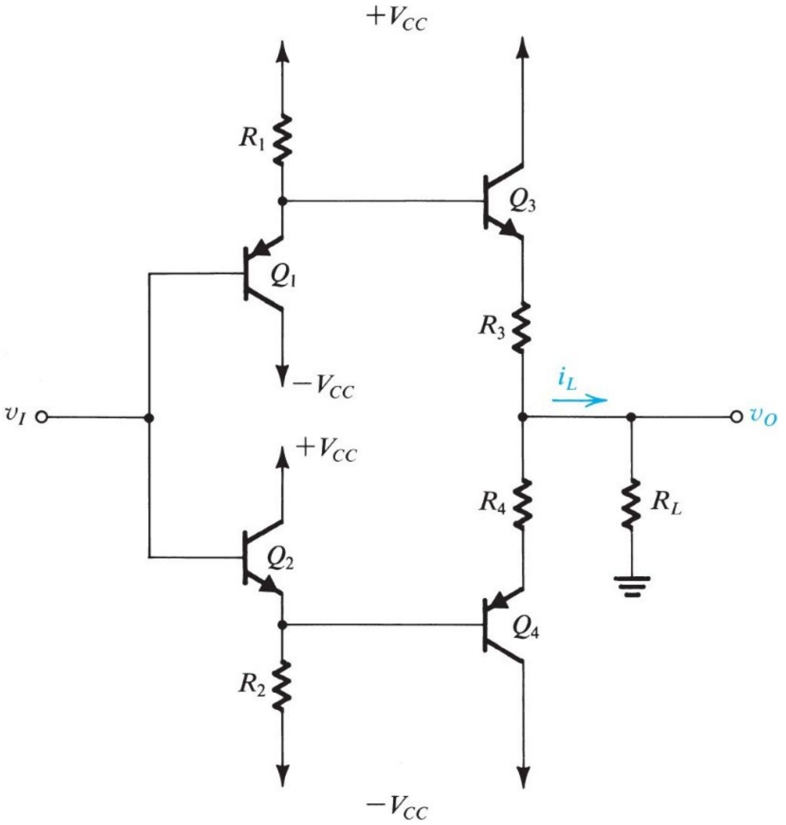
$$I_R = \frac{V_{BE1}}{R_1}$$

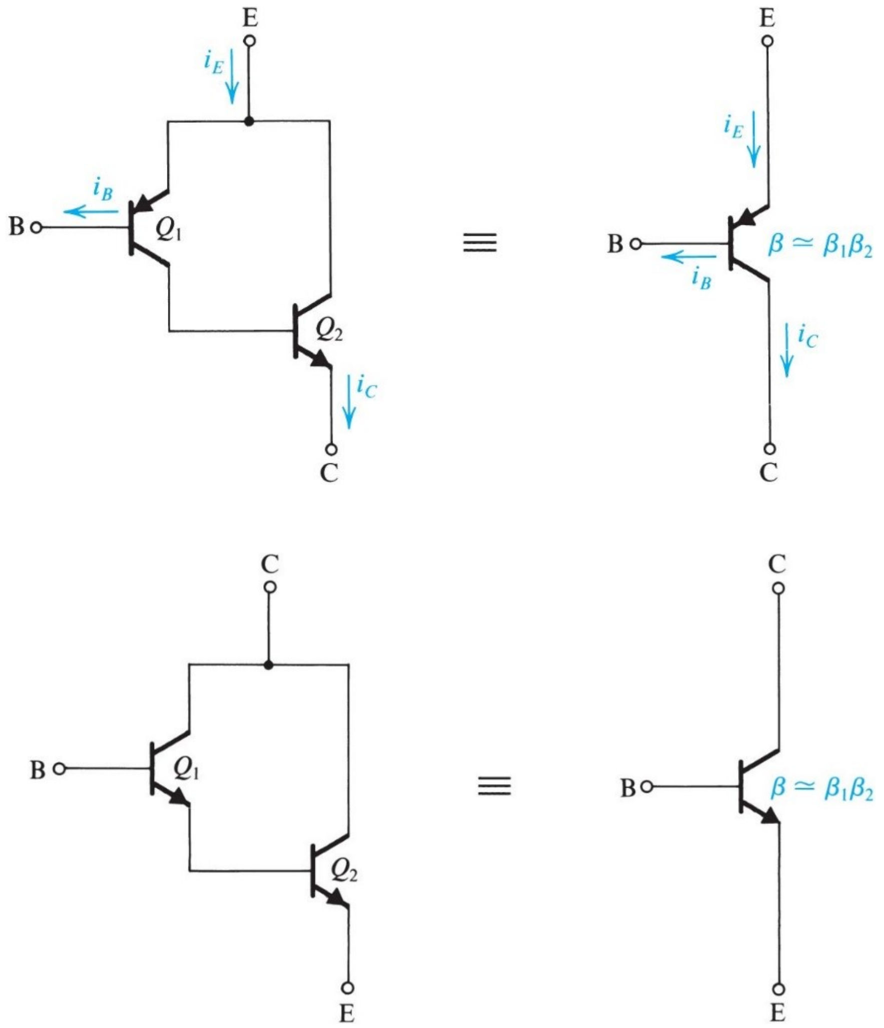
$$V_{BB} = I_R(R_1 + R_2) = V_{BE1}\left(1 + \frac{R_2}{R_1}\right)$$

(Class AB: BJT Variations)

- Input emitter followers
  - Buffers input signal
  - Provides AB biasing

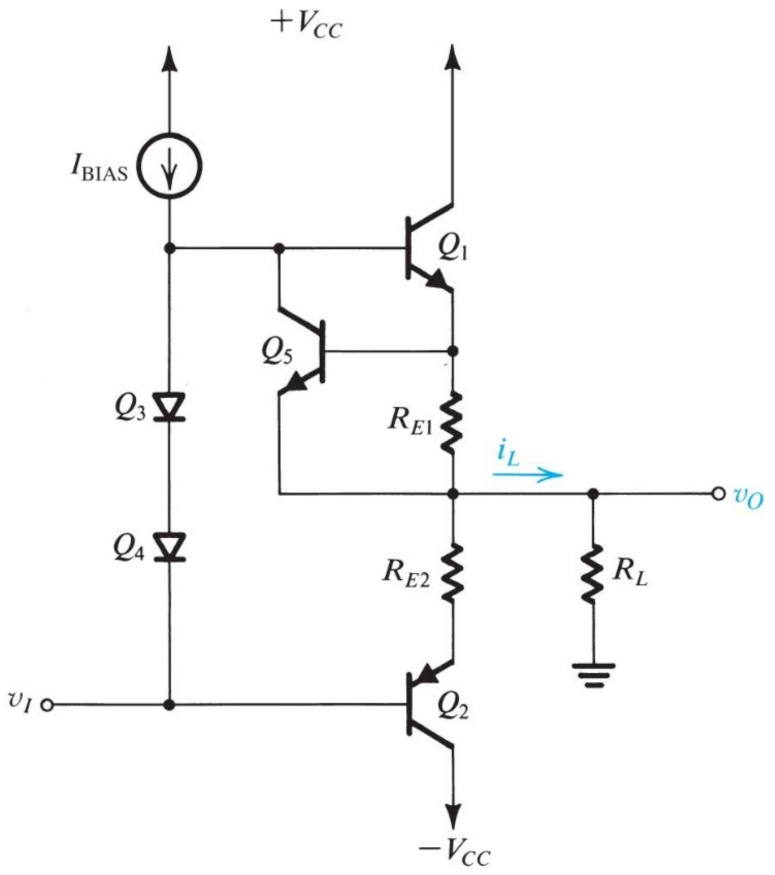
- Compound devices boost performance
  - Darlington configuration
  - Compound PNP

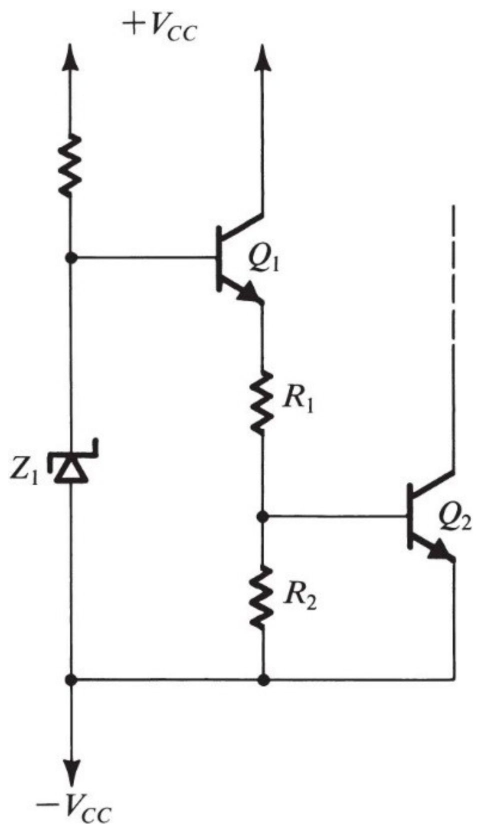




(Protection Circuits)

- Output short circuit protection, protects against too high load current
  - Q5 normally off
  - High current in R_{E1} turns Q5 on
  - Q5 on turns Q1 off
- Thermal shutdown, protects chip against meltdown
  - Q2 normally off
  - Z1 positive temperature coefficient
  - Q1 negative temperature coefficient
  - High temp turns Q2 on
  - Q2 on robs bias from another stage





Protect the amplifier from the user.

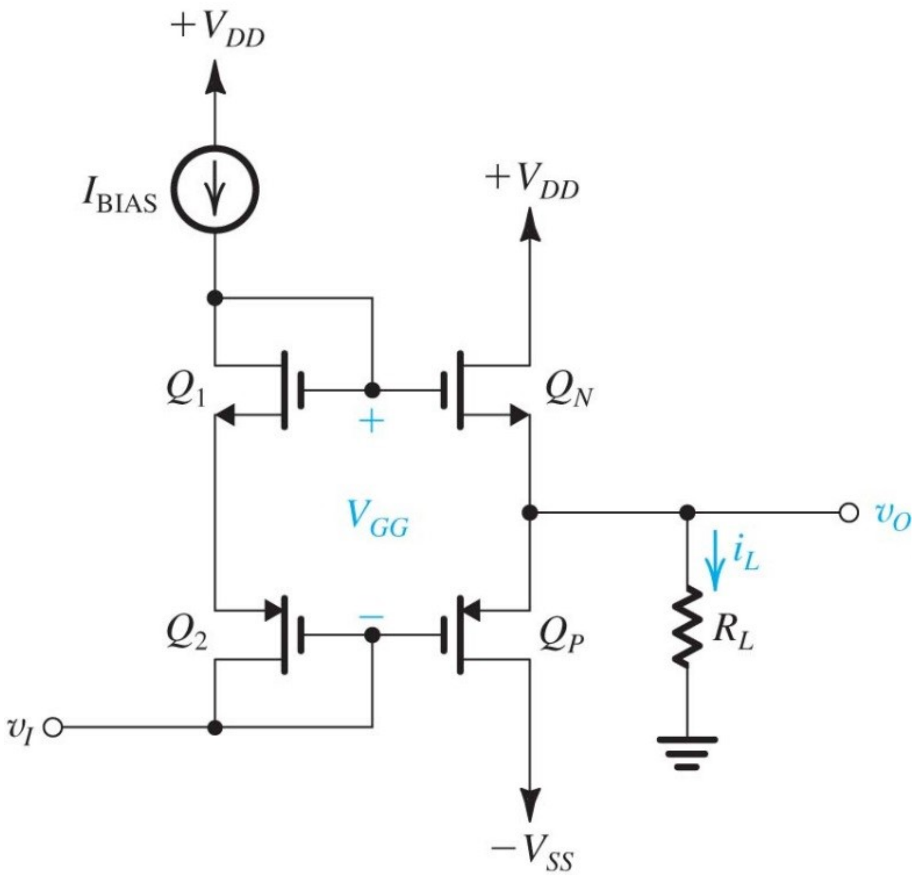
Class AB: Classical CMOS Configuration

- Complementary source follower with diode connected input devices
  - Equivalent to BJT AB with diode bias
  - Voltage buffer
  - Low output resistance
  - Limits to the output swing
    - QN and QP overdrive voltages
    - Input circuit active load overdrive voltage
    - Bias current source overdrive voltage

$$-V_{SS} + V_{OVI} + |V_{tp}| + |v_{OVP}| < v_O < V_{DD} - V_{OVB} - V_{tn} - v_{OVN}$$

  - Quiescent current due to input bias

$$i_{DN}\Big|_{v_O=0} = i_{DP}\Big|_{v_O=0} = I_Q = I_{BIAS}\frac{(W/L)_n}{(W/L)_1}$$



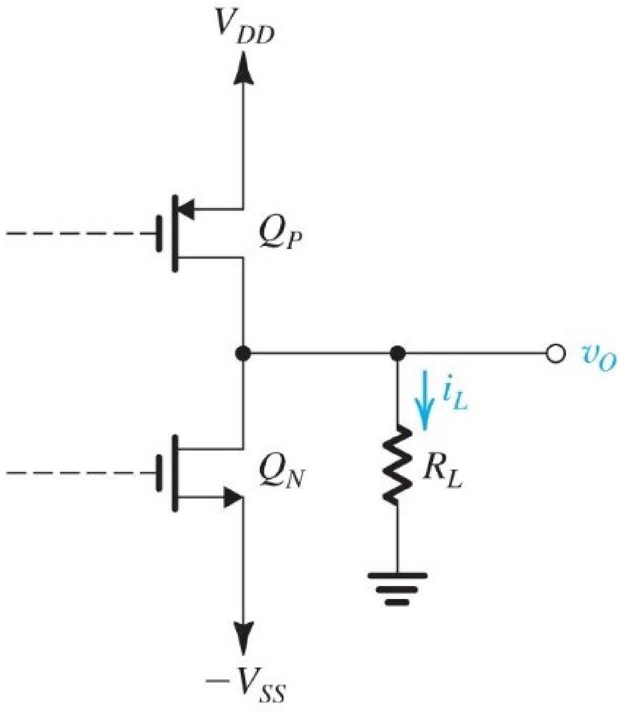
Class AB: Wide Swing CMOS Configuration

- Complementary push-pull common source
  - Provides high voltage gain, as compared to follower
  - Moderately high output impedance

$$R_o = r_{on} || r_{op}$$

  - Output swing improved to within an overdrive voltage from the supplies

$$-V_{SS} + v_{OVN} < v_O < V_{DD} - v_{OVP}$$



Output resistance can be improved by feedback.

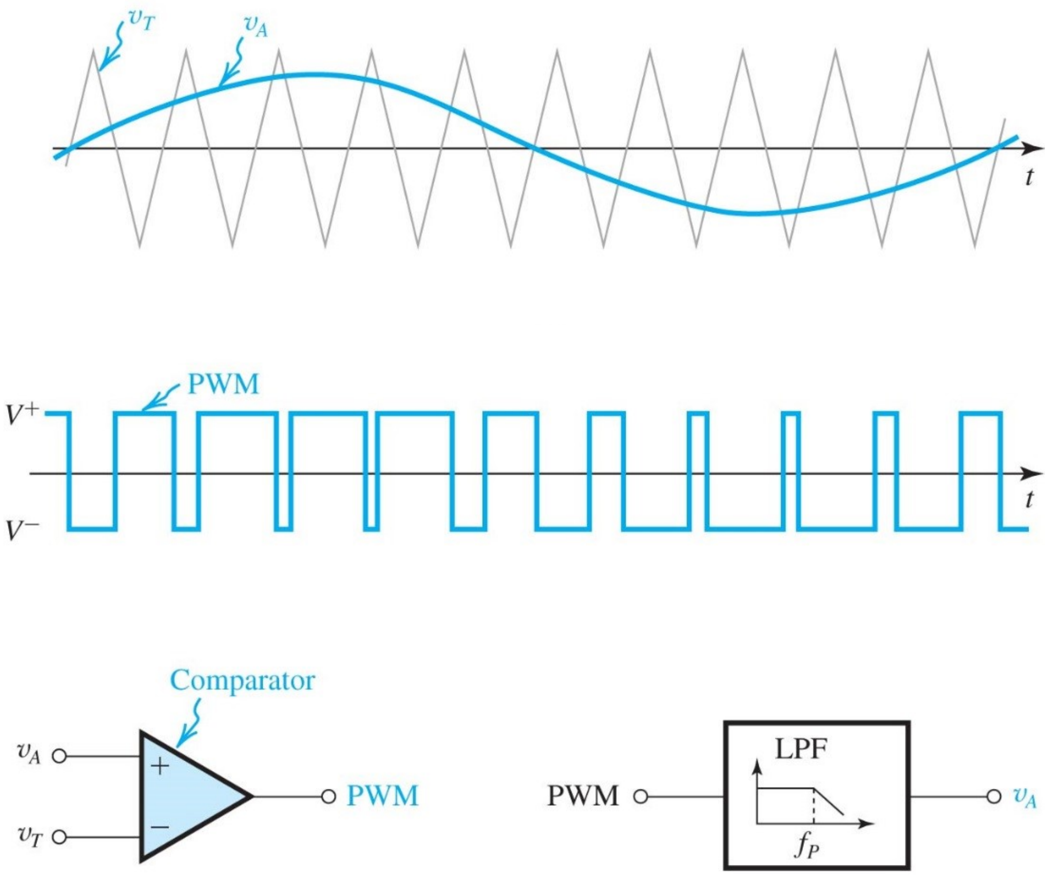
Class D: High Efficiency Switching Amplifier

- High efficiency (ideally 100%)
  - Rapid switch between on and off yields only device power dissipation in a brief moment
  - On or off, no simultaneous voltage and current

$$P_L = v_L i_L \approx V_S I_S = P_S$$

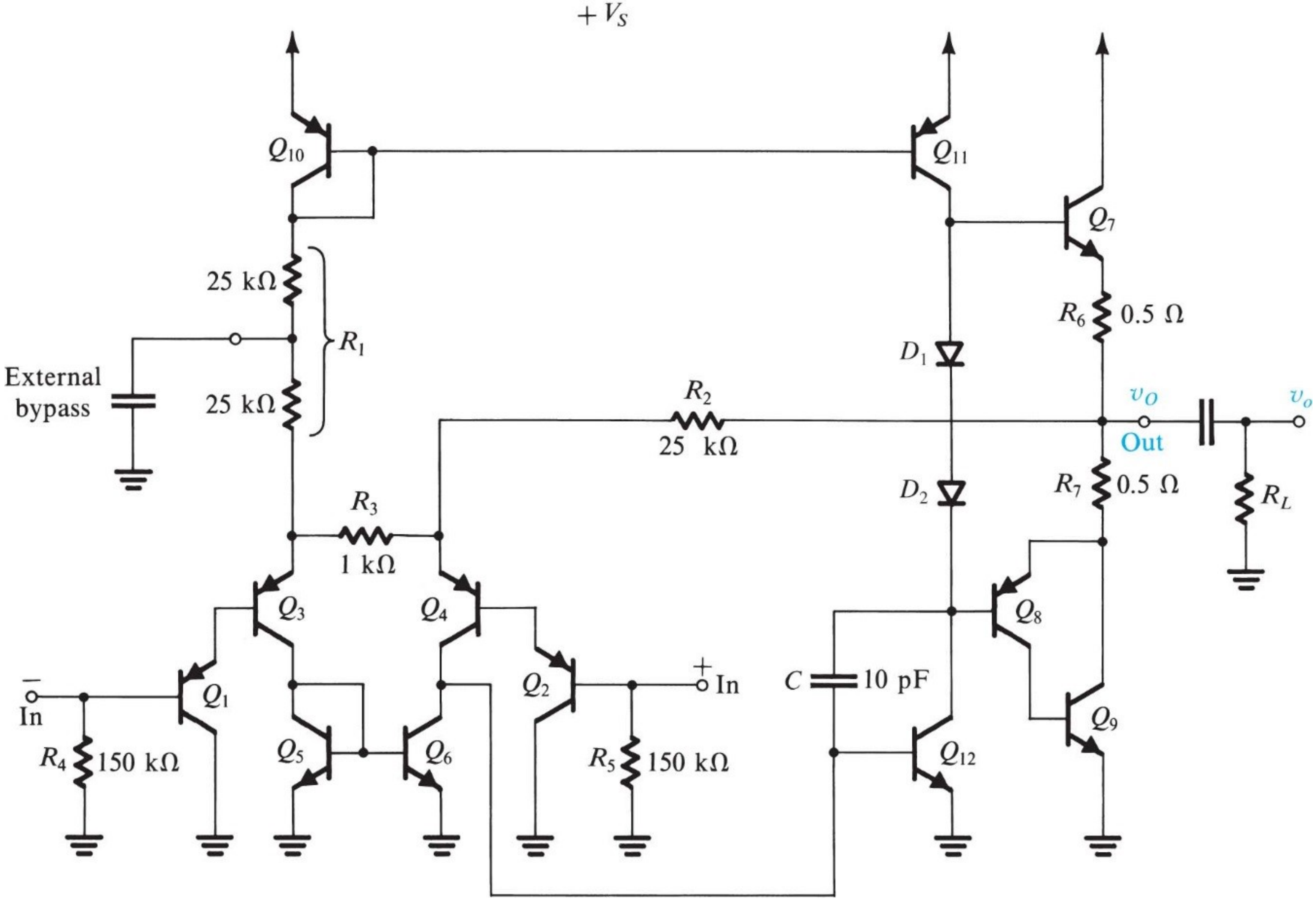
- Transmitter
  - Pulse width modulation (PWM) of signal at a high frequency w.r.t. signal frequency

- Receiver
  - Demodulation by low-pass filtering (moving average)



Power dissipation is high when there is current and voltage simultaneously.

Is it possible to build power amplifiers (PAs) from “normal” transistors?



(Power Transistors)

- High current requires large device: low frequency bandwidth
- High thermal dissipation: temperature coefficients and heat sinks
- High electric fields: velocity saturation