F9 – Differential and Multistage Amplifiers

Outline

- MOS differential pair
  - Common mode signal operation
  - Differential mode signal operation
  - Large signal operation
  - Small signal operation
- Differential and common mode half-circuits
- Common mode rejection
- DC offset
- Differential amplifier w/ current mirror load
- Multistage amplifiers

Reading Guide *Sedra/Smith 7ed int*

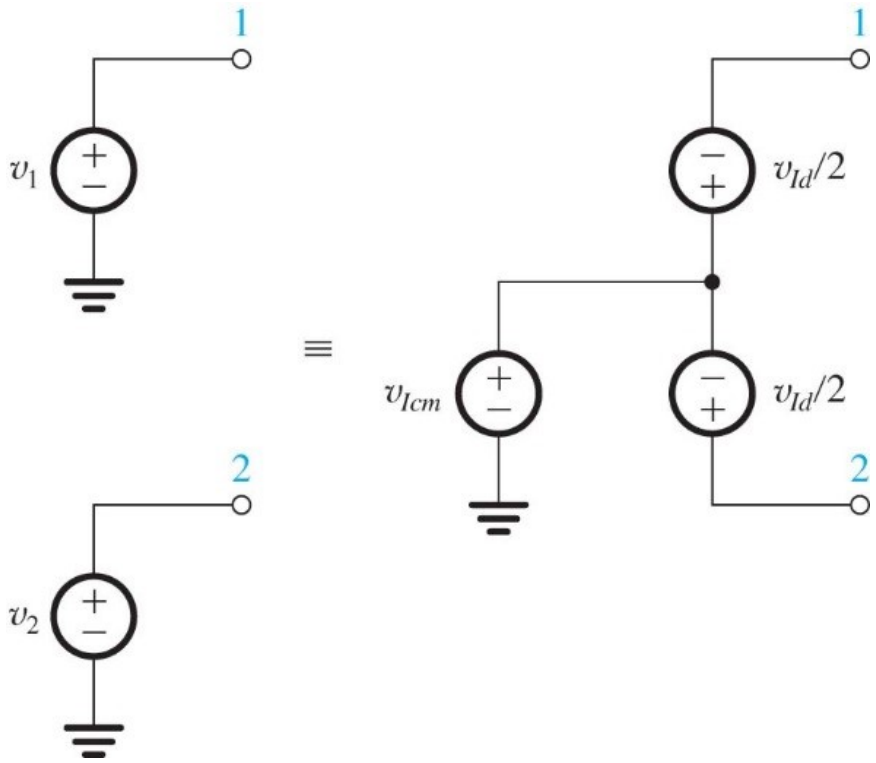
- Chapter 8

Problems *Sedra/Smith 7ed int*

- P8.2, 8.8, 8.17(a-b), 8.18, 8.84

Common and Differential Mode Signals (recap)

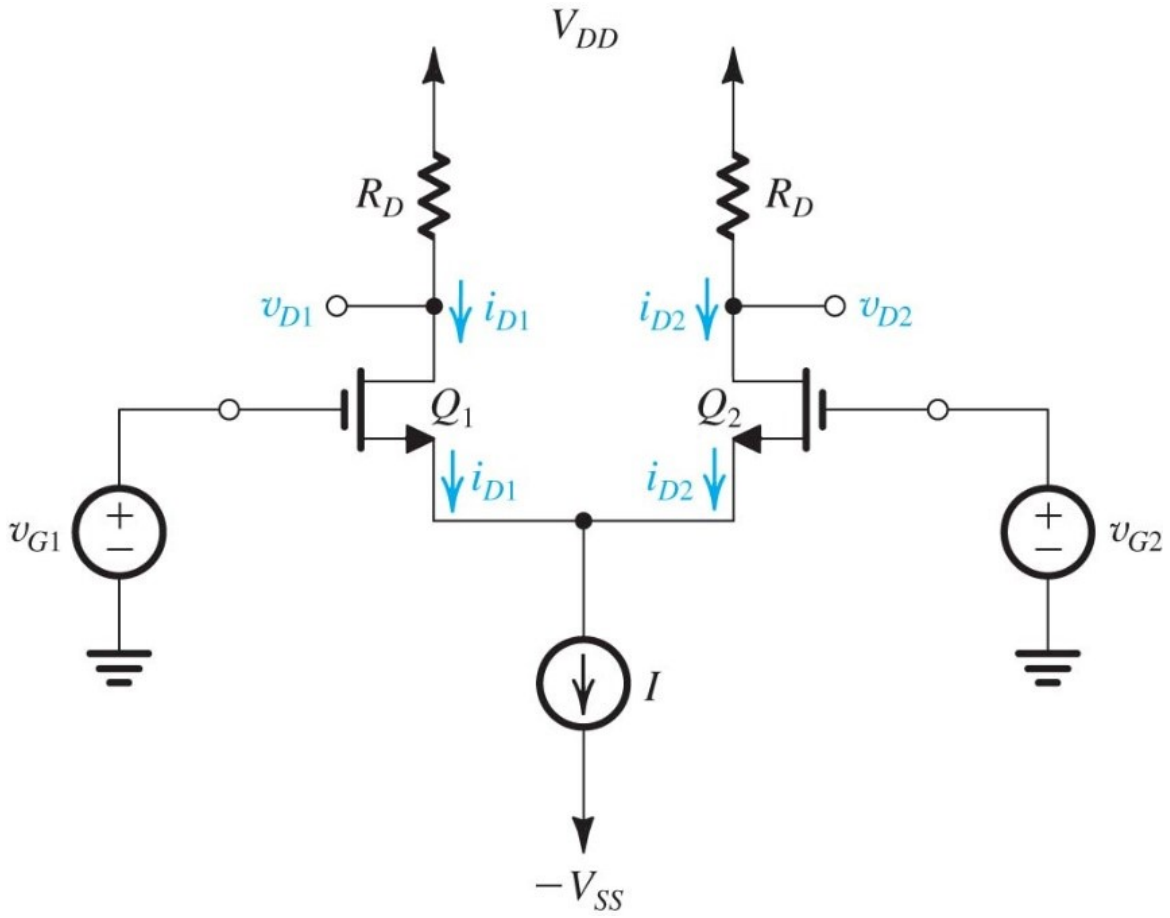
- Two signal sources
  - v_1: reference signal minus a (half) component
  - v_2: reference signal plus a (half) component
- Differential mode signal component, $v_{Id} = v_2 - v_1$
  - Typically the “interesting” part of the signal
- Common mode signal component, $v_{Icm} = \frac{1}{2}(v_1 + v_2)$
  - Typically a reference or noise level, not desired
- Common mode rejection ratio (CMRR)
  - Differential to common mode power gain ratio, $CMRR = 20\log_{10}\left(\frac{A_d}{A_{cm}}\right)$



Observe the split and polarity of the differential sources.

MOS Differential Pair

- Two balanced transistors
  - Same technology, k_n
  - Same threshold, V_{tn}
  - Same size, W/L
- Arranged symmetrically
  - Equal load, R_D
  - Share one current sink, I
  - Source terminals joined, V_S
  - Equal gate bias, V_G
  - Equal overdrive bias, $V_{OV} = V_{GS} - V_{tn}$
- Differential ports
  - Input over gates
  - Output over drains



The MOSFETs in the differential pair (and current sink) must be operated in saturation mode.

Common Mode Operation

- Drain level: constant
  - Forced current through load
  - Resistance sets voltage drop

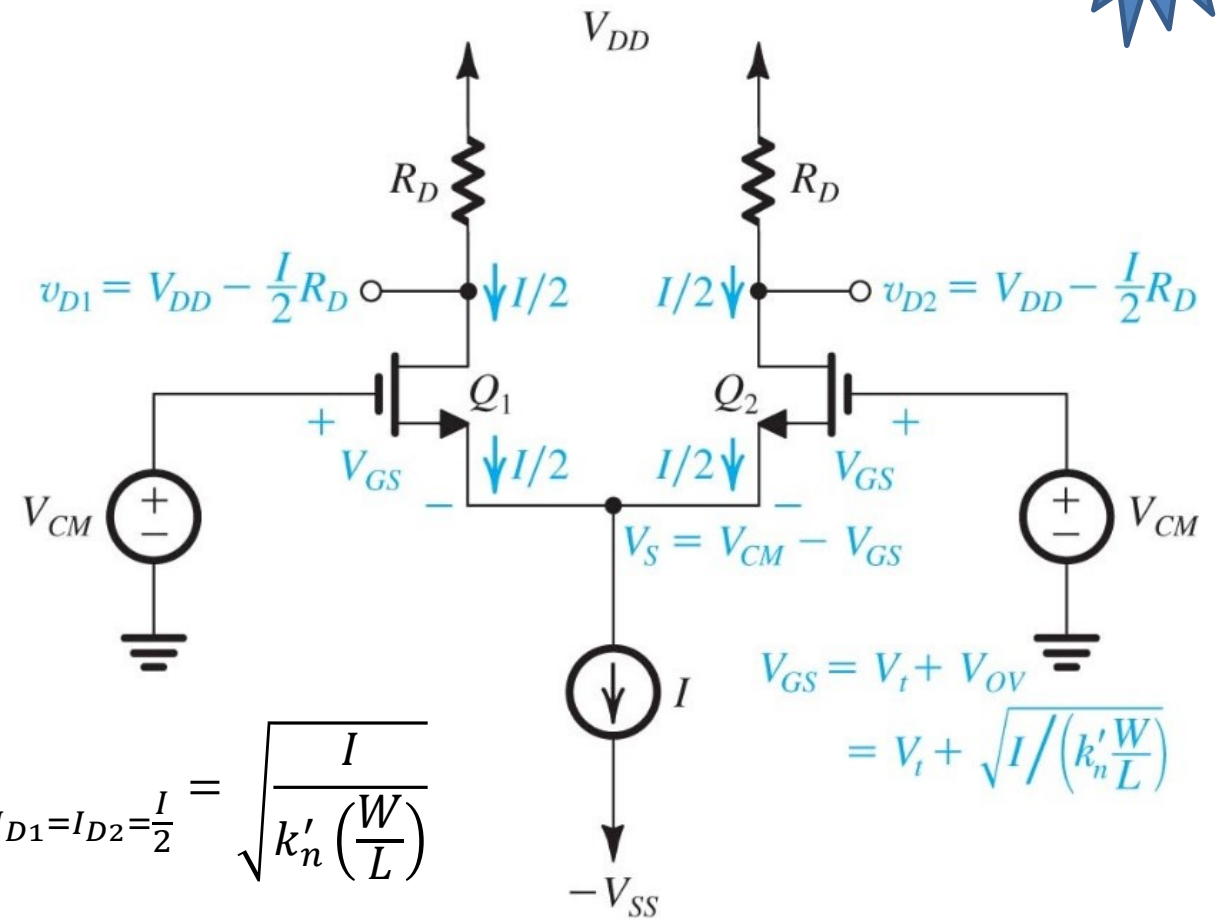
$$V_{D1}, V_{D2} = V_{DD} - \frac{R_D I}{2}$$

- Gate overdrive: constant
  - Forced current through saturated MOSFETs
  - Materials and design sets overdrive

$$I_{D1}, I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2 = \frac{I}{2}$$

- Source level: varies with CM input
  - Sink must “absorb” gate voltage offsets

$$V_S = V_{CM} - V_{GS} = V_{CM} - V_{tn} - V_{OV}$$



$$V_{OV}\Big|_{I_{D1}=I_{D2}=\frac{I}{2}} = \sqrt{\frac{I}{k_n' \left(\frac{W}{L}\right)}}$$

The MOSFETs in the differential pair share one current sink.

Differential Mode Operation

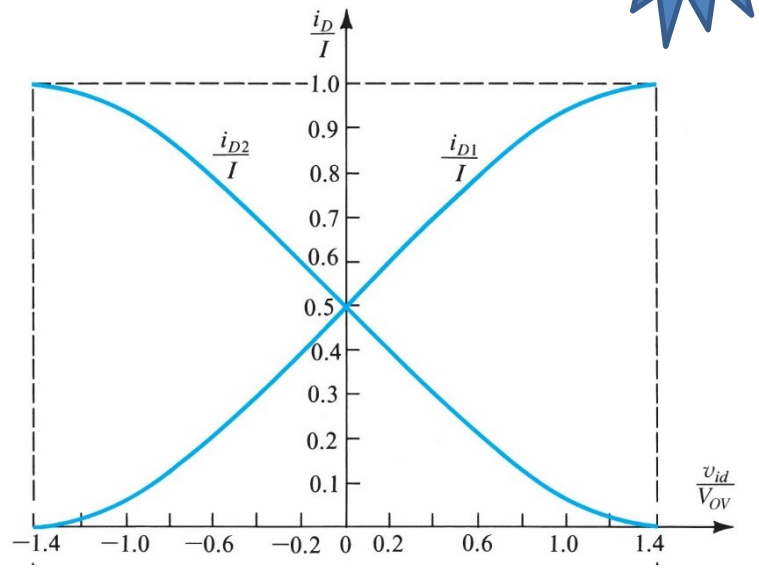
- Difference signal between Q1 and Q2
  - Input over gates, $v_{id} = v_{G1} - v_{G2}$
  - Output over drains, $v_{od} = v_{D2} - v_{D1}$

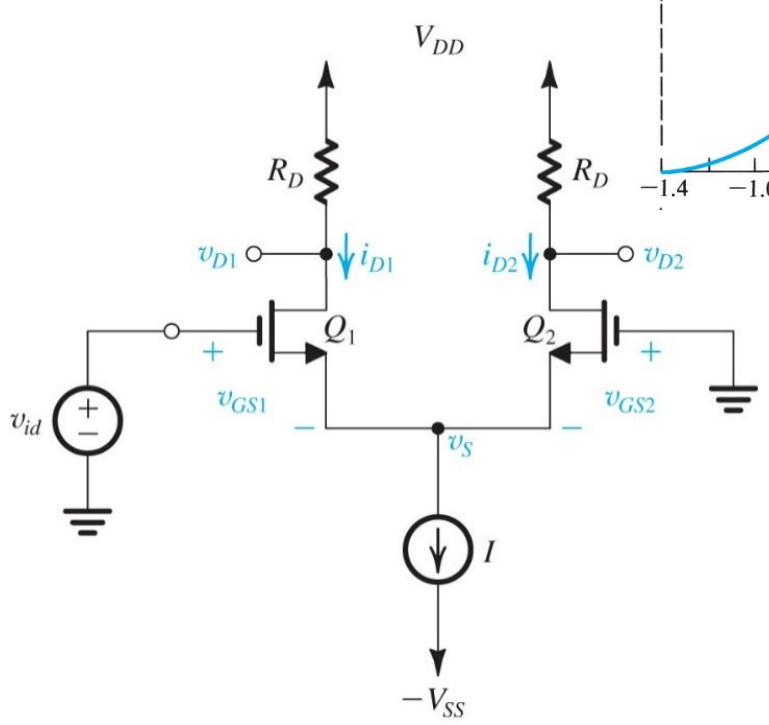
- Positive(/ negative) differential input
  - Different overdrive in Q1 and Q2
  - Redistribution of current towards Q1(/ Q2) branch of the pair

- Limit of operation
  - Steering all current to one transistor

$$-\sqrt{2}V_{OV} < v_{id} < \sqrt{2}V_{OV}$$

$$V_{OV}\Big|_{I_{D1}=I_{D2}=\frac{I}{2}} = \sqrt{\frac{I}{k_n'\left(\frac{W}{L}\right)}}$$



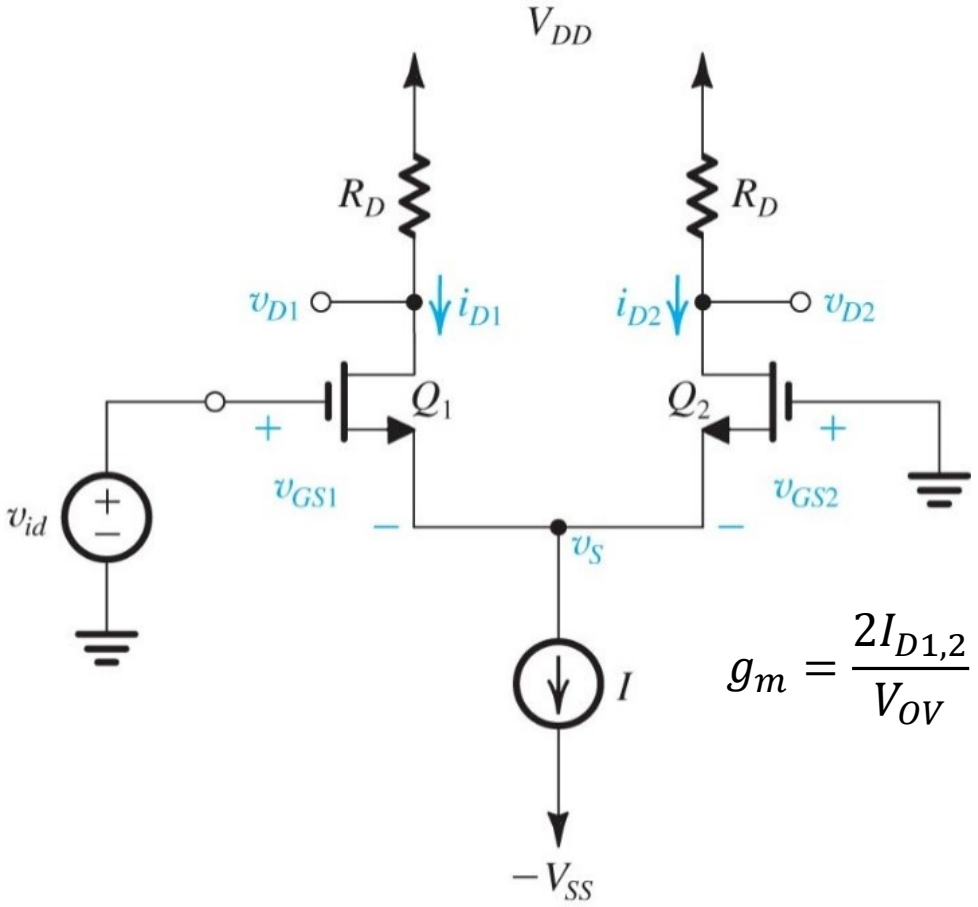


Large Signal Operation

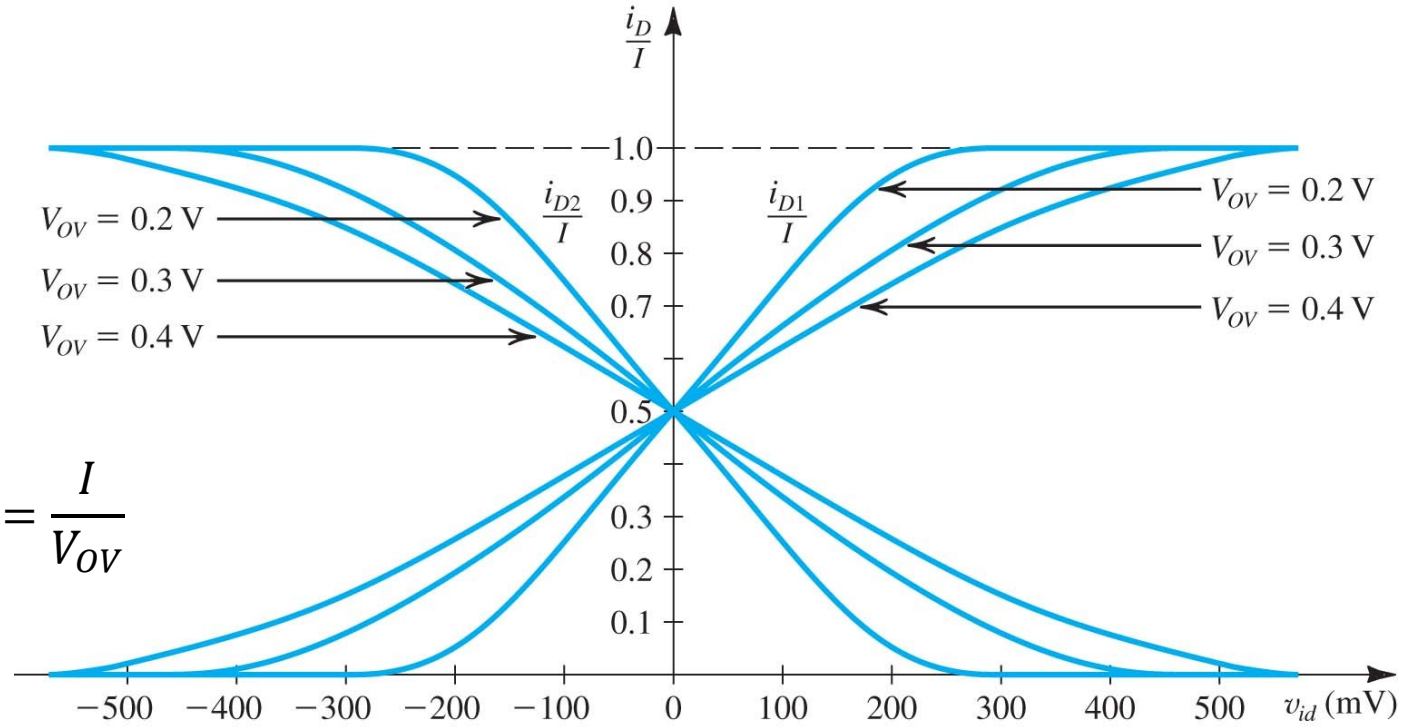
- Gate overdrive level determines differential voltage window

$$i_{D1,2} = I_{D1,2} \pm i_d = \frac{I}{2} \pm \left(\frac{I}{V_{OV}}\right)\frac{v_{id}}{2}\sqrt{1-\left(\frac{v_{id}}{2V_{OV}}\right)^2}$$

$$i_d = \{v_{id} \ll 2V_{OV}\} \approx g_m \frac{v_{id}}{2}$$



$$g_m = \frac{2I_{D1,2}}{V_{OV}} = \frac{I}{V_{OV}}$$



Small Signal Operation

- Small signal differential input voltage superimposed on bias point

$$v_{G1,G2} = V_{CM} \pm \frac{v_{id}}{2}$$

- Small signal perturbation of current

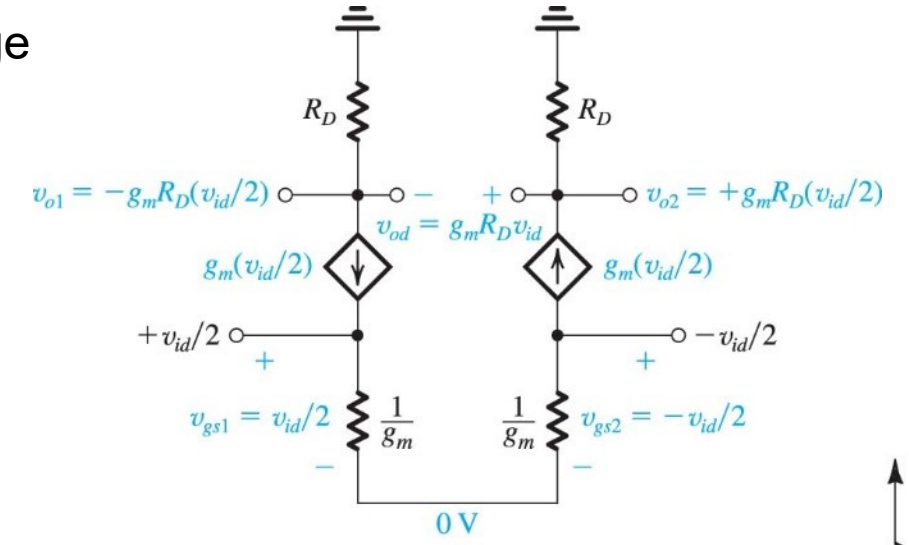
$$i_{D1,D2} = \frac{I}{2} \pm g_m \frac{v_{id}}{2}$$

- Differential voltage developed over drain terminals

$$v_{D1,D2} = V_{DD} - R_D\left(\frac{I}{2} \pm g_m \frac{v_{id}}{2}\right)$$

- Differential gain results

$$A_d = \frac{v_{od}}{v_{id}} = g_m R_D$$

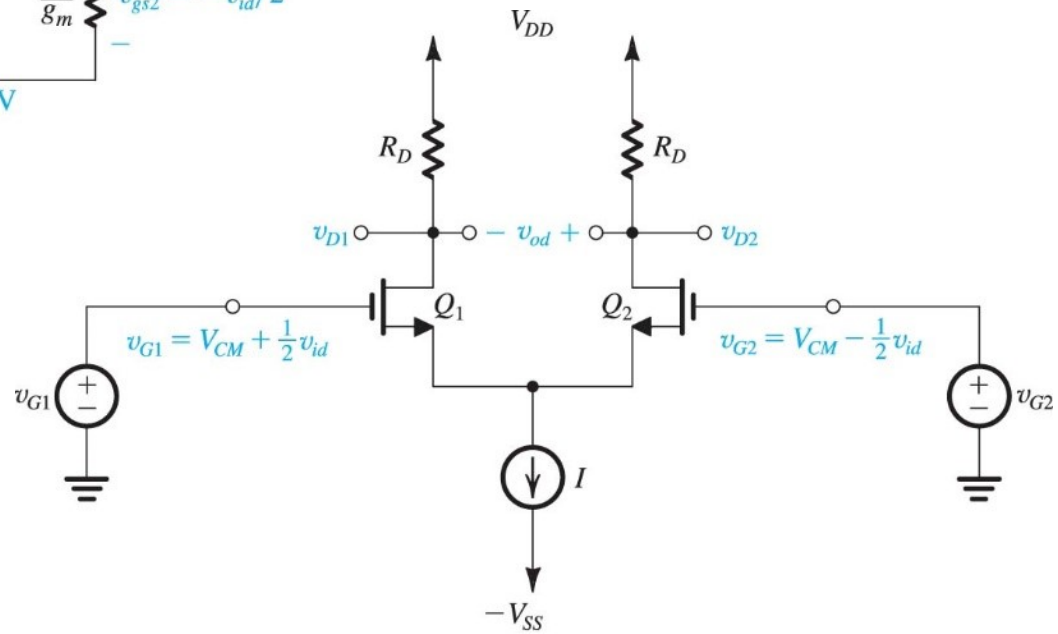


$$g_m = \frac{2I_{D1,2}}{V_{OV}} = \frac{I}{V_{OV}}$$

$$v_{id} = v_{g1} - v_{g2} \ll 2V_{OV}$$

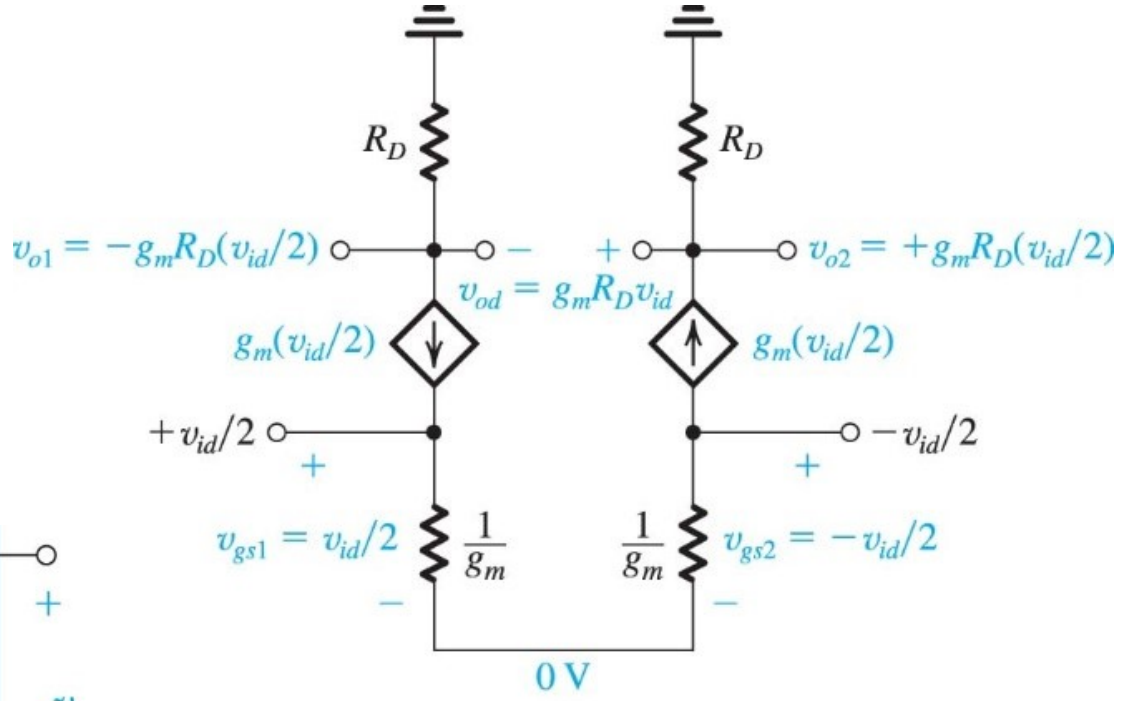
$$i_d = i_{d1} = -i_{d2} = g_m \frac{v_{id}}{2}$$

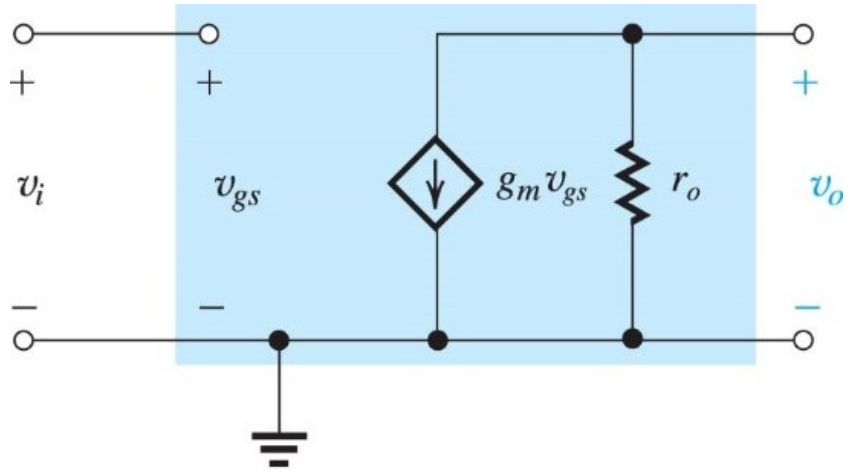
$$v_{od} = v_{d2} - v_{d1} = g_m v_{id} R_D$$



How does a finite MOSFET output resistance affect the gain expression?

$$A_d = \frac{v_{od}}{v_{id}} = g_m R_D'$$

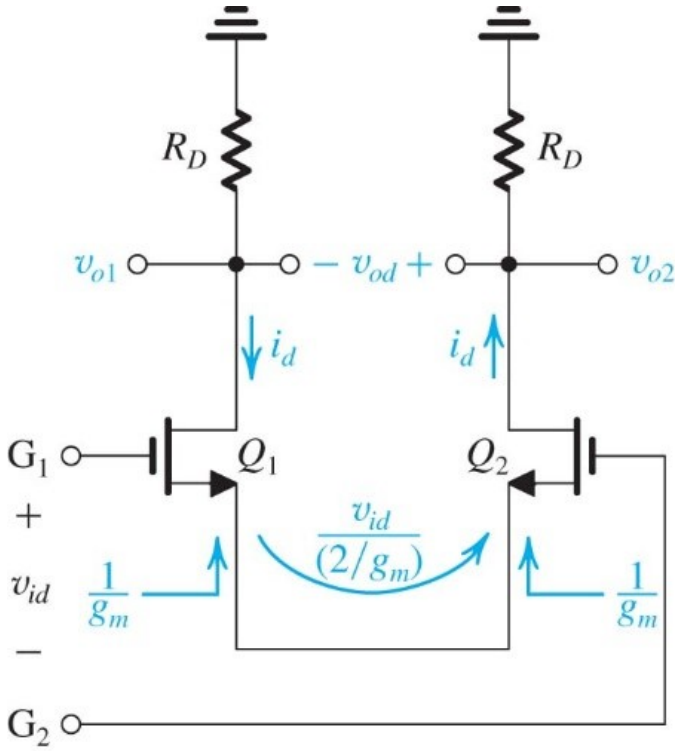


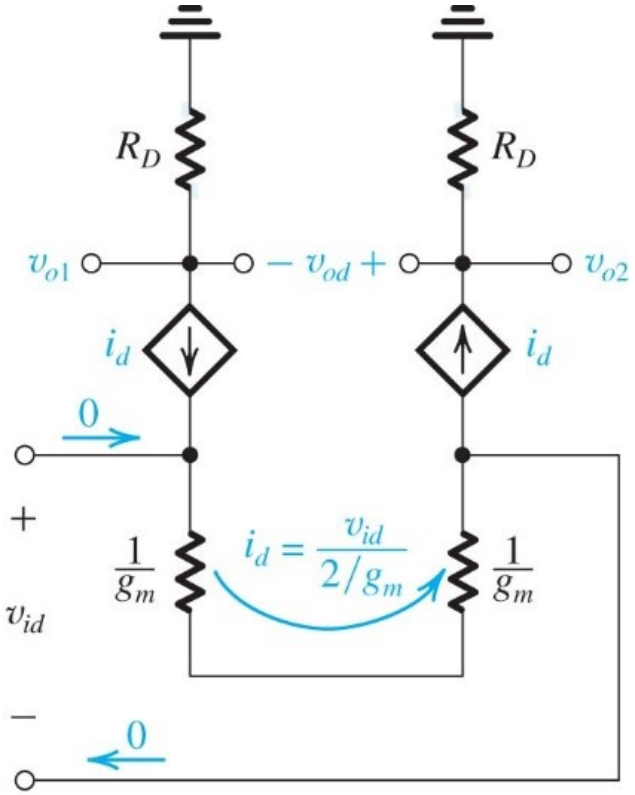


(Small Signal Analysis Directly on the Circuit Schematic)

- You may save some ink and time…
  …or make grave mistakes

$$A_d = \frac{v_{od}}{v_{id}} = g_m(r_o||R_D)$$

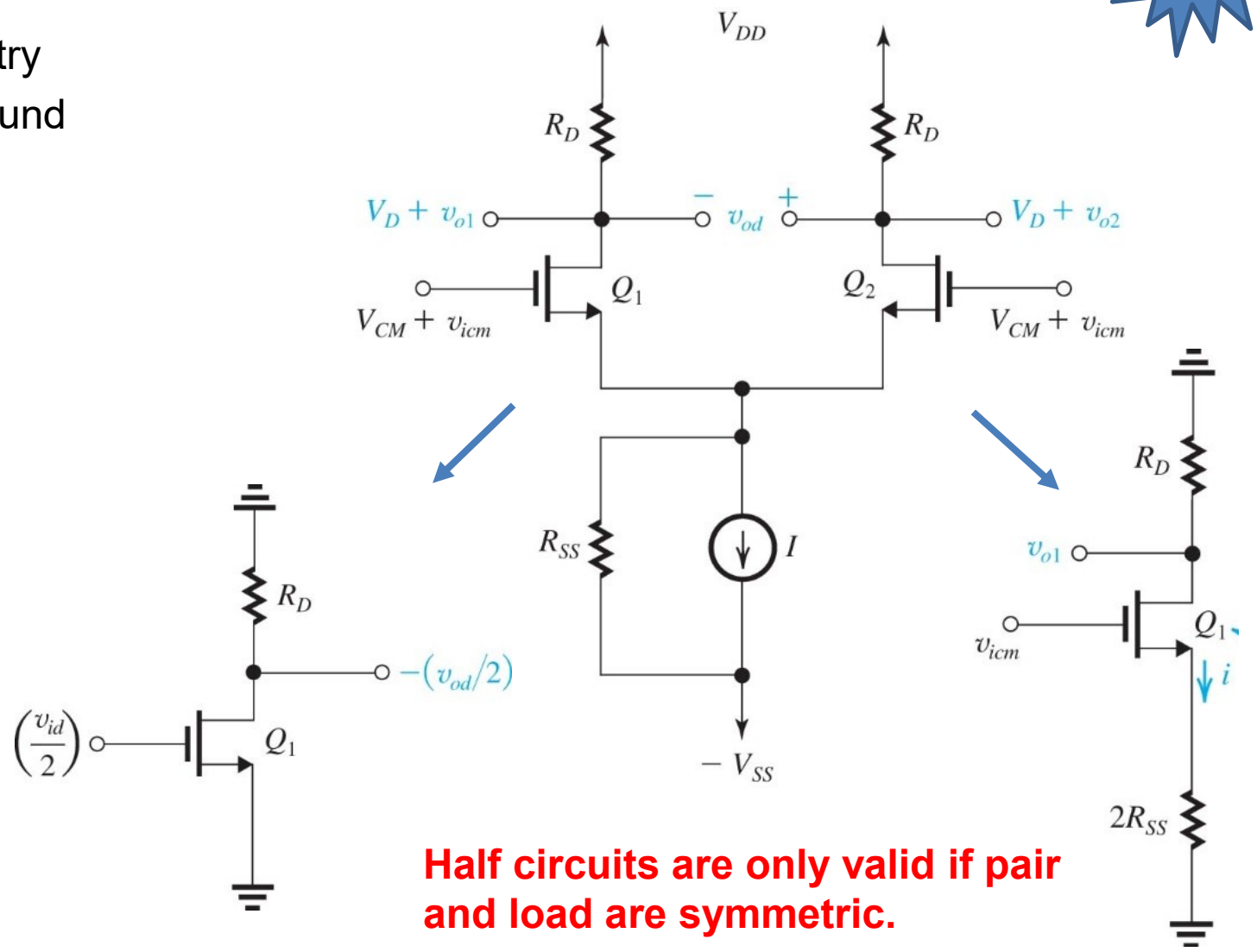




Imagine the small signal model and work on the original schematic (experienced users only).

Differential and Common Mode Half Circuits

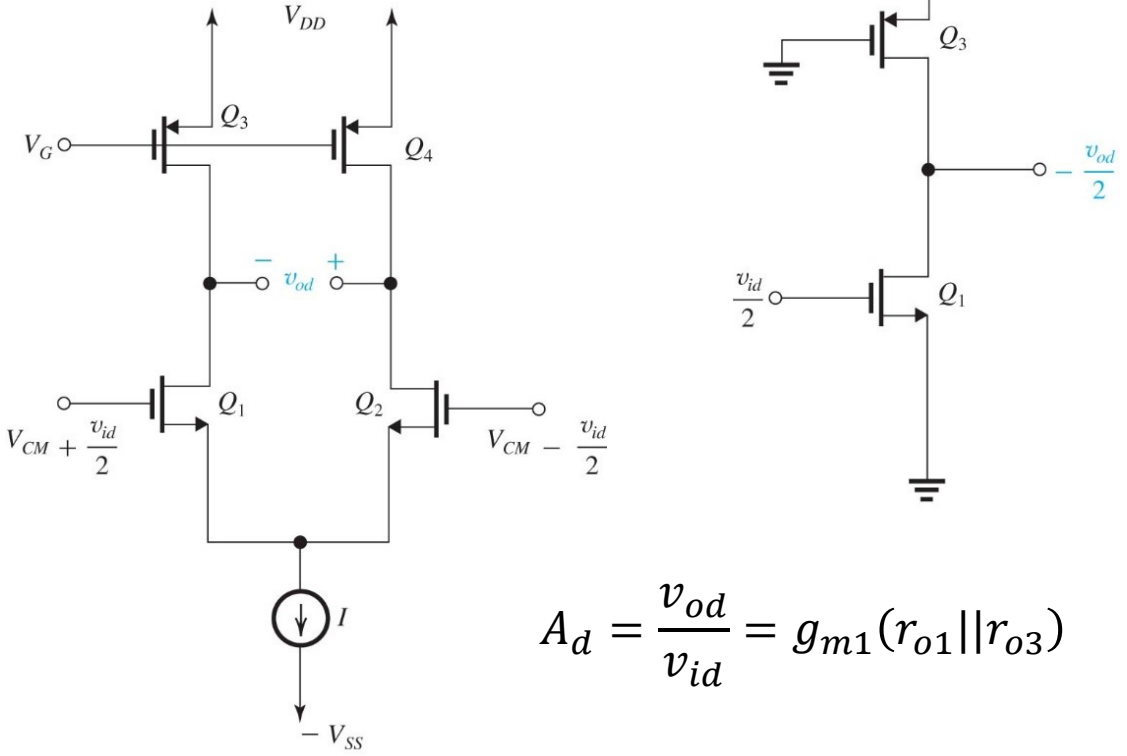
- Differential mode: Push-pull anti-symmetry
  - Source output resistance: virtual ground
    - No differential current flow
    - Constant bias condition
  - Load resistance: split
    - Half the voltage level
    - Half the impedance value
- Common mode: Push-push symmetry
  - Source output resistance: split
    - Half the current level
    - Twice the impedance value
  - Load resistance ignored
    - Same voltage on both sides



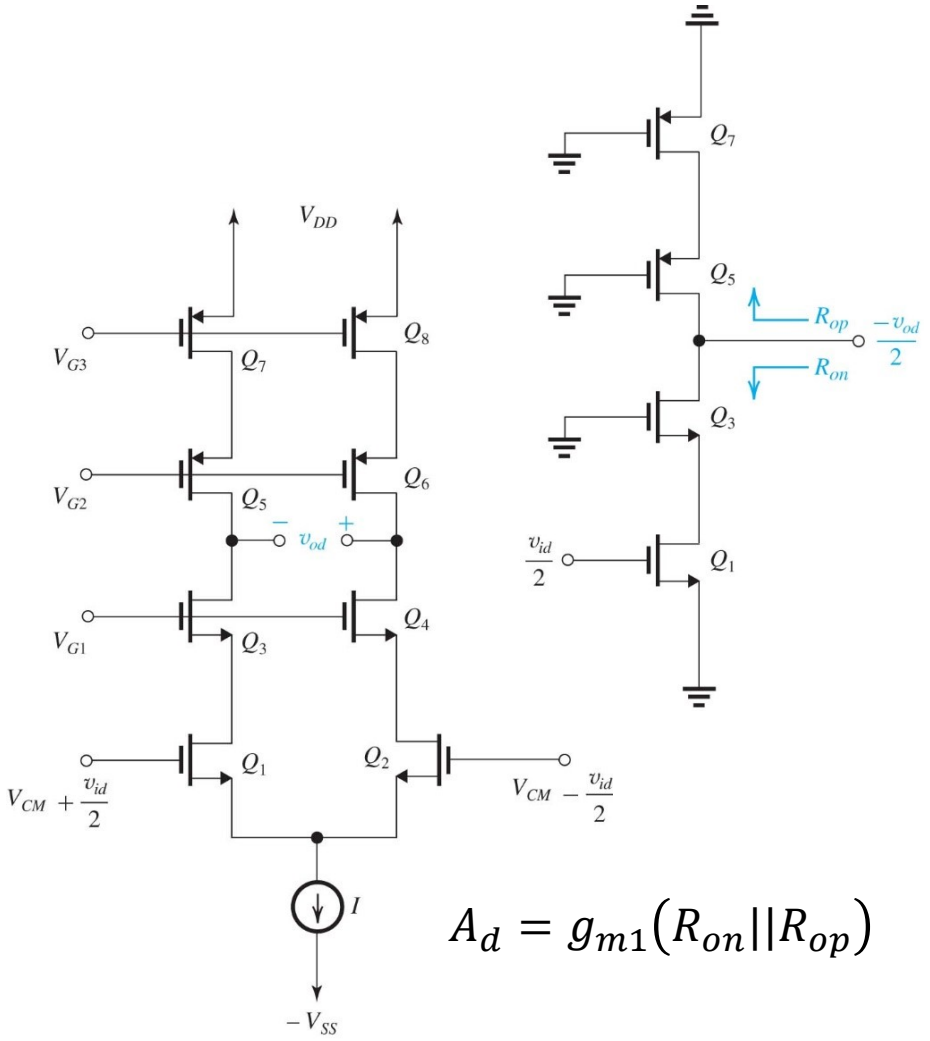
Half circuits are only valid if pair and load are symmetric.

MOS Differential Pair w/ Active Load

- Improved performance as compared to passive load, essentially a differential CS amplifier w/ active load



$$A_d = \frac{v_{od}}{v_{id}} = g_{m1}(r_{o1}||r_{o3})$$



$$A_d = g_{m1}(R_{on}||R_{op})$$

BREAK

Common Mode Gain and CMRR

- Differential gain, A_d

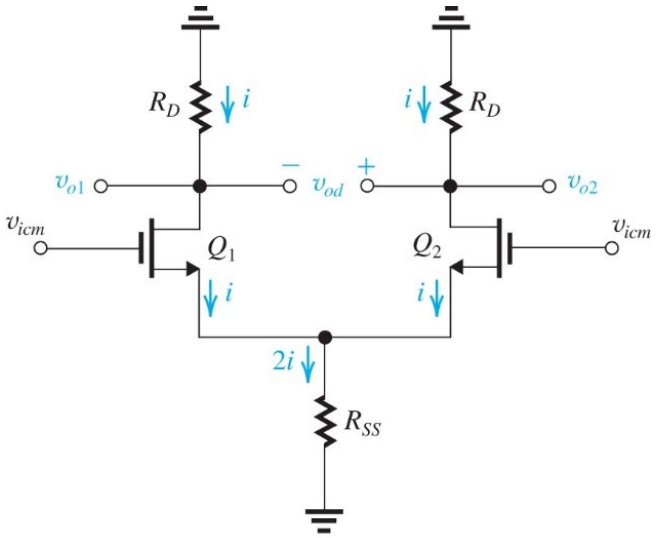
$$A_d = g_m R_D$$

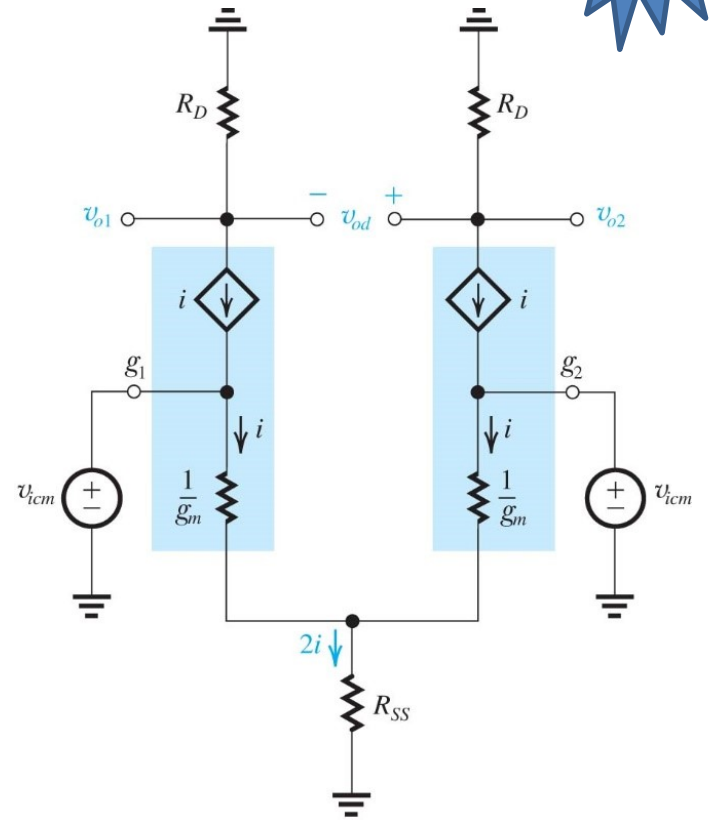
- Common mode gain, A_{cm}
  - Arises from mismatch

$$A_{cm} = \left(\frac{-R_D}{2R_{SS}}\right)\left[\left(\frac{\Delta R_D}{R_D}\right) + \left(\frac{\Delta g_m}{g_m}\right)\right]$$

- Common mode rejection ratio (CMRR)
  - Ratio of differential to common mode gain

$$CMRR = \frac{A_d}{A_{cm}} = \frac{-2g_m R_{SS}}{\left(\frac{\Delta R_D}{R_D}\right) + \left(\frac{\Delta g_m}{g_m}\right)}$$





Device matching and high current source resistance keeps CMRR high.

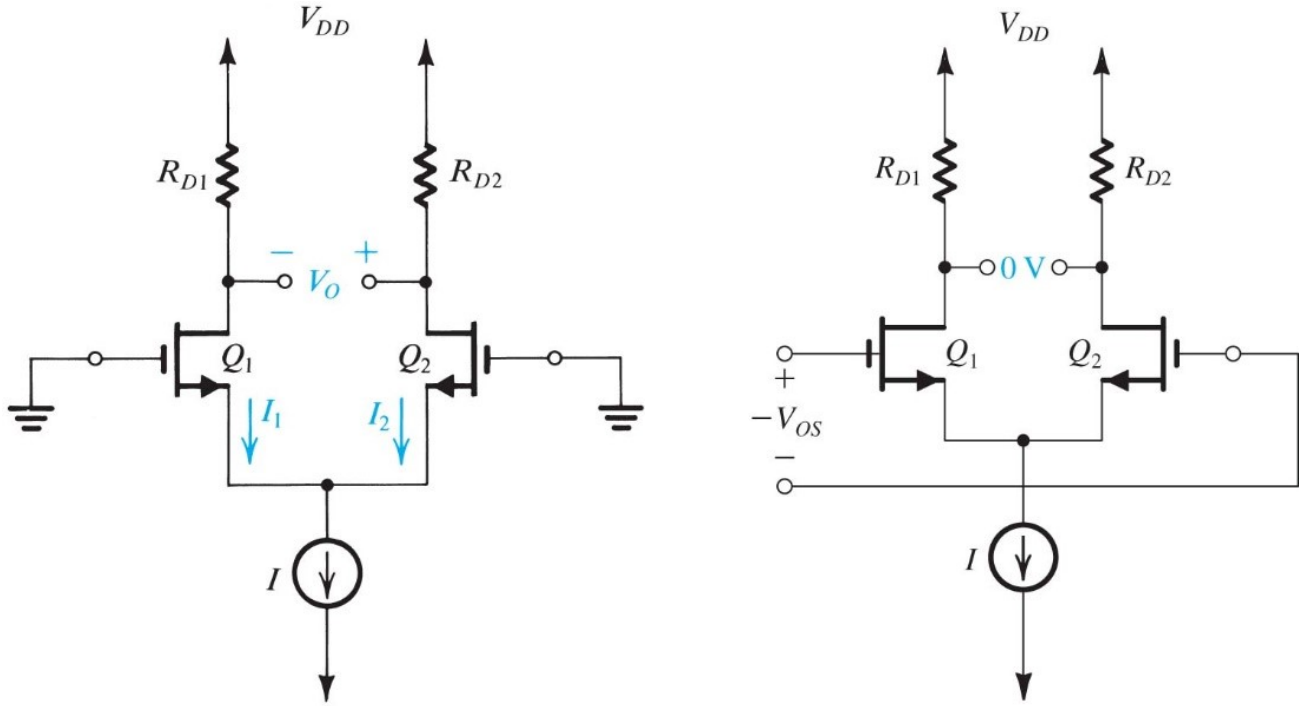
DC Offset

- Imperfectly balanced pair…
  - Unequal load, $\Delta R_D = R_{D1} - R_{D2}$
  - Unequal size, $\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2$
  - Unequal threshold, $\Delta V_{tn} = V_{tn1} - V_{tn2}$
  - …

- Output non-zero at zero input, as current not balanced

- Input referred offset voltage, V_{OS}
  - Input that cancels offset

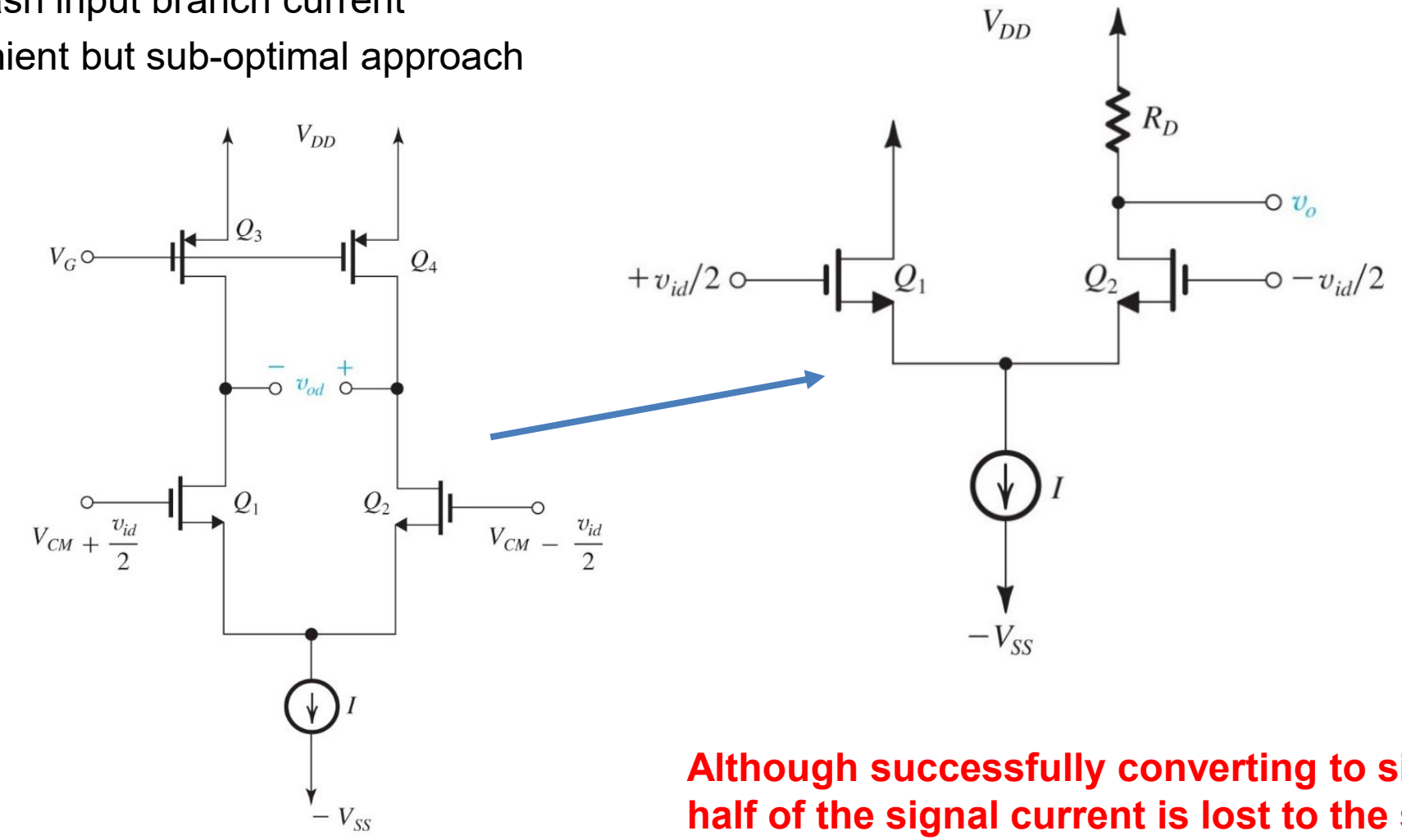
$$V_{OS} = \frac{V_O|_{V_{Id}=0}}{A_d}$$



$$V_{OS} \approx \sqrt{\sum_n (V_{OSn})^2} = \sqrt{\left(\frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{V_{OV}}{2}\frac{\Delta(W/L)}{W/L}\right)^2 + (\Delta V_{tn})^2}$$

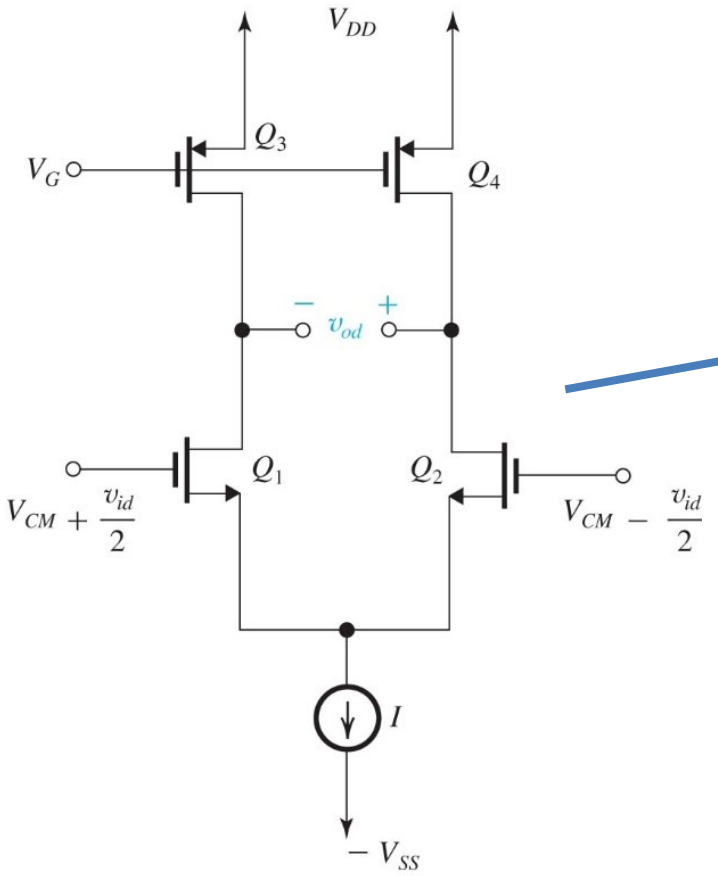
Differential to Single Ended Conversion?

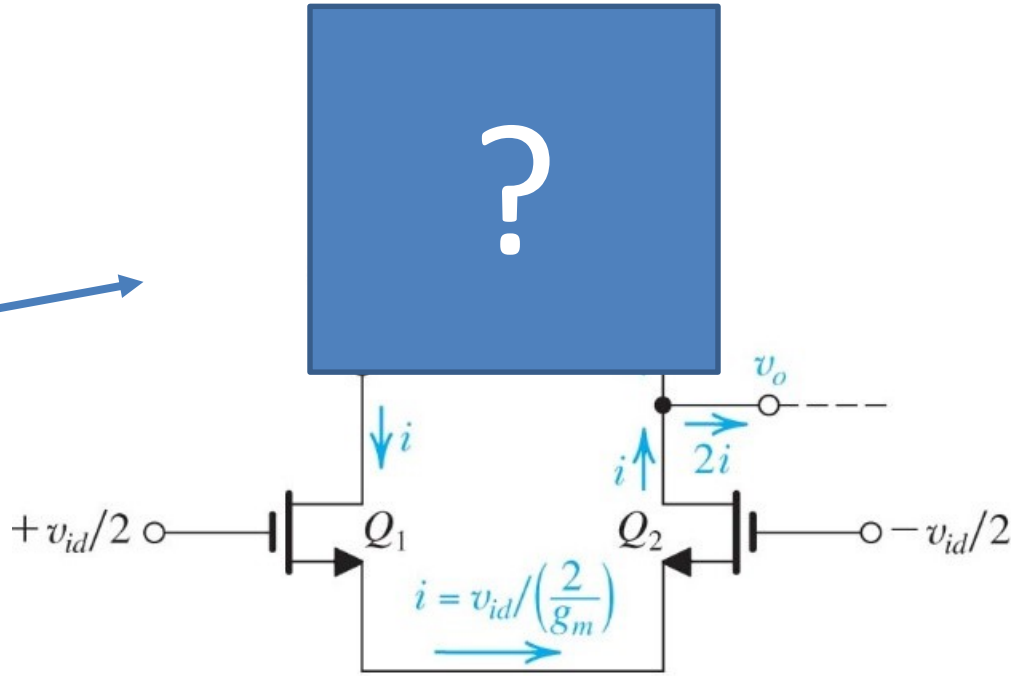
- Option 1: Trash input branch current
  - A convenient but sub-optimal approach



Although successfully converting to single ended, half of the signal current is lost to the supply.

How to reflect differential pair input branch current to output branch?





MOS Differential Amplifier w/ Current Mirror Load

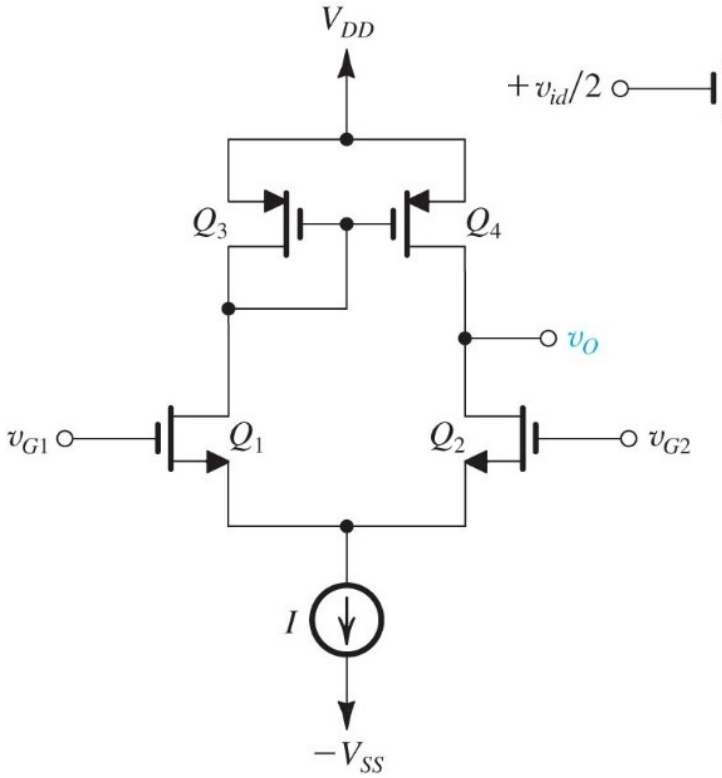
- Option 2: Mirror current to output
  - Superimposes both branch currents

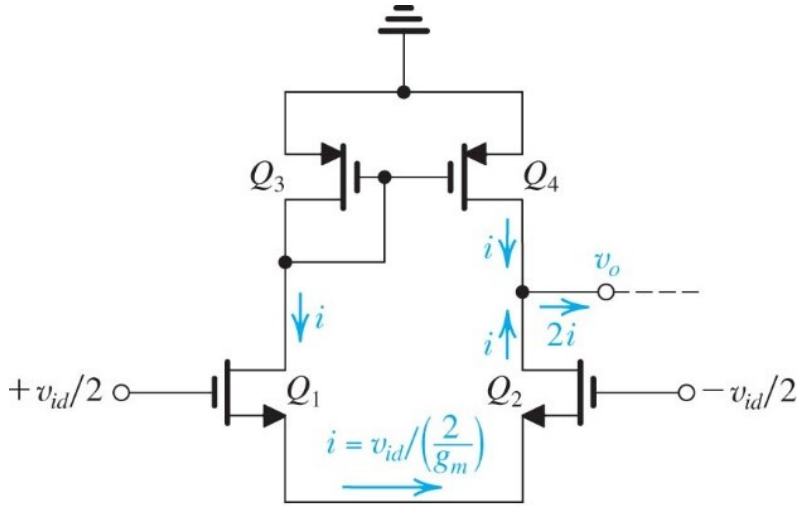
- KCL “magic” at output node
  - Differential mode currents cleverly forced into load

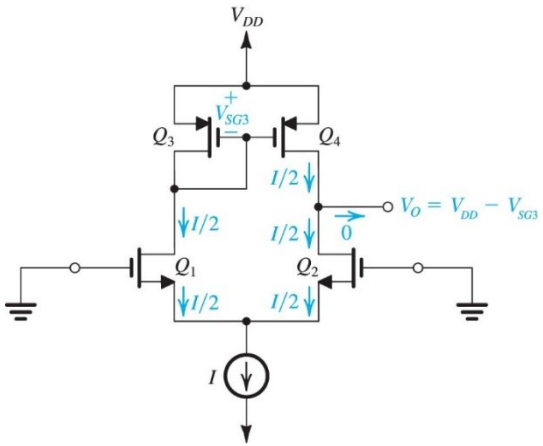
$$i_d = \frac{I}{2} + i_d - \left(\frac{I}{2} - i_d\right) = 2i_d$$

  - Common mode and dc currents must ignore load

$$i_{CM} = \frac{I}{2} + i_{cm} - \left(\frac{I}{2} + i_{cm}\right) = 0$$





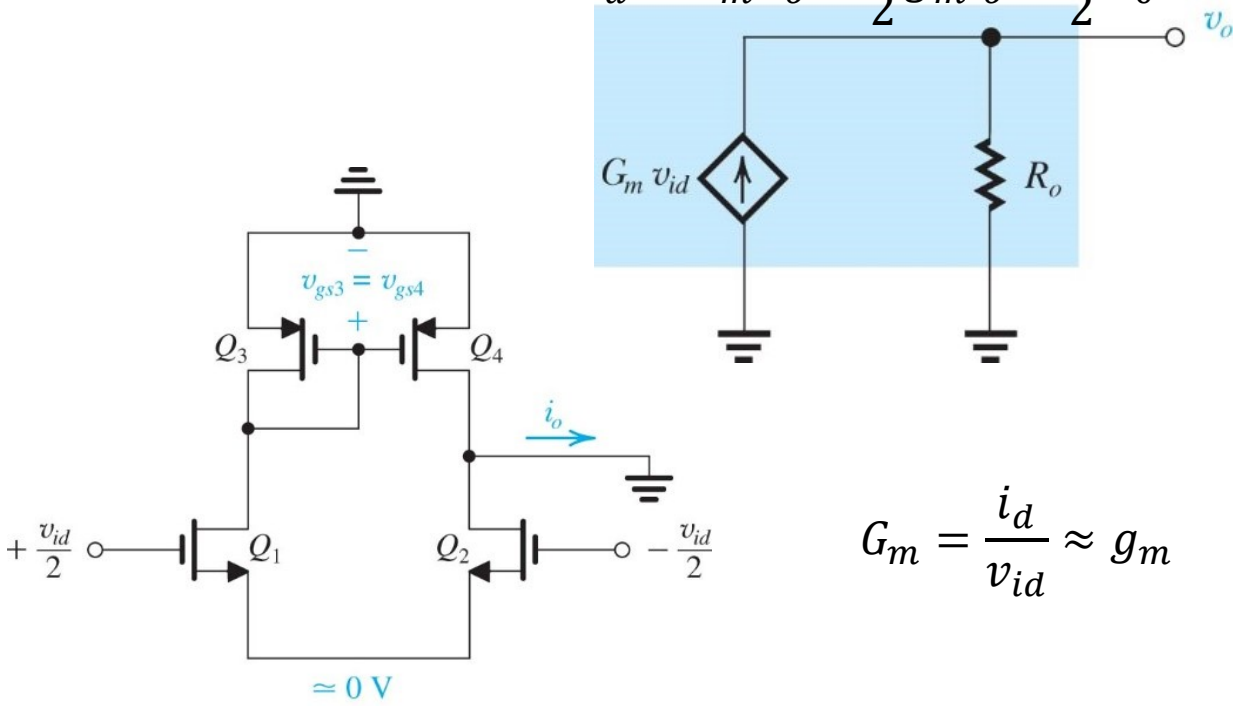


Current mirror does not load the differential pair symmetrically.

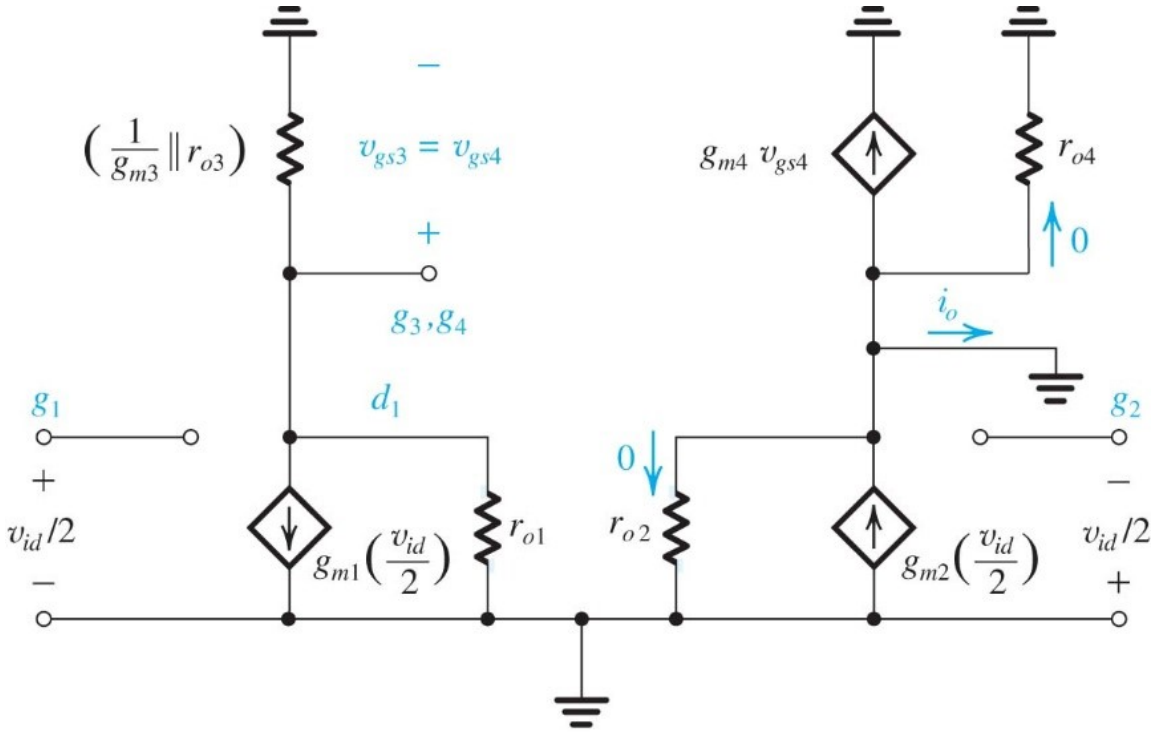
Differential Amplifier: Short Circuit Transconductance

- Identify equivalent transconductance amplifier
  - Infinite input resistance
  - Transconductance
  - Finite output resistance

$$A_d = G_m R_o \approx \frac{1}{2} g_m r_o = \frac{1}{2} A_0$$



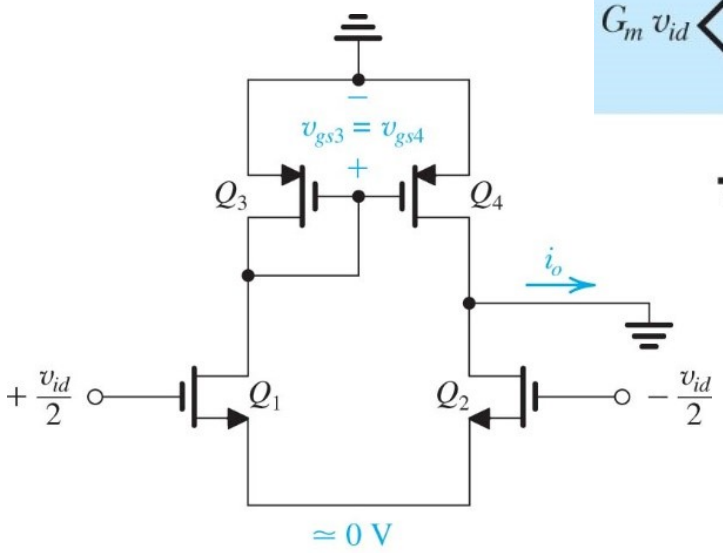
$$G_m = \frac{i_d}{v_{id}} \approx g_m$$

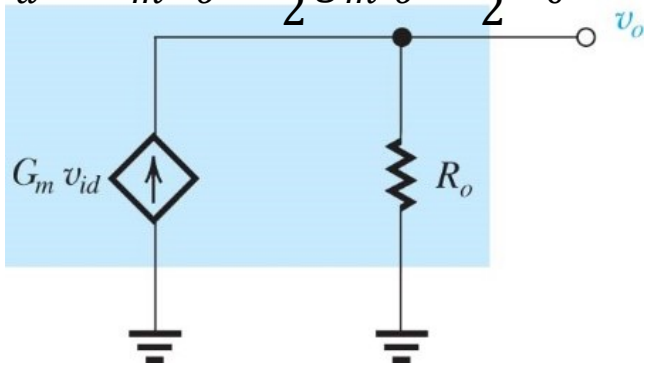


Differential Amplifier: Output Resistance

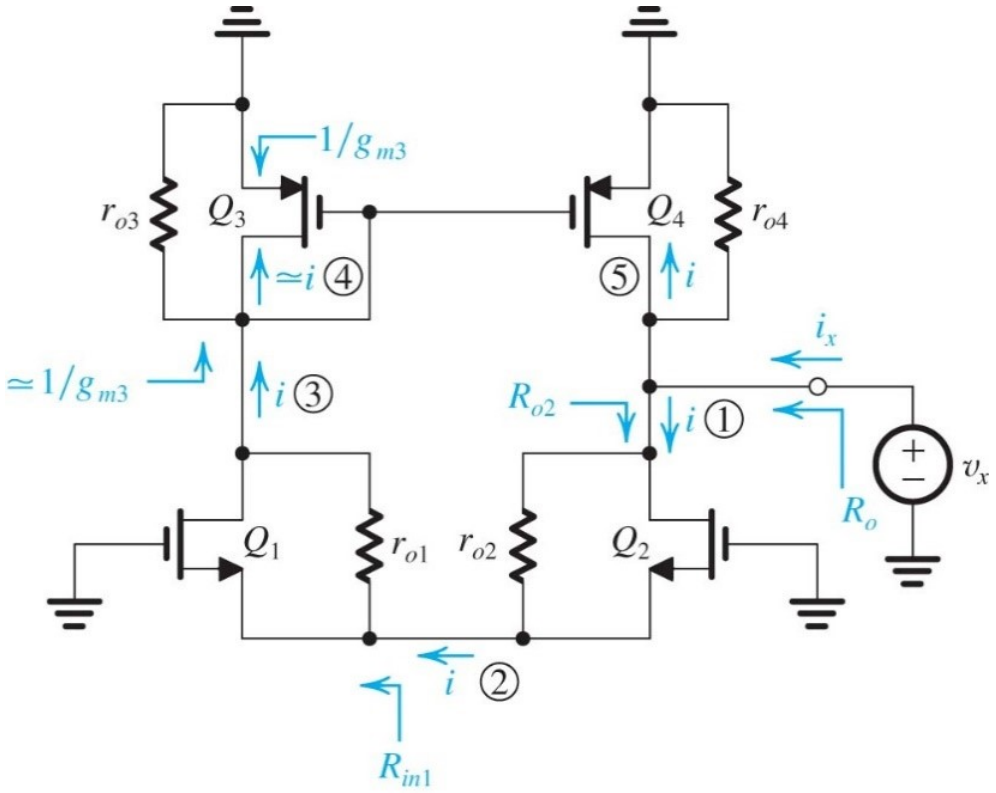
- Identify equivalent transconductance amplifier
  - Infinite input resistance
  - Transconductance
  - Finite output resistance

$$A_d = G_m R_o \approx \frac{1}{2} g_m r_o = \frac{1}{2} A_0$$





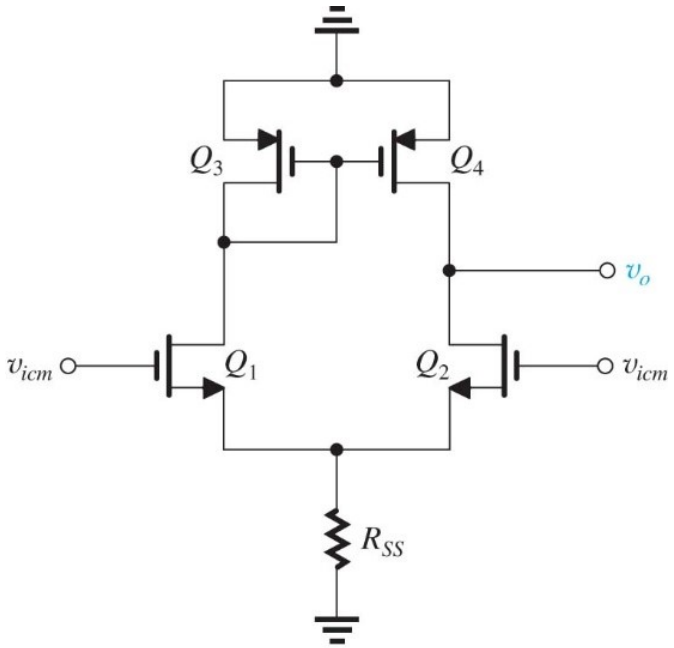
$$R_o = \frac{v_x}{i_x} \approx (r_{o2} || r_{o4})$$

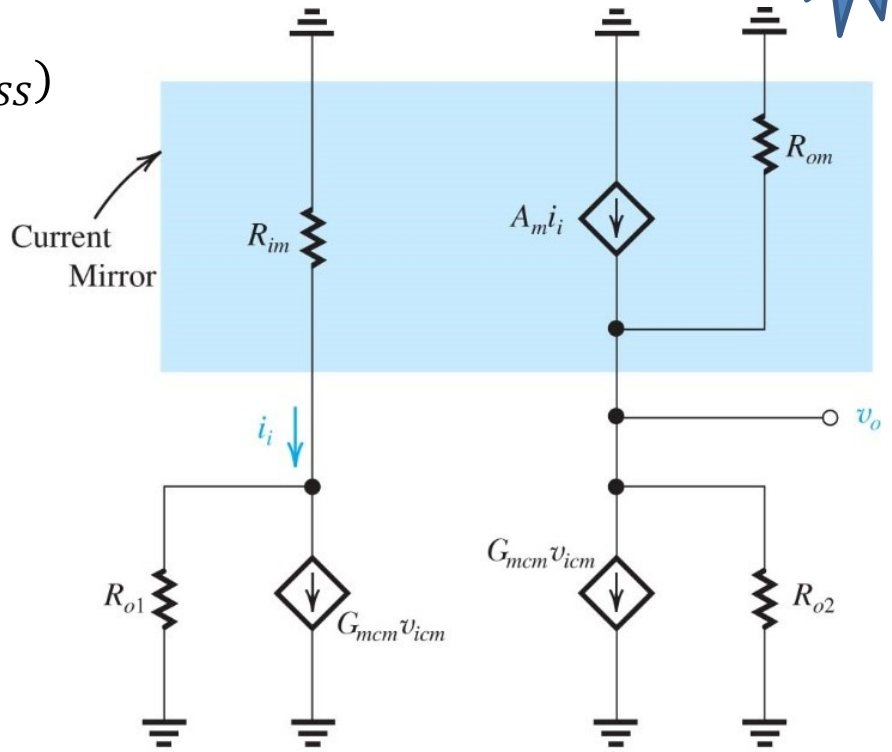


Differential Amplifier: Common Mode Gain and CMRR

- Asymmetrical loading
  - Diode connected transistor
  - Common source transistor
- Mirror approximately buffers current
- Common gate source/ load transformations useful

$$CMRR = \frac{A_d}{A_{cm}} \approx -(g_m r_o)(g_m R_{SS})$$





$$A_d = \frac{v_{od}}{v_{id}} = G_m R_o \approx g_m(r_{o2} || r_{o4})$$

$$A_{cm} = \frac{v_o}{v_{icm}} = -(1 - A_m) G_{mcm}(R_{om} || R_{o2}) \approx \frac{-1}{2 g_m R_{SS}}$$

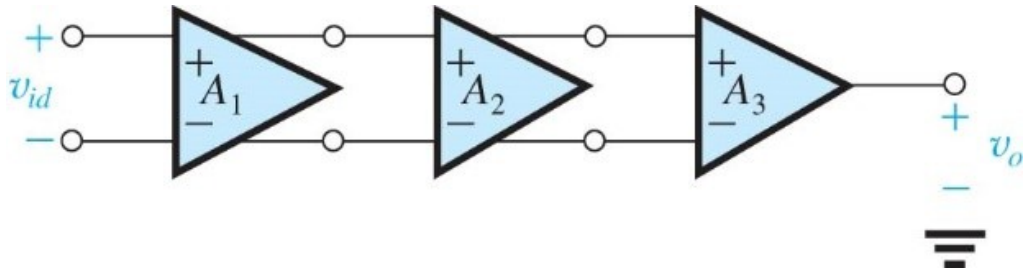
Multistage Amplifiers

- Multistage seen as functional blocks
  - Noise/ CM rejection
  - Signal gain (small signal)
  - Power (linearity)

- Differential input and interstage
  - Differential gain
  - CM (noise or interference) rejection

- Single ended output stages
  - Gain and power level
  - Resistance transformation

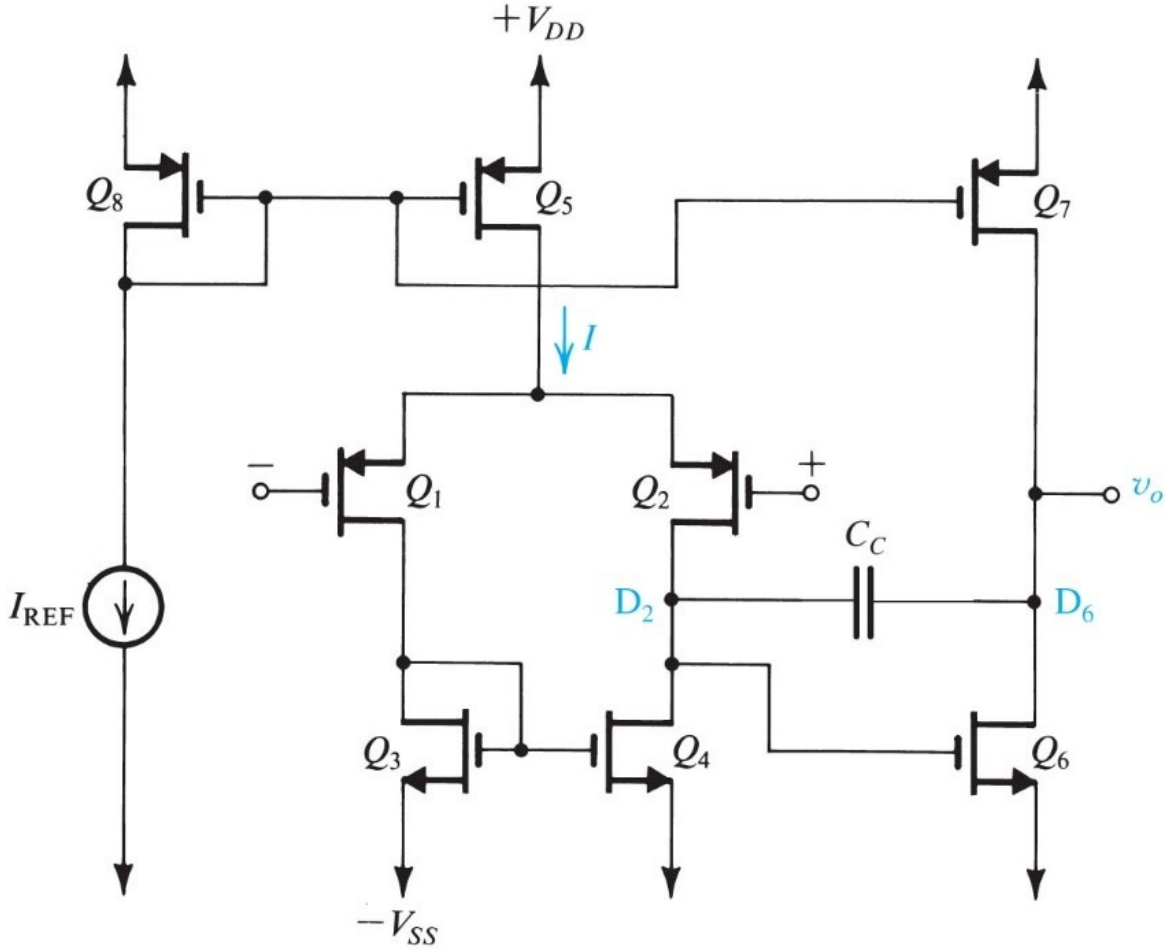
- Single ended output typically
  - Load to ground



Multistage amplifier is co-desiged system, its stages dedicated to specific tasks.

Two-Stage CMOS Op Amp

- Bias current steering circuit
- Input stage: differential PMOS pair
  - Gain and single ended conversion
  - NMOS current mirror load
- Output stage: common source NMOS
  - Gain w/ active load
- Stability
  - Frequency compensation feedback capacitor
- Compact, moderate gain, but rather high output impedance



Four Stage BJT Op Amp

- Bias current steering circuit
- Input stage: differential NPN pair
  - Differential in/ out gain
- Second stage: differential NPN pair
  - Gain and single-ended conversion
- Third stage: degenerated common emitter PNP
  - Gain and level shift
- Output stage: emitter follower
  - Low output impedance
- Higher gain, lower output impedance