F8 – Building Blocks of Integrated Circuit Amplifiers

Outline
- Integrated circuits
- Current mirrors, steering circuits, sources, sinks
- Common source (CS) amplifier w/ output resistance
- CS amplifier w/ active load
- Common gate (GS) amplifier w/ output resistance
- CS-CG Compound Device: Cascode amplifier
- Common drain (CD) amplifier w/ output resistance
- CD-CS Compound Device
- CD-CG Compound Device

Reading Guide

Sedra/Smith 7ed int
- Chapter 7.1-7.5
- Chapter 7.7 CD-CS, CD-CG

Problems

Sedra/Smith 7ed int
- P7.7, 7.20(a), 7.26, 7.51, 7.64
Integrated Circuits (ICs) and Components

- Area = $$$
  - Performance vs. integration density tradeoff
  - Avoid large components if possible

- Complementary MOS (CMOS) technology
  - Best cost per transistor if mass produced in very-large-scale ICs (VLSI) technology
  - Low-power digital logic ($V_{DD} < 1\,\text{V}$ in scaled CMOS) + decent analogue circuits = very versatile!

- BJT technology
  - Very useful, but mainly for special applications

- Historically, IC scaling improved performance

IC design allows for good relative device uniformity, as compared to discrete devices.
MOSFET Current Mirror

- Resistance to supply provides reference current

- Reference (input) branch
  - Diode connected (G bound to D) CS device Q1, $V_{DS1} = V_{GS1} > V_{OV1}$, enforces saturation
    \[
    I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_{tn})^2 = I_{REF} - 0 = \frac{V_{DD} - V_{GS}}{R}
    \]

- Source (output) branch
  - CS device Q2 shares S and G with Q1, in saturation if $V_{DS2} > V_{OV1}$
    \[
    I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_{tn})^2 \approx \frac{(W/L)_2}{(W/L)_1} I_{REF}
    \]

Current mirrors only make sense in IC technology, where variability is low.
MOSFET Current Mirror w/ Output Resistance

- Output resistance yields dependence on output voltage

\[ R_O = \frac{\partial V_O}{\partial I_O} = r_o = \frac{1}{\lambda_2 I_{D2}} \]

- Exact transfer requires equivalent voltages on all terminals of Q1 and Q2

\[ I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF} (1 + \lambda_2 (V_O - V_{GS})) \]

\[ R_O = \frac{\partial V_O}{\partial I_O} = r_O = \frac{1}{\lambda_2 I_{D2}} \]
Current Steering Circuit

- One reference path can control several current sources/ sinks
(Current Source vs Current Sink)

- Current source
  - Extracts current from supply

- Current sink
  - Injects current into ground

\[ V_{DD} \]
\[ V_{CS\text{min}} \]
\[ V_{O} \leq V_{DD} - V_{CS\text{min}} \]
\[ V_{O} \geq -V_{SS} + V_{CS\text{min}} \]

This is a matter of definition.
BJT Current Mirror

- BJT current mirror similar to MOSFET, but scaling w.r.t. BE junction area

- Base current loss may be compensated by additional BJT

$$I_O = \frac{A_2/A_1}{1 + \frac{1 + A_2/A_1}{\beta} I_{REF}} \left(1 + \frac{V_O - V_{BE}}{V_A}\right)$$

Advanced current mirror circuits can suppress the BJT base current error.
MOSFET Current Mirror: Small Signal Operation

- Excellent linearity
  - Small signal current gain and bias current ratio virtually equal

\[ R_i = \frac{v_i}{i_i} = r_{o1} \parallel \frac{1}{g_{m1}} \approx \frac{1}{g_{m1}} \]

\[ R_o = \left. \frac{v_o}{i_o} \right|_{i_{\text{sig}}=0} = r_{o2} \]

\[ A_{is} = \left. \frac{i_o}{i_i} \right|_{R_L=0} = g_{m2} \left( r_{o1} \parallel \frac{1}{g_{m1}} \right) \approx \frac{g_{m2}}{g_{m1}} \frac{(W/L)_2}{(W/L)_1} = \frac{i_o}{i_{\text{REF}}} \]

\[ g_m = k_n' \left( \frac{W}{L} \right) V_{OV} \]
The Basic Gain Cell: CS Amplifier w/ Active Load

- CS amplifier with current source load
  - Load is an active component
  - Small signal analysis, $I = 0$, i.e. open circuit
  - Intrinsic SC stage gain, $A_0 = g_m r_o$

- $R_i = \frac{v_i}{i_i} = \infty$
- $R_o = \left. \frac{v_o}{i_o} \right|_{v_{sig}=0} = r_o$
- $A_{vo} = A_v \big|_{R_L=\infty} = \left. \frac{v_o}{v_i} \right|_{R_L=\infty} = -g_m r_o = -A_0$
- $A_v = -g_m r_o = A_{vo} = A_0$

\[
A_0 \gg 1 \iff \frac{1}{g_m} \ll r_o
\]
Intrinsic Gain

- **MOSFET**
  - Intrinsic can be designed to vary among different devices
    - Tradeoff: gain vs. BW
    
    \[
    A_0 = g_m r_o \approx \frac{2}{\lambda V_{OV}} = \frac{2L}{\lambda' V_{OV}} = \frac{1}{\lambda'} \sqrt{2k_n'WL/I_D}
    \]

- **BJT**
  - Intrinsic gain is a technology constant
    
    \[
    A_0 = g_m r_o \approx \frac{V_A}{V_T}
    \]

\[
\begin{align*}
g_m &= k_n' \left( \frac{W}{L} \right) V_{OV} = \sqrt{2k_n' \left( \frac{W}{L} \right)} I_D = \frac{2I_D}{V_{OV}} \\
r_o &= \frac{1}{\lambda I_D'} = \frac{L}{\lambda' I_D'} = \frac{V_A' L}{I_D'} = \frac{V_A}{I_D'}
\end{align*}
\]

Intrinsic gain is magnitude of open circuit voltage gain of the basic CS(/ CE) amplifier.
Active Load w/ Output Resistance

- CS amplifier with active load w/ output conductance
  - Small signal analysis, $I = 0$, i.e. open circuit
  - CG presents load similar to CS output conductance

- $R_i = \frac{v_i}{i_i} = \infty$
- $R_o = \left. \frac{v_o}{i_o} \right|_{v_{\text{sig}}=0} = r_o1 || r_o2 \approx \frac{r_o2}{2}$
- $A_{v0} = -\frac{g_m r_o}{2} = -\frac{A_0}{2}$

Output resistance of active load reduces the gain.
Increasing the Gain of the Basic Cell

- Need to insert a circuit, between output and load, that...
  - Transfers current unchanged
  - Increases output resistance

![Diagram](image)
What transfers current unchanged and increases output conductance?
Common Gate (CG) Amplifier as a Current Buffer (recap)

- Low input resistance, moderate output resistance

- \[ R_i = \frac{v_i}{i_i} = \frac{1}{g_m} \]

- \[ R_o = \frac{v_o}{i_o}_{v_{\text{sig}}=0} = R_D \]

- \[ A_{v_o} = A_v |_{R_L=\infty} = g_m R_D \]

- \[ A_v = A_{v_o} \frac{R_L}{R_L + R_o} = g_m (R_D || R_L) \]

- \[ G_v = \frac{R_i}{R_i + R_{\text{sig}}} A_v = \frac{R_D || R_L}{R_{\text{sig}} + 1/g_m} < A_v \]

Transistor output resistance would somewhat complicate analysis.
CG Amplifier w/ Output Resistance

- Low input resistance, moderate output resistance
  - Buffers current even w/ output resistance (of device), but output/ input resistance depend on source/ load

\[
R_i = \frac{v_i}{i_i} = \frac{r_o + R_L}{1 + g_m r_o} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o}
\]

\[
R_o = \left. \frac{v_o}{i_o} \right|_{v_{sig}=0} = r_o + R_s + g_m r_o R_s \approx r_o + g_m r_o R_s
\]

\[
A_{v_0} = A_v \bigg|_{R_L=\infty} = g_m R_o \approx g_m^2 r_o R_s
\]

\[
A_v = g_m (R_o || R_L)
\]

\[
g_{mb} = \chi g_m
\]

\[
\frac{1}{g_m} \ll r_o
\]
CG Amplifier w/ Output Resistance: Output Resistance

\[ R_{\text{out}} = \frac{v_x}{i_x} \]
CG Amplifier w/ Output Resistance: Input Resistance
CG Output/ Input Resistance: Source/ Load Transformations

- CG w/ vs w/o output resistance

- Input
  - Value w/o plus reduced load
    \[ R_i = \frac{r_o + R_L}{1 + g_m r_o} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} = \frac{1}{g_m} + \frac{R_L}{A_0} \]

- Output
  - Value w/o plus increased source
    \[ R_o = r_o + R_s + g_m r_o R_s \approx r_o + g_m r_o R_s = r_o + A_0 R_s \]

- Output/ input resistance w/o \( r_o \) plus scaled up/ down source/ load resistance.

\[ g_{mb} = \chi g_m \]
\[ \frac{1}{g_m} \ll r_o \]
(CG Body Effect)

- Body transconductance $g_{mb}$
  - An additional gate
    $$g_{mb} = \chi g_m$$
    $$0.1 < \chi < 0.2$$

- Buffer CG stage
  - Source not on ground potential, but gate is
  - Body also on ground
  - Body effect acts in parallel to main gate
    $$g'_m = (1 + \chi)g_m \approx g_m$$

We neglect the body effect, once again, as it has small (positive) impact.
CS-CG Compound Device: Cascode Amplifier

- **CS gain input stage**
  - Loaded by buffer

- **CG current buffer output stage**
  - Increases output resistance

\[
R_i = \frac{v_i}{i_i} \approx \frac{R_L}{g_m r_{o2}}
\]

\[
R_o = \left. \frac{v_o}{i_o} \right|_{v_{sig}=0} = K r_{o1} \approx (g_m r_{o2}) r_{o1}
\]

\[
A_{vo} = A_v \big|_{R_L=\infty} = g_m R_o \approx g_m (g_m r_{o2}) r_{o1}
\]

\[
A_v = g_m (R_o || R_L)
\]

Cascaded cathode, cf. vacuum tube technology.
Cascode w/ Active Load

- Ideal active load
  - Cascode output resistance preserved
    \[ A_v \approx g_{m1}(g_{m2}r_{o2})r_{o1} \]

- Real active load
  - Implemented with a PMOS w/ output resistance
  - Gain lowered approximately to intrinsic gain
    \[ A_v = g_{m1}(R_o||R_L) \approx g_{m1}r_{o3} \]

Output resistance kills gain increase, but active load improves BW.
Cascode w/ Cascode Active Load

- Problem
  - Output resistance of active load reduces cascode gain

- Solution
  - Cascode the active load to increase its output resistance

\[ A_v \approx \frac{g_{m1} (g_{m2} r_{o2}) r_{o1}}{2} \]

- Problems remain
  - Source resistance higher, but still similar to cascode output resistance
  - Very high supply voltage required (four stacked saturation conditions)
Folded Cascode

- CS gain NMOS input stage
- CG current buffer PMOS output stage

Popular CMOS stage that limits the required dive voltage.
CD w/ Output Resistance

- Useful input stage
  - High input impedance
  - Output resistance and body effect shunt to ground

- $R_i = \frac{v_i}{i_i} = \infty$

- $R_o = \frac{v_o}{i_o} \bigg|_{\text{v}_{\text{sig}}=0} = \frac{1}{g_m} || r_{o1} || \frac{1}{g_{mb}} || r_{o3} \approx \frac{1}{g_m(1+\chi)}$

- $A_{vo} = \frac{r'_o}{r_o + \frac{1}{g_m}} \approx \frac{1}{1+\chi}$

- $A_v = \frac{r'_o || r_L}{r_o || r_L + \frac{1}{g_m}}$

Body effect limits the gain, in proportion relative to gate strength.
CD-CS Compound Device

• **CD voltage follower input stage**
  - High input resistance (but CS already has that)

• **CS gain output stage**
  - CD input isolation provides increased BW

- \( R_i = \frac{v_i}{i_i} = \infty \)
- \( R_o = \left. \frac{v_o}{i_o} \right|_{v_{sig}=0} \approx \frac{r_{o2}}{2} \)
- \( A_{vo} = A_v \mid_{R_L=\infty} \approx -g_{m2}R_o \approx -\frac{g_{m2}r_{o2}}{2} \)
- \( A_v = \frac{-g_{m2}(R_o || R_L)}{1 + \chi} \)

Similar to just CS at low frequency, but improved bandwidth.
CD-CG Compound Device

- CD voltage follower input stage
  - High input resistance (better than CG)

- CG gain output stage
  - CD input isolation provides increased BW

- \( R_i = \frac{v_i}{i_i} = \infty \)
- \( R_o = \frac{v_o}{i_o} \bigg|_{v_{sig}=0} \approx (g_{m2}r_{o2}) \left( \frac{1}{g_{m1} \parallel r_{o1}} \right) || r_{o1} \)
- \( A_{vo} = A_v \big|_{R_L=\infty} = -g_{m2}R_o \)
- \( A_v = -g_{m2}(R_o \parallel R_L) \)

Higher input resistance than CG, and improved bandwidth.