F8 – Building Blocks of Integrated Circuit Amplifiers

Outline

- Integrated circuit (IC) design
- Current mirrors, steering circuits, sources, sinks
- Intrinsic gain cell
- Common source (CS) amplifier w/ output resistance
- CS amplifier w/ active load
- Common gate (GS) amplifier w/ output resistance
- CS-CG Compound Device: Cascode amplifier
- Common drain (CD) amplifier w/ output resistance

Reading Guide *Sedra/Smith 7ed int*

- Chapter 7.1-7.5

Problems *Sedra/Smith 7ed int*

- P7.7, 7.20(a), 7.26, 7.51, 7.64

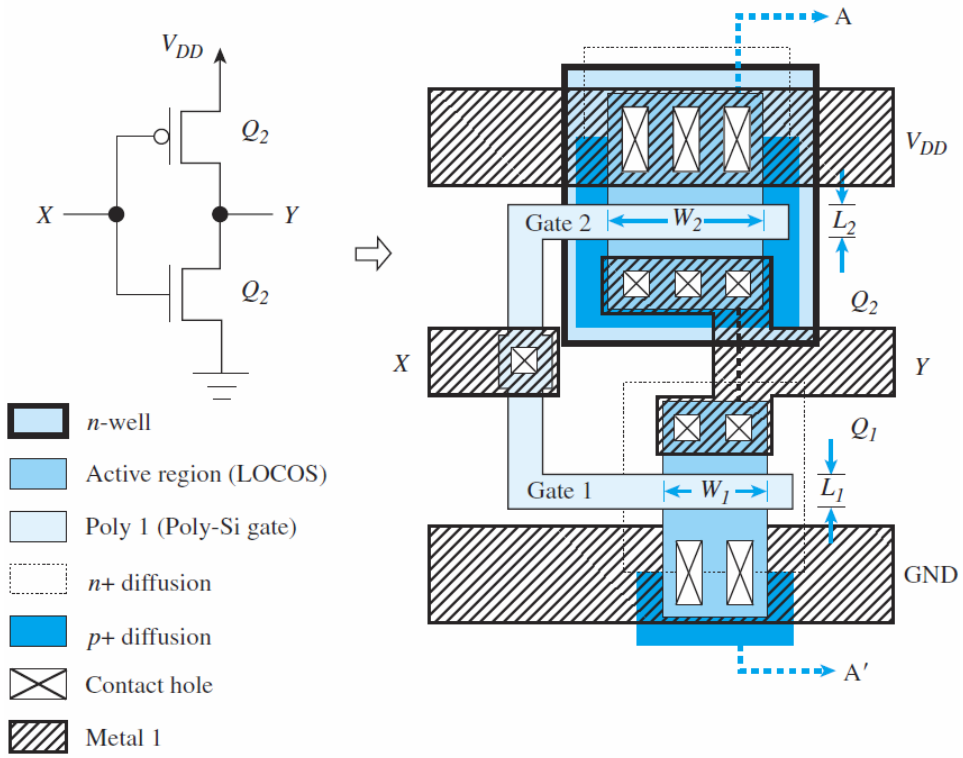
Integrated Circuits (ICs) and Components

- Area = $$$
  - Performance vs. integration density tradeoff
  - Avoid large components if possible

- Complementary MOS (CMOS) technology
  - Best cost per transistor if mass produced in very-large-scale ICs (VLSI) technology
  - Low-power digital logic ($V_{DD} < 1$ V in scaled CMOS)
    + decent analogue circuits
    = very versatile!

- BJT technology
  - Very useful, but mainly for special applications

- Historically, IC size scaling improved performance



IC design provides good device uniformity, as compared to discrete devices.

MOSFET Current Mirror

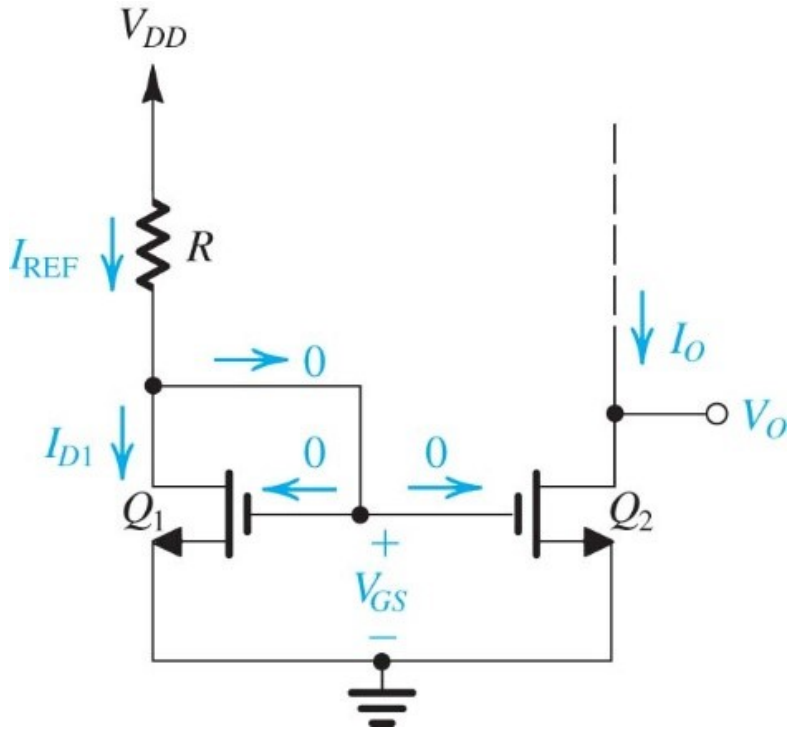
- Resistance to supply provides reference current

- Reference (input) branch
  - Diode connected (G bound to D) CS device Q1, $V_{DS1} = V_{GS1} > V_{OV1}$, enforces saturation

$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_{tn})^2 = I_{REF} - 0 = \frac{V_{DD} - V_{GS}}{R}$$

- Source (output) branch
  - CS device Q2 shares S and G with Q1, in saturation if $V_{DS2} > V_{OV1}$

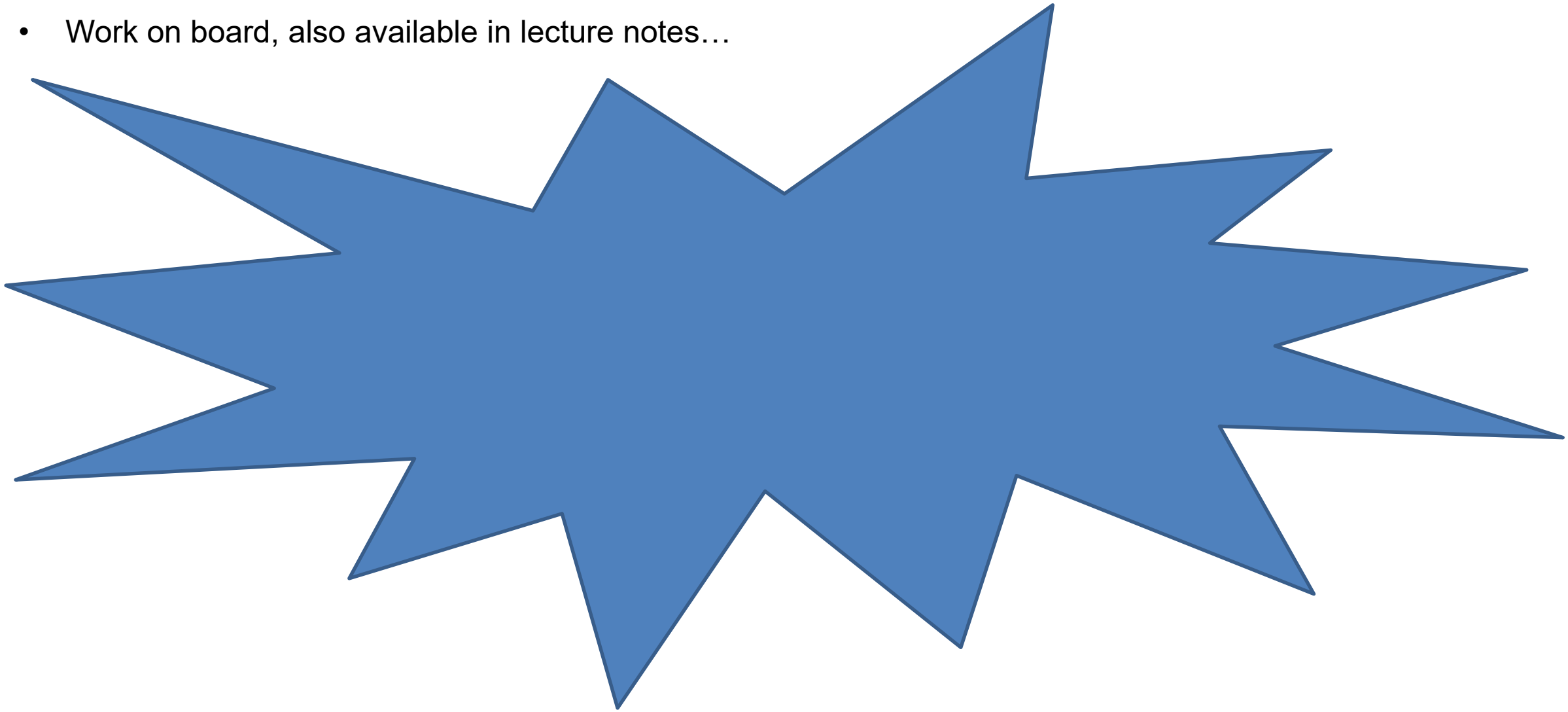
$$I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_{tn})^2 = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$



Current mirrors only make sense in IC technology, where variability is low.

MOSFET Current Mirror w/ Output Resistance

- Work on board, also available in lecture notes…



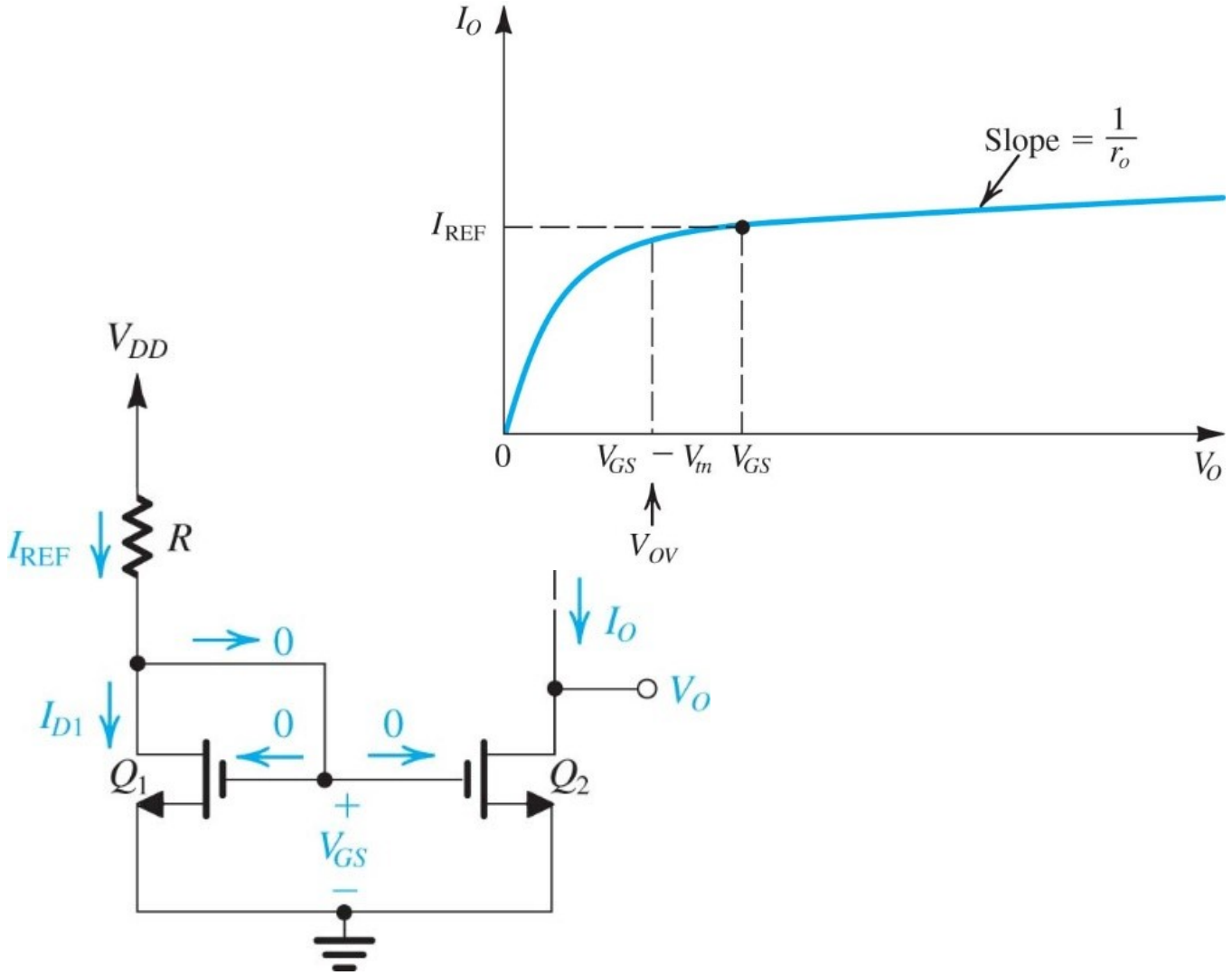
MOSFET Current Mirror w/ Output Resistance

- Output resistance yields dependence on output voltage

$$R_O = \frac{\partial V_O}{\partial I_O} = r_{o2} = \frac{1}{\lambda_2 I_{D2}}$$

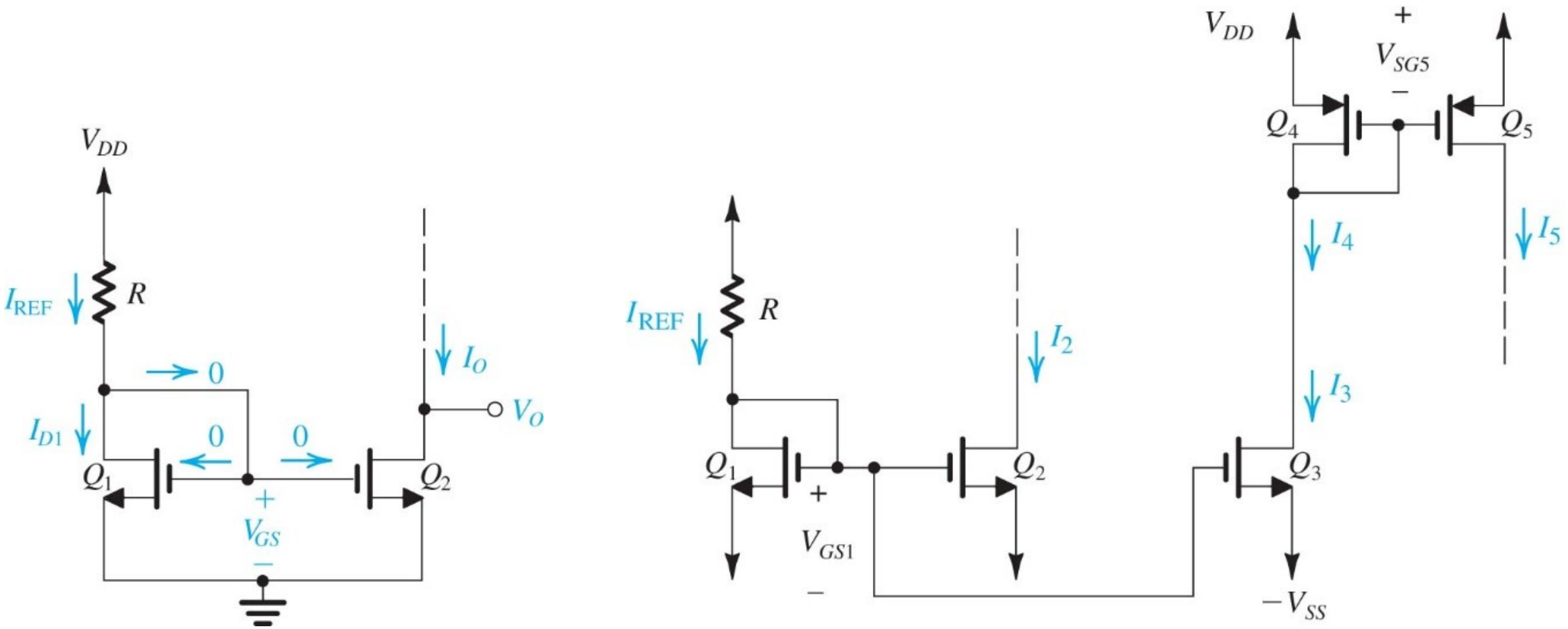
- Exact transfer requires equivalent voltages on all terminals of Q1 and Q2

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF}(1 + \lambda_2[V_O - V_{GS}])$$



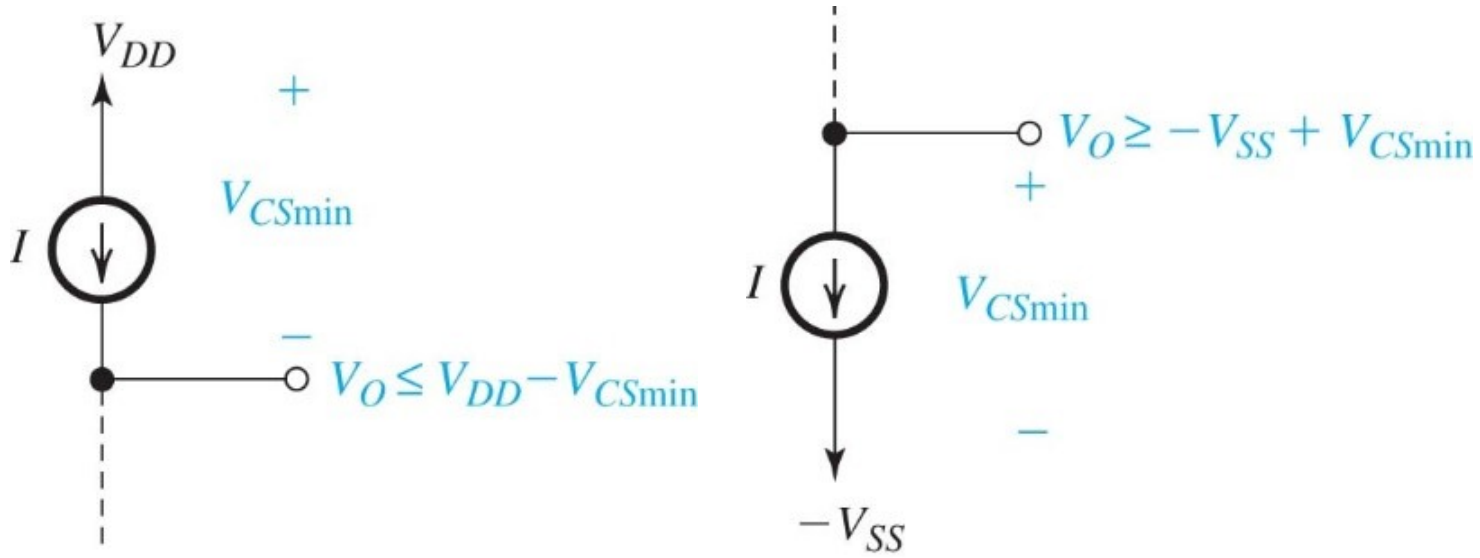
Current Steering Circuit

- One reference path can control several current sources/ sinks



(Current Source vs Current Sink)

- Current source
  - Extracts current from supply
- Current sink
  - Injects current into ground

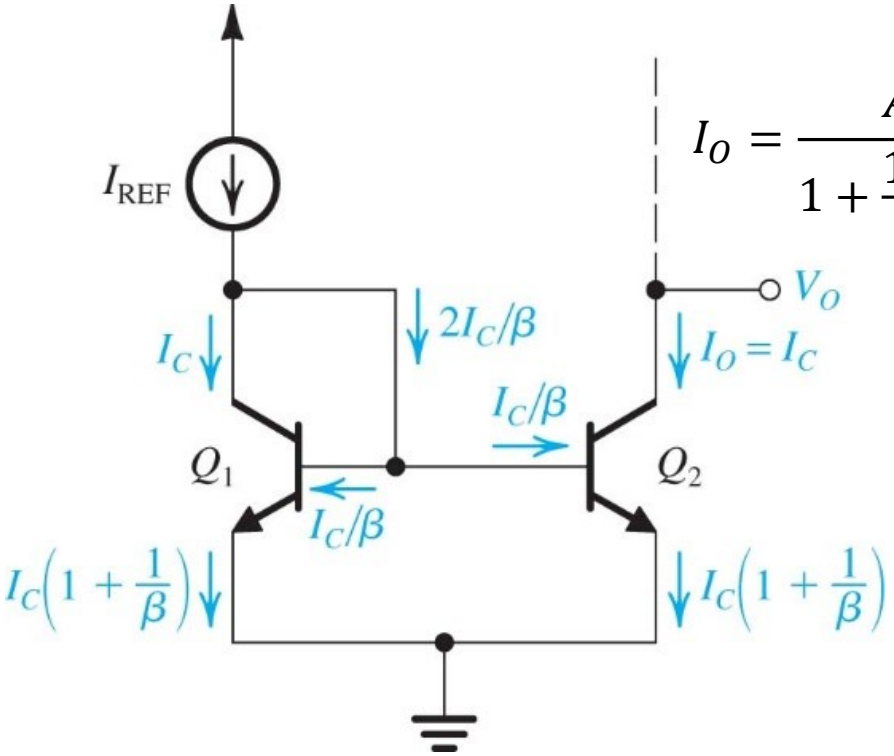


This is a matter of definition.

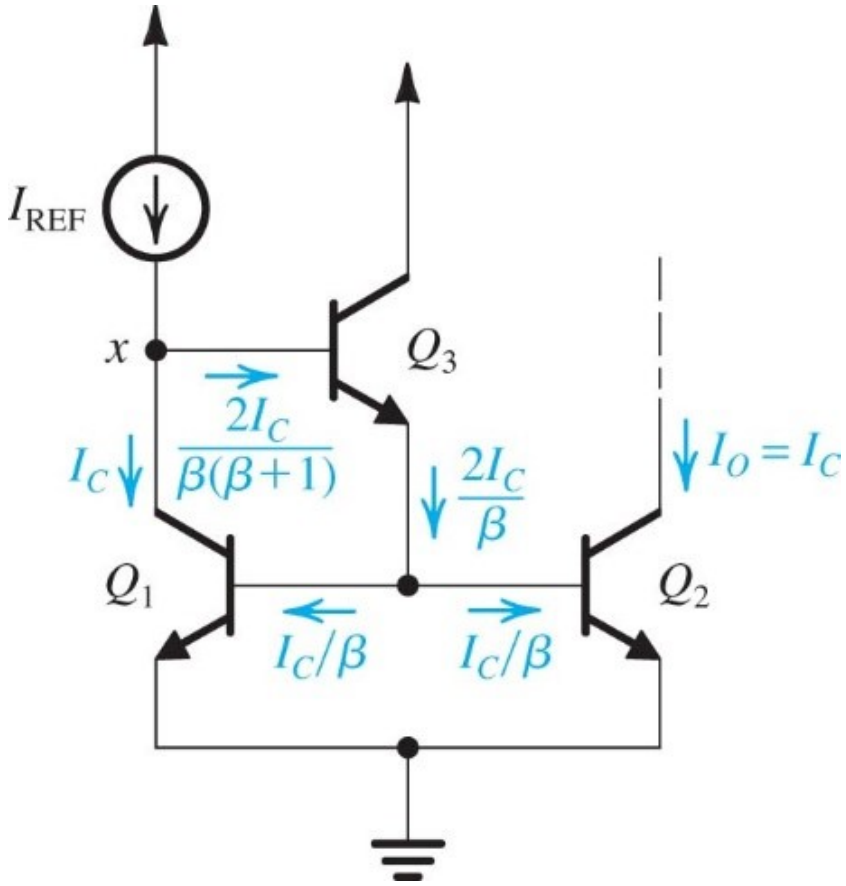
BJT Current Mirror

- BJT current mirror similar to MOSFET, but scaling w.r.t. BE junction area

- Base current loss may be compensated by additional BJT



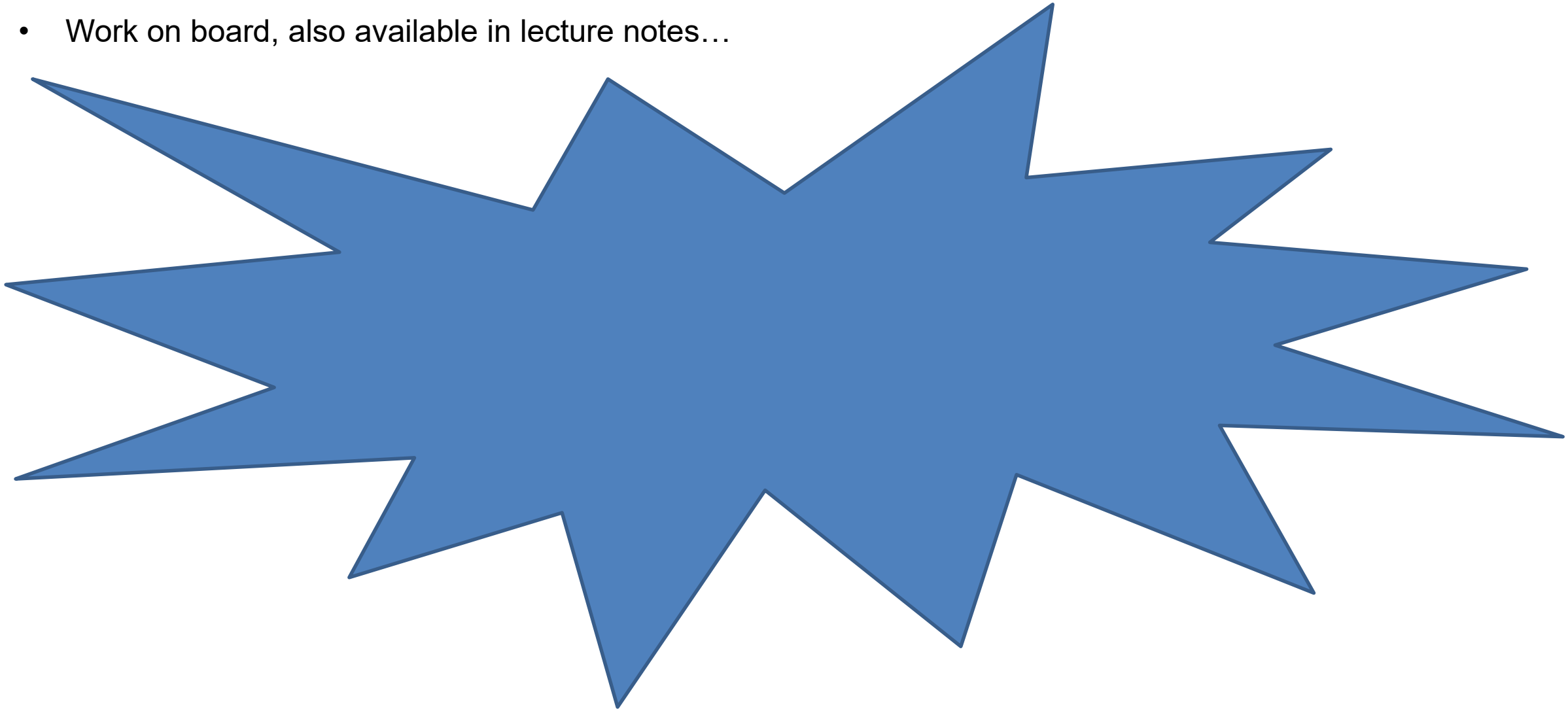
$$I_O = \frac{A_2/A_1}{1+\frac{1+A_2/A_1}{\beta}} I_{REF}\left(1+\frac{V_O - V_{BE}}{V_A}\right)$$



Advanced current mirror circuits can supress the BJT base current error.

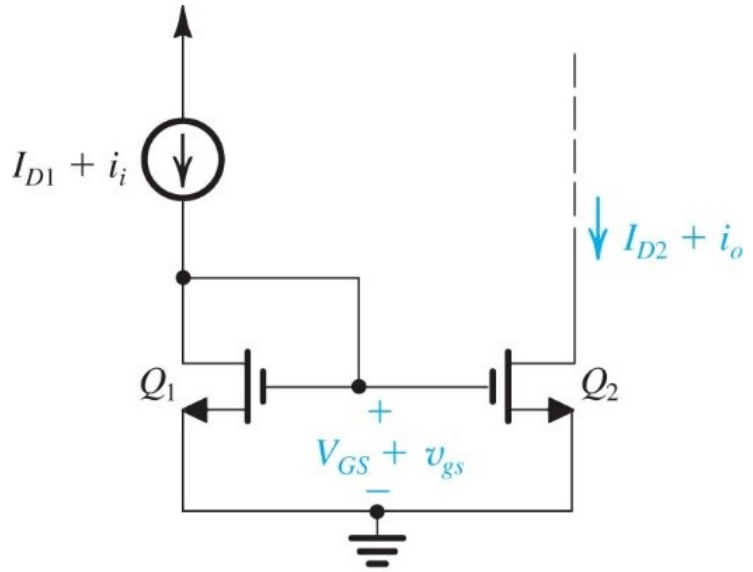
MOSFET Current Mirror: Small Signal Operation

- Work on board, also available in lecture notes…



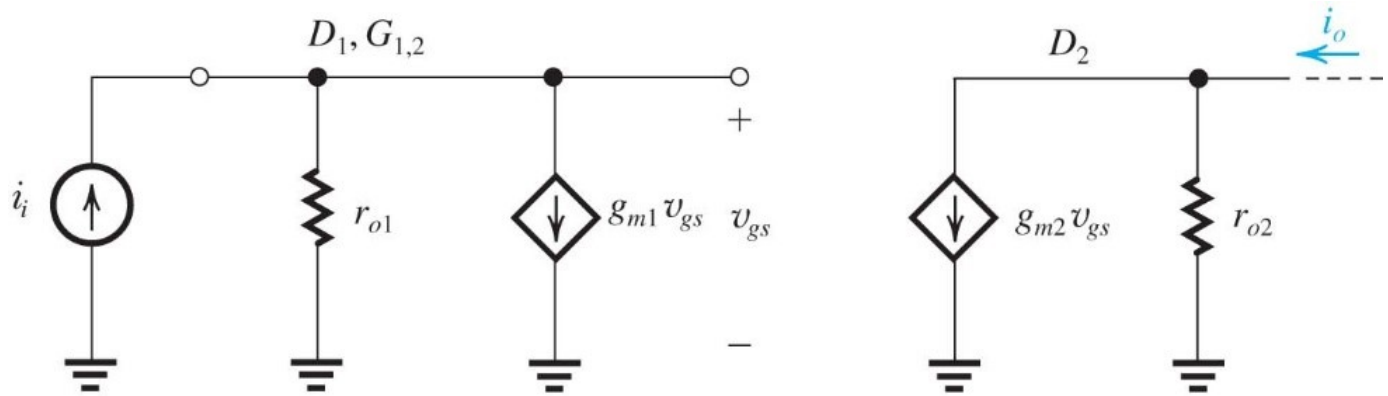
MOSFET Current Mirror: Small Signal Operation

- Excellent linearity
  - Small signal current gain and bias current ratio virtually equal



- $R_i = \frac{v_i}{i_i} = r_{o1} || \frac{1}{g_{m1}} \approx \frac{1}{g_{m1}}$
- $R_o = \frac{v_o}{i_o}\Big|_{i_{sig}=0} = r_{o2}$
- $A_{is} = \frac{i_o}{i_i}\Big|_{R_L=0} = g_{m2}\left(r_{o1} || \frac{1}{g_{m1}}\right) \approx \frac{g_{m2}}{g_{m1}} = \frac{(W/L)_2}{(W/L)_1} = \frac{I_O}{I_{REF}}$

$$g_m = k_n' \left(\frac{W}{L}\right) V_{OV}$$

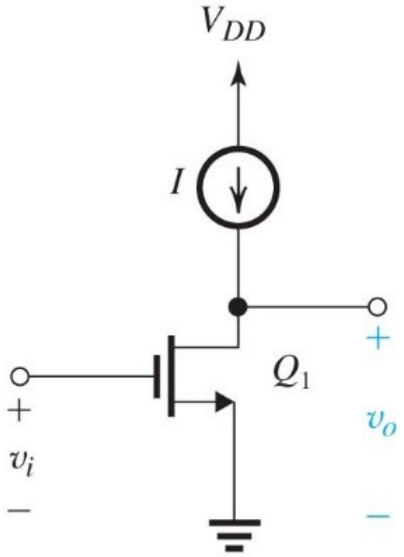


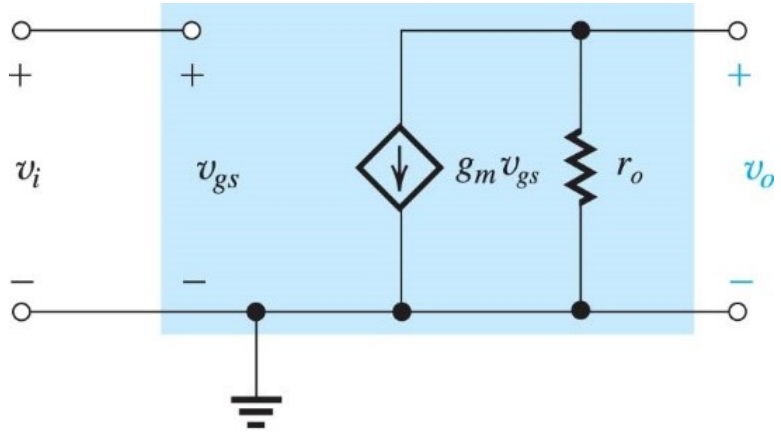
The Basic Gain Cell: CS Amplifier w/ Active Load

- CS amplifier with current source load
  - Load is an active component
  - Small signal analysis, $I = 0$, i.e. open circuit
  - Intrinsic SC stage gain, $A_0 = g_m r_o$

$$A_0 \gg 1 \Leftrightarrow \frac{1}{g_m} \ll r_o$$

- $R_i = \frac{v_i}{i_i} = \infty$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = r_o$
- $A_{vo} = A_v|_{R_L=\infty} = \frac{v_o}{v_i}\Big|_{R_L=\infty} = -g_m r_o = -A_0$
- $A_v = -g_m r_o = A_{vo} = A_0$





Intrinsic Gain

- MOSFET
  - Intrinsic can be designed to vary among different devices
    - Tradeoff: gain vs. BW

$$A_0 = g_m r_o \approx \frac{2}{\lambda V_{OV}} = \frac{2L}{\lambda' V_{OV}} = \frac{1}{\lambda'}\sqrt{2k_n' WL/I_D}$$

$$g_m = k_n'\left(\frac{W}{L}\right)V_{OV} = \sqrt{2k_n'\left(\frac{W}{L}\right)I_D} = \frac{2I_D}{V_{OV}}$$

$$r_o = \frac{1}{\lambda I_D'} = \frac{L}{\lambda' I_D'} = \frac{V_A' L}{I_D'} = \frac{V_A}{I_D'}$$

- BJT
  - Intrinsic gain is a technology constant

$$A_0 = g_m r_o \approx \frac{V_A}{V_T}$$

$$g_m = \frac{I_C}{V_T}$$

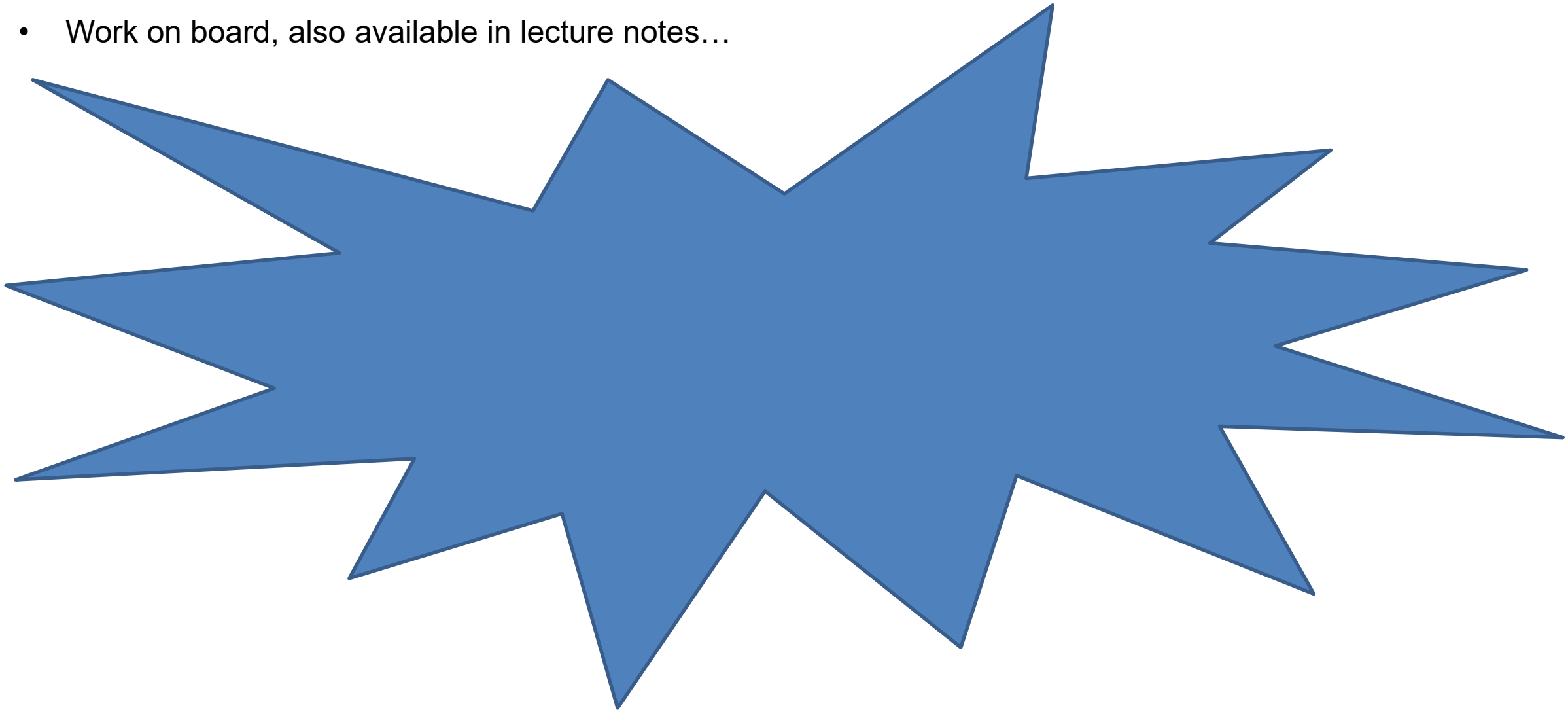
$$r_o = \frac{V_A}{I_C'}$$

$$A_0 \gg 1 \Leftrightarrow \frac{1}{g_m} \ll r_o$$

Intrinsic gain is magnitude of open circuit voltage gain of the basic CS(/ CE) amplifier.

Active Load w/ Output Resistance

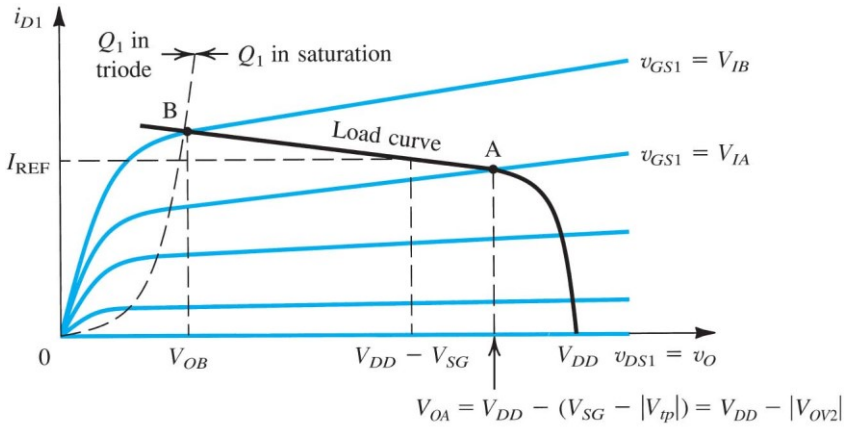
- Work on board, also available in lecture notes…

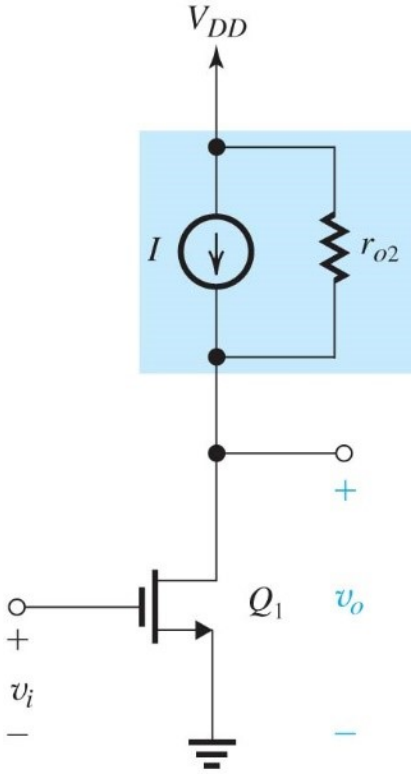


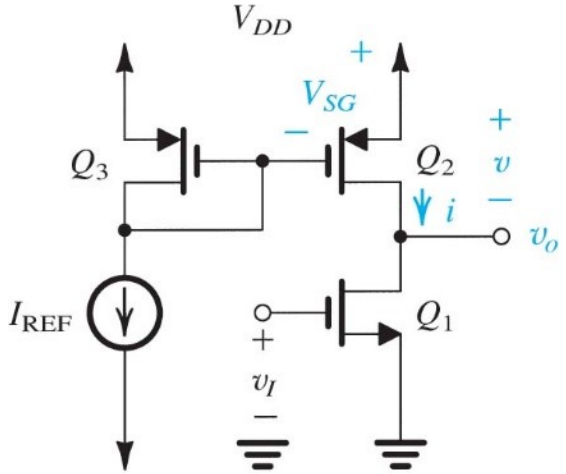
Active Load w/ Output Resistance

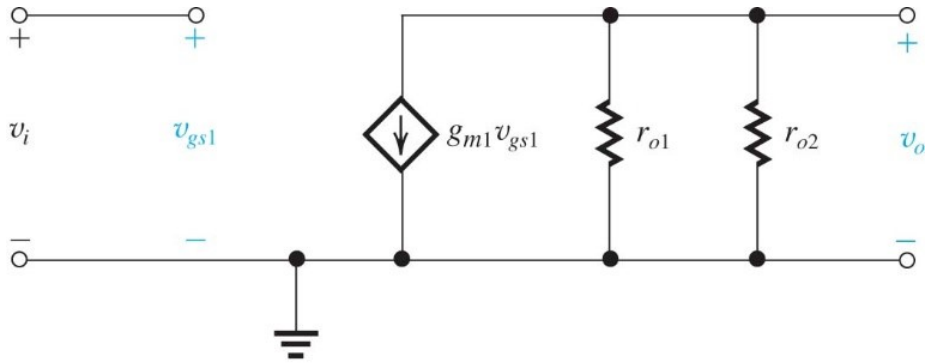
- CS amplifier with active load w/ output conductance
  - Small signal analysis, $I = 0$, i.e. open circuit
  - CG presents load similar to CS output conductance

- $R_i = \frac{v_i}{i_i} = \infty$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = r_{o1} || r_{o2} \approx \frac{r_o}{2}$
- $A_{vo} = \frac{-g_m r_o}{2} = -\frac{A_0}{2}$



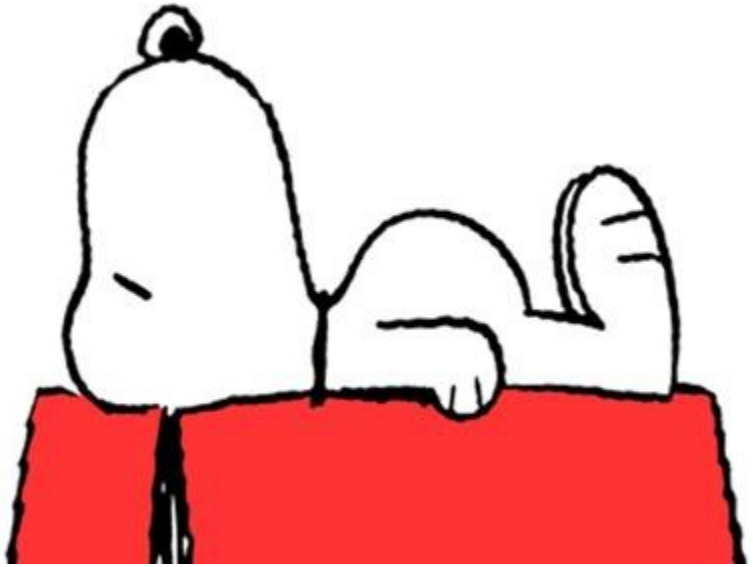






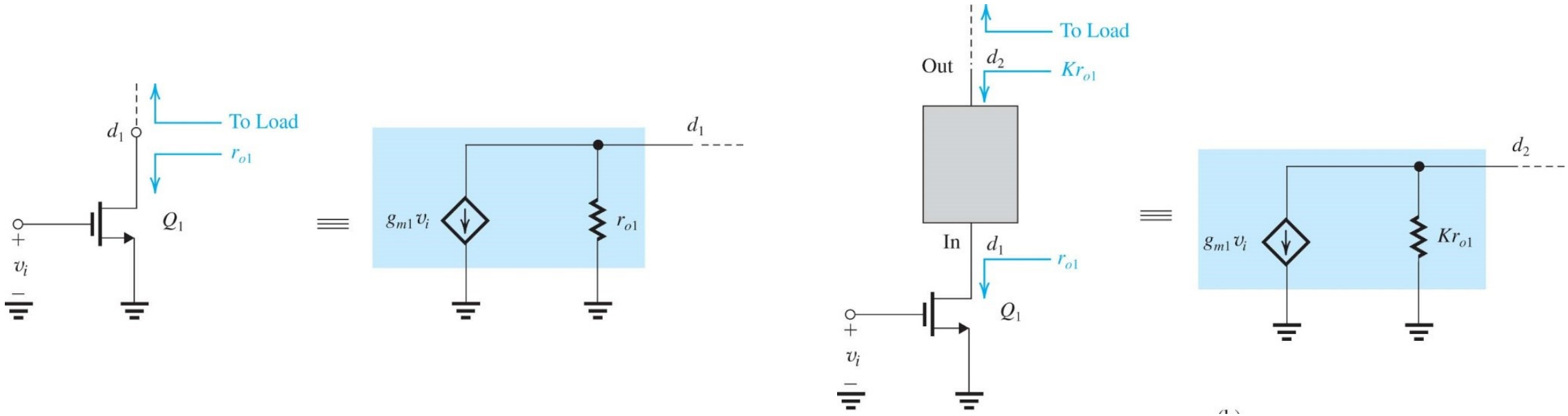
Output resistance of active load reduces the gain.

BREAK

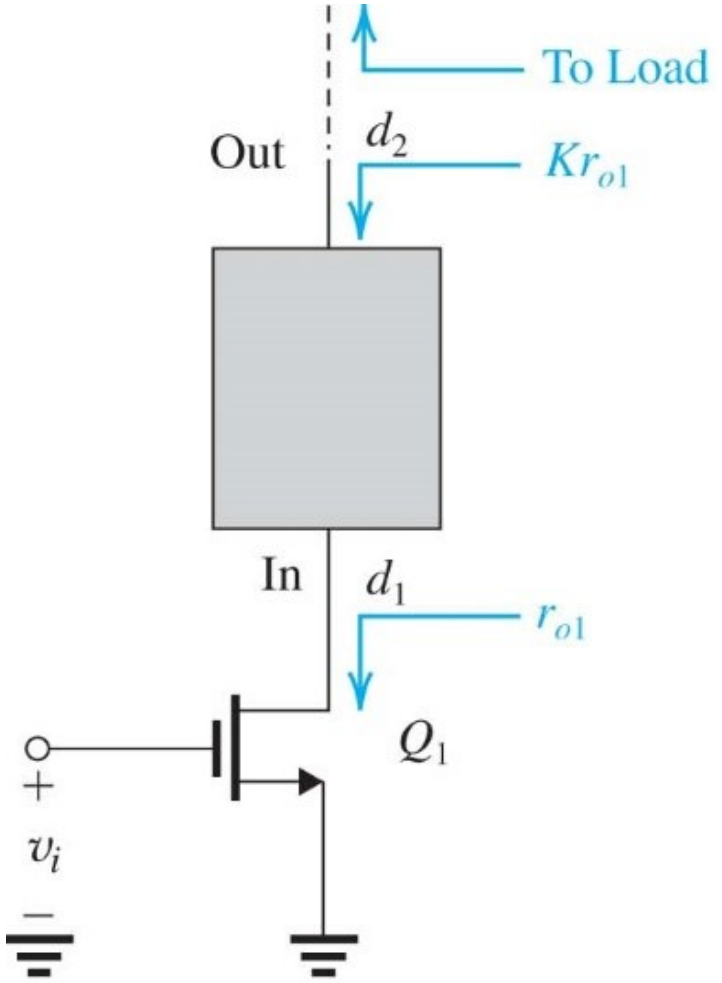


Increasing the Gain of the Basic Cell

- Need to insert a circuit, between output and load, that…
  - Transfers current unchanged
  - Increases output resistance



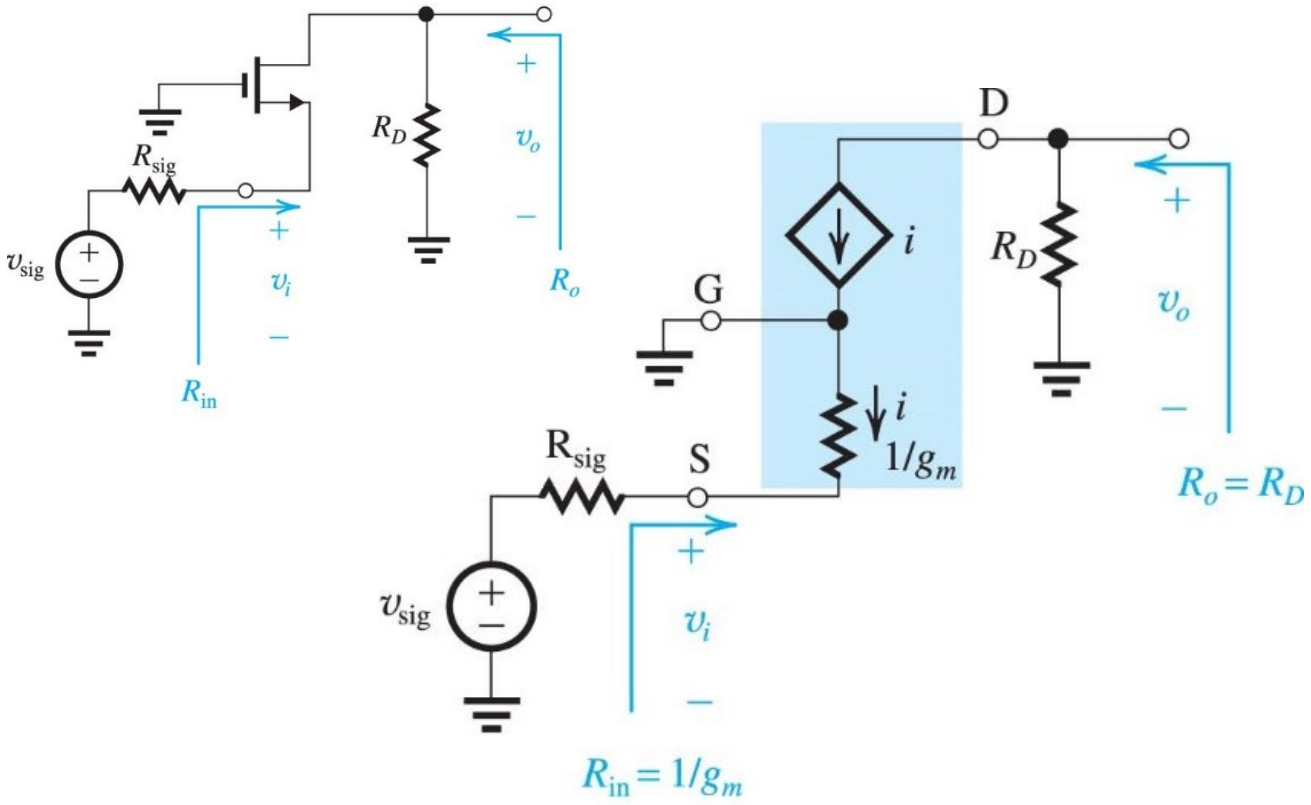
What transfers current unchanged and increases output conductance?



Common Gate (CG) Amplifier as a Current Buffer (recap)

- Low input resistance, moderate output resistance

- $R_i = \frac{v_i}{i_i} = \frac{1}{g_m}$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = R_D$
- $A_{vo} = A_v|_{R_L=\infty} = g_m R_D$
- $A_v = A_{vo}\frac{R_L}{R_L+R_o} = g_m(R_D||R_L)$
- $G_v = \frac{R_i}{R_i+R_{sig}}A_v = \frac{R_D||R_L}{R_{sig}+1/g_m} < A_v$



Transistor output resistance would somewhat complicate analysis.

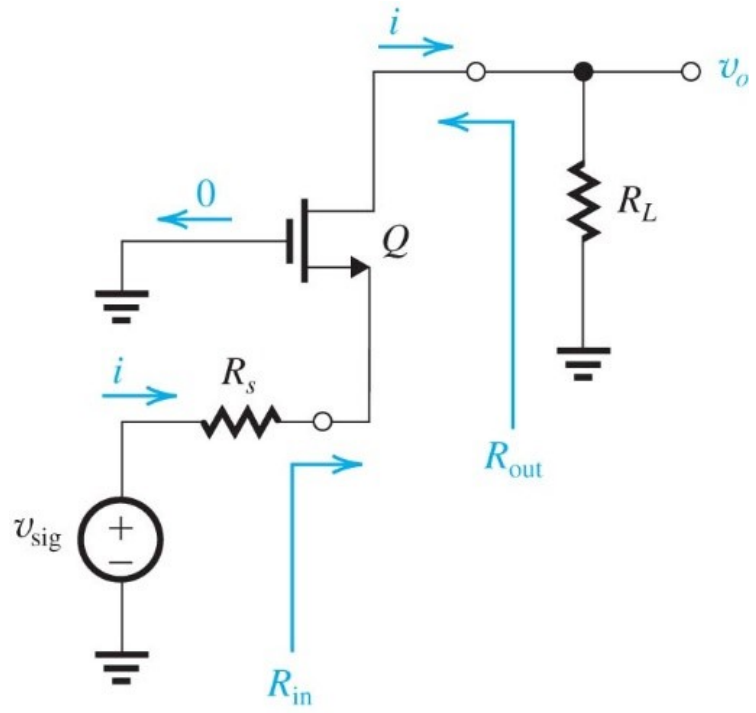
CG Amplifier w/ Output Resistance

- Low input resistance, moderate output resistance
  - Buffers current even w/ output resistance (of device), but output/ input resistance depend on source/ load

- $R_i = \frac{v_i}{i_i} = \frac{r_o + R_L}{1 + g_m r_o} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o}$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = r_o + R_s + g_m r_o R_s \approx r_o + g_m r_o R_s$
- $A_{vo} = A_v|_{R_L=\infty} = g_m R_o \approx g_m^2 r_o R_s$
- $A_v = g_m(R_o || R_L)$

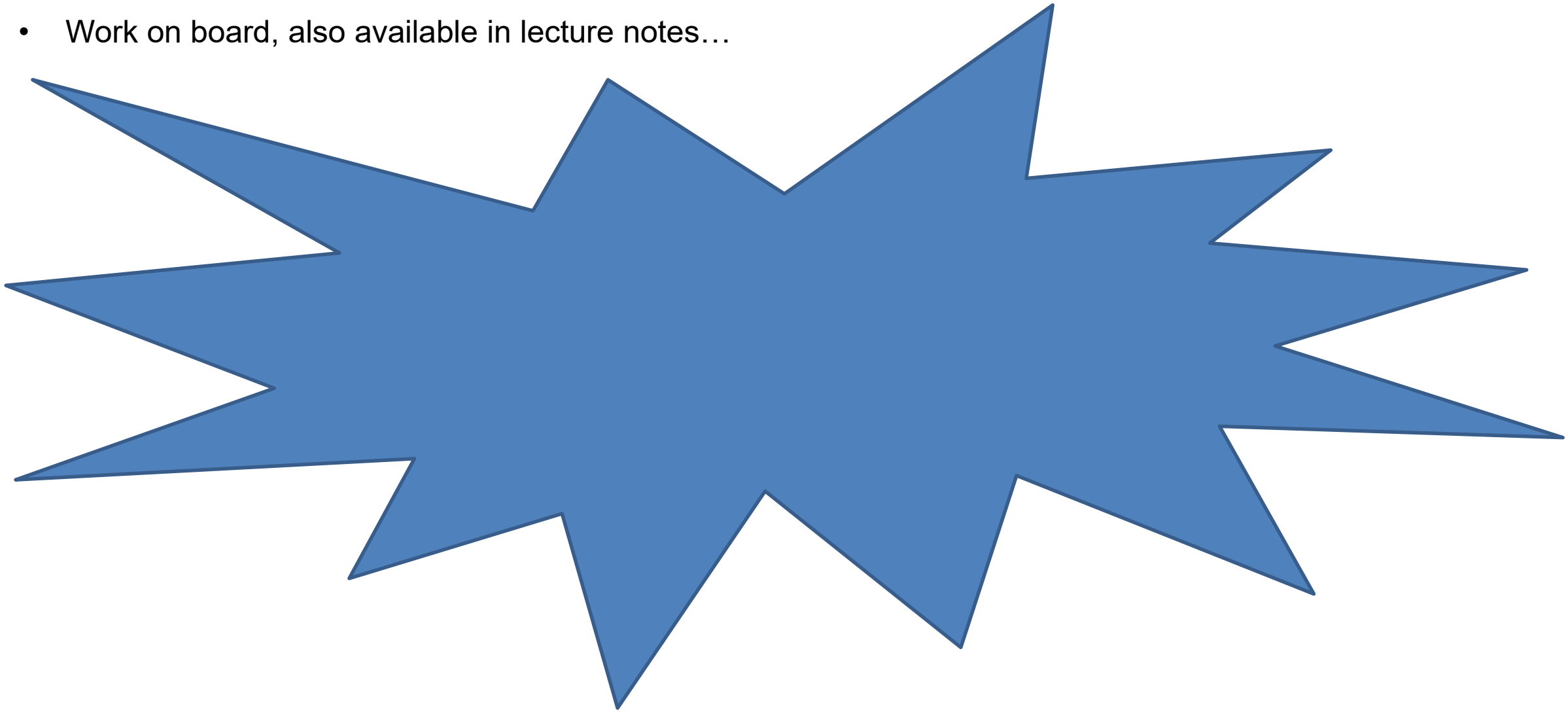
$$g_{mb} = \chi g_m$$

$$\frac{1}{g_m} \ll r_o$$

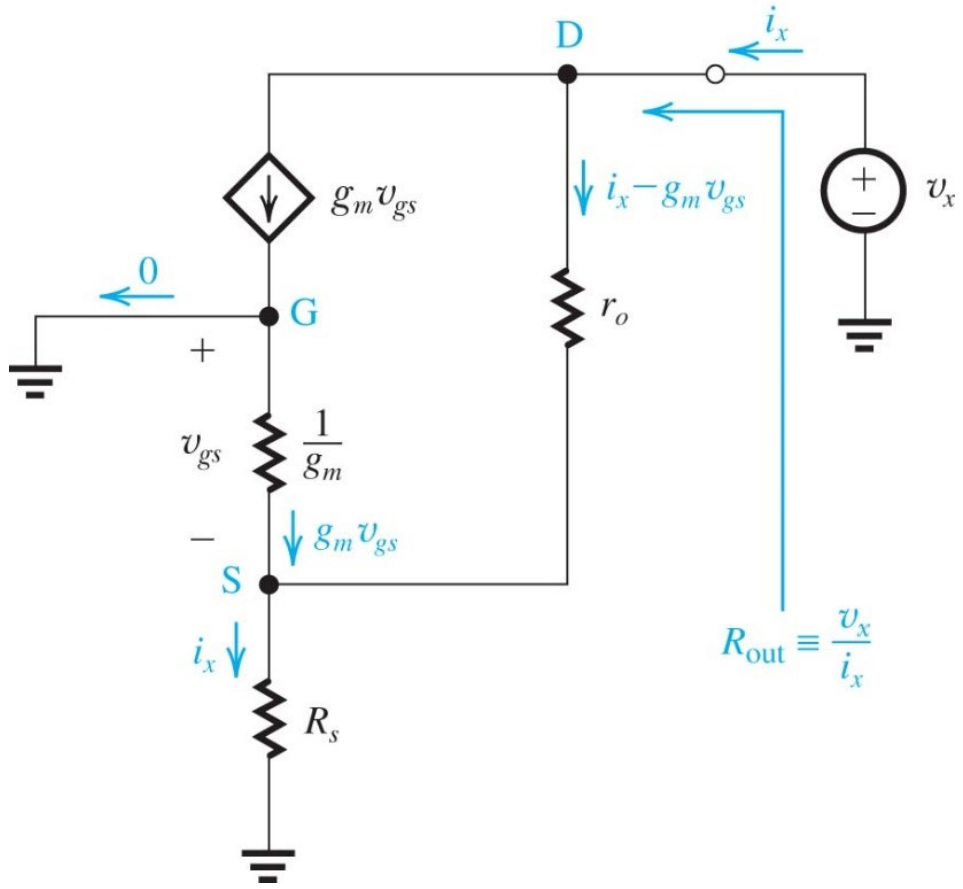


CG Amplifier w/ Output Resistance: Output Resistance

- Work on board, also available in lecture notes…

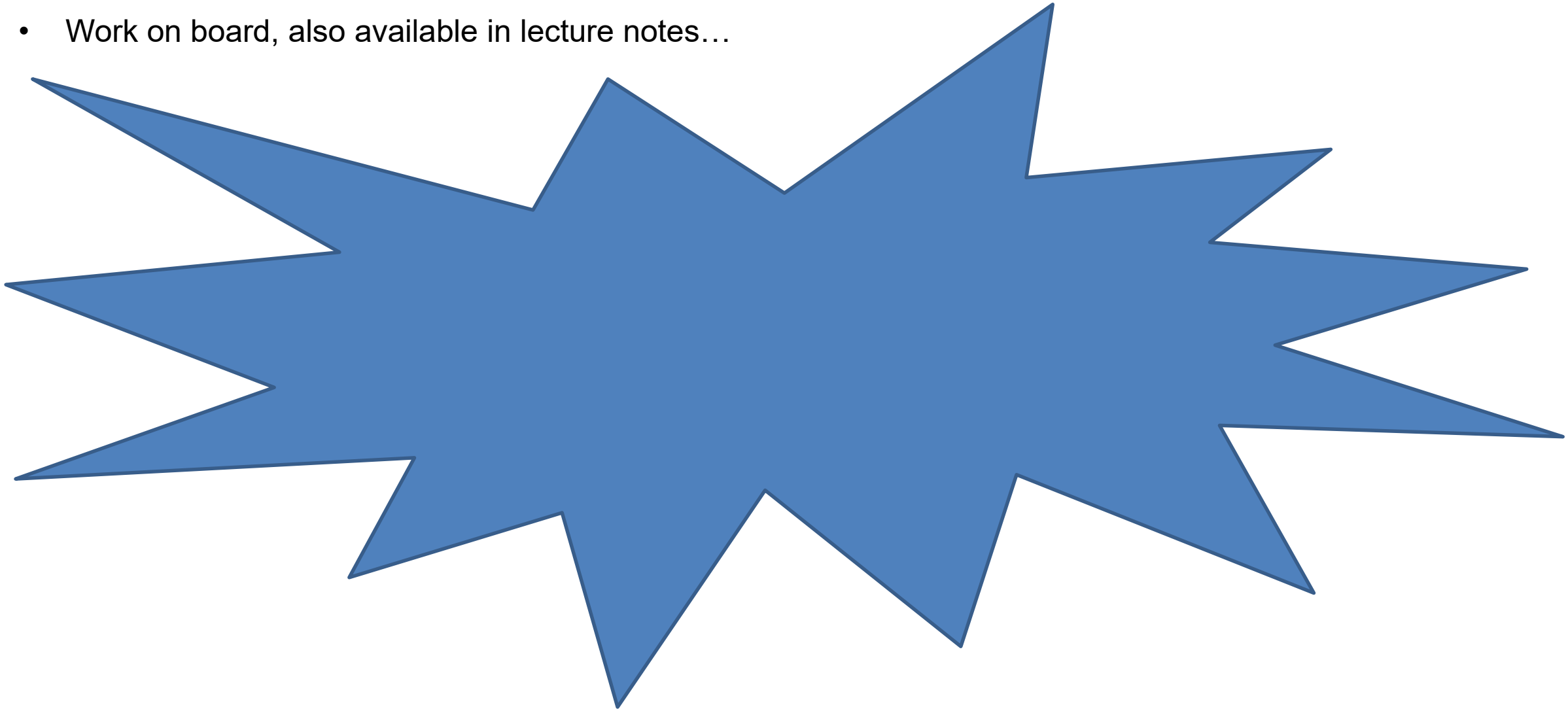


CG Amplifier w/ Output Resistance: Output Resistance

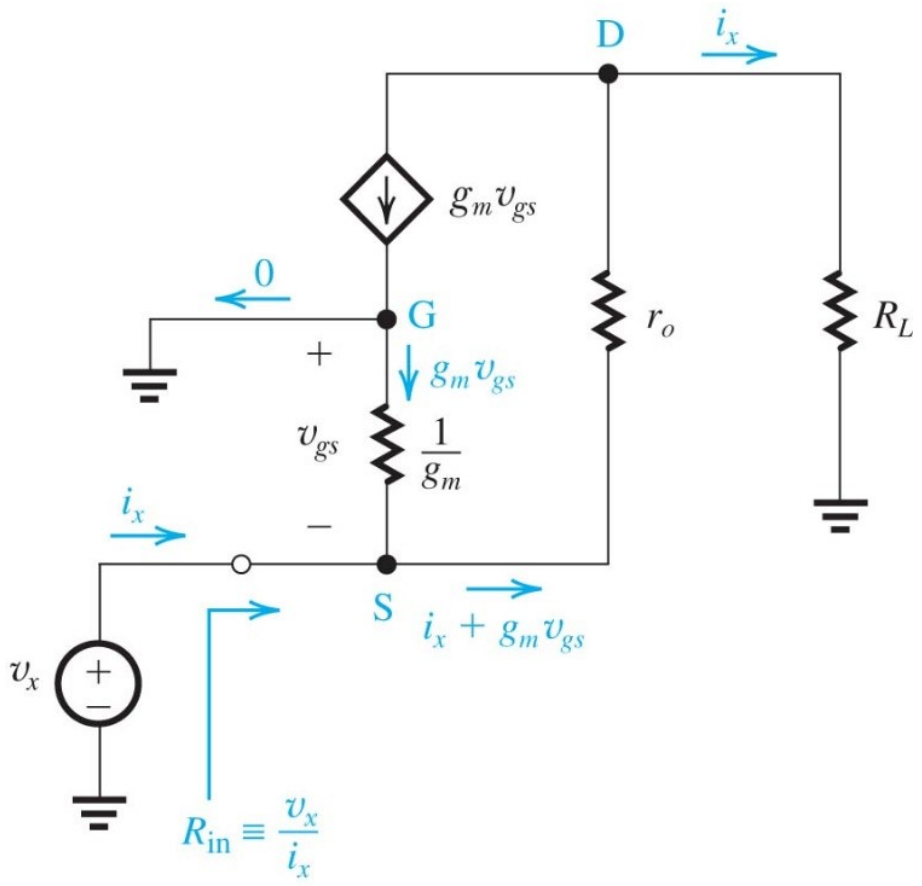


CG Amplifier w/ Output Resistance: Input Resistance

- Work on board, also available in lecture notes…



CG Amplifier w/ Output Resistance: Input Resistance



CG Output/ Input Resistance: Source/ Load Transformations

- CG w/ vs w/o output resistance

- Input
  - Value w/o plus reduced load

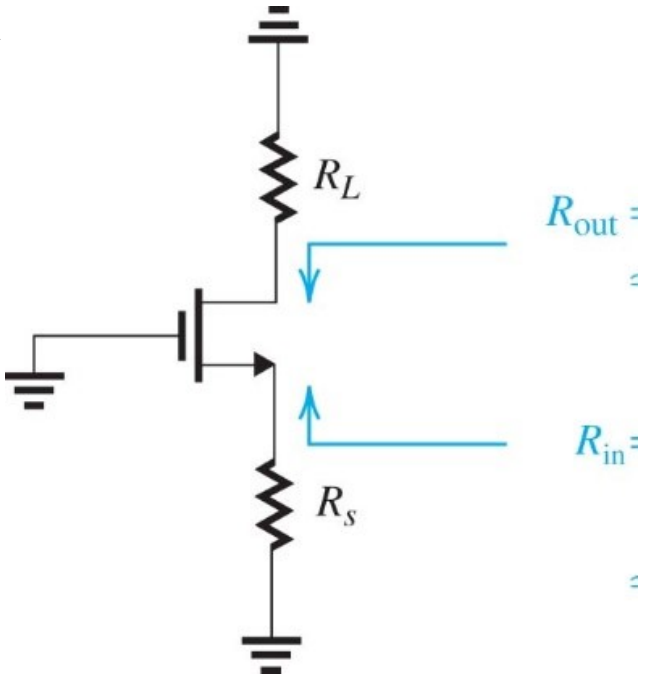
$$R_i = \frac{r_o + R_L}{1 + g_m r_o} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} = \frac{1}{g_m} + \frac{R_L}{A_0}$$

- Output
  - Value w/o plus increased source

$$R_o = r_o + R_s + g_m r_o R_s \approx r_o + g_m r_o R_s = r_o + A_0 R_s$$

$$g_{mb} = \chi g_m$$

$$\frac{1}{g_m} \ll r_o$$



Output/ input resistance w/o r_o plus scaled up/ down source/ load resistance.

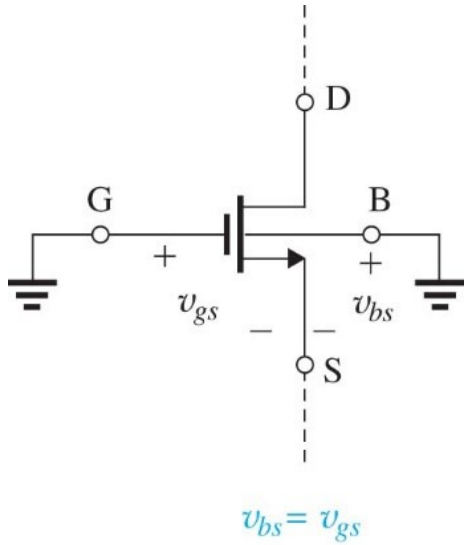
(CG Body Effect)

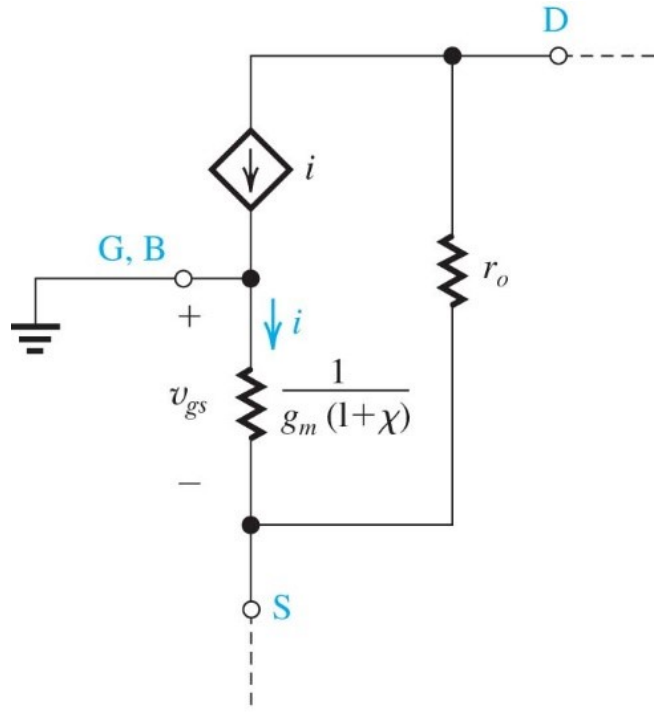
- Body transconductance g_mb
  - An additional gate

$$g_{mb} = \chi g_m$$
$$0.1 < \chi < 0.2$$

- Buffer CG stage
  - Source not on ground potential, but gate is
  - Body also on ground
  - Body effect acts in parallel to main gate

$$g'_m = (1+\chi) g_m \approx g_m$$



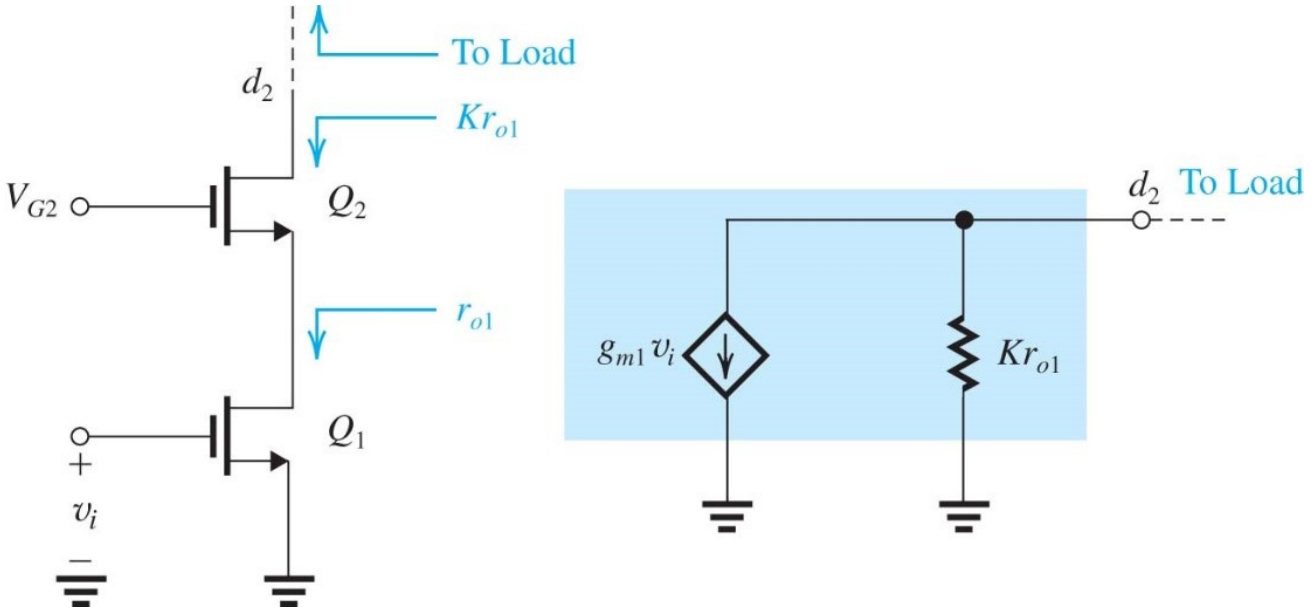


We neglect the body effect, once again, as it has small (positive) impact.

CS-CG Compound Device: Cascode Amplifier

- CS gain input stage
  - Loaded by buffer
- CG current buffer output stage
  - Increases output resistance

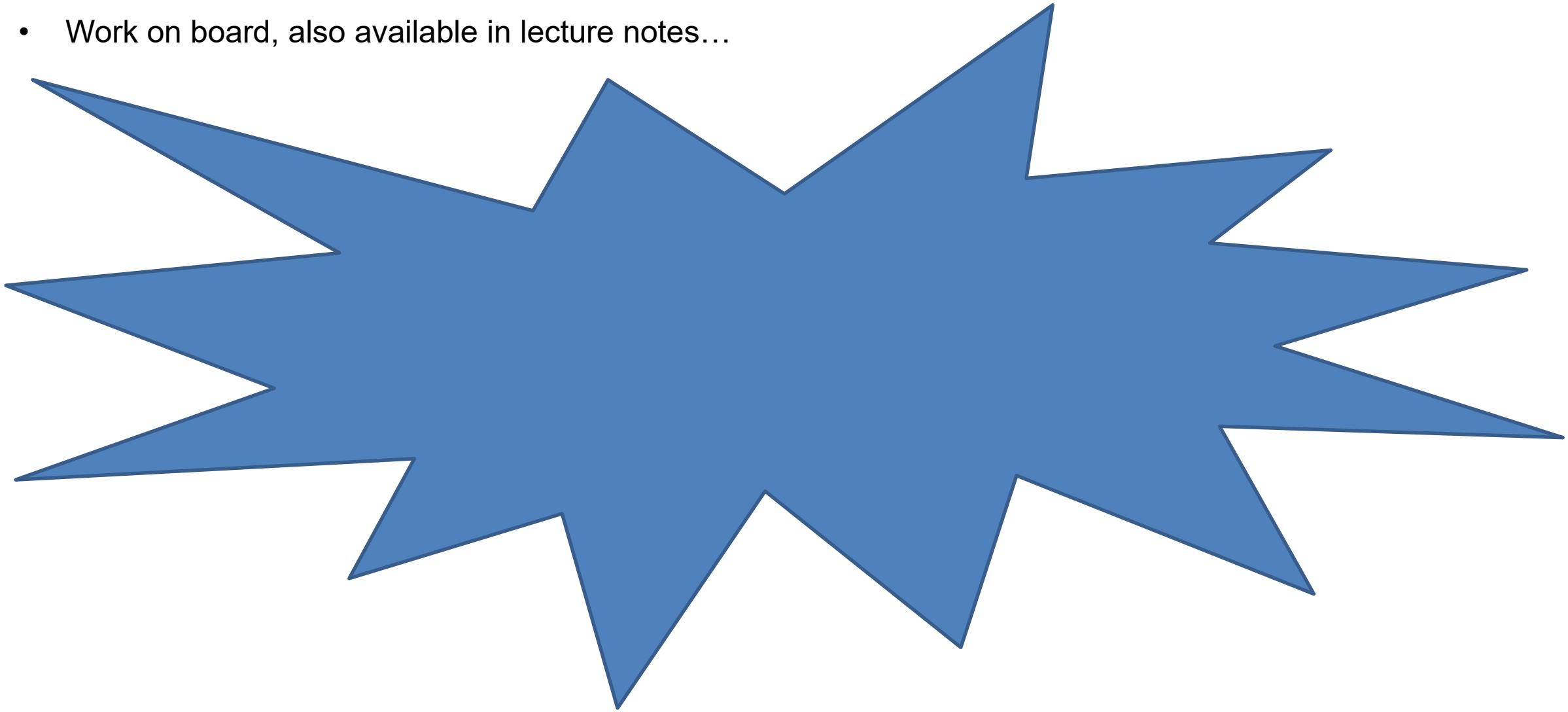
- $R_i = \frac{v_i}{i_i} \approx \frac{R_L}{g_m r_{o2}}$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = Kr_{o1} \approx (g_{m2} r_{o2}) r_{o1}$
- $A_{vo} = A_v|_{R_L=\infty} = g_{m1} R_o \approx g_{m1}(g_{m2} r_{o2}) r_{o1}$
- $A_v = g_{m1}(R_o || R_L)$



Cascaded cathode, cf. vacuum tube technology.

Cascode w/ Active Load

- Work on board, also available in lecture notes…



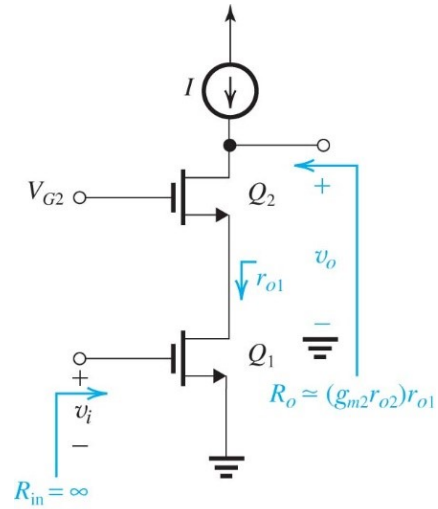
Cascode w/ Active Load

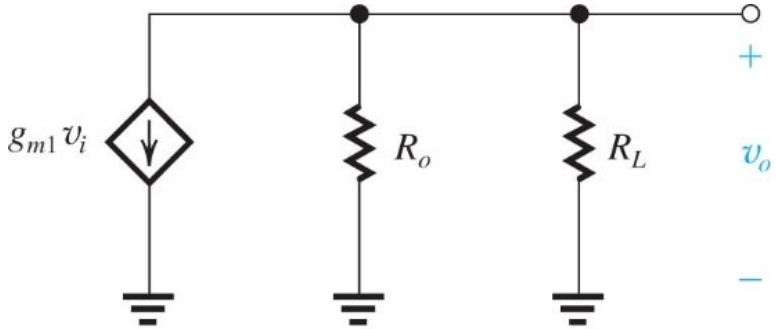
- Ideal active load
  - Cascode output resistance preserved

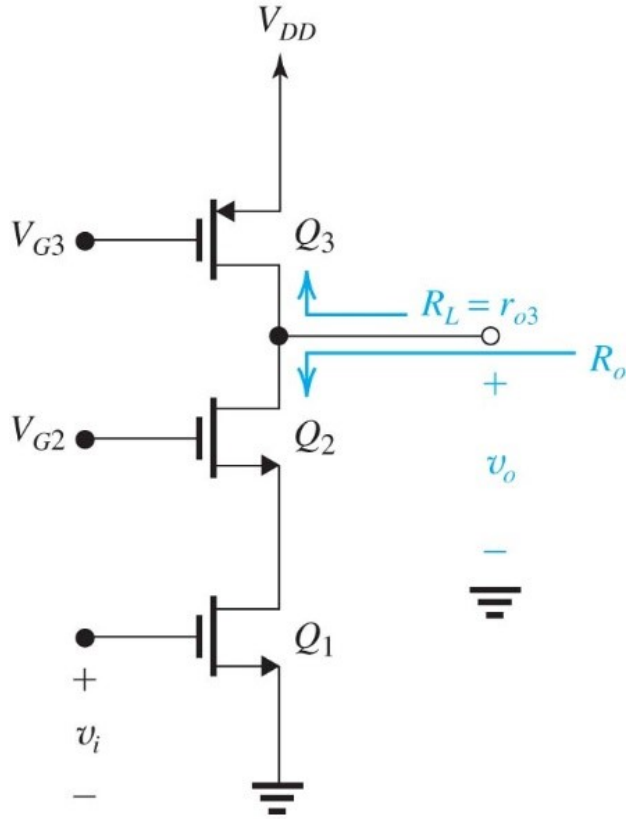
$$A_v \approx g_{m1}(g_{m2}r_{o2})r_{o1}$$

- Real active load
  - Implemented with a PMOS w/ output resistance
  - Gain lowered approximately to intrinsic gain

$$A_v = g_{m1}(R_o||R_L) \approx g_{m1}r_{o3}$$





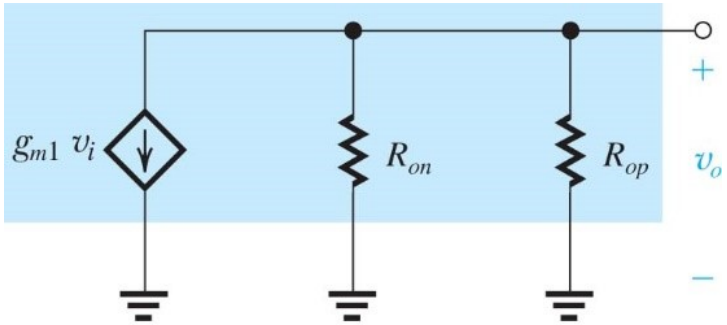


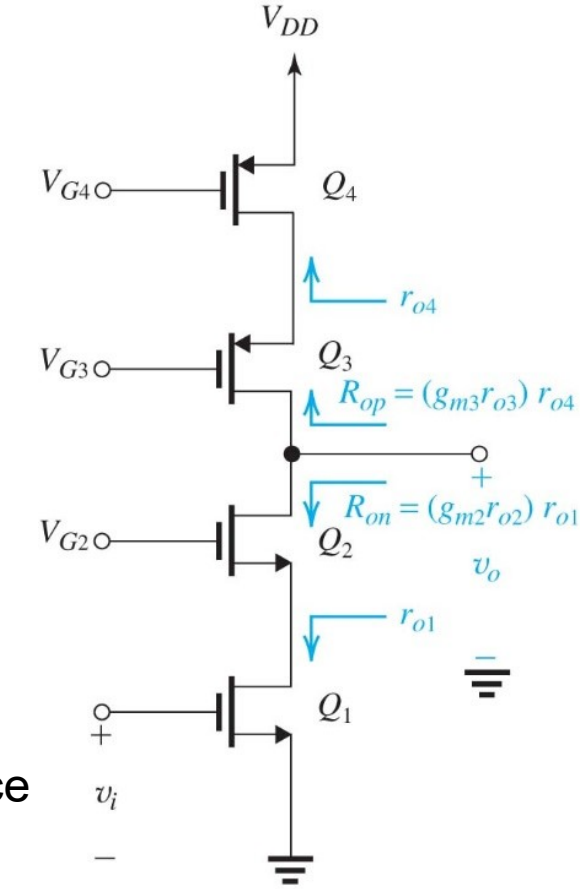
Output resistance ruins the gain boost, but active load improves BW.

Cascode w/ Cascode Active Load

- Problem
  - Output resistance of active load reduces cascode gain
- Solution
  - Cascode the active load to increase its output resistance

$$A_v \approx \frac{g_{m1}(g_{m2}r_{o2})r_{o1}}{2}$$

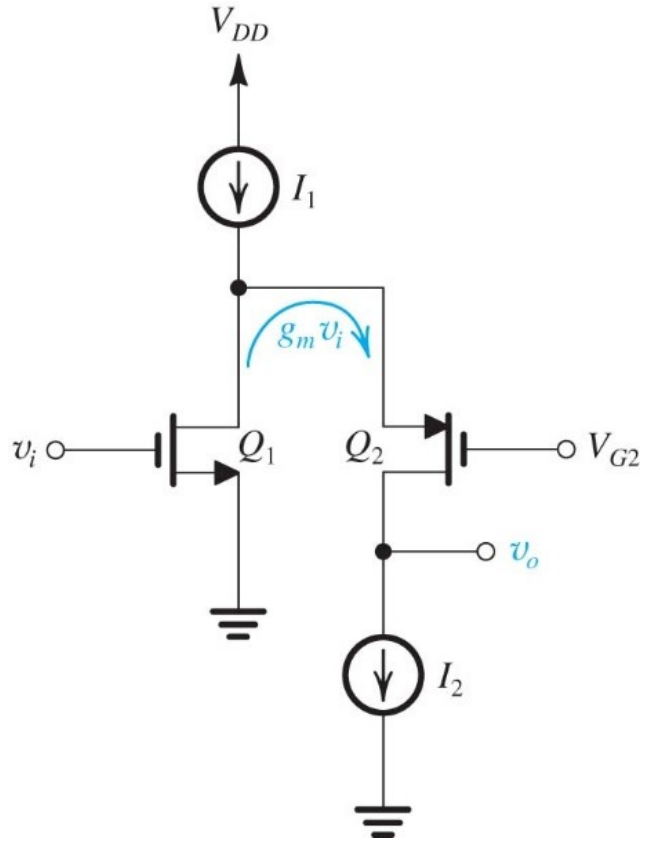




- Problems remain
  - Current source resistance higher, but still similar to cascode output resistance
  - Very high supply voltage required (four stacked saturation conditions)

Folded, Instead of Telescopic, Cascode

- CS gain NMOS input stage
- CG current buffer PMOS output stage

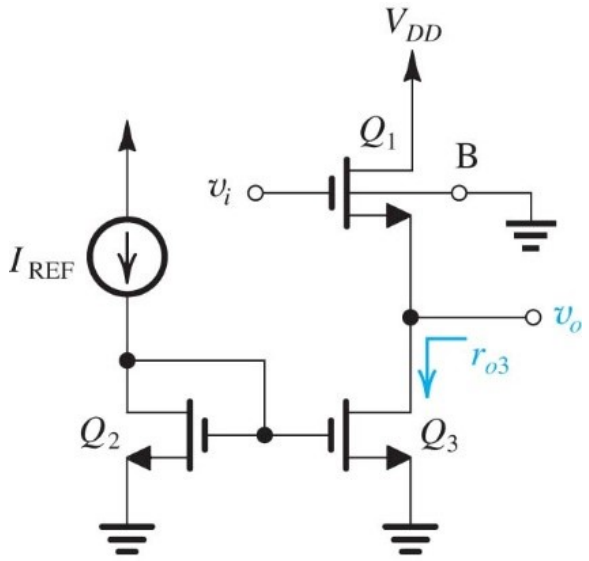


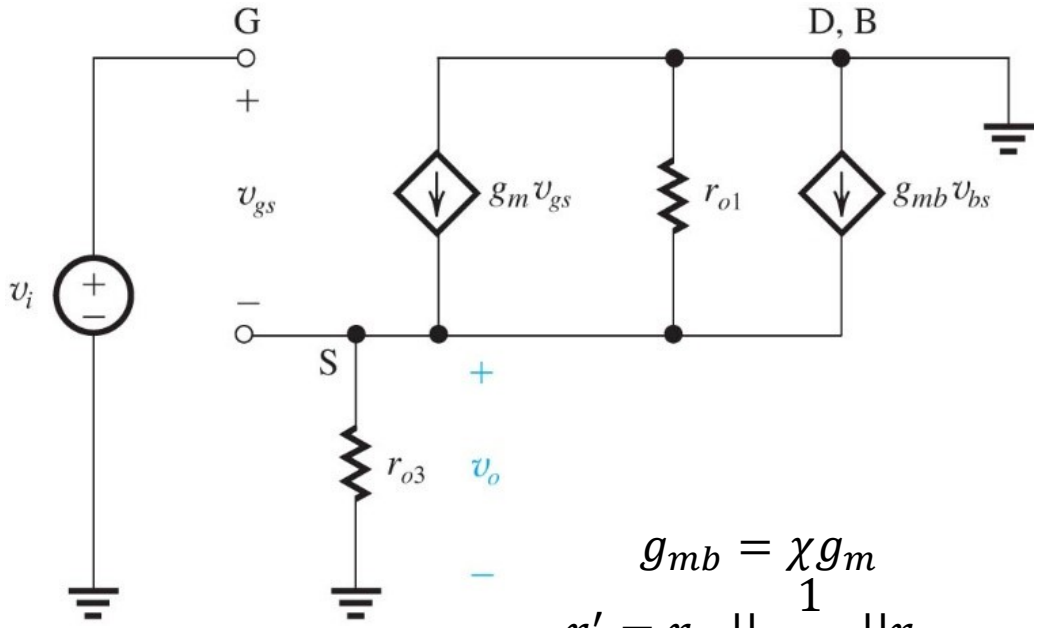
Popular CMOS stage that limits the required dive voltage.

CD w/ Output Resistance

- CD is useful as input stage
  - High input impedance
  - Output resistance and body effect shunt to ground

- $R_i = \frac{v_i}{i_i} = \infty$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = \frac{1}{g_m} || r_{o1} || \frac{1}{g_{mb}} || r_{o3} \approx \frac{1}{g_m(1+\chi)}$
- $A_{vo} = \frac{r_o'}{r_o' + \frac{1}{g_m}} \approx \frac{1}{1+\chi}$
- $A_v = \frac{r_o' || R_L}{r_o' || R_L + \frac{1}{g_m}}$





$$g_{mb} = \chi g_m$$

$$r_o' = r_{o1} || \frac{1}{g_{mb}} || r_{o3}$$

$$\frac{1}{g_m} \ll r_{o1}, r_{o3}$$

Body effect limits the gain, in proportion relative to gate strength.