F7 – Transistor Amplifiers

Outline

- Transfer characteristics and biasing
- Small signal operation and models
- Basic configurations
  - Common source (CS)
  - CS/CE w/ source/ emitter degeneration resistance
  - Common gate (CG)
  - Common drain (CD or source follower)
- Transistor + biasing = amplifier

Reading Guide *Sedra/Smith 7ed int*

- Chapter 6.1-6.3
- (Chapter 6.4-6.5)

Problems *Sedra/Smith 7ed int*

- P6.5, 6.13, 6.27, 6.48, 6.61

CATCH UP AFTER LAST WEEK'S FIRE DRILL

- Check final F6 slides from last week…

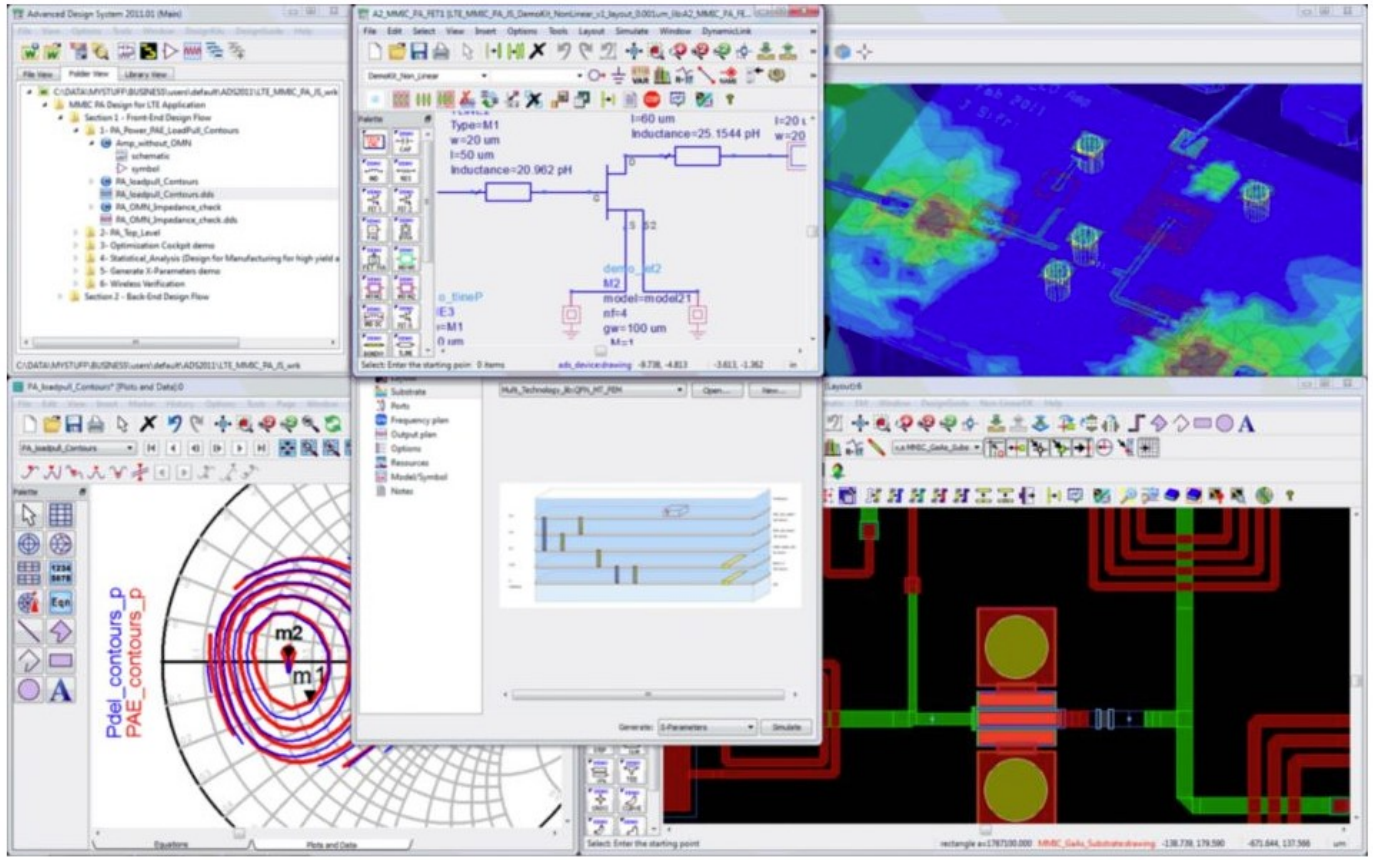
SIMULATION PROJECT STARTS TOMORROW

- Prepare
  - Join a simulation project group on LU Canvas > Modern Electronics > People (2 students per group)
  - Read the project instructions beforehand, if possible
- Project introduction (2x 4 hours with supervisor Stefan Andric)
  - “ADS start-up assistance”
  - Project workspace and import of pre-defined component library
    - Focus on making the basic simulation setup
    - Think about the device or circuit theory later
- Independent project work and report (~24 h, perhaps less) + supervision (4x 2 hours with supervisor)
  - Independent work in computer lab room required
  - Supervisor available only at scheduled times
- Debriefing and report hand-in (yields total 1.5 hp ~ 1 week of work ~ 40 hours)
  - Simulation project debriefing by supervisor on October 10 at 8:15-10 in E:2311
  - Project report handed in through LU Canvas by midnight on October 14
  - Only one (1) single report correction allowed, make sure to amend all comments

Keysight ADS – Electronic Design Automation (EDA) Software

- ADS provides a holistic suite of EDA tools
  - Technology setup
  - Schematic, layout, user-defined models
  - Verilog-A hardware models
  - EM simulations (planar or 3D)
  - DRC (design rule checking)
  - AEL (application extension language)
  - …

- Keysight ADS is used by professionals in RFIC, MMIC, and millimetre wave design
  - Silicon PDKs include:
    Samsung, ST Microelectronics, TSMC, …
  - III-V PDKs include:
    Northrop Grumman, OMMIC, UMS, …



https://www.keysight.com/en/pc-1297113/advanced-design-system-ads

PDK = process design kit

npn-BJT Modes of Operation (F3 recap)

- BJT cutoff
  - Not interesting for basic amplifier operation
- BJT saturation
  - Not interesting for basic amplifier operation
- BJT active (EB forward, CB reverse)

$$i_C = i_E - i_B = I_S \exp\left(\frac{v_{BE}}{V_T}\right)\left(1 + \frac{v_{CE}}{V_A}\right) = i'_C\left(1 + \frac{v_{CE}}{V_A}\right)$$

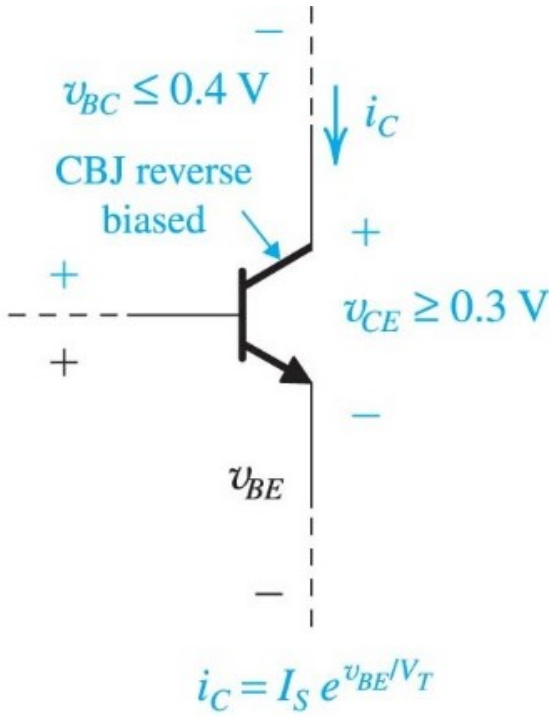
$$i_B = \frac{i_C}{\beta} = \frac{1-\alpha}{\alpha} i_C$$

$$i_E = \frac{i_C}{\alpha} = \frac{1+\beta}{\beta} i_C$$

$$v_{CE} = v_{BE} - v_{BC} \geq 0.3\ \text{V}$$

$$v_{BC} = v_{CE} - v_{BE} \leq 0.4\ \text{V}$$

$$v_{BE} \approx 0.7\ \text{V}$$



Active mode is used in a BJT amplifier.

n-MOSFET Modes of Operation (F4-5 recap)

- MOSFET cutoff(/ weak inversion)
  - Not interesting for basic amplifier operation
- MOSFET triode(/ linear)
  - Not interesting for basic amplifier operation
- MOSFET saturation(/ active)

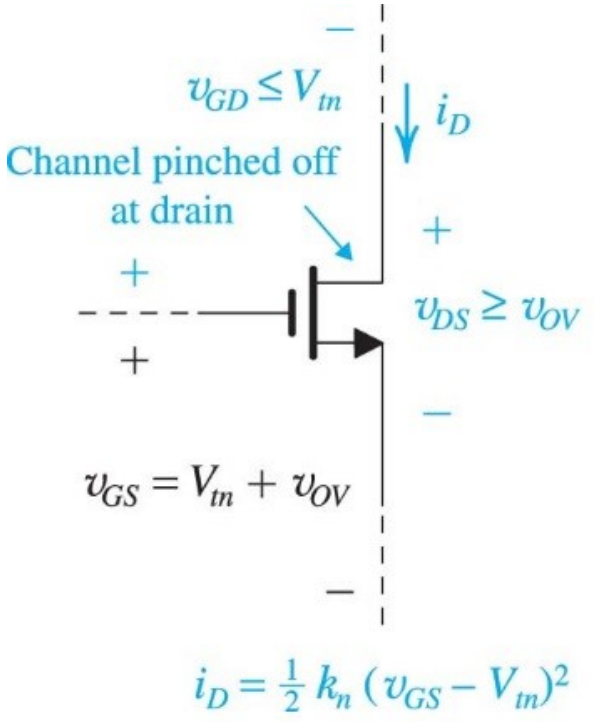
$$i_D = i_S - i_G = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2(1 + \lambda v_{DS}) = i_D'(1 + \lambda v_{DS})$$

$$i_G = 0$$

$$i_S = i_D$$

$$0 < v_{OV} = v_{GS} - V_{tn} = V_{DSsat}$$

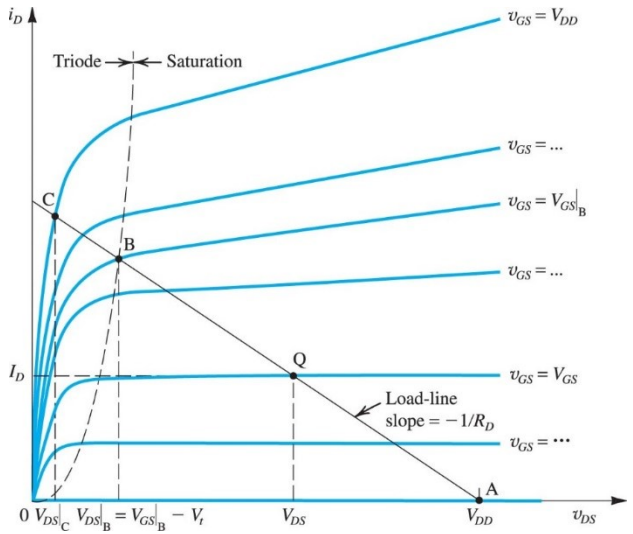
$$v_{DS} > V_{DSsat}$$



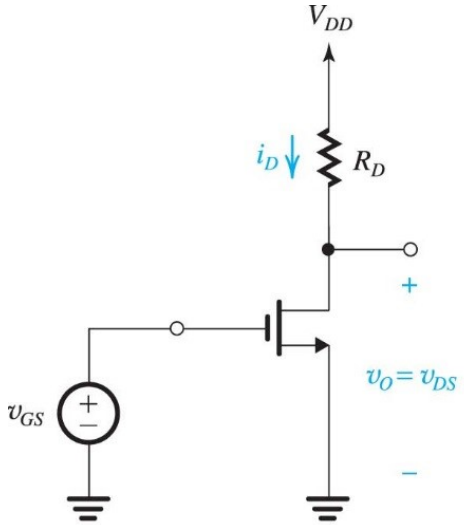
Saturation mode is used in a MOSFET amplifier, sometimes (cf. BJT) called active mode.

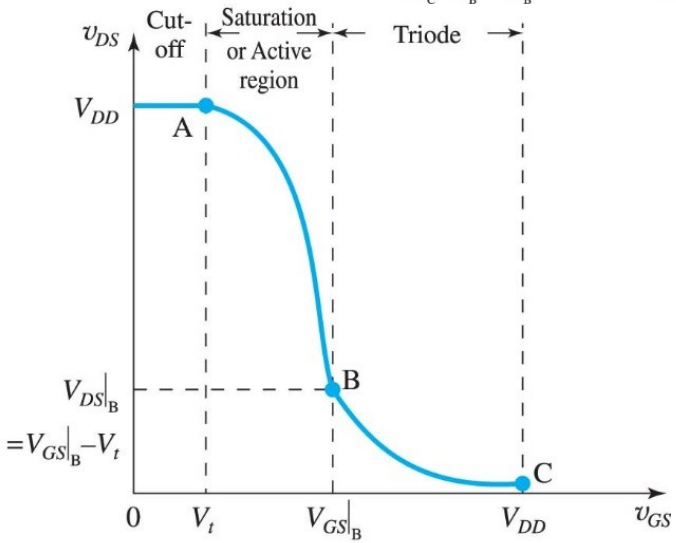
Voltage Transfer Characteristics (VTC) – Discrete Transistor

- MOSFET and BJT on a load line
  - Non-linear characteristics

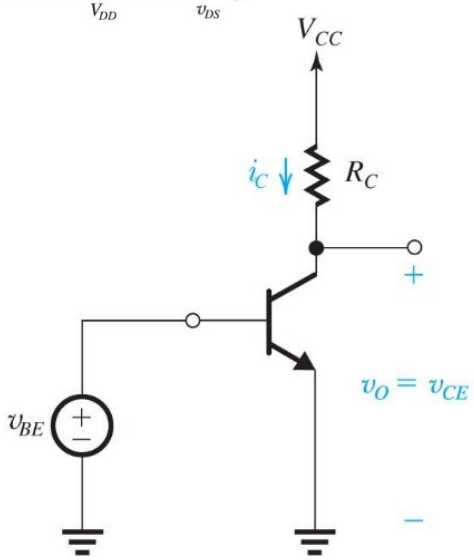


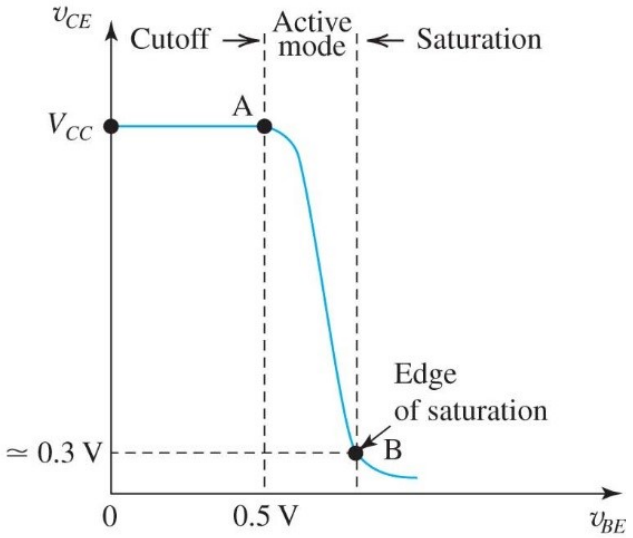
$$v_{DS} = V_{DD} - R_D i_D$$





$$v_{BE} = V_{CC} - R_C i_C$$

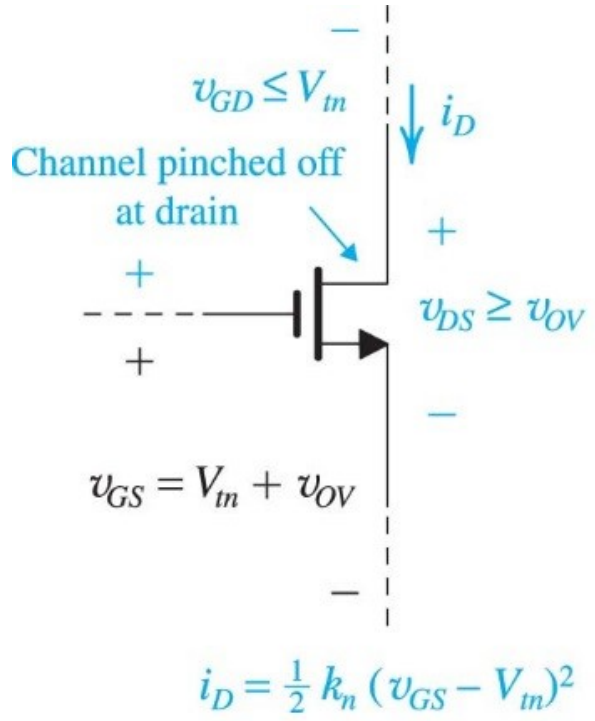


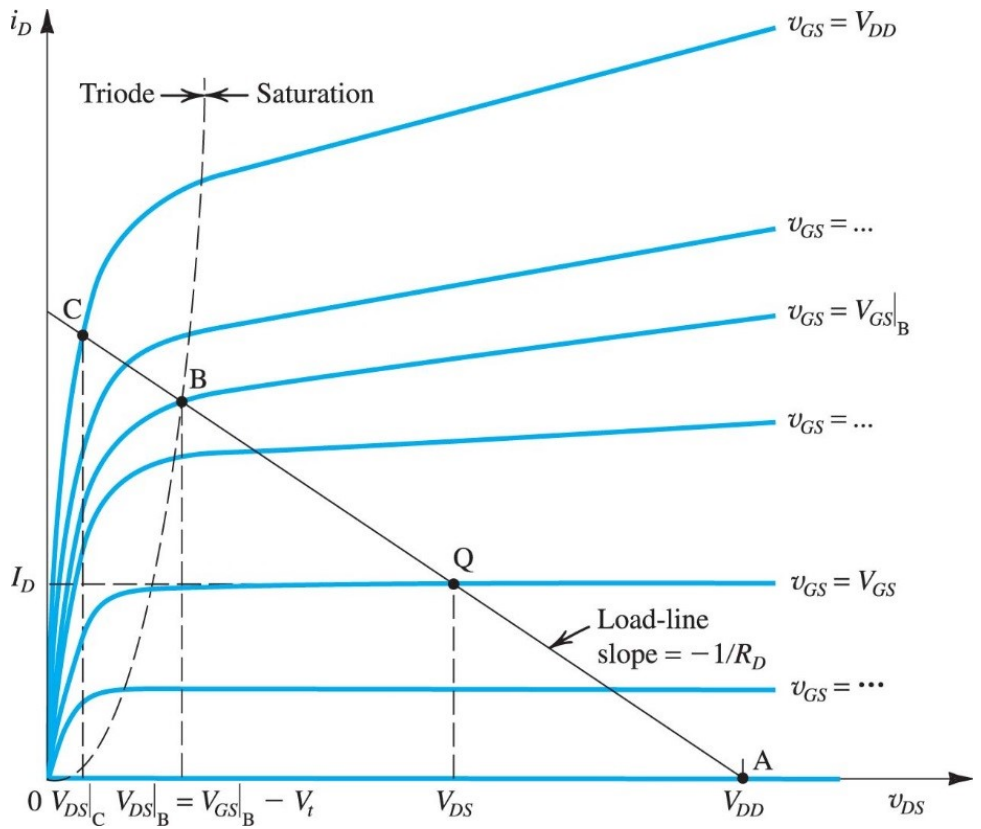


Quiescent (Bias) Point Selection – Discrete Transistor

- MOSFET saturation(/ BJT active) region
  - Voltage controlled current source

- Resistor load line limits selection of quiescent point, Q, and the allowed signal swing



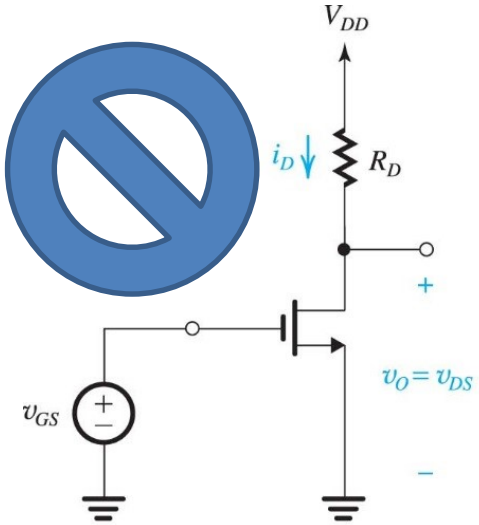


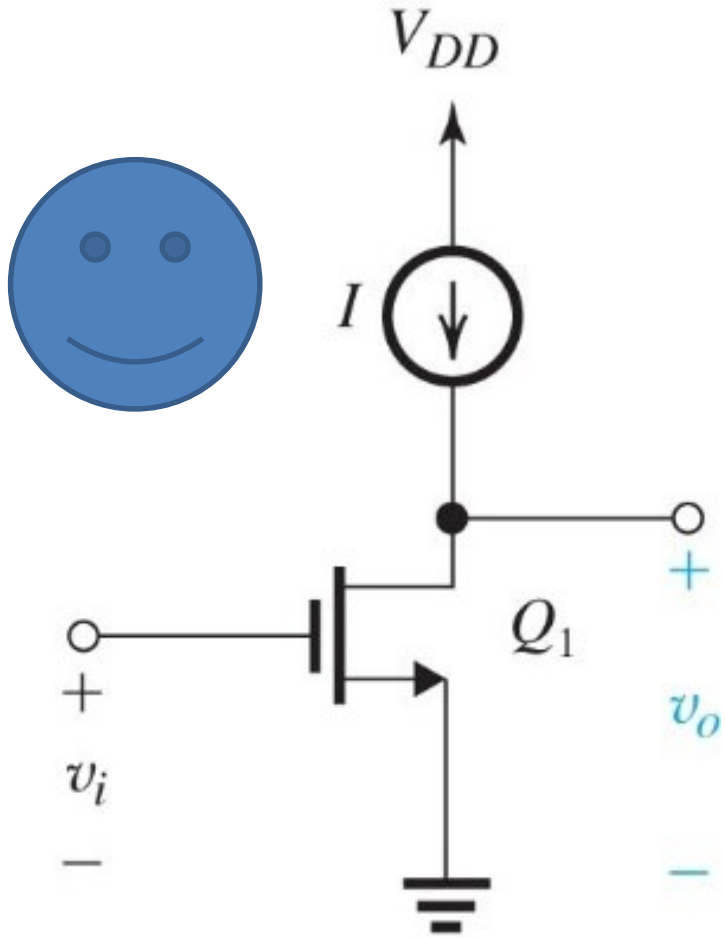
Quiescent point yields from device technology and circuit design specification.

Quiescent (Bias) Point Selection – Integrated Transistor

- MOSFET saturation(/ BJT active) region
  - Voltage controlled current source

- Use another MOSFET as an active load
  - Output conductance (better with long gate)
  - Knee voltage (operate in saturation region)
  - Breakdown (limit bias voltage and signal swing)

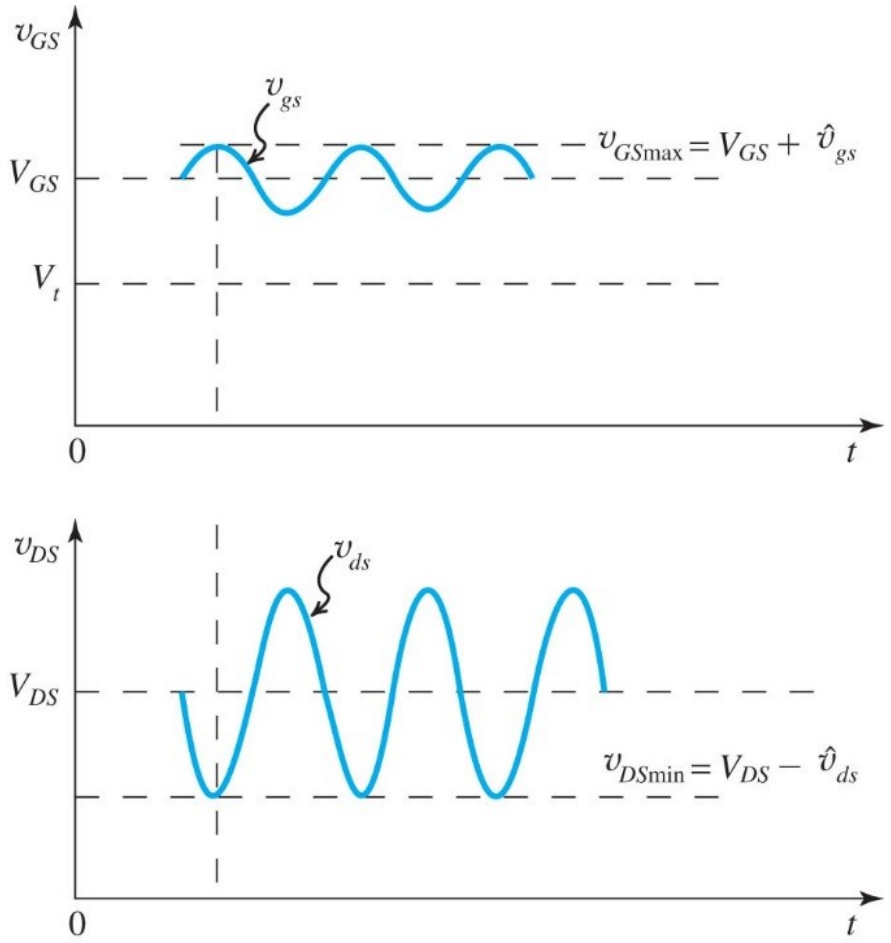




We focus on integrated technology, using active current sources for biasing.

Quiescent (Bias) and Signal Notations

- Quiescent (bias) voltages, V_{GS}, V_{DS}, and currents, I_G, I_D, I_S
  - Set the quiescent (no signal) conditions of the circuit
- Signal voltages, v_{gs}, v_{ds}, and currents, i_g, i_d, i_s
  - Describe variations about the quiescent conditions
- Total operation voltages, $v_{GS} = V_{GS} + v_{gs}$, $v_{DS} = V_{DS} + v_{ds}$, and currents, $i_G = I_G + i_g$, $i_D = I_D + i_d$, $i_S = I_S + i_s$
  - Superposition of the bias and signal components
- (BJT? Same principle, different terminal names.)



Notation is case sensitive in signal parameter and terminal subscript.

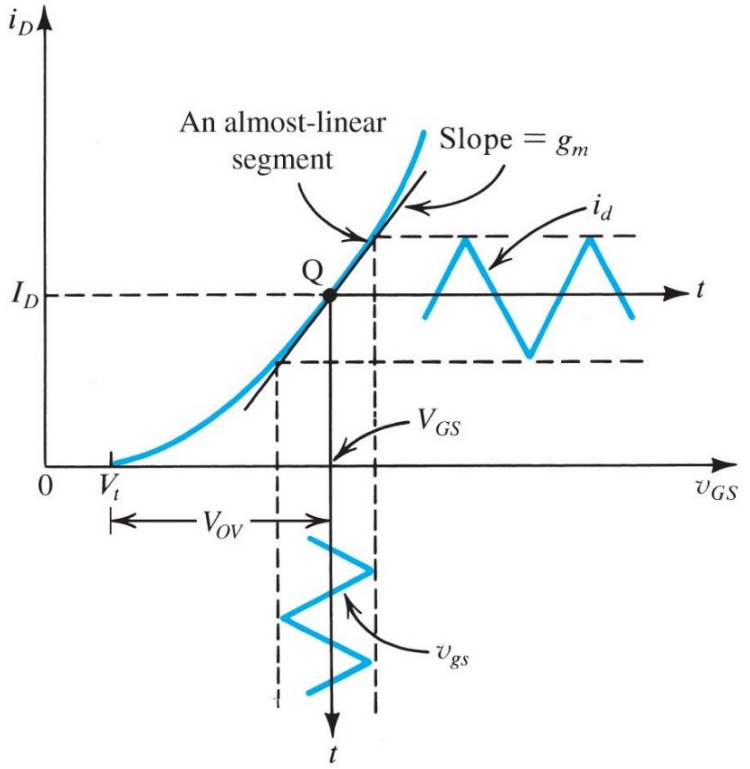
Small Signal Approximation (Linearization)

- Large signals require iterative solution of non-linear transistor (MOSFET or BJT) current-voltage equations

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2(1 + \lambda v_{DS}) \qquad i_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right)\left(1 + \frac{v_{CE}}{V_A}\right)$$

- Operation with small signals about quiescent point
  - Approximately linear range (cf. Taylor series)

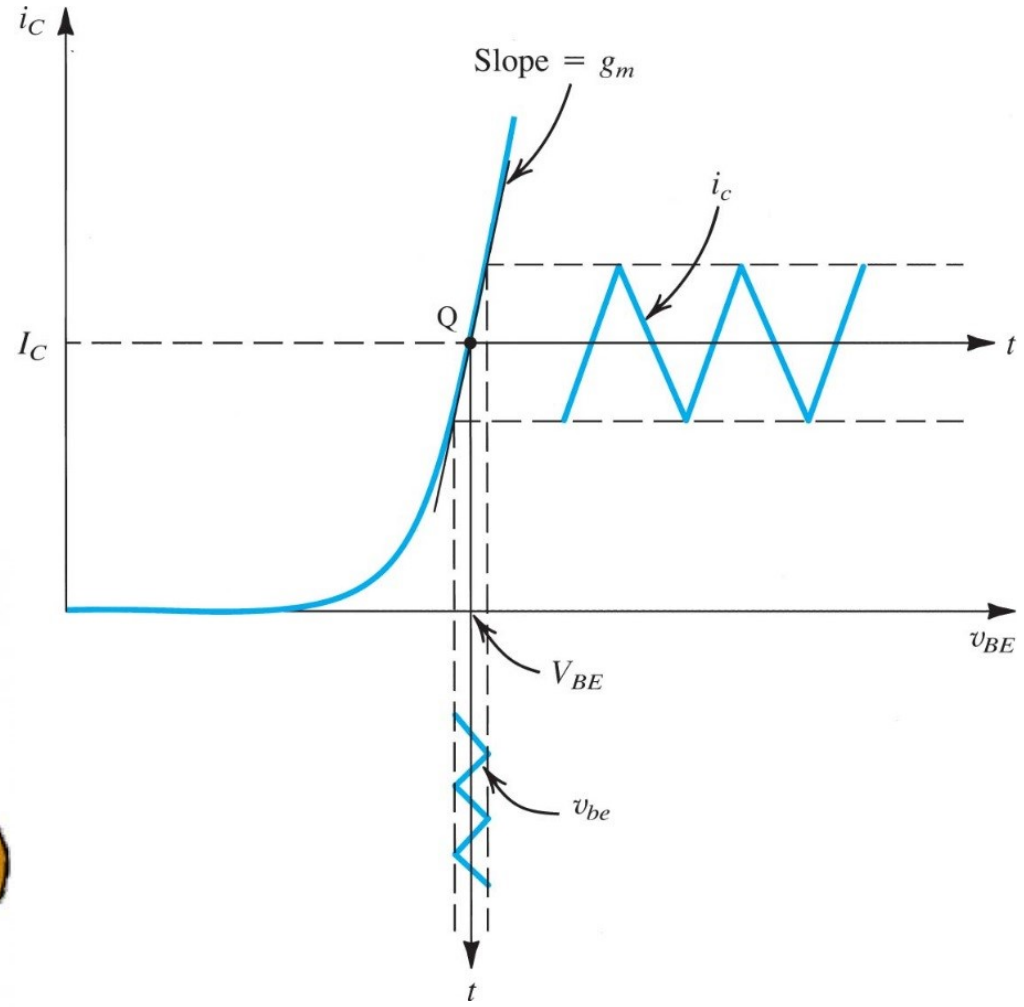
$$f(X + x) = \sum_{n=0}^{\infty} \frac{f^{(n)}(X)}{n!}(x - X)^n \approx f(X) + \frac{f'(X)}{1}(x - X)^1$$

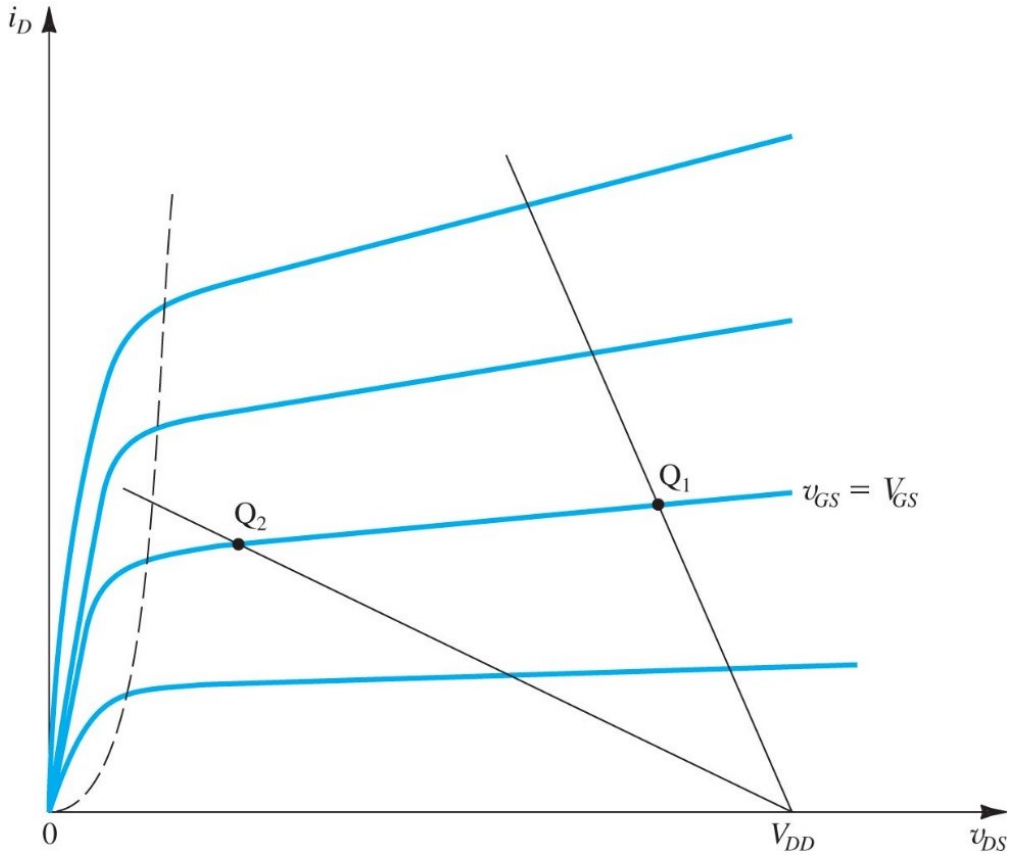


- Small signal parameters at Q-point
  - Input resistance, $R_i = \frac{\partial v_I}{\partial i_I} = \frac{\partial(V_I + v_i)}{\partial(I_I + i_i)} = \frac{v_i}{i_i}$
  - Transconductance, $g_m = \frac{\partial v_O}{\partial i_I} = \frac{\partial(V_O + v_o)}{\partial(I_I + i_i)} = \frac{v_o}{i_i}$, or current gain, $\beta = \frac{\partial i_O}{\partial i_I} = \frac{\partial(I_O + i_o)}{\partial(I_I + i_i)} = \frac{i_o}{i_i}$
  - Output resistance, $R_o = \frac{\partial v_O}{\partial i_O} = \frac{\partial(V_O + v_o)}{\partial(I_O + i_o)} = \frac{v_o}{i_o}$

Physical origins of the MOSFET and BJT current-voltage characteristics were discussed earlier.

Which effects limit the allowed signal range at Q?





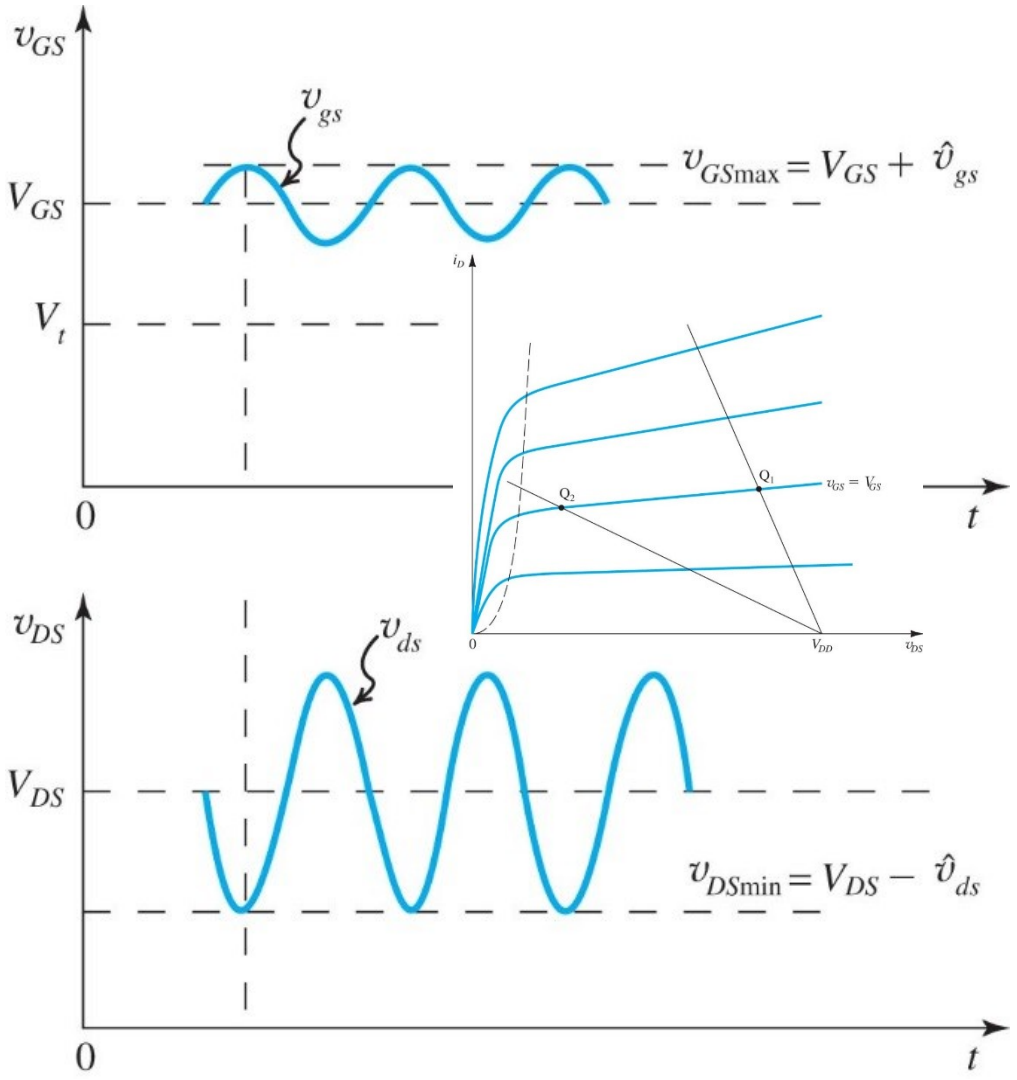
Input and Output Signal Range

- MOSFET only linear for very small signals
- MOSFET must stay in saturation mode on load line
- MOSFET breakdown effects at high voltages
- Input voltage above threshold, but allow saturation

$$v_{GSmin} > V_{tn}$$
$$v_{GSmax} < V_{DD} - v_{DSmin}$$

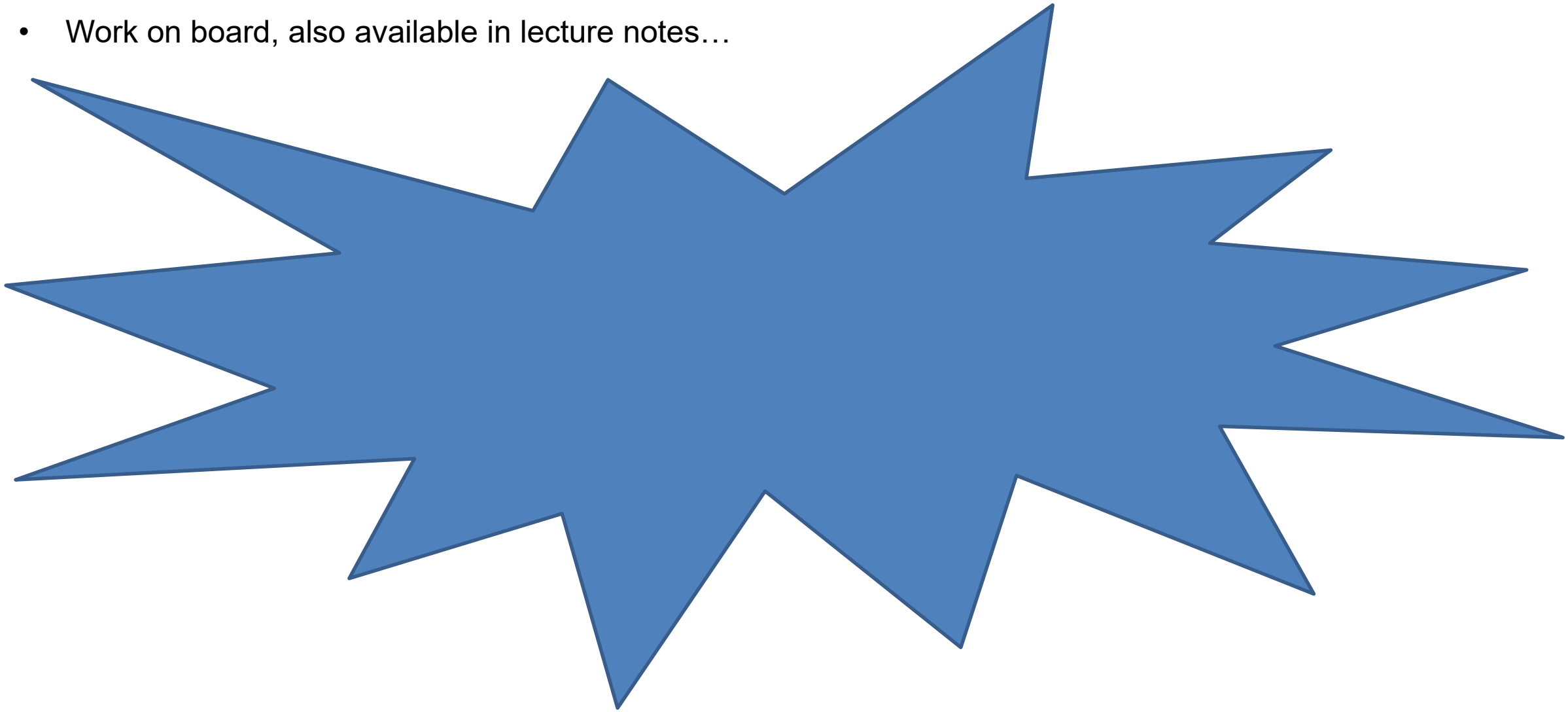
- Output voltage above overdrive, but allow saturation

$$v_{GSmax} - V_{tn} < v_{DSmin} < V_{DD}$$



MOSFET as Small Signal Amplifier – Linearization Applied

- Work on board, also available in lecture notes…



MOSFET as Small Signal Amplifier – Linearization Applied

- Transconductance, $g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q$
  - Slope of (voltage-current) transfer characteristics at Q-point

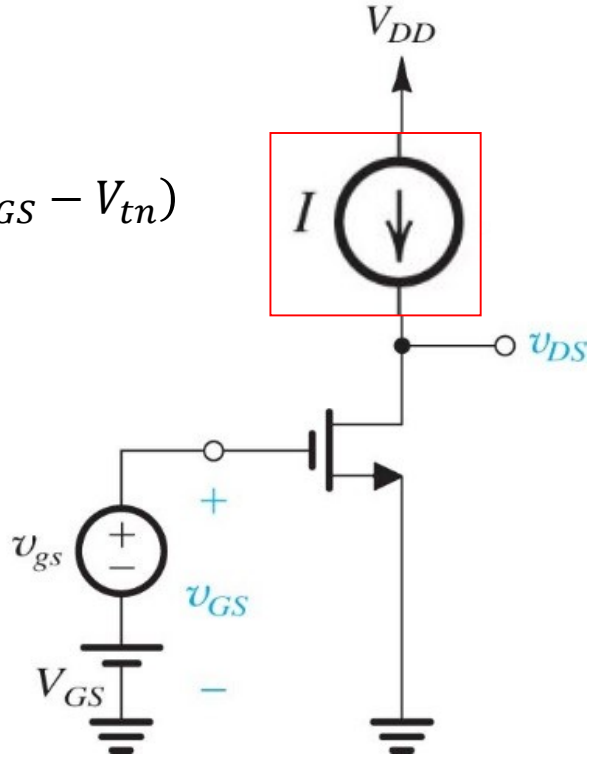
$$i_D(V_{GS} + v_{gs}) = \cdots = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left[V_{OV}^2 + 2V_{OV}v_{gs} + v_{gs}^2\right](1 + \lambda v_{DS})$$

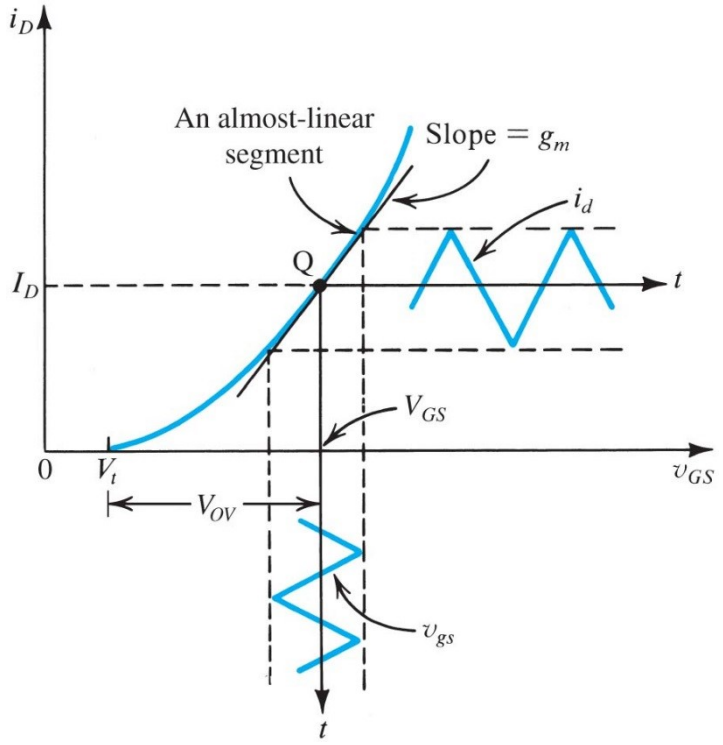
- Linear term must dominate high order term(s)

$$v_{gs} \ll 2V_{OV} = 2(V_{GS} - V_{tn})$$

- Voltage gain, $A_v = \left.\frac{\partial v_{DS}}{\partial v_{GS}}\right|_Q = \left.\frac{\partial v_{DS}}{\partial i_D}\right|_Q \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q$
  - Slope of VTC at Q-point
  - Load resistance converts current to voltage

$$v_{DS} = V_{DD} - R_D i_D(v_{GS}, v_{DS})$$





Linearization of polynomial.

MOSFET Hybrid Pi Model (recap)

- Gate resistance

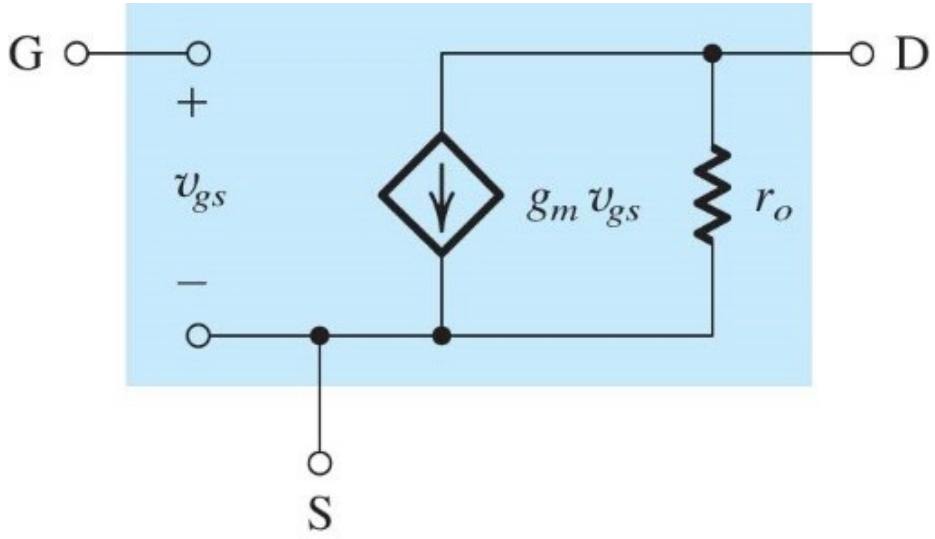
$$r_g = \frac{v_{gs}}{i_g} = \infty$$

- Transconductance

$$g_m = \frac{i_d}{v_{gs}} = k_n' \left(\frac{W}{L}\right) V_{OV} = \sqrt{2k_n' \left(\frac{W}{L}\right) I_D} = \frac{2I_D}{V_{OV}}$$

- Output resistance

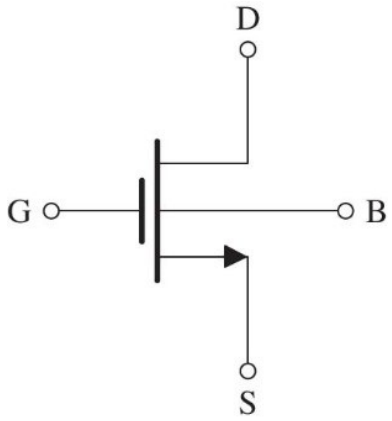
$$r_o = \frac{v_{ds}}{i_d} = \frac{1}{\lambda I_D'} = \frac{L}{\lambda' I_D'} = \frac{V_A' L}{I_D'} = \frac{V_A}{I_D'}$$

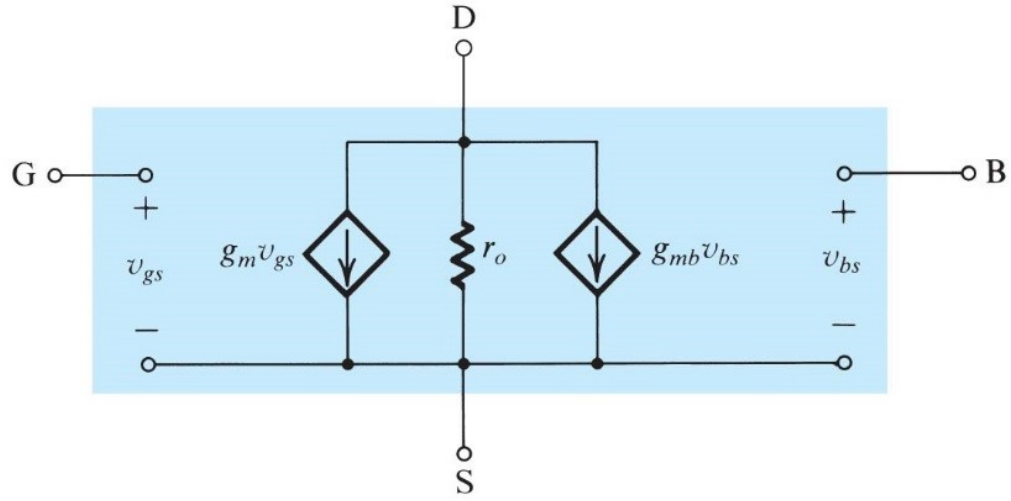


Physical origins of the MOSFET and BJT hybrid pi small signal models were discussed earlier.

MOSFET Body Effect

- Substrate well devices have a parasitic body transistor
  - Body effect can be circumvented by connection of body to source
  - Body effect can be used to fine-tune MOSFET performance
  - Body effect is not available in gate-all-around technologies





Body effect is often small and is typically bypassed, or overlooked, unless specifically noted.

BJT as Small Signal Amplifier – Linearization Applied

- Transconductance, $g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q$
  - Slope of (voltage-current) transfer characteristics at Q-point

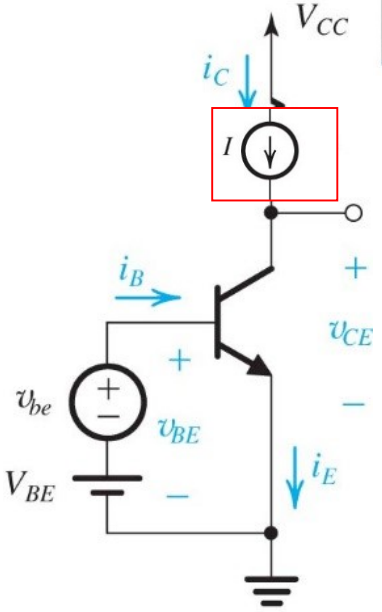
$$i_C(V_{BE} + v_{be}) = \cdots = I_C(V_{BE})\left(1 + \frac{v_{be}}{V_T} + \frac{v_{be}^2}{2V_T^2} + \frac{v_{be}^3}{6V_T^3} + \cdots\right)$$

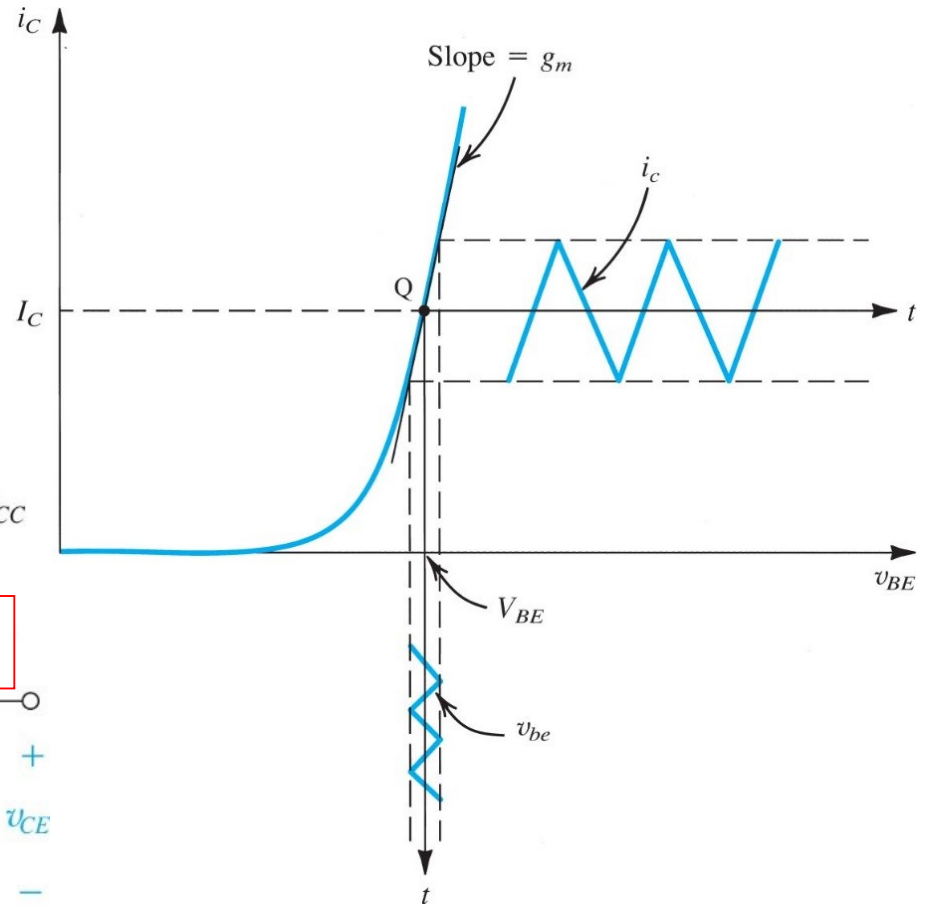
- Linear term must dominate high order term(s)

$$v_{be} \ll 2V_T$$

- Voltage gain, $A_v = \left.\frac{\partial v_{CE}}{\partial v_{BE}}\right|_Q = \left.\frac{\partial v_{CE}}{\partial i_C}\right|_Q \left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q$
  - Slope of VTC at Q-point
  - Load resistance converts current to voltage

$$v_{CE} = V_{CC} - R_C i_C(v_{BE}, v_{CE})$$





Linearization of exponential by reduced Taylor series.

BJT Hybrid Pi Model (recap)

- Base resistance

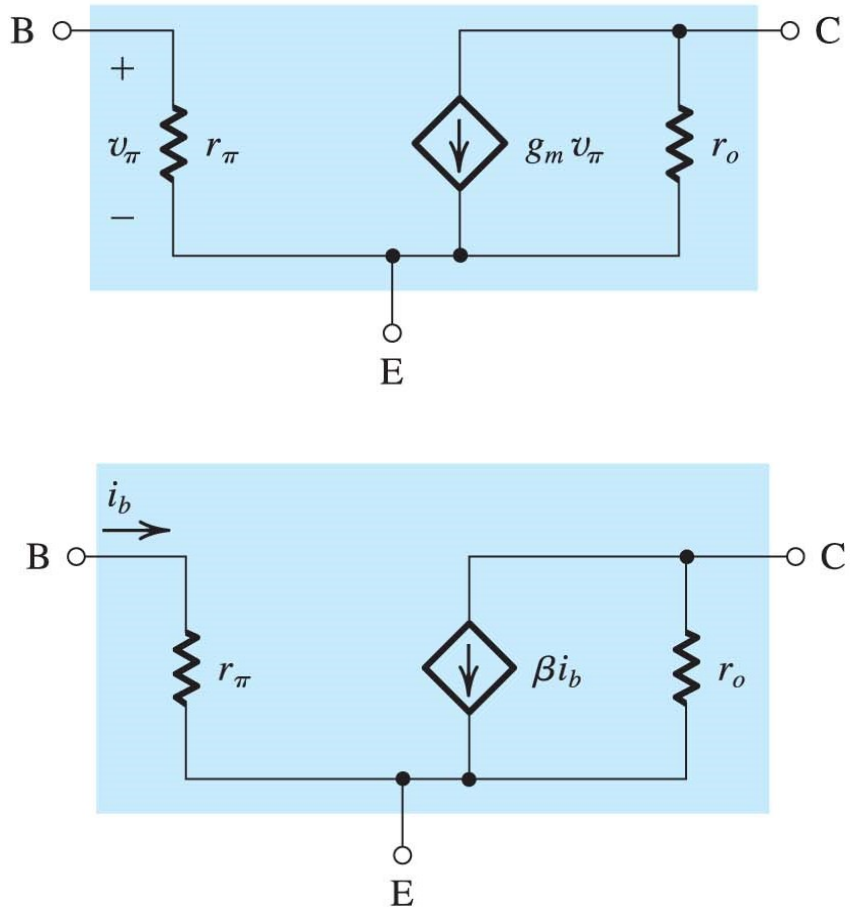
$$r_\pi = \left.\frac{v_{be}}{i_b}\right|_{v_{ce}=0} = \frac{I_C}{V_T} = \frac{\beta}{g_m}$$

- Transconductance or current gain

$$g_m = \left.\frac{i_c}{v_{be}}\right|_{v_{ce}=0} = \frac{V_T}{I_B} = \frac{\beta}{r_\pi} \Leftrightarrow \beta = \left.\frac{i_c}{i_b}\right|_{v_{ce}=0} = g_m r_\pi$$

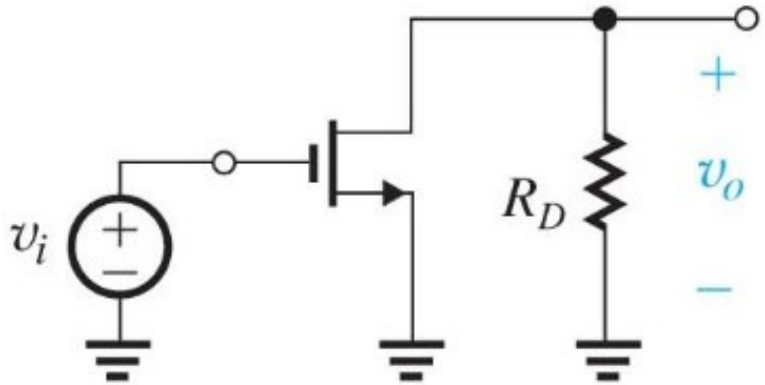
- Output resistance

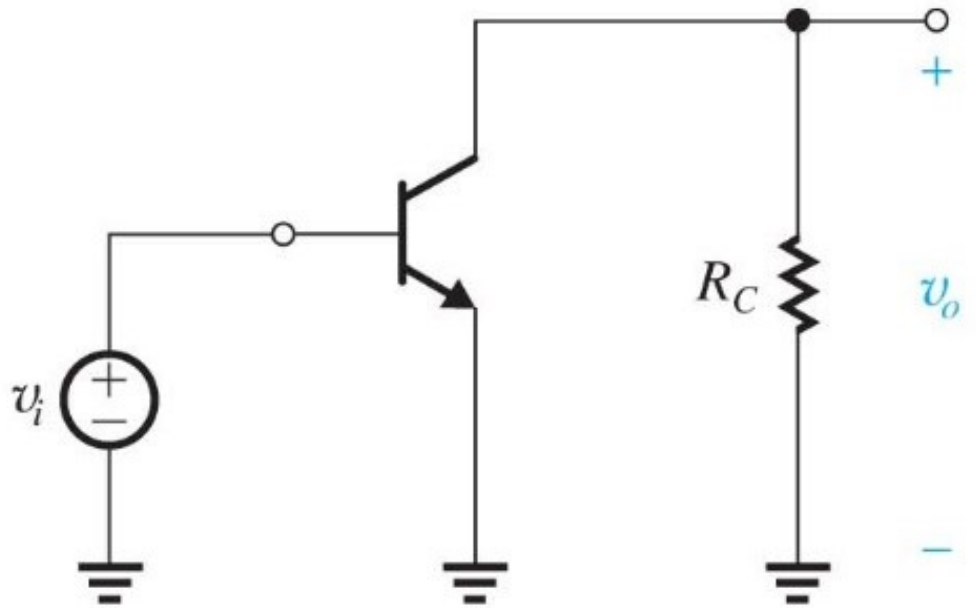
$$r_o = \left.\frac{v_{ce}}{i_c}\right|_{v_{be}=v_\pi=0} = \frac{V_A}{I_C'}$$



Physical origins of the MOSFET and BJT hybrid pi small signal models were discussed earlier.

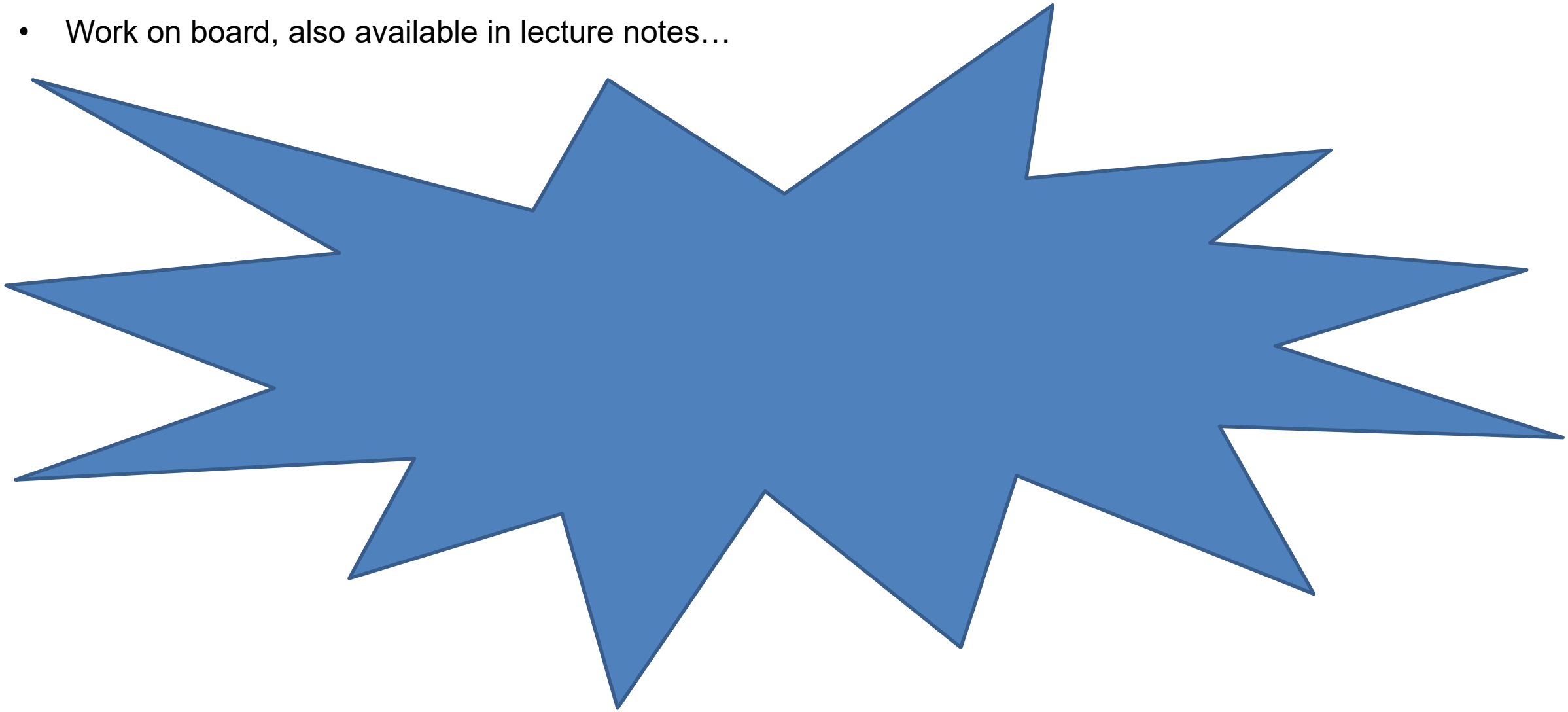
BJT vs n/p-MOSFET, what is the difference from a circuit perspective?





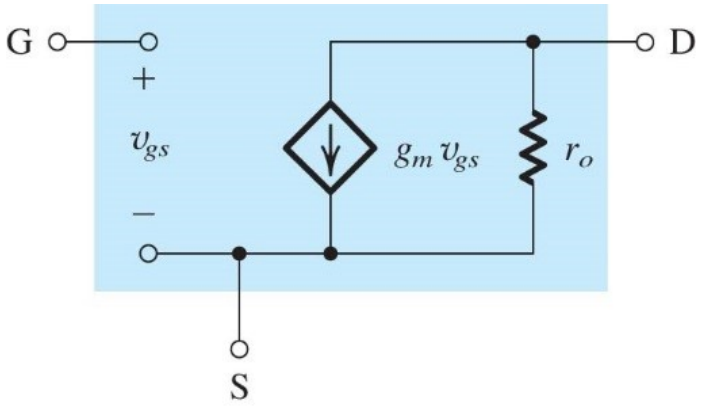
MOSFET T-Model

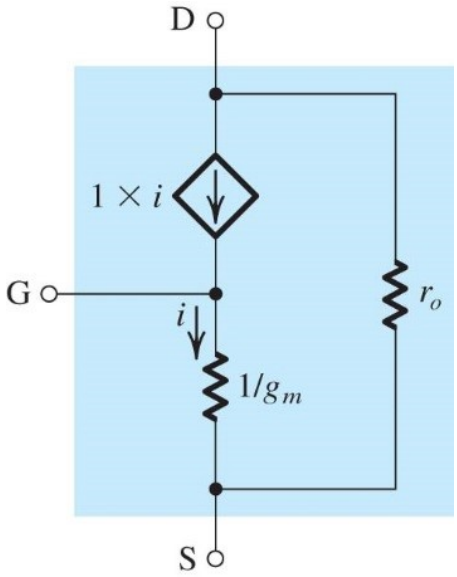
- Work on board, also available in lecture notes…



MOSFET T-Model

- A useful transformation of the hybrid pi model…
  - Equivalent terminal characteristics as compared to hybrid pi
  - Simplifies circuit analysis if component in the source lead





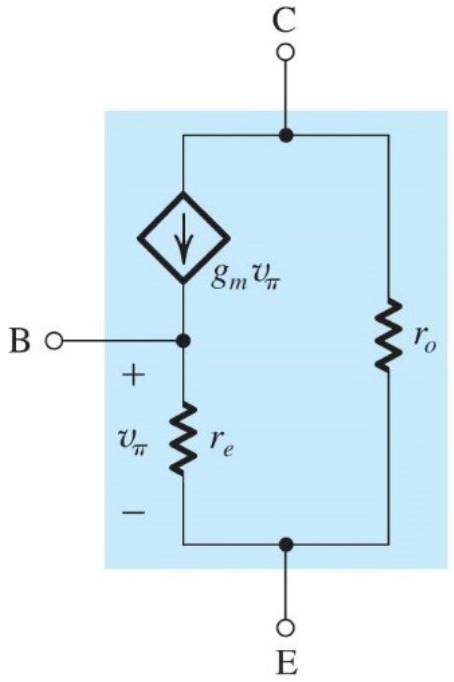
T-model is electrically equivalent to hybrid pi model, but they are useful under different circumstances.

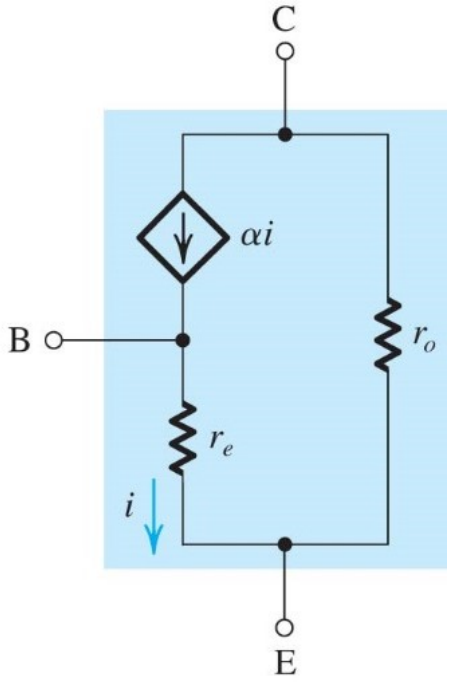
BJT T-Model

- A useful transformation of the hybrid pi model…
  - Equivalent terminal characteristics as compared to hybrid pi
  - Simplifies circuit analysis if component in the emitter lead

$$I_C = \beta I_B = \frac{\beta}{\beta+1} I_E = \alpha I_E$$

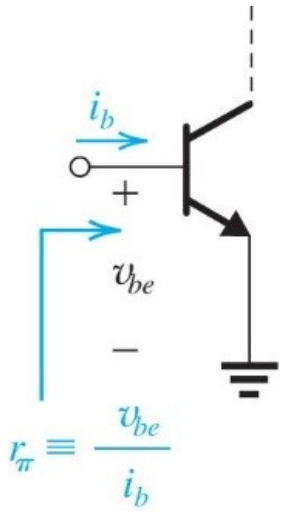
$$r_e = \left.\frac{v_{be}}{i_e}\right|_{v_{ce}=0} = \frac{V_T}{I_E} = \frac{r_\pi}{(1+\beta)} = \frac{\alpha}{g_m} \approx \frac{1}{g_m}$$

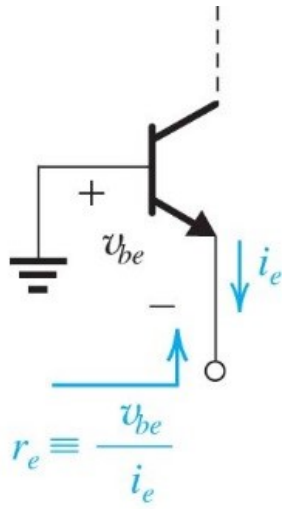


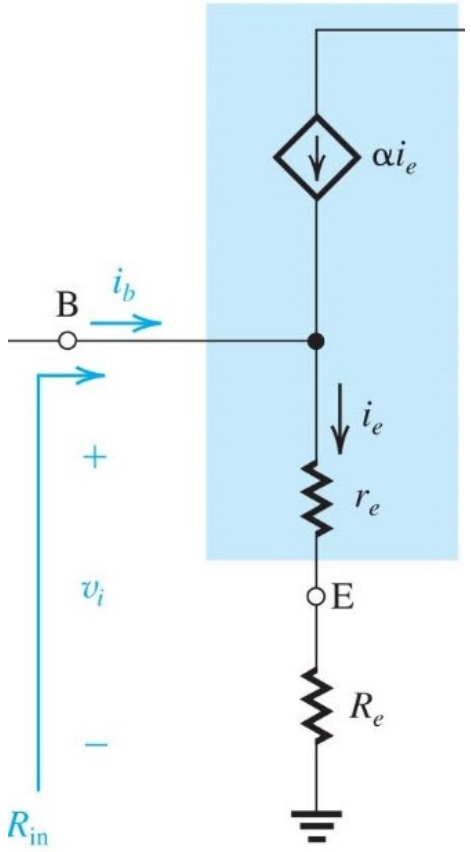


(BJT Resistance Reflection)

- Hybrid pi model
  - Base resistance, r_π
- T model
  - Emitter resistance, $r_e = \frac{\alpha}{g_m} \approx \frac{1}{g_m}$
- Input resistance towards base or emitter, with the other terminal grounded
  - Inversely proportional to terminal current



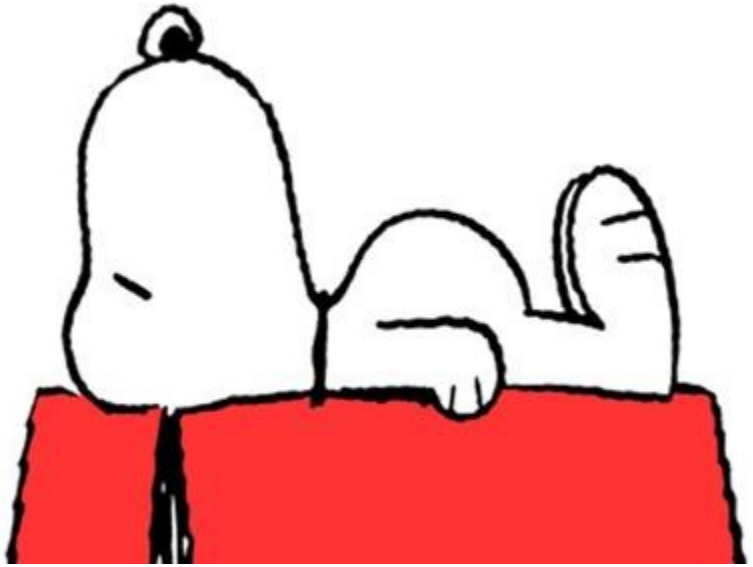




$$i_e = i_b + i_c = (1+\beta)i_b \Rightarrow r_\pi = (1+\beta)r_e$$

The resistance reflection factor yields from conservation of base-emitter voltage and the terminal currents.

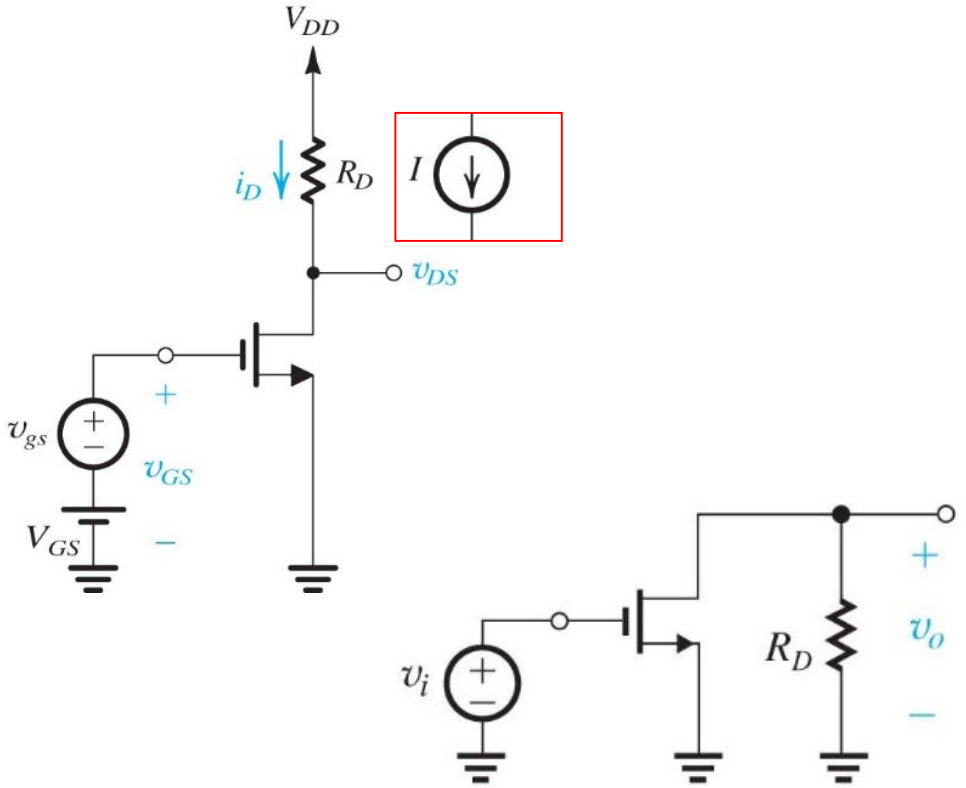
BREAK



Systematic Analysis of Transistor Amplifier Circuits

- Linearization of large signal characteristics
  - Eliminate signal sources;
    $v = \{\text{short circuit}\} = 0$
    $i = \{\text{open circuit}\} = 0$
  - Determine dc operating point of the transistor
  - Calculate parameter values for small signal model

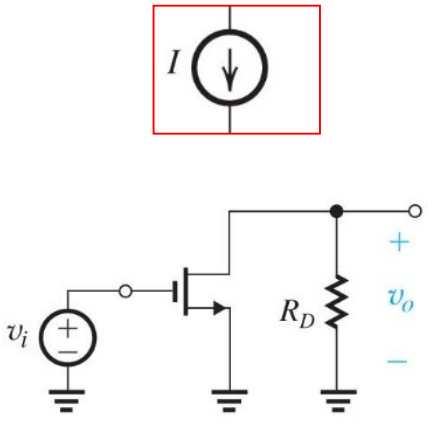
- Linear analysis of small signal characteristics
  - Eliminate dc sources;
    $V = \{\text{short circuit}\} = 0$
    $I = \{\text{open circuit}\} = 0$
  - Replace transistor with small signal model
    - Hybrid pi model: often most useful
    - T model: simplifies analysis if component at source(/ emitter)
  - Analyse the linearized circuit to determine characteristics



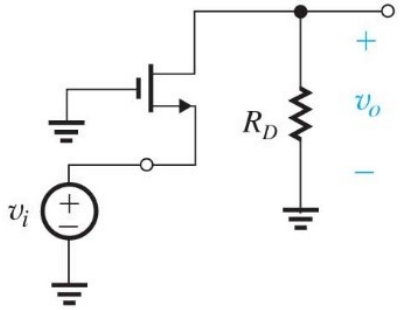
Open circuit eliminates a current, short circuit eliminates a voltage.

Basic Amplifier Configurations

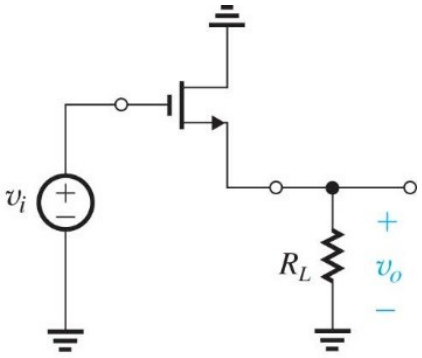
- Amplifier designation scheme
  - Common terminal (ground)
- Input (MOSFET) terminal
  - Gate (CS/CD) or source (CG)
  - Never drain input
- Output (MOSFET) terminal
  - Drain (CS/CG) or source (CD)
  - Never gate output
- BJT vs MOSFET amplifiers
  - BJT has finite input resistance
  - BJT has higher gain
  - BJT has other terminal names



(a) Common Source (CS)



(b) Common Gate (CG)



(c) Common Drain (CD) or Source Follower

INTEGRATEED ACTIVE CURRENT SOURCE (OR BIAS RESISTOR) WITH OUTPUT RESISTANCE IS ESSENTIAL PART OF THE AMPLIFIER STAGE

We focus on MOSFETs in this course, but are aware that similar concepts apply to BJTs.

Characterisation of Voltage Amplifiers

- Input resistance

$$R_i = \frac{v_i}{i_i}$$

- Output resistance

$$R_o = \left.\frac{v_o}{i_o}\right|_{v_{sig}=0}$$

- Open circuit voltage gain (neglect source and load)

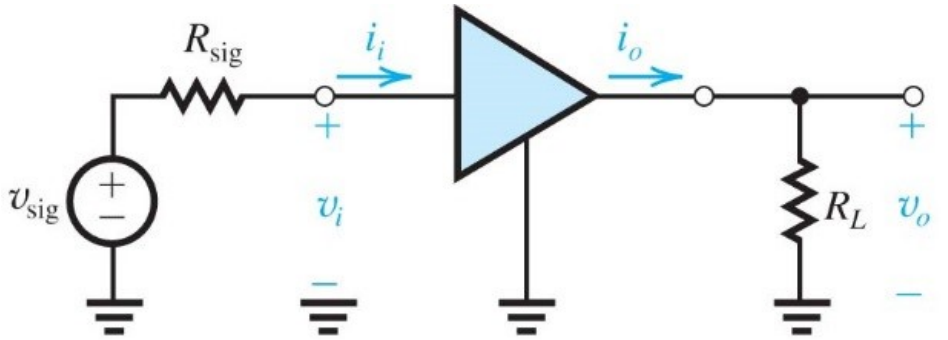
$$A_{vo} = A_v\Big|_{R_L=\infty}$$

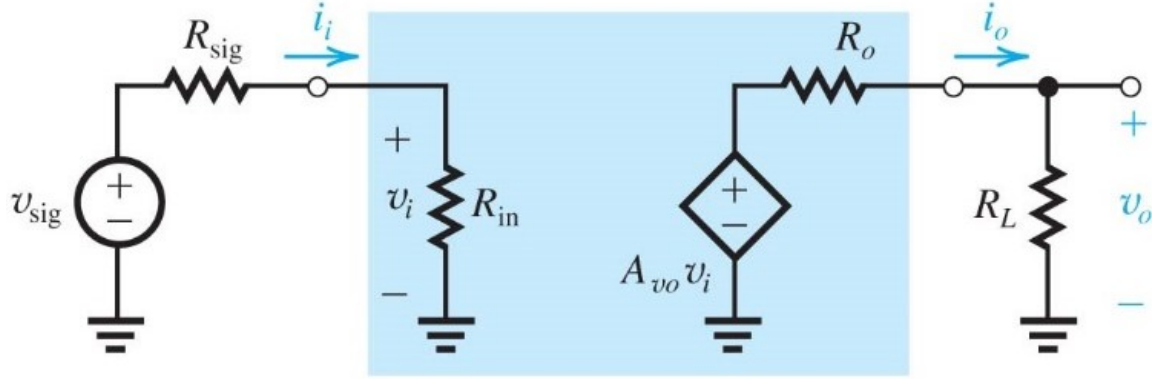
- Voltage gain (neglect source)

$$A_v = \frac{v_o}{v_i} = A_{vo}\frac{R_L}{R_L + R_o}$$

- Overall gain

$$G_v = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} A_{vo} \frac{R_L}{R_L + R_o}$$

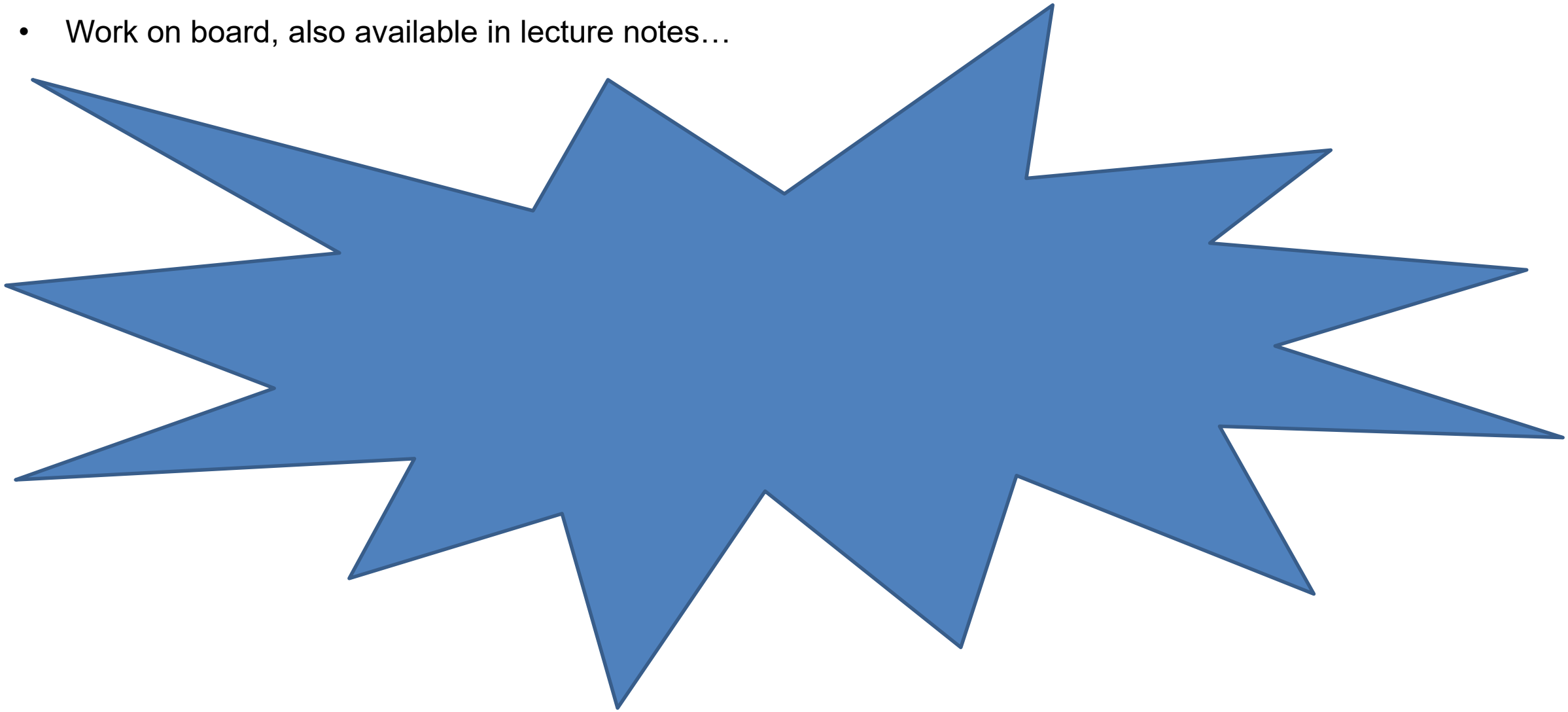




To find a port resistance, at a quiescent point, cancel independent sources and inject a test signal.

Common Source (CS) Amplifier

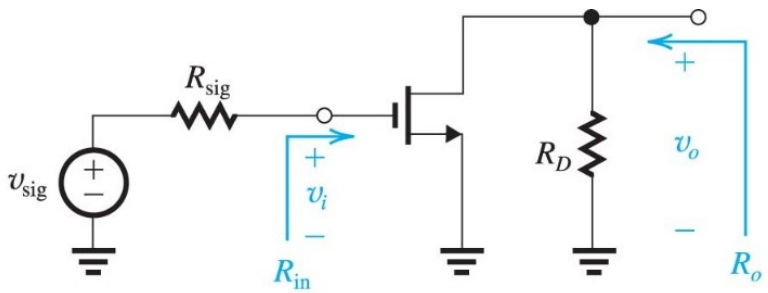
- Work on board, also available in lecture notes…

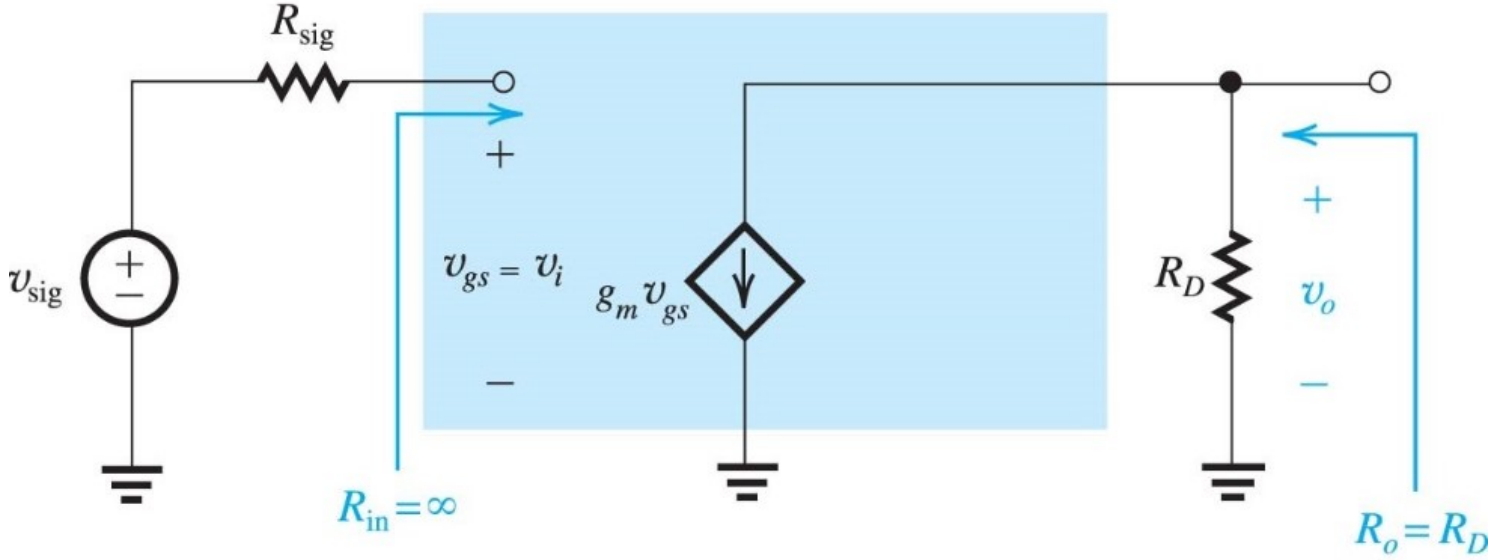


Common Source (CS) Amplifier

- High input resistance, moderate output resistance

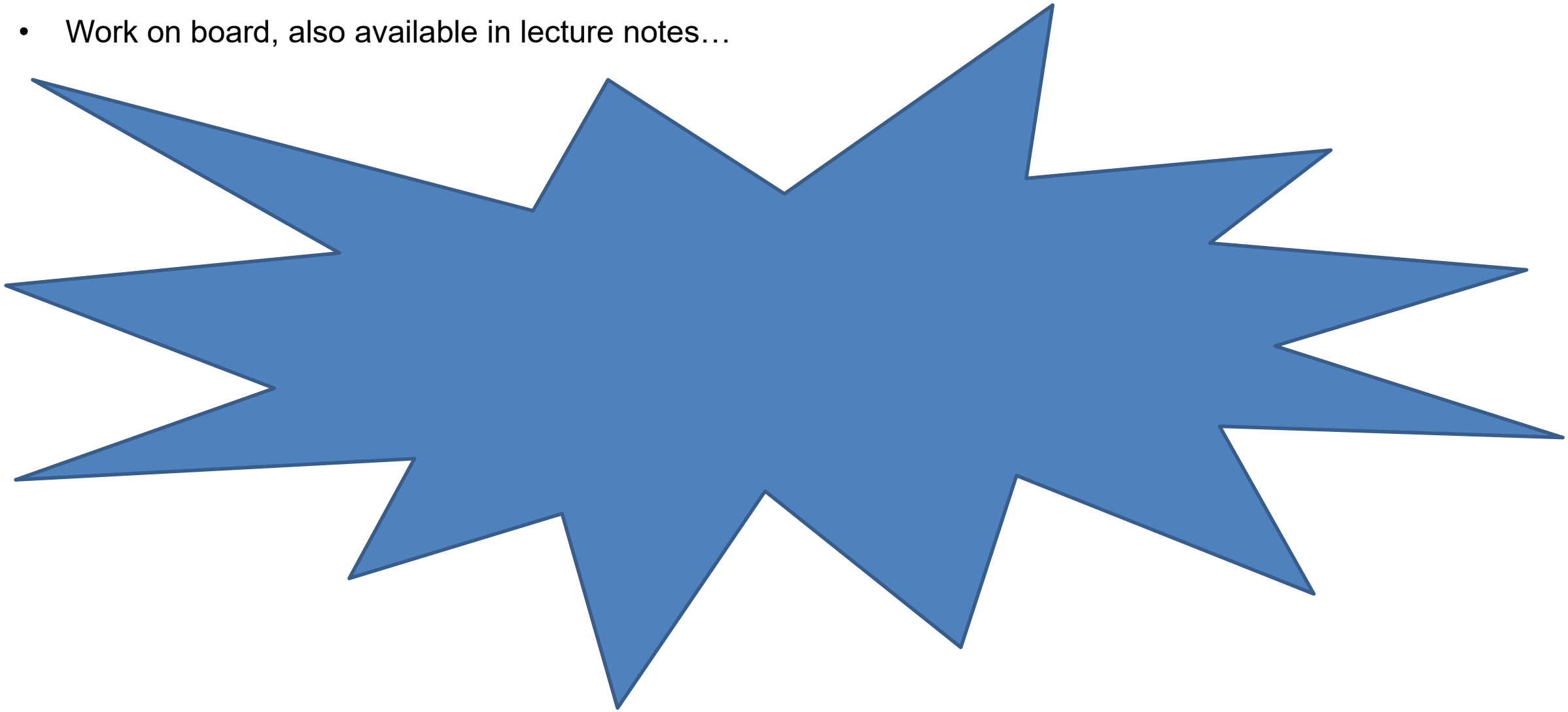
- $R_i = \frac{v_i}{i_i} = \infty$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = R_D$
- $A_{vo} = A_v|_{R_L=\infty} = -g_m R_D$
- $A_v = A_{vo}\frac{R_L}{R_L+R_o} = g_m(R_D||R_L)$
- $G_v = \frac{R_i}{R_i+R_{sig}} A_{vo} \frac{R_L}{R_L+R_o} = A_v$





Common Source (CS) Amplifier w/ Source Degeneration Resistance

- Work on board, also available in lecture notes…



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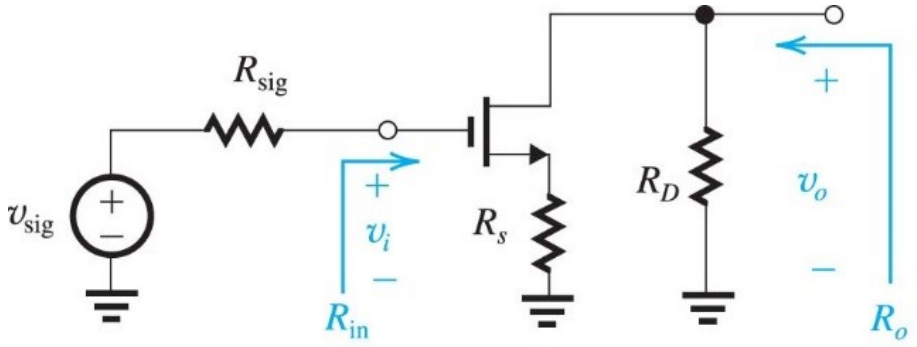
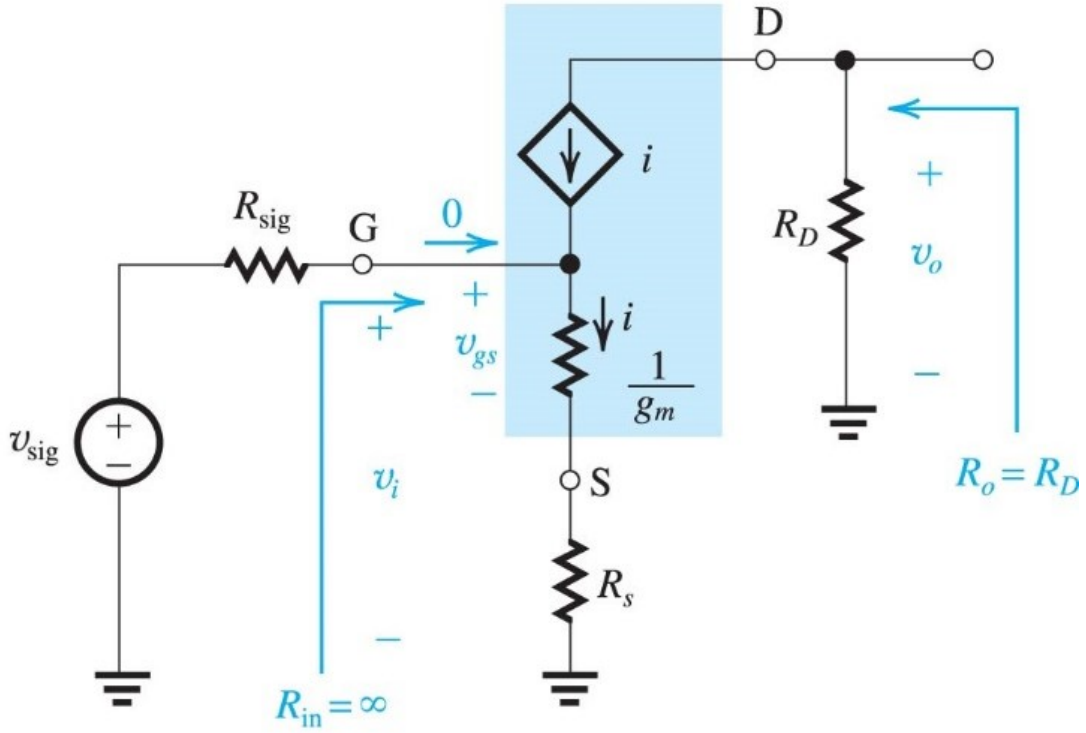
- $A_{vo} = A_v|_{R_L=\infty} = \frac{-g_m R_D}{1+g_m R_s}$
- $A_v = A_{vo}\frac{R_L}{R_L+R_o} = \frac{-g_m(R_D||R_L)}{1+g_m R_s}$
- $G_v = \frac{R_i}{R_i+R_{sig}} A_{vo} \frac{R_L}{R_L+R_o} = A_v$





Transistor output resistance would somewhat complicate analysis.

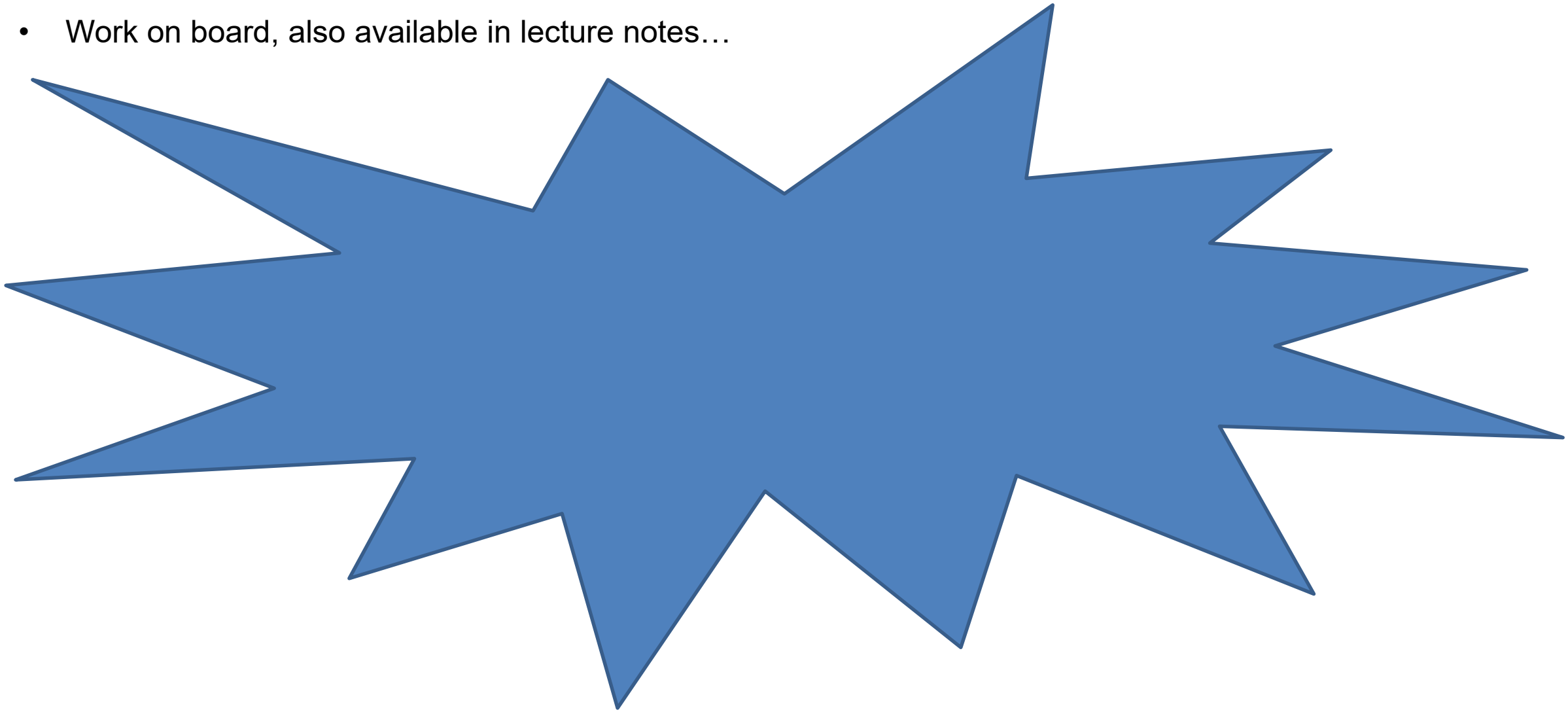
Current Buffer

- Problem
  - Supply current signal from low impedance source to high impedance load
- Current buffer
  - Protects source (Norton/ Thevenin) from output current depletion
- Ideal characteristics
  - Low input impedance, $R_i \ll R_{sig}$
  - High output impedance, $R_o \gg R_L$
  - Unity current gain, $A_i = \frac{i_o}{i_i} \approx \frac{i_L}{i_{sig}} \approx 1$

Current gain includes source and load effects, in contrast to short circuit current gain.

Common Gate (CG) Amplifier

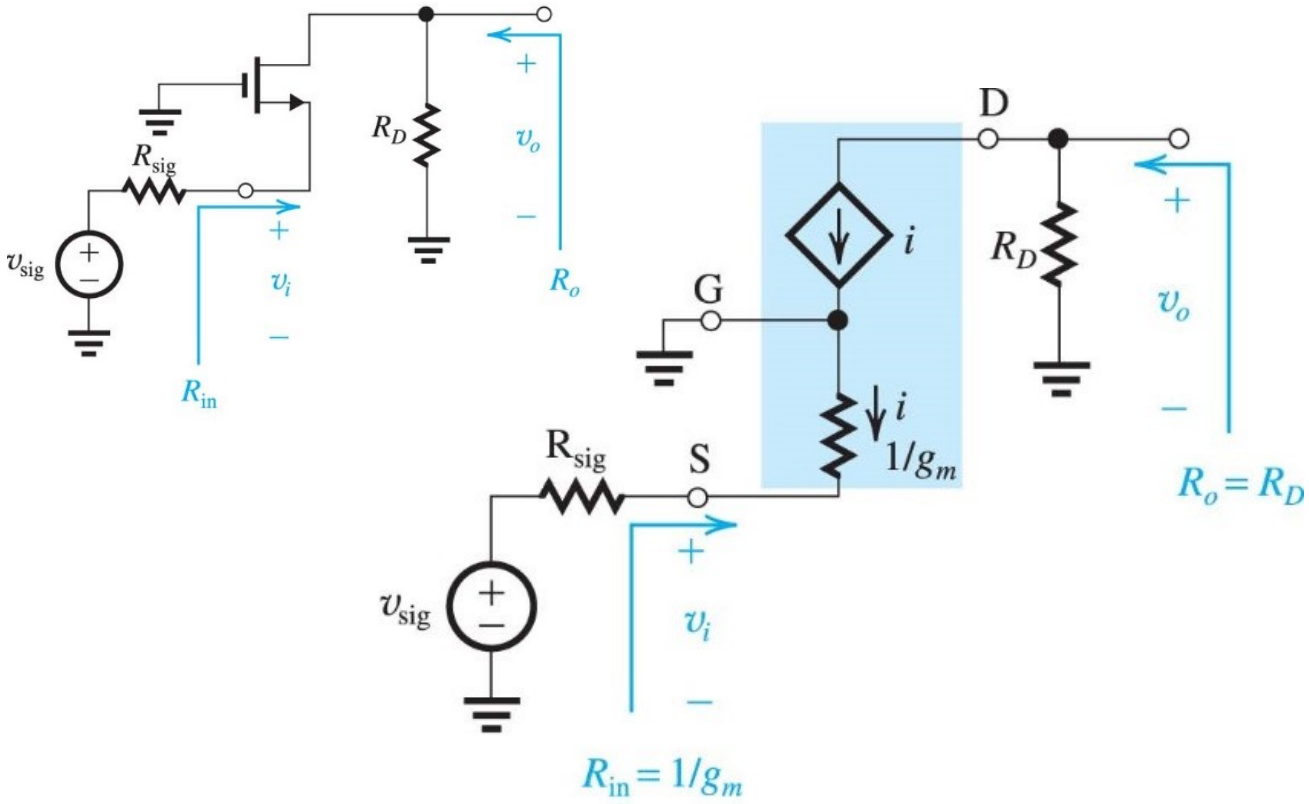
- Work on board, also available in lecture notes…



Common Gate (CG) Amplifier

- Low input resistance, moderate output resistance

- $R_i = \frac{v_i}{i_i} = \frac{1}{g_m}$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = R_D$
- $A_{vo} = A_v|_{R_L=\infty} = g_m R_D$
- $A_v = A_{vo}\frac{R_L}{R_L+R_o} = g_m(R_D||R_L)$
- $G_v = \frac{R_i}{R_i+R_{sig}} A_{vo} \frac{R_L}{R_L+R_o} = \frac{R_D||R_L}{R_{sig}+1/g_m} < A_v$



Transistor output resistance would somewhat complicate analysis.

Voltage Buffer

- Problem
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- Voltage buffer
  - Protects source (Thevenin/ Norton) from output voltage depletion
- Ideal characteristics
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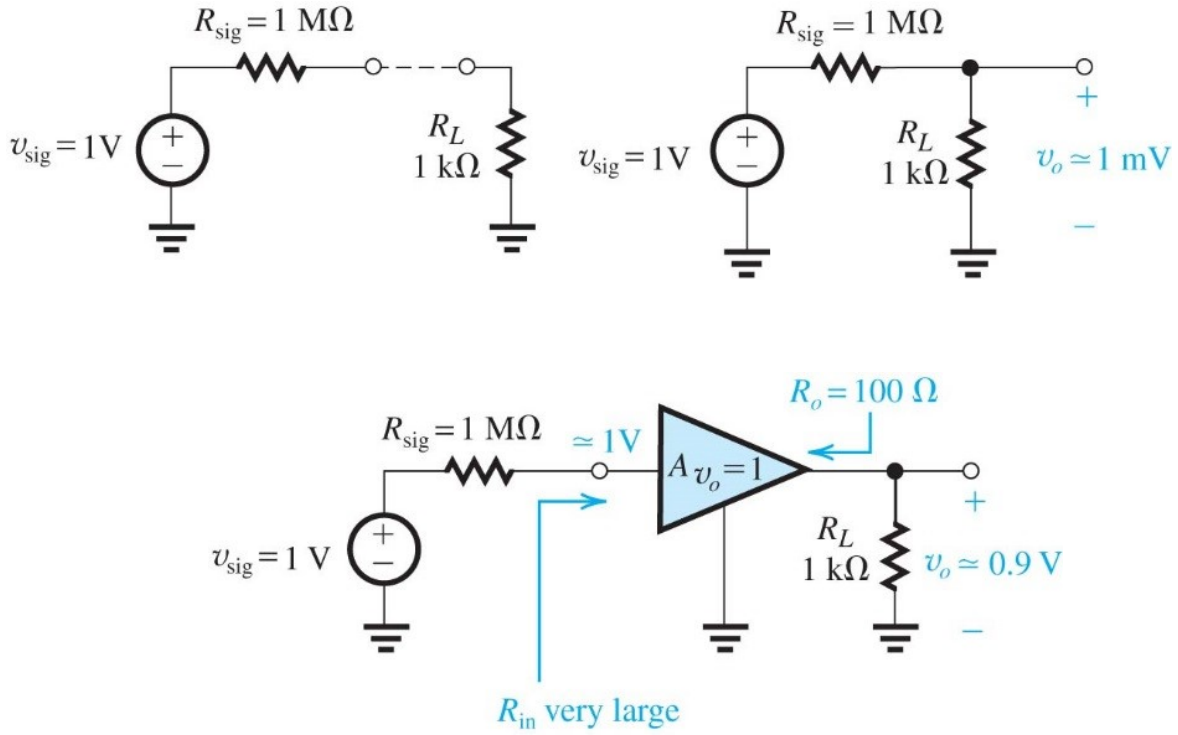
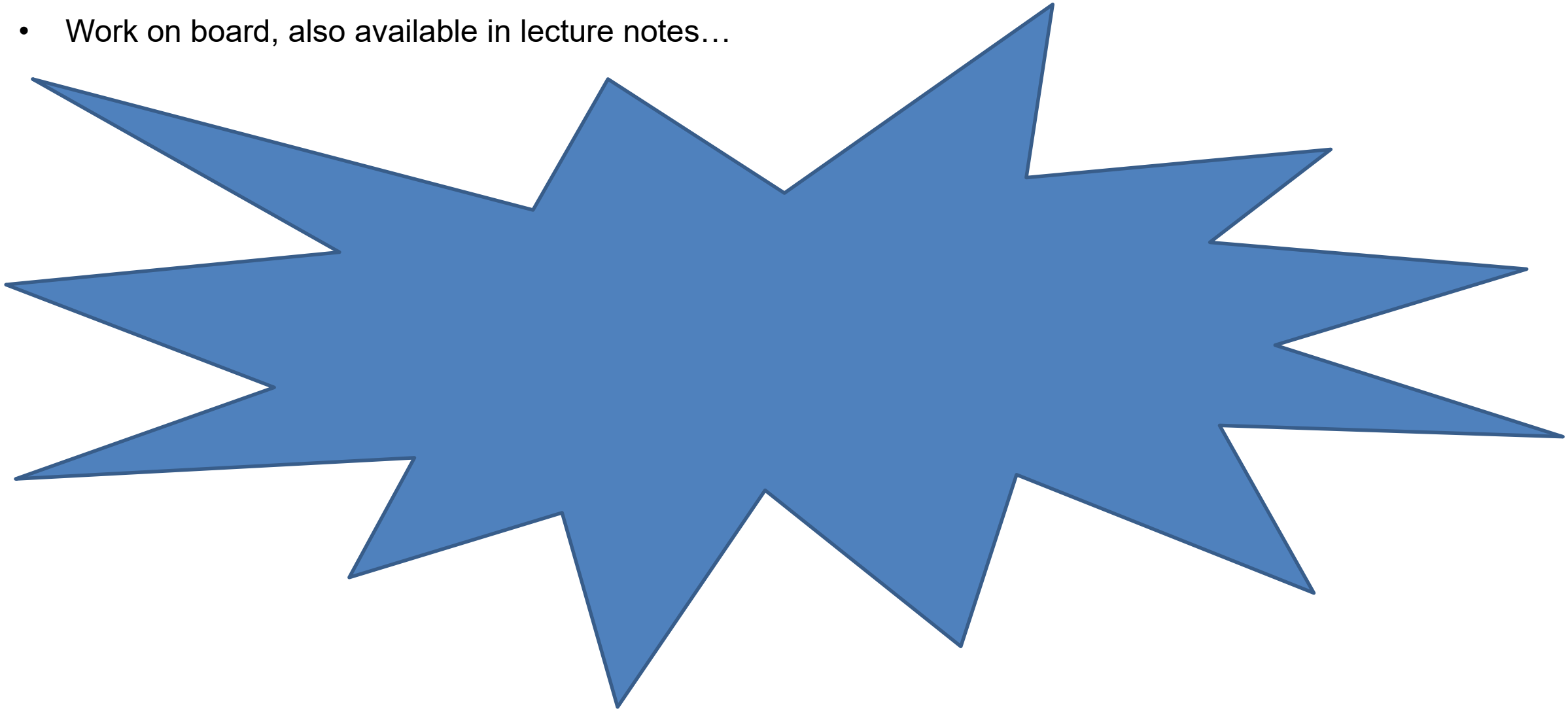
  - Low output impedance, $R_o \ll R_L$
  - Unity voltage gain, $A_v = \frac{v_o}{v_i} \approx \frac{v_L}{v_{sig}} \approx 1$



Voltage gain includes source and load effects, in contrast to open circuit voltage gain.

Common Drain (CD) Amplifier a.k.a. Source Follower

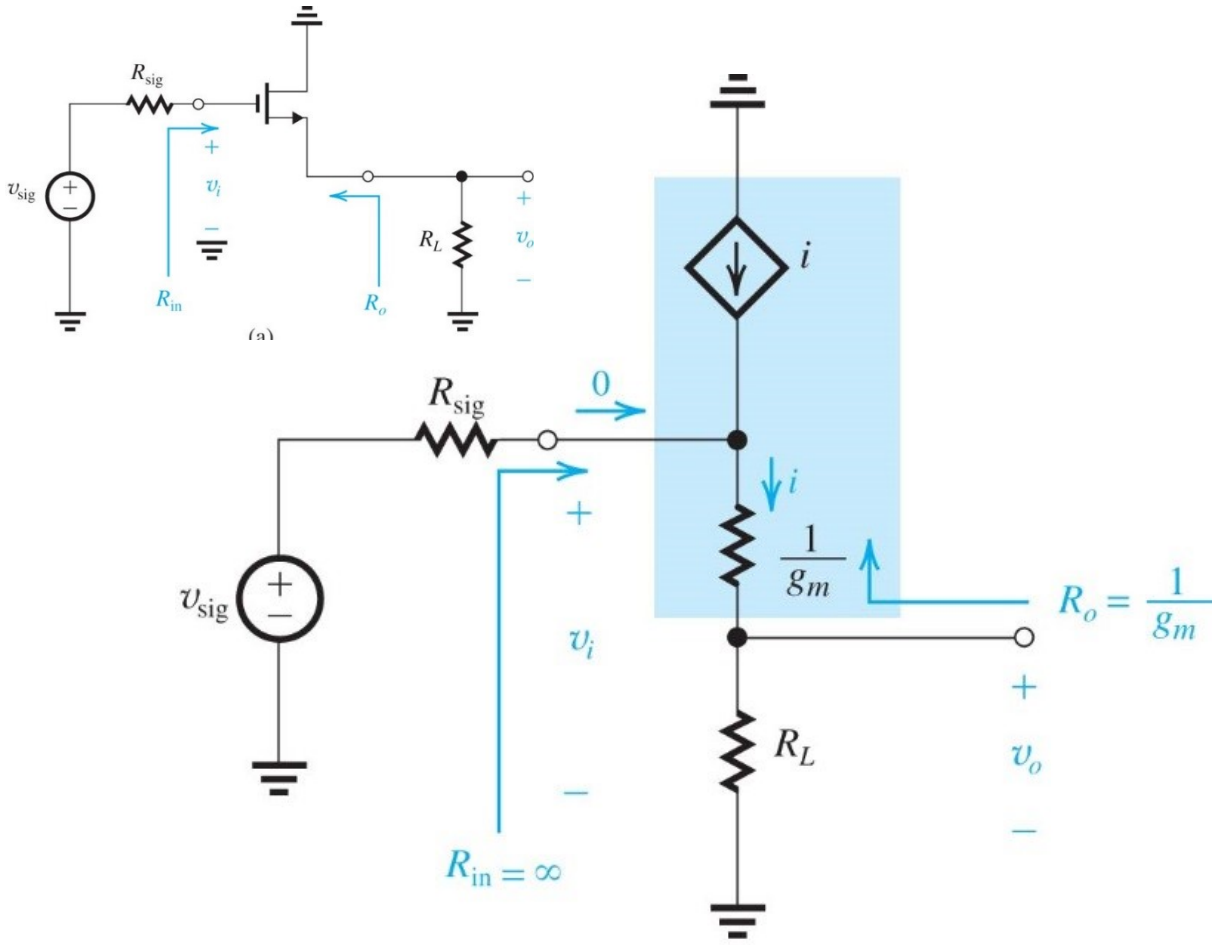
- Work on board, also available in lecture notes…



Common Drain (CD) Amplifier a.k.a. Source Follower

- High input resistance, moderate output resistance

- $R_i = \frac{v_i}{i_i} = \infty$
- $R_o = \frac{v_o}{i_o}\Big|_{v_{sig}=0} = \frac{1}{g_m}$
- $A_{vo} = A_v|_{R_L=\infty} = 1$
- $A_v = A_{vo}\frac{R_L}{R_L+R_o} = \frac{R_L}{R_L+1/g_m}$
- $G_v = \frac{R_i}{R_i+R_{sig}} A_{vo} \frac{R_L}{R_L+R_o} = A_v$



First evaluate voltage gain, then open circuit gain.

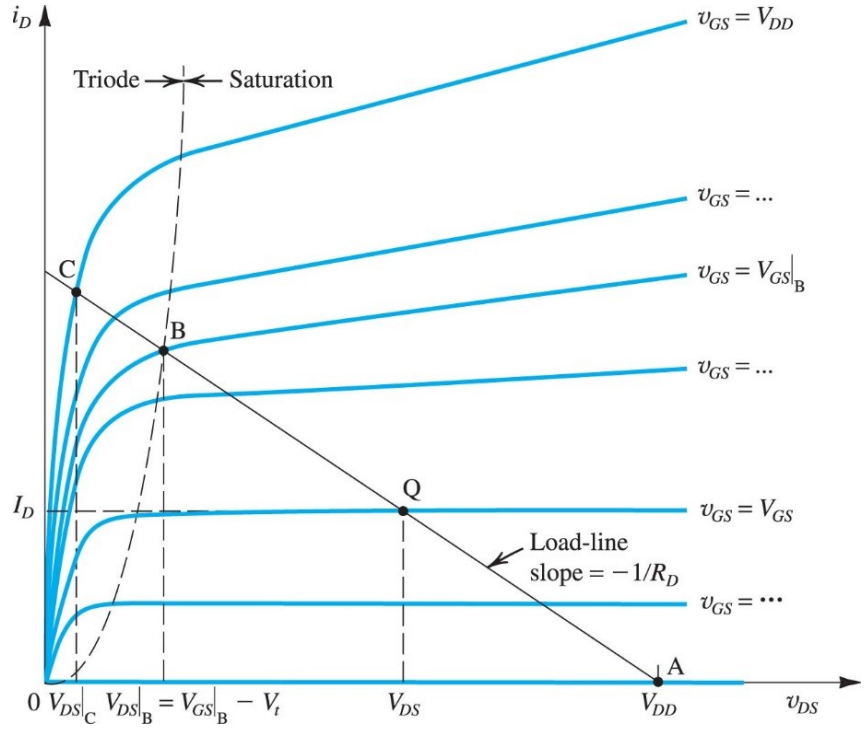
Transistor Design/ Technology + Biasing = Amplifier Gain

- MOSFET design and technology
  - Threshold voltage, V_{tn}
  - Gate width to length ratio, $\frac{W}{L}$
  - Oxide (thickness) capacitance, C_{ox}

$$g_m = k_n'\left(\frac{W}{L}\right)(V_{GS} - V_{tn}) = \sqrt{2k_n'\left(\frac{W}{L}\right)I_D} = \frac{2I_D}{V_{OV}}$$

- BJT technology
  - Current gain, β

$$g_m = \frac{I_C}{V_T} = \frac{\beta}{r_\pi}$$



- Biasing methods
  - Identify required drain(/ collector) current from gain and power requirement
  - (Discrete – Negative feedback used to combat device performance variations)
  - Integrated – Use active current sources

Devices in integrated circuits (ICs) have more uniform performance, as compared to discrete devices.