Exercise 2: BJTs and MOSFETs

1. A BJT is specified to have I_S=5*10^{-15} A and a gain β between 50 and 200. If the transistor is operated in the active mode with V_{BE} = 0.650 V, calculate the expected range of I_C, I_B, and I_E. The Early effect can be disregarded.

Ans:

The collector current is given by $I_C = I_S\left(1+\frac{V_{CE}}{V_A}\right)e^{\frac{V_{BE}}{V_T}}$ but since the Early effect is disregarded

V_A=∞ which gives I_C=5*10^{-15}*exp(0.650/0.025)=978 µA. Note that result of the calculation is very sensitive to the choice of V_T of 25 or 26 mV and that I_C is independent of β. The base current is I_B=I_C/β which gives a range of I_B=978*10^{-6} / 50 = 19.6 µA to I_B=978*10^{-6} / 200 = 4.89 µA. Since the sum of the currents have to be zero $I_E + I_B + I_C = 0$ and therefore the emitter current has a range of I_E=-I_C-I_B = -978-4.89=-983 µA to I_E=-I_C-I_B = -978-19.6=-998 µA.

2. (similar to problem 4.1 in Sedra-Smith) The terminal voltages of npn transistors biased in different ways are measured which gives (in Volts)

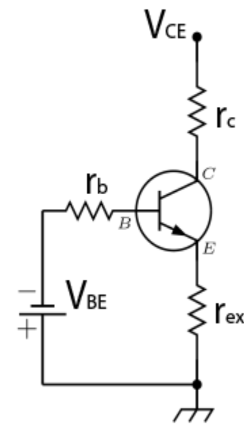
Case	Emitter	Base	Collector	Mode
1	0	0.7	0.8	
2	0	0.8	0.1	
3	-0.7	0	0.8	
4	-0.7	0	-0.6	
5	2.7	2	0	
6	0	0	5.0	
7	0.5	-0.1	4.0	

Where 0 V indicates the connection to the reference terminal (ground) probe of the voltmeter. Identify the mode of the transistor for the 7 cases. The possible modes are cut-off, active, saturation (in lecture 3 slides) and inverse active (see fig 1.12 in book).

Ans:
In the cut-off mode the emitter-base junction and the collector-base junction should be reverse biased i.e. the potential of both emitter and collector should be higher than the base.
In the active mode the emitter-base junction should be forward biased and the collector-base junction reverse biased (or unbiased with just the built-in potential sweeping out carriers) i.e. the potential of the base should be higher than the emitter and the potential of the collector should be higher than the base.
In saturation both the emitter-base junction and the collector-base junction should be forward biased i.e. the potential of both emitter and collector should be lower than the base.
In the inverse active mode the emitter-base junction should be reverse biased and the collector-base junction forward biased i.e. the potential of the base be higher than the collector and the potential of the emitter should be higher than the base. If the doping in the collector and emitter would be equal, this mode would give an equal current as the active mode. However, real BJTs are not symmetric and have a higher doping in the emitter than in the collector to improve gain by minimizing the base current injected into the emitter while avoiding breakdown in the base-collector junction. Therefore the inverse active mode gives a lower current and gain and is not usually used.
This means that the result is

Case	Emitter	Base	Collector	Mode
1	0	0.7	0.8	Active (built-in potential in base-collector junction sweeps the carriers into the collector)
2	0	0.8	0.1	Saturation
3	-0.7	0	0.8	Active
4	-0.7	0	-0.6	Saturation
5	2.7	2	0	Inverse active
6	0	0.5	5.0	Active
7	0.5	-0.1	4.0	Cut-off

3. An npn bipolar transistor with $I_s = 10^{-15}A$, $\beta = \beta_0 = 300$, and $V_{CE} = 10V$.



(a) Find V_{BE} so that $I_C = 5mA$ in the case when the resistances are ignored. Repeat for $I_C = 10mA$.

(b) If the transistor have $r_c = r_{ex} = 10\Omega, r_b = 100\Omega$, calculate V_{be} so that $I_c = 5mA$.

(c) For the transistor in (b), derive the low-frequency hybrid-π model. The Early voltage is V_A=100 V. Hint: consider how capacitances behave at low frequency.

(d) For the same transistor, derive the high-frequency hybrid-πmodel, assuming a base width of $W_B = 0.5\mu m, D_n = 15cm^2/s, C_{je} = 2pF, C_\mu = 2pF$.

Ans:

a) *The collector current is given by*

$$I_C = I_S(e^{V_{BE}/V_T} - 1)$$

Solve for V_{BE} to get

$$V_{BE} = V_T \cdot \ln\left(\frac{I_C}{I_S} + 1\right) = 0.025 \cdot \ln\left(\frac{5 \cdot 10^{-3}}{10^{-15}}\right) = \begin{cases} 0.731\, V & for\ I_C = 5\, mA \\ 0.748\, V & for\ I_C = 10\, mA \end{cases}$$

b) *The voltage between the base and emitter was calculated to be V_{BE}'=0.731 V for I_C=5 mA in exercise a) where no resistances where taken into account. Use Kirchoffs voltage law (KVL) and make one full loop around the ground point to get*

$$V_{BE} - I_B \cdot r_b - V_{BE}^{'} + I_E \cdot r_{ex} = 0 \quad (*)$$

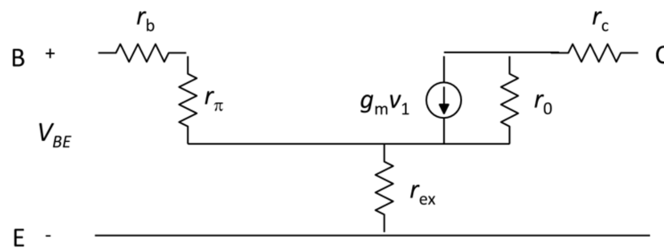
Use that $I_C = \beta_0 * I_B$ to get $I_B = I_C / \beta_0$. The sum of all current in the BJT must be zero which gives $I_E = -I_B - I_C = -\frac{I_C}{\beta_0} - IC = -I_C\left(\frac{1}{\beta_0} + 1\right)$. *Insert these expressions for I_B and I_E in the expression for KVL (*) to get*

$$V_{BE} = \frac{I_C}{\beta_0} \cdot r_b + V_{BE}^{'} + I_C\left(\frac{1}{\beta_0} + 1\right) \cdot r_{ex} = \ldots$$

$$= \frac{5 \cdot 10^{-3}}{300} \cdot 100 + 0.731 + 5 \cdot 10^{-3}\left(\frac{1}{300} + 1\right) \cdot 10 = \ 0.783 \text{ V}$$

As expected the voltage have to be increased slightly to get the same I_C when the resistances are added.

c) *In a low frequency small-signal model all capacitances can be treated as open circuits. The model is*



The resistances in the terminals r_b =100 Ω ,r_c = r_{ex} = 10 Ω are already given. The transconductance (controlling the current source) is

$$g_m = \frac{I_C}{V_T} = \frac{5 \cdot 10^{-3}}{25 \cdot 10^{-3}} = 0.2 \ S$$

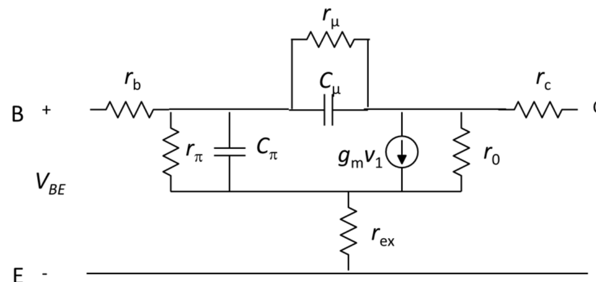
The input resistance (due to the change in I_B when changing V_{BE}) is

$$r_\pi = \frac{\beta_0}{g_m} = \frac{300}{0.2} = 1.5 \ k\Omega$$

Finally the output resistance (due to the Early effect i.e. the change in the base width with V_{CE}) is

$$r_0 = \frac{V_A}{I_C} = \frac{100}{5 \cdot 10^{-3}} = 20 \ k\Omega$$

d) *In an intermediate-frequency model the capacitances have to be taken into account. However, for very high frequencies the capacitances act as shorts. The model at intermediate frequencies is*



Most of the circuit elements are given or calculated in c). The only capacitance missing is the base-emitter capacitance. Since this is a forward biased junction the total capacitance consists of both base charging capacitance (C_{de}) and junction capacitance (C_{je}) so

$C_\pi = C_{de} + C_{je} = \tau_F * g_m + C_{je}$

where the base transit time is related to the base with and the diffusion constant as $\tau_F = W_B^2/2D_n$
This gives a base-emitter capacitance of

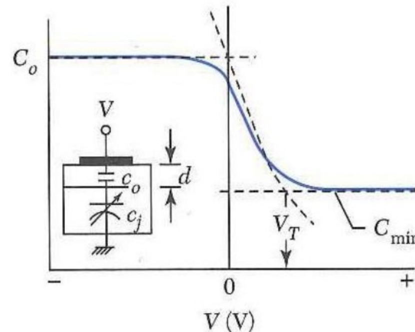
$$C_\pi = \frac{\omega_B^2}{2D_n} \cdot g_m + C_{je} = \frac{0.5 \cdot 10^{-6}}{2 \cdot 15 \cdot 10^{-4}} \cdot 0.2 + 2 \cdot 10^{-12} = 18.6\ pF$$

Finally the base-collector resistance is

$$r_\mu = \beta_0 r_0 = 300 \cdot 20 \cdot 10^3 = 6 M\Omega$$

However, this last term is not discussed in book

4. For an ideal metal-SiO_2-Si capacitor having a Si doping of $N_A = 10^{17} cm^{-3}$ and an oxide thickness of d=5 nm, calculate the minimum capacitance (per unit area) of the C-V curve in figure below and the percentage of capacitance modulation with voltage. The relative dielectric constants of SiO_2 and Si are 3.9 and 11.9, respectively, and the intrinsic carrier density of Si is n=9.65*10^9 cm^{-3}.



Ans

The minimum capacitance occurs just before an inversion layer starts to form under the oxide. In this case the distance between the metal contact and the majority carriers outside the depletion region in the Si is at its maximum. Inversion is reached when the surface potential is $\Phi \approx 2\Phi_f$ where Φ_f is the distance between the Fermi level (doped case) and the intrinsic Fermi level (undoped case) in the bulk i.e. the Fermi level at the Si-oxide interface should have a distance to E_C equal to its distance to E_V in the bulk (see lecture 2). The Fermi level position (relative to the intrinsic position) is related to the doping giving

$$\Phi \approx 2\Phi_f = \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right) = 2 \cdot 0.026 \cdot \ln\left(\frac{10^{17}}{9.65 \cdot 10^9}\right) = 0.84\ V$$

The depletion region width is given by (note that N_A was given in cm^{-3})

$$X = \sqrt{\frac{2\varepsilon_s\varepsilon_0\Phi}{qN_A}} = \sqrt{\frac{2\cdot 11.9\cdot 8.85\cdot 10^{-12}\cdot 0.84}{6.022\cdot 10^{-19}\cdot 10^{23}}} = 54\ nm$$

The total capacitance can be obtained by considering that the oxide and the depletion region capacitance are connected in series giving

$$C_{\min} = \left(C_{dep}^{-1} + C_{ox}^{-1}\right)^{-1} = \left(\left(\frac{\varepsilon_s\varepsilon_0}{X}\right)^{-1} + \left(\frac{\varepsilon_{ox}\varepsilon_0}{d}\right)^{-1}\right)^{-1} = \ldots$$

$$= \left(\left(\frac{11.9\cdot 8.85\cdot 10^{-12}}{54\cdot 10^{-9}}\right)^{-1} + \left(\frac{3.9\cdot 8.85\cdot 10^{-12}}{5\cdot 10^{-9}}\right)^{-1}\right)^{-1} = 152\ nF/cm^2$$

The capacitance modulation is given by

$$\frac{C_{\min}}{C_0} = \frac{C_{\min}}{C_{ox}} = \frac{C_{\min}}{\frac{\varepsilon_{ox}\varepsilon_0}{d}} = \frac{152\cdot 10^{-5}}{\frac{3.9\cdot 8.85\cdot 10^{-12}}{5\cdot 10^{-9}}} = 22\ \%$$

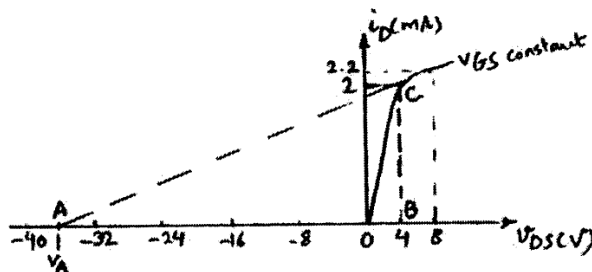
Note that the curve corresponds to the high-frequency case where an inversion layer at the semiconductor-oxide interface does not have time to form by recombination-generation during the AC modulation in the measurment. In the low-frequency case the capacitance would increase again for high voltages with only a minimum for intermediate voltages.

5. For a MOSFET operating in the saturation region at a constant V_{GS}, I_{DS} is measured to be 2 mA for V_{DS} = 4 V and 2.2 mA for V_{DS} = 8 V. Calculate the output resistance r_0, the Early voltage V_A (similar as in BJTs) and the channel length modulation parameter λ.

Ans

The output resistance is given by $r_0 = \frac{dV_{DS}}{dI_D} = \frac{8-4[V]}{(2.2-2)*10^{-3}[A]} = 20k\Omega$

The Early voltage (V_A) can be calculated by extrapolating I_{DS} to 0. Consider the triangle in



*The base of the triangle is given by the slope*max(I_{DS}) as r_0*2 mA=40 V.*
Then V_A=40-4=36V. The channel length modulation parameter is given by $\lambda=1/V_A$ = 1/36=0.028 V^{-1}.

6. (from exam 151028) Several different Si n-MOSFETs have been measured and the results can be seen in the table below. The source is grounded (V_S=0 V). Fill out the missing information in each row. The three operating modes are cut-off, saturation and linear. k´/2*(W/L) = 36 mA/V^2 for all the devices.

In the cut-off region $V_{GS}<V_t$ there is no channel formed since inversion is not achieved.
In the triode region $V_{GS} > V_t$ and $V_{DS} < V_t+V_{GS}$. In this region a channel has formed under the gate but has not been pinched off yet.
In the saturation region $V_{GS} > V_t$ and $V_{DS} > V_t+V_{GS}$. Here the channel has been pinched off at the drain and the current saturates.

Device	V_t [V]	λ [V^{-1}]	V_{GS} [V]	V_{DS} [V]	I_D [mA]	Operating mode
1	+1	0.005	+0.5	+1.0	0	Cut-off
2	0	0.05	+2	+2.5	162	Saturation
3	+0.5	0	+1.5	+0.75	33.75	Linear
4	-0.5	0.03	+0.5	+1.5	37.62	Saturation

Device 1: $V_{GS} < V_T$ -> cut-off -> I_D=0 (no inverted channel is formed)
Device 2: $V_{DS} > V_{GS}-V_T$ -> saturation

$$I_D = \frac{\overbrace{\mu_n C_{ox}}^{k'}}{2}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS}) = 36\cdot(2-0)^2\cdot(1+0.05\cdot 2.5) = 162\ mA$$

Device 3: V_t is unknown so we don't know if we are in saturation or linear region. Test both by solving for V_t.

Linear: $$V_t = V_{GS} - \frac{\frac{I_D}{36}+V_{DS}^2}{2V_{DS}} = 1.5 - \frac{\frac{33.75}{36}+0.75^2}{2\cdot 0.75} = 0.5\ V$$

Saturation: $$V_t = V_{GS} - \sqrt{\frac{I_D}{36(1+\lambda V_{DS})}} = 1.5 - \sqrt{\frac{33.75}{36(1+0)}} = 0.53\ V$$

For both results $V_{DS} < V_{GS}-V_T$ -> linear region i.e. V_t=0.5V

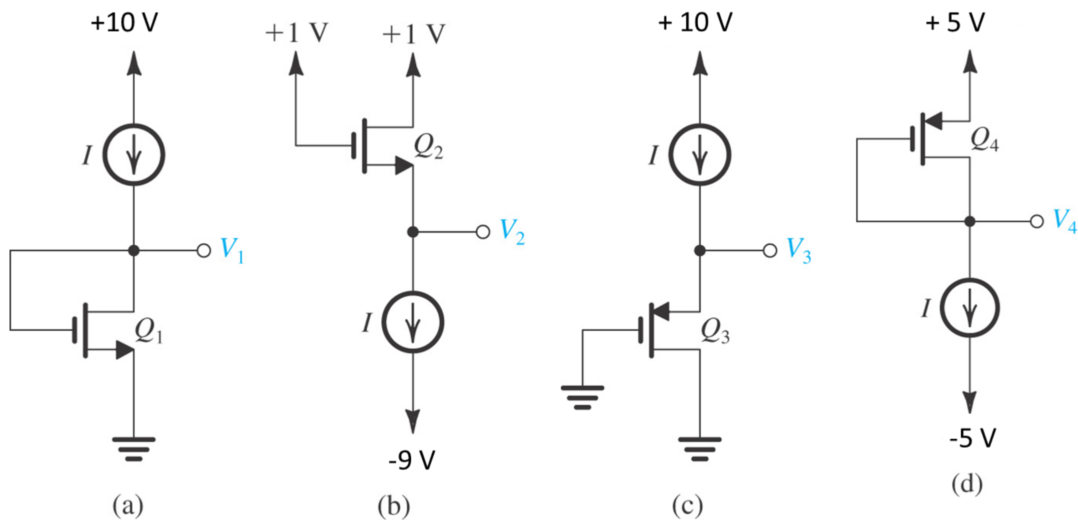
Device 4: $V_{DS} > V_{GS}-V_T$ -> saturation. Solve for λ:

$$\lambda = \frac{\frac{I_D}{36(V_{GS}-V_t)^2}-1}{V_{DS}} = \frac{\frac{37.62}{36(0.5-(-0.5))^2}-1}{1.5} = 0.03\ V^{-1}$$

7. (similar to 5.39 from Sedra-Smith)

All transistors (both n and p-type) in the four circuits below have the same value of $|V_t|$, k' and W/L. The channel length modulation is small i.e. λ is negligible. All operate in saturation at I_D=I and $|V_{GS}|=|V_{DS}|$=3 V.

- Find the four voltages V_1 to V_4.
- If $|V_t|$=1 V and I=2 mA, for each case how large resistor can be inserted in series with the each drain connection while still keeping the transistor in saturation?
- What is the largest resistor that can be placed in series with the gate?
- If the current source I requires at least 2 V between its terminals to operate properly, what is the largest resistor that can be placed in series with each MOSFET source while ensuring that that each transistor operates in the saturation region with I_D=I?
- With the resistors in the previous task added, calculate V_1 to V_4.



5.29

a) $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \Rightarrow 2 = \frac{1}{2} k_n' \frac{W}{L} (3-1)^2$

$\Rightarrow k_n' \frac{W}{L} = 1\ mA/V^2$

$V_1 = V_{DS} = 3V$

b) $V_2 = V_S = V_D - V_{DS} = 1 - 3 = -2^V$

c) $V_3 = V_S = V_D - V_{DS} = 0 - (-3) = 3^V$

d) $V_4 = V_D = V_S + V_{DS} = 5 + (-3) = 2^V$

In order to calculate R_{max} that can be inserted in series with the drain, V_{DS} has to be equal to $V_{GS} - V_t$, so that the device is operating on the edge of saturation: $|V_{DS}| = 3 - 1 = 2^V$. Note that since i_D is the same, V_{GS} stays the same.

a) $R_{D\,max} = \frac{3-2}{2^{mA}} = 0.5 K\Omega$

b) $V_2 = -2^V \Rightarrow V_D = -2 + 2 = 0 \Rightarrow R_{D\,max} = \frac{1}{2} = 0.5^{K\Omega}$

Note that V_2 is fixed through $V_{GS} = 3V$.

c) $V_{GS} = -3V \Rightarrow V_S = V_3 = 3^V$. Now for V_{DS} to be $-2V$, V_D has to be 1^V.

$R_{D\,Max} = \frac{1^V}{2^{mA}} = 0.5 K\Omega$

d) $V_{GS} = -3V \Rightarrow V_G = V_4 = 2^V$. Adding the resistor between V_4 and drain means that V_D has to be $5 - 2 = 3^V$ and this leaves 1^V voltage drop on the resistor $\therefore R_{D\,max} = \frac{1}{2} = 0.5^{K\Omega}$

In order to calculate the Largest Resistor added to the gates, note that since the gate doesn't draw any current, the value of the resistor is immaterial.

Now we calculate $R_{S\,max}$, assuming that the voltage drop across the current source is at least 2^V:

a) $V_1 = 8^V$ then $V_{GS} = 3^V \Rightarrow V_S = 8 - 3 = 5^V$

$R_{S\,Max} = \frac{5}{2} = 2.5 K\Omega$

b) $V_2 = -9 + 2 = -7^V$, $V_S = 1 - |V_{GS}| = -2^V$

$R_{S\,max} = \frac{-2-(-7)}{2} = 2.5 K\Omega$

c) $V_3 = 10 - 2 = 8^V$, $V_S = 0 + |V_{GS}| = 3^V$

$R_{S\,max} = \frac{8-3}{2} = 2.5 K\Omega$

d) $V_4 = -5 + 2 = -3^V$, $V_S = -3 + |V_{GS}| = 0^V$

$R_{S\,max} = \frac{5}{2} = 2.5 K\Omega$