Exercise 2: BJTs and MOSFETs

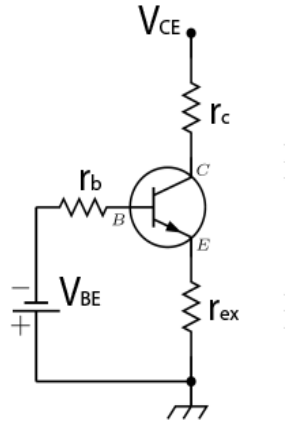
1. A BJT is specified to have I_S=5*10^{-15} A and a gain β between 50 and 200. If the transistor is operated in the active mode with V_{BE} = 0.650 V, calculate the expected range of I_C, I_B, and I_E. The Early effect can be disregarded.

2. (similar to problem 4.1 in Sedra-Smith) The terminal voltages of npn transistors biased in different ways are measured which gives (in Volts)

Case	Emitter	Base	Collector	Mode
1	0	0.7	0.8	
2	0	0.8	0.1	
3	-0.7	0	0.8	
4	-0.7	0	-0.6	
5	2.7	2	0	
6	0	0	5.0	
7	0.5	-0.1	4.0	

Where 0 V indicates the connection to the reference terminal (ground) probe of the voltmeter. Identify the mode of the transistor for the 7 cases. The possible modes are cut-off, active, saturation (in lecture 3 slides) and inverse active.

3. An npn bipolar transistor with $I_s = 10^{-15}A$, $\beta = \beta_0 = 300$, and $V_{CE} = 10V$.



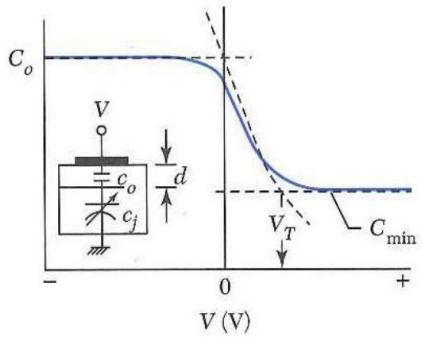
(a) Find V_{BE} so that $I_C = 5mA$ in the case when the resistances are ignored. Repeat for $I_C = 10mA$.

(b) If the transistor have $r_c = r_{ex} = 10\Omega, r_b = 100\Omega$, calculate V_{be} so that $I_c = 5mA$.

(c) For the transistor in (b), derive the low-frequency hybrid-π model. The Early voltage is V_A=100 V. Hint: consider how capacitances behave at low frequency.

(d) For the same transistor, derive the high-frequency hybrid-πmodel, assuming a base width of $W_B = 0.5\mu m, D_n = 15cm^2/s, C_{je} = 2pF, C_\mu = 2pF$.

4. For an ideal metal-SiO_2-Si capacitor having a Si doping of $N_A = 10^{17}cm^{-3}$ and an oxide thickness of d=5 nm, calculate the minimum capacitance (per unit area) of the C-V curve in figure below and the percentage of capacitance modulation with voltage. The relative dielectric constants of SiO_2 and Si are 3.9 and 11.9, respectively, and the intrinsic carrier density of Si is n=9.65*10^9 cm^{-3}.



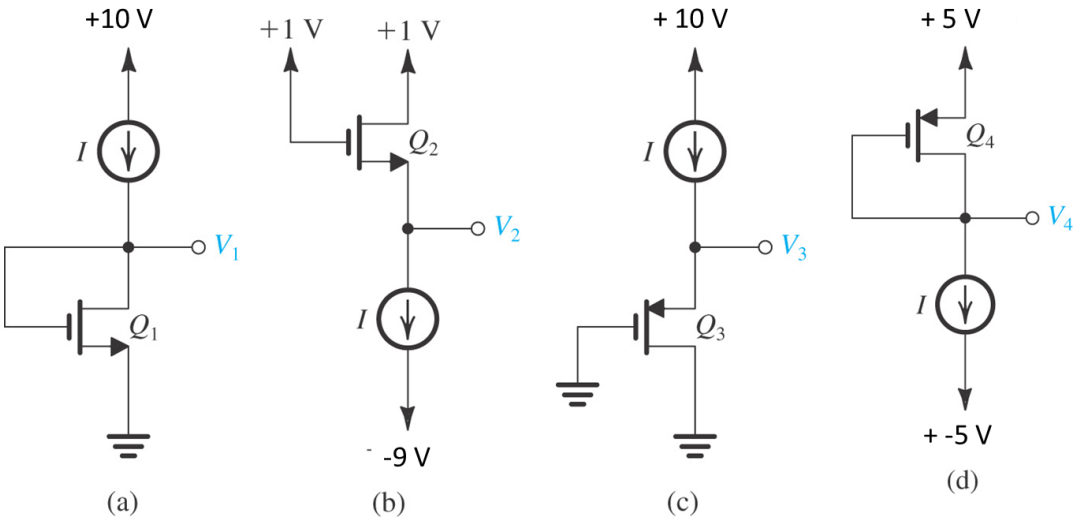
5. For a MOSFET operating in the saturation region at a constant V_{GS}, I_{DS} is measured to be 2 mA for V_{DS} = 4 V and 2.2 mA for V_{DS} = 8 V. Calculate the output resistance r_0, the Early voltage V_A (similar as in BJTs) and the channel length modulation parameter λ.

6. (from exam 151028) Several different Si n-MOSFETs have been measured and the results can be seen in the table below. The source is grounded (V_S=0 V). Fill out the missing information in each row. The three operating modes are cut-off, saturation and linear. k´*(W/L) = 36 mA/V^2 for all the devices.

Device	V_t [V]	λ [V^{-1}]	V_{GS} [V]	V_{DS} [V]	I_D [mA]	Operating mode
1	+1	0.005	+0.5	+1.0	**???**	**???**
2	0	0.05	+2	+2.5	**???**	**???**
3	**???**	0	+1.5	+0.75	33.75	**???**
4	-0.5	**???**	+0.5	+1.5	37.62	**???**

7. (similar to 5.39 from Sedra-Smith)
All transistors (both n and p-type) in the four circuits below have the same value of $|V_t|$, k' and W/L. The channel length modulation is small i.e. λ is negligible. All operate in saturation at I_D=I and $|V_{GS}|=|V_{DS}|$=3 V.

- Find the four voltages V_1 to V_4.
- If $|V_t|$=1 V and I=2 mA, for each case how large resistor can be inserted in series with the each drain connection while still keeping the transistor in saturation?
- What is the largest resistor that can be placed in series with the gate?
- If the current source I requires at least 2 V between its terminals to operate properly, what is the largest resistor that can be placed in series with each MOSFET source while ensuring that that each transistor operates in the saturation region with I_D=I?
- With the resistors in the previous task added, calculate V_1 to V_4.


+10 V
I
V1
Q1
(a)
+1 V
+1 V
Q2
V2
I
-9 V
(b)
+ 10 V
I
V3
Q3
(c)
+ 5 V
Q4
V4
I
+ -5 V
(d)