Exam – modern electronics (ETIN70) 2017-10-26 8.00-13.00

GOOD LUCK!
Total number of points = 20
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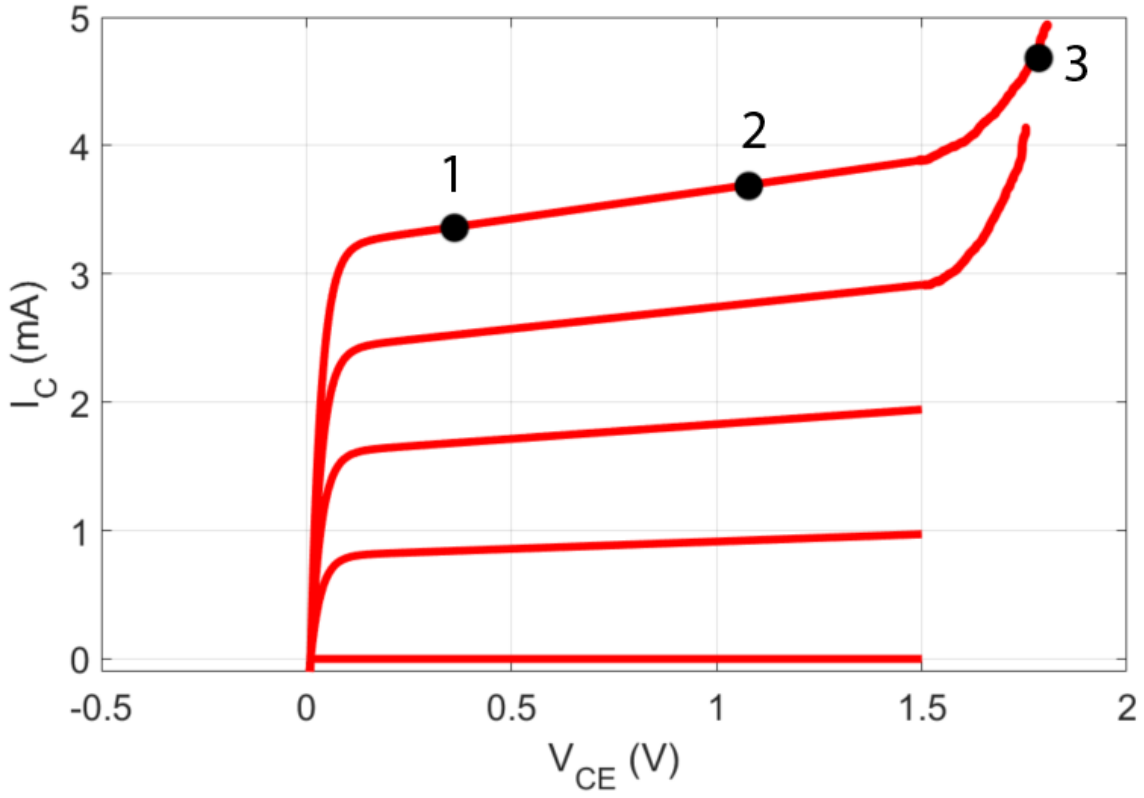
1. BJTs (3p)

A NPN BJT gives the I_C-V_{CE} characteristics below.



a) Sketch the minority carrier concentration in the base for the bias conditions in point 1 and 2 and clearly indicate any differences. You can assume that the base is short i.e. recombination can be disregarded. (1 p)

b) Calculate the Early voltage using the data in the figure. (1 p)

c) I_C increases rapidly for sufficiently high V_{CE} (point 3 in the figure). Sketch the band structure (not carrier concentration) including Fermi levels for the entire BJT (emitter, base, collector) for bias point 3 and explain the reason for the rapid increase in I_C. (1 p)

2. MOSFETs (4p)

In some MOSFETs the current does not saturate above $V_{DS} > V_{GS}-V_t$ but show a slow increase with V_{DS} in the saturation region.

a) What is the name of this effect? Why does the current increase with V_{DS}? (1 p)

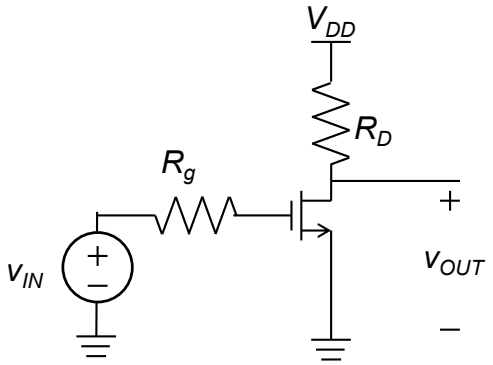
b) Describe two changes to the MOSFET in order to decrease this effect and obtain better saturation. Motivate why your suggestions would improve saturation. You can ignore if other characteristics gets worse. (1 p)

c) Three different Si n-MOSFETs have been measured and the results can be seen in the table below. The source is grounded (V_S=0 V). Fill out the missing information in each row. Note that device 1 has been measured at two different bias conditions. You should present your full calculations for the values and motivate your answers for the operating modes. The three possible operating modes are cut-off, saturation and linear. $k'/2*(W/L)$ = 2.92 mA/V^2 for all the devices. (2 p)

Device	V_t [V]	λ [V^{-1}]	V_{GS} [V]	V_{DS} [V]	I_D [mA]	Operating mode
1	0.5	**???**	**??? (same as below)**	2.5	3.427	**???**
1	0.5	**???**	**??? (same as above)**	2	3.325	**???**
2	0.8	0.1	0.6	3	**???**	**???**
3	**???**	0.05	1.25	0.75	2.516	**???**

3. Amplifiers I (7p)

Consider the following amplifier.



(a) Draw the schematic small-signal equivalent circuit. (1p)

(b) Derive the frequency-dependent transfer function $H(s)=v_o/v_{in}$ You may neglect the transistor output resistance. (2p)

(c) You want to optimize the transistor to enhance the amplifier performance. What methods can you use in the optimization and what are the expected benefits for the amplifier? (2p)

(d) Add a bias network to the circuit to bias the gate at 0.6V. Determine the elements (relative values) in the resistive network assuming that Vdd=3V. (2p)

4. Amplifiers II (3p)

Discuss the benefits and drawbacks for the common-gate and common-drain amplifiers! (3p)

5. Memories (3p)

Describe the general layout for two types of memory cells including DRAM and SRAM. How are the cells addressed? How are the transistors connected? When are the different types considered? (3p)