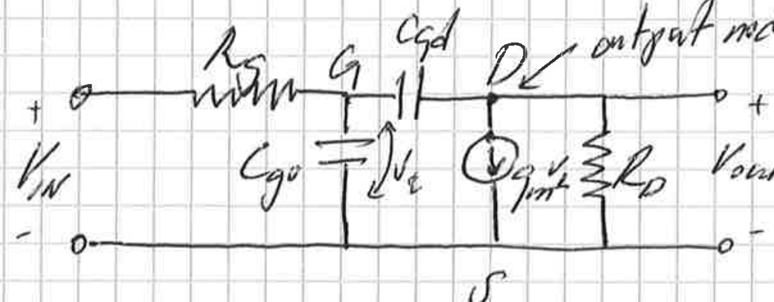
4.

(2016 exam)

a) 

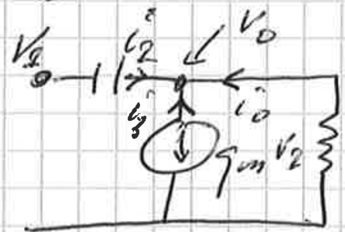
[fig 1]

b) $A_v = \frac{V_o}{V_1}$ at low-f $\Rightarrow A_v = \frac{V_{out}}{V_{IN}} = -g_m R_D$

$C_M = C_{gd}(1 - A_v) = C_{gd}(1 + g_m R_D)$

c) see page 492 in book (analysis and design... ...)

$$\begin{cases} i_1 = (V_1 - V_0)\, s C_{gd} \quad (i) \quad [j\omega] \\ g_m v_1 + \frac{V_0}{R_D} + (V_0 - V_1)\, s C_{gd} = 0 \quad (\text{KCL @ output node}) \quad (ii) \end{cases}$$

[fig 2] $\Rightarrow$ 

$$\begin{cases} -i_1 = (v_0 - v_1)\, s C_{gd} \\ -i_3 = g_m v_1 \\ -i_0 = \frac{V_0}{R_D} \end{cases}$$

find $A_v(s)$

from (ii) $\Rightarrow A_v(s) = -g_m R_D \left(\frac{1 - s\frac{C_{gd}}{g_m}}{1 + s R_D C_{gd}} \right)$

insert in (i) $\Rightarrow i_1 = (1 - A_v(s))\, s C_{gd} V_1$

$= s C_M V_1 \Rightarrow C_M = (1 - A_v(s)) C_{gd}$

when approximating the parasitic the low freq. volt. amp. is used

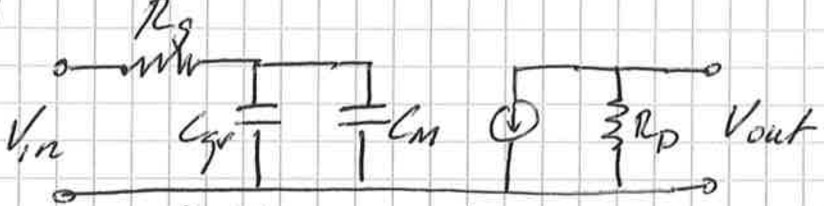
$A_v(s) = A_{v0} \Rightarrow C_M = (1 - A_{v0}) C_{gd}$

Decoupling output from input by approximating current through C_{gd}.

4.

[2016 exam]

d)



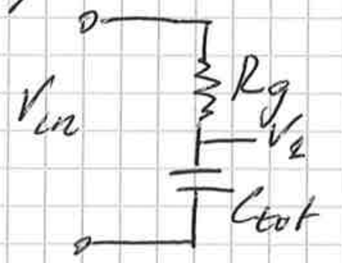
parallell capacitances are added

$\Rightarrow C_{tot} = C_{gs} + C_M = C_{gs} + C_{gd}(1 + g_m R_D)$

looking at the input;

$(s = j\omega)$

$\Rightarrow$



voltage div.

$$\Rightarrow V_1 = \frac{\frac{1}{sC_{tot}}}{R_g + \frac{1}{sC_{tot}}} V_{in} = \frac{1}{1 + sR_g C_{tot}} V_{in}$$

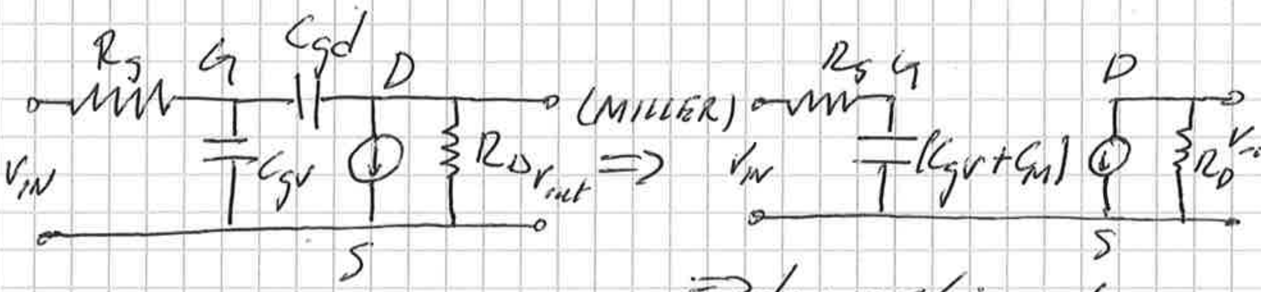
$$H(s) = \frac{V_{out}}{V_{IN}} = -g_m R_D \cdot \frac{1}{1 + sR_g C_{tot}}$$

5. (2016 exam)

$$g_m = \sqrt{2k' \frac{W}{L} I_D} = \sqrt{2 \cdot 60 \cdot 10^{-6} \cdot \frac{100}{2} \cdot 10 \cdot 10^{-3}}$$

$$= 7{,}7 \cdot 10^{-3} \, A/V \qquad (\text{note } R_L = R_D)$$

$$A_v = -g_m R_D = -7{,}7 \cdot 10^{-3} \cdot 5 \cdot 10^{3} = -38{,}5$$



⇒ decoupling of gate and drain with miller approximation

$$C_M = C_{gd}(1 - A_v)$$

$$|p_1| = \frac{1}{R_g (C_{gs} + C_{gd}(1 - A_v))}$$

$$= \frac{1}{10 \cdot 10^{3} (30 \cdot 10^{-12} + 20 \cdot 10^{-12} \cdot 39{,}5)} = 1{,}2 \, Mrad/s$$

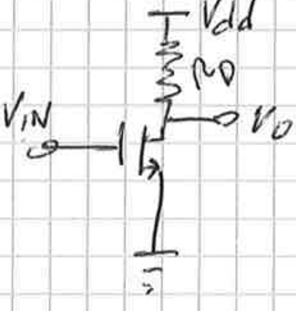
$$f_{-3dB} = \frac{|p_1|}{2\pi} = 0{,}2 \, MHz$$

2016 EXAM

6\.

Common source

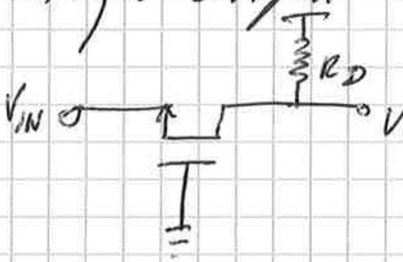
- gives rise to gain
- large input resistance
- load @ drain determines gain



- unilateral
  ⇒ output disconnected from input

Common gate

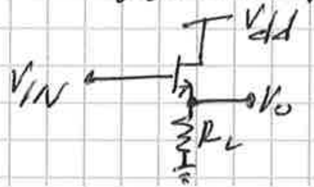
- "current buffer" $i_i = i_o$ (input = output)
- low input resistance
- high output resistance



- bilateral
  output influences input

Common drain

- "voltage buffer" $A_v \leq 1$
- source follower
- low output resistance
  ⇒ works well for an output stage
- level shifter ⇒ offsets the voltage



6. Cascode (CS–CG) p. 207

- two stage amplifier
- increases output resistance
  ⇒ common gate at output
- gain set by a first stage CS transistor
- good high frequency properties
- high input resistance and output resistance ⇒ increased by ~~a factor~~ gain of the second stage