Exam – modern electronics (ETIN70) 2016-10-25 14.00-19.00

GOOD LUCK!
Total number of points = 20
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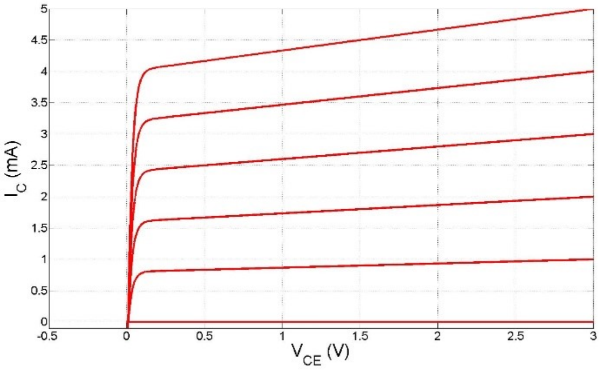
1. BJTs (2p)

In an ideal BJT, I_C should be constant with increasing V_{CE} in the forward active mode. However, in reality the characteristics in the figure below can be obtained.



a) What is the name and origin of the effect causing I_C to not saturate? You are welcome to draw images to explain. (1 p)

Early effect due to increased base-collector depletion width with V_{CE}. This reduces the base width which leads to a higher gradient in minority carrier concentration in the base which increases the diffusion current and I_C.

b) Describe <u>two</u> different modifications you can do in the device design to reduce this effect. Motivate your answers. What detrimental effects (if any) would your suggested modifications have on the transistor performance? (1 p)

1. **Increasing doping in base would result in that the base-collector depletion width would change less with increasing V_{CE} i.e. the base width would not change so much and thus the change in minority carrier gradient would be smaller. However, higher doping would lead to more backinjection from base into emitter increasing I_B and lowering the gain. It may also lead to lower breakdown voltage (avalanche and/or tunneling) for the B-E junction.**

2. A longer base would lead to that the relative change in base width with V_{CE} is smaller and the minority carrier gradient in the base changes less with V_{CE}. However, a longer base leads to a lower I_C (smaller minority carrier gradient), more recombination leading to higher I_B and a higher base resistance (important for high frequency performance).

2. MOSFETs I (4p)

a) Three different Si n-MOSFETs have been measured and the results can be seen in the table below. The source is grounded (V_S=0 V). Fill out the missing information in each row. Note that device 1 has been measured at two different bias conditions. You should present your full calculations for the values and motivate your answers for the operating modes. The three possible operating modes are cut-off, saturation and linear. k´*(W/L) = 44 mA/V^2 for all the devices. (2 p)

Device	V_t [V]	λ [V^{-1}]	V_{GS} [V]	V_{DS} [V]	I_D [mA]	Operating mode
1	**???**	**???**	2.5	2.5	198	**???**
1	**???**	**???**	2.5	3.5	206.8	**???**
2	-0.5	0.02	1	**???**	55	**???**
3	1	0.005	0.8	3	**???**	**???**

Device	V_t [V]	λ [V^{-1}]	V_{GS} [V]	V_{DS} [V]	I_D [mA]	Operating mode
1	**0.5**	**0.05**	**2.5**	**2.5**	**198**	**Saturation**
1	**0.5**	**0.05**	**2.5**	**3.5**	**206.8**	**Saturation**
2	**-0.5**	**0.02**	**1**	**0.5**	**55**	**Linear**
3	**1**	**0.005**	**0.8**	**3**	**0**	**Cut-off**

Device 1: find λ first. The operating mode is saturation since I_D increases only little with 1V V_{DS} difference. Use info in both rows to get

$198 = const * (1 + \lambda*2.5)$

$206 = const * (1 + \lambda*3.5)$

Which gives λ= 0.045. Can now insert this in $198 = 44(2.5 - V_t^2)(1+0.045*2.5)$ which give

$V_t = 2.5 \pm 2 =$ 0.5 V or 4.5 V. If V_t =4.5 V the mosfet would be cut-off and I_D=0 so 0.5 is the correct answer.

Device 2: The operating mode is unknown so test both

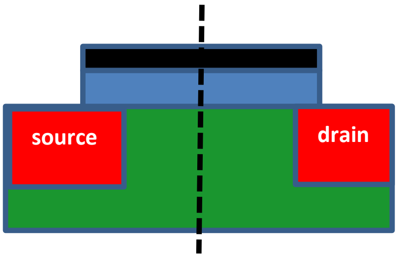
Linear: $55 = 44*(2(1+0.5)*V_{DS}-V_{DS}^2)$ -> solving gives $V_{DS} = (3 \pm sqrt(5)) /2 =$ 2.61 V or 0.5 V. V_{DS} = 2.61 V would be in saturation (2.61 > 1-(-0.5)) so it's incorrect.

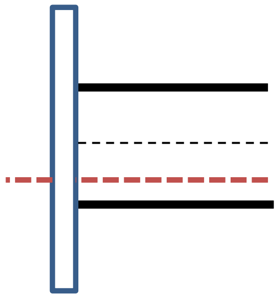
Saturation: $55 = 44*(1+0.5)^2(1+0.02*V_{DS})$ -> V_{DS} = -22V. This is incorrect since a negative V_{DS} could not give a positive I_D (current direction defined from drain to source).

This means that the device is in the linear mode and V_{DS}= 0.5 V.

Device 3: $V_{GS} < V_t$ and thus device is cut-off. Since the channel is not inverted I_D= 0.

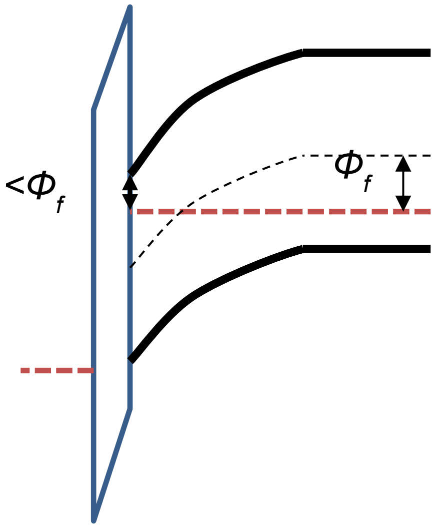
b) Consider device 2 and 3 (at the corresponding bias conditions) in problem 2a. Sketch the band structure perpendicular to the transport direction (similar to the right image) for the position indicated by the dashed line in the figure to left. Make sure you draw the Fermi level position with respect to the bands correctly and indicate any differences for the two cases. (2p)





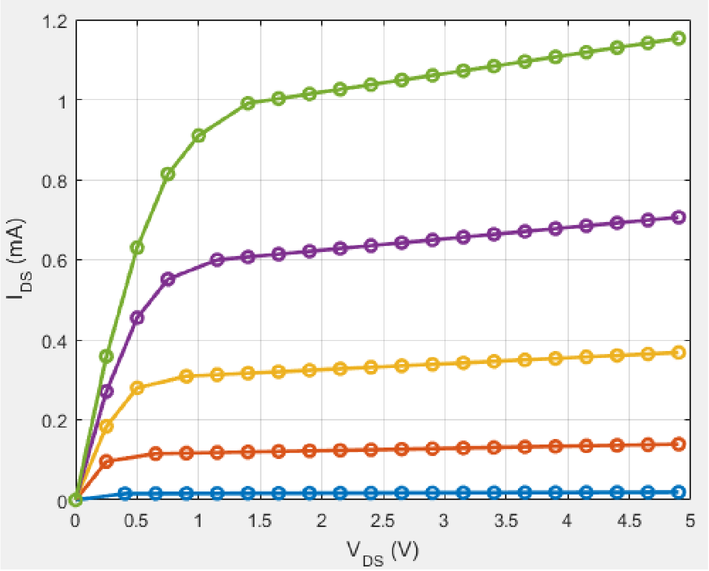
Device 2 is in the linear region i.e. $V_{GS}>V_t$ the Si underneath the gate is inverted. For this case the difference between E_F and E_C as the surface is <u>smaller</u> than the difference between E_F and E_V in the bulk.

Device 3 is in the cut-off region i.e. $V_{GS}<V_t$. For this condition, there is no channel formed since the Si is still only in depletion, intrinsic surface or weak inversion. For this case the difference between E_F and E_C as the surface is <u>larger</u> than the difference between E_F and E_V in the bulk.



3. MOSFETs II (2p)

A n-MOSFET with W=12 µm, L=1.5 µm, V_t=0.6 V and μ_n=350 cm^2/Vs has the following output characteristics for V_{GS}= 0.75, 1, 1.25, 1.5, 1.75 V.



(a) Plot the transconductance as function of V_{GS} at V_{DS}= 3 V. (1 p)

Use the figure to calculate $g_m=dI_{DS}/dV_{GS}$. The V_{GS} points should preferably be inbetween the ones in the figure.

V_{GS}= 0.825 V / g_m = (0.13-0.02)/0.25 = 0.44 mS

V_{GS}= 1.112 V / g_m = (0.34-0.13)/0.25 = 0.84 mS

V_{GS}= 1.37 V / g_m = (0.65-0.34)/0.25 = 1.24 mS

V_{GS}= 1.62 V / g_m = (1.07-0.65)/0.25 = 1.68 mS

(b) Calculate the thickness of the SiO_2 gate dielectric. (1 p)

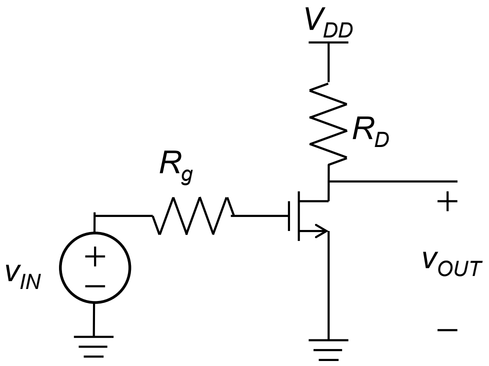
Use a point in the linear region (to avoid taking into account channel length modulation) e.g.

V_{DS}=1, V_{GS}=1.5 V, I_{DS} = 0.9 mA. Using the expression for the linear region and solving for C_{ox} gives

C_{ox}= 0.00494 F/m^2. The thickness of the oxide is then given by $t=\varepsilon_r\varepsilon_0/C_{ox}$ = 6.9 nm.

4. Amplifiers I (5p)

A basic common-source amplifier is shown below.



(a) Draw the schematic small-signal equivalent circuit. (1p)

(b) Calculate the Miller capacitance (1p)

(c) What is the physical origin of the Miller capacitance? (1)

(d) Derive the frequency-dependent transfer function $H(s)=v_o/v_{in}$ (2p)

5. Amplifier II (3p)

Calculate the -3-dB frequency of the small-signal voltage gain of the MOS common-source stage shown above in task Amplifier I. Use the following NMOS transistor data:

R_g=10 kΩ, R_L=5 kΩ, C_{gd}=20 pF, C_{gs}=30 pF, I_d=10 mA, W=100 µm, L=2 µm, k'= 60µA/V^2 (3p)

6. Amplifiers III (4p)

During the course a number of single transistor amplifiers as well as more advanced transistor coupled amplifiers have been discussed. Draw the basic configuration of four different amplifiers and discuss the advantages and characteristic features for the four different amplifiers! (4p)