Exam – Modern Electronics (ETIN70) 2018-11-01 8.00-13.00

GOOD LUCK!
Total number of points = 20 [Grade limits, 3: 10p, 4: 14p, 5: 17p]
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1. BJTs (2p)

a) An engineer made a mistake during fabrication of an NPN BJT and exchanged the doping concentrations in the emitter and collector. How does this affect the electrical characteristics when operated in the forward active mode as compared to "correct" device? (1p)

Ans: Due to the mistake the emitter will have a lower doping than the collector which will be highly doped. Therefore the forward active mode will be the same as the reverse active mode in the "correct" device.

I_C will be reduced due to lower amount of carriers injected into the base from the emitter.

The breakdown voltage will be decreased since the reverse biased B-C junction now has a higher doping on the collector side resulting in tunneling/avalanche breakdown at lower voltages.

b) Describe the name and origin of the largest contribution to the intrinsic (can ignore e.g. overlapping capacitances due to device geometry) capacitance of a BJT operated in the forward active mode. If the base width is doubled, what happens to the capacitance assuming that recombination in the base and the Early effect can be neglected? (1p)

The base charging capacitance dominates. The physical origin is the change in the amount of charge injected into the base from the emitter when changing V_{BE}. It's given by $C_b = \tau_F g_m$ (from sheet of formulas). As the base width is doubled, g_m is halved due to the smaller I_C (due to the smaller concentration gradient). However the base transit time increases as (base width)^2 since the both the distance is doubled and the minority carrier concentration gradient is halved. This means that the capacitance is doubles as the base width is doubled.

2. MOSFETs (4p)

a) Three different Si n-MOSFETs have been measured and the results can be seen in the table below. The source is grounded (V_S=0 V). Fill out the missing information in each row. Note that device 1 has been measured at two different bias conditions. You should present your full calculations for the values and motivate your answers for the operating modes. The three possible operating modes are cut-off, saturation and linear. k´/2*(W/L) = 2 mA/V^2 for all the devices. (2 p)

Device	V_t [V]	λ [V^{-1}]	V_{GS} [V]	V_{DS} [V]	I_D [mA]	Operating mode
1	**???** **0.25**	**???** **0.09**	0.75	1	0.545	**???** **Saturation**
1	**???** **0.25**	**???** **0.09**	1.75	1	4	**???** **linear**

2	0.5	0.03	2	2	**???** **4.77**	**???** **Saturation**
3	-0.5	0.05	**???** **1**	2	4.95	**???** **Saturation**

Device 1: if operating mode for first 2nd bias point is saturation, bias point for 1st also has to be in saturation since the V_{GS} is lower. However assuming saturation for both bias points gives a Vt (~0.17 V) which does not fulfil the condition for saturation for point 2. Assuming linear for both gives Vt=0.11 from bias point 1, however inserting in bias point 2 gives the wrong ID. This means that bias point 1 must be saturation and bias point 2 must be linear.

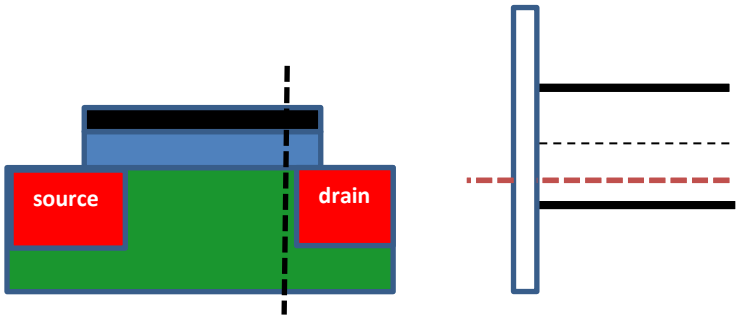
Point 1: 2*(0.75-Vt)^2*(1+ λ*1) = 0.545 mA

Point 2: 2*(2*(1.75-Vt)*1-1^2) = 4 mA -> Vt= 0.25 V which can be inserted in 1 to obtain $\lambda=0.09\ V^{-1}$

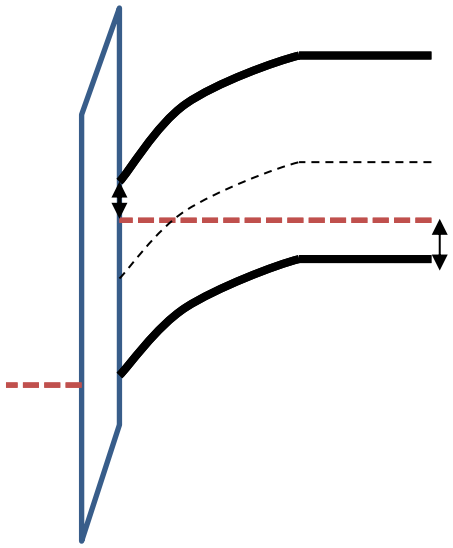
Point 3: Since VDS > VGS –Vt this is saturation which gives ID=2*(2-0.5)^2*(1+0.03*2) = 4.77 mA

Point 4: Test with linear gives 2*(2*(VGS+0.5)*2-2^2)) = 4.95 mA which gives VGS=1.12 V, however since VDS > VGS –Vt the point can be in the linear region. Saturation gives 2*(VGS+0.5)^2*(1+0.05*2)=4.95 mA which gives VGS=1 V which fulfils the requirement for being in saturation.

b) A MOSFET with V_t =1 V and $\lambda=0.1\ V^{-1}$ is biased at V_{DS}=1 V / V_{GS}=3 V and at V_{DS}=3 V / V_{GS}=2 V. Sketch the band structure perpendicular to the transport direction for these two bias points (similar to the right image) at the position close to the drain indicated by the dashed line in the figure to left. Make sure you draw the Fermi level position with respect to the bands correctly and indicate any differences for the two cases. (2 p)



The first bias point is in the linear region i.e. there is still a channel formed under the gate close to the drain i.e. the bands and bent to achieve strong inversion and the energy difference between E_F and E_C at the surface is smaller than that between E_F and E_V in the bulk.



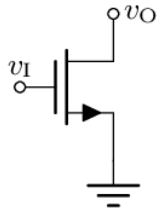
The second bias point is in the saturation region and since there is considerable channel length modulation at this high V_{DS} the pinch off point has move away from the drain and into the channel (decreasing the effective channel length which increases the current). Here the MOS band structure is only in weak inversion and there is no channel formed under the gate close to the drain.

3 – Linear Amplifier Concepts **(4p)**

Consider an n-MOSFET in common source (CS) configuration and its characteristics when operated as a linear amplifier element. The amplifier is fed from a signal source with resistance, r_S, and it feeds a load resistance, r_L. Neglect the body effect and all capacitances, internal and external, but take channel length modulation into account.

a) Draw the transistor symbol, then denote the input and output terminal voltages, v_I and v_O, and connect their common reference terminal to a suitable reference symbol. (0.5p)
b) Assume an appropriate mode of operation, then linearize the MOSFET drain current equation, $i_D(v_{GS}) = i_D(V_{GS} + v_{gs}) = I_D + i_d(v_{gs})$, and specify the associated small signal condition on the input voltage in relation to the overdrive voltage. (1.5p)
c) Draw the CS amplifier small signal schematic and use it to derive the input resistance, the output resistance, and the open circuit voltage gain. (1.0p)
d) Derive the voltage gain of the CS amplifier, then evaluate the result for the following list of load resistances, $r_L = \infty$, r_o, $\frac{1}{g_m}$, and 0. (1.0p)

a) Transistor symbol with source connected to ground, v_I on gate, and v_O on drain. Use of a bias circuit is optional.



b) Saturation is the appropriate mode of operation.

Drain current expression including channel length modulation

$$i_D(v_{GS}) = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2(1 + \lambda v_{DS})$$

insert quiescent and small signal components

$$v_{GS} = V_{GS} + v_{gs}$$

group constants

$$V_{GS} - V_{tn} = V_{OV}$$

expand the product

$$i_D(V_{GS} + v_{gs}) = \frac{1}{2}k_n'\left(\frac{W}{L}\right)[V_{OV}^2 + 2V_{OV}v_{gs} + v_{gs}^2](1 + \lambda v_{DS}) = I_D(V_{GS}) + i_d(v_{gs})$$

identify the small signal component

$$i_d(v_{gs}) = \frac{1}{2}k_n'\left(\frac{W}{L}\right)[2V_{OV}v_{gs} + v_{gs}^2](1 + \lambda v_{DS})$$

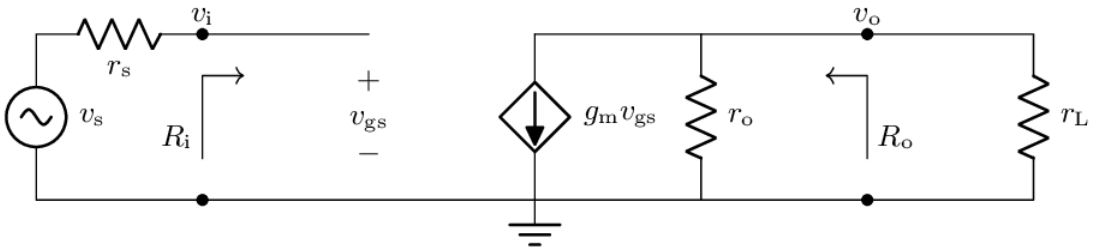
linearize the small signal drain current component (discard non-linear terms)

$$i_d(v_{gs}) \approx k_n'\left(\frac{W}{L}\right)V_{OV}v_{gs}(1 + \lambda v_{DS})$$

which is valid under the condition

$$2V_{OV}v_{gs} \gg v_{gs}^2 \Rightarrow v_{gs} = v_i \ll 2V_{OV}$$

c) Hybrid pi small signal model



Input resistance, $R_i = \frac{v_i}{i_i} = \frac{v_{gs}}{i_g} = \frac{v_{gs}}{0} = \infty$

Output resistance, $R_o = \frac{v_o}{i_o}\Big|_{v_i=0} = \frac{v_{ds}}{i_d}\Big|_{v_{gs}=0} = r_o$

Open circuit voltage gain, $A_{vo} = \frac{v_o}{v_i}\Big|_{r_L=\infty} = -g_m R_o = -g_m r_o$

d) Voltage gain includes load effect, $A_v = \frac{v_o}{v_i} = -g_m(R_o||r_L) = -g_m(r_o||r_L) = -g_m\frac{r_o r_L}{r_o + r_L}$

$$r_L = \infty \rightarrow r_o||r_L = r_o \rightarrow A_v = -g_m r_o$$

$$r_L = r_o \rightarrow r_o||r_L = \frac{r_o}{2} \rightarrow A_v = \frac{-g_m r_o}{2}$$

$$r_L = \frac{1}{g_m} \rightarrow r_o||r_L = \frac{r_o}{1 + g_m r_o} \rightarrow A_v = \frac{-g_m r_o}{1 + g_m r_o}$$

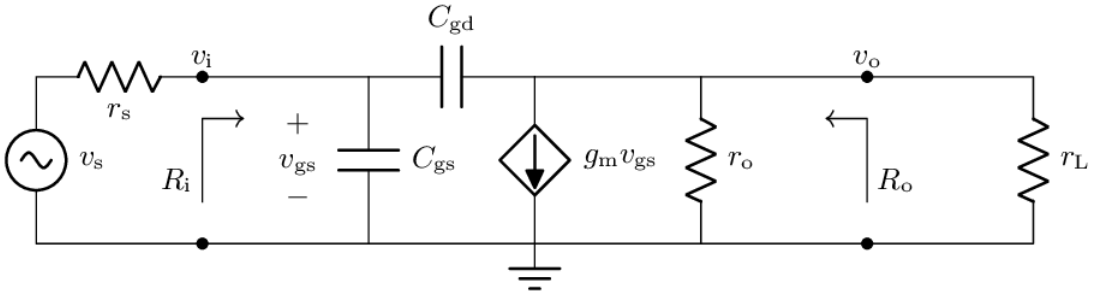
$$r_L = 0 \rightarrow r_o||r_L = r_o \rightarrow A_v = (-)0$$

4 – Cascode Amplifier **(4p)**

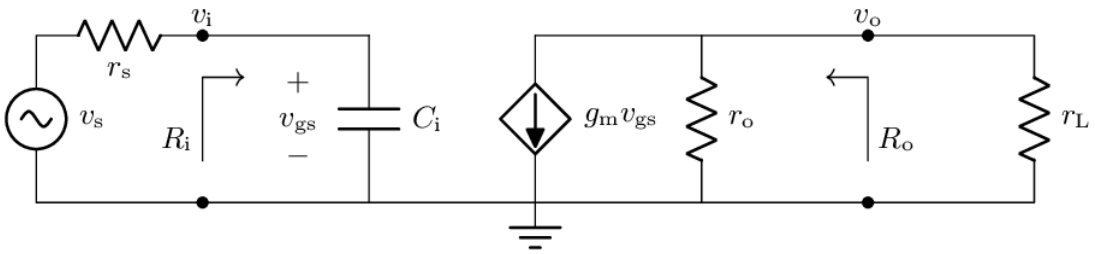
Analyze a cascode amplifier that consists of two integrated n-MOSFETs, which feeds a load resistance, $r_L = r_o$. Assume that the transistor sizes are matched, an intrinsic voltage gain $A_0 = 10$, and gate capacitances to source and drain where $C_{gs} = 10C_{gd}$. Also, the amplifier is fed from a signal source with resistance $r_S = r_o$. Neglect the body effect and external capacitances, but take channel length modulation into account. Note that it is instructive to think about the cascode amplifier as the combination of two separate amplifier stages.

a) Use Miller's theorem (approximation) and a time constant method to estimate the frequency bandwidth of a (standalone) CS amplifier (fed by the same source, and loaded directly by the load resistance, effectively omitting the CG stage of the cascode). (1.5p)
b) Derive the low frequency (neglect capacitances) load transformation of the CG amplifier stage of the cascade, for example by measuring the resistance seen looking into its input (use KCL node equations at source and drain to track the test current, followed by a KVL loop equation to determine the test voltage). (1.0p)
c) Use the methods and results from above to derive the low frequency partial gain and the input frequency bandwidth in the CS amplifier stage of a cascode amplifier (not the full gain of the whole cascode amplifier, and neglect capacitances of the CG stage). (1.0p)
d) How does the cascode amplifier frequency bandwidth compare to a (standalone) CS amplifier, if as above dominated by the Miller effect of the input CS amplifier stage? (0.5p)

a) Standalone CS amplifier small signal hybrid pi model before Miller approximation



Miller approximation is to model the feedback capacitor C_{gd} with an effective Miller capacitor C_M in parallel to C_{gs}, yielding an effective input capacitance, $C_i = C_{gs} + C_M$



Miller capacitance

$$C_M = (1 + g_m R_L)C_{gd} = \left(1 + g_m(r_o||r_L)\right)C_{gd} = \left(1 + \frac{g_m r_o}{2}\right)C_{gd} = \left(1 + \frac{A_0}{2}\right)C_{gd} = 6C_{gd}$$

Method of OCTCs on effective input capacitor and source resistance

$$C_1 = C_i = C_{gs} + C_M = (10+6)C_{gd} = 16C_{gd}$$
$$R_{10} = r_s = r_o$$
$$\tau_H = \frac{1}{\omega_H} = \sum_k C_k R_{k0} = 16C_{gd}r_o$$

Bandwidth is identical to high corner frequency, derived from high corner angular frequency that is inverse of effective time constant from OCTC

$$f_H|_{standalone} = \frac{\omega_H}{2\pi} = \frac{1}{32\pi C_{gd}r_o}$$

b) Standalone CG amplifier small signal T model (low frequency)

THIS IS FOUND IN THE LECTURE NOTES

KCL on source node

KCL on drain node

KVL from input impedance probe to load

Identify and insert

$$v_{gs} = -v_x$$

Perform algebraic manipulation

$$R_{iCG} = \frac{v_x}{i_x} = \frac{r_o + r_L}{1 + g_m r_o} = \frac{2}{11}r_o$$

c) Use input resistance of CG amplifier as load resistance for input CS stage of cascode amplifier, then repeat previous analysis

$$A_v = -g_m(r_o||R_{iCG}) = -g_m\left(r_o||\frac{2}{11}r_o\right) = \frac{-2}{13}g_m r_o = \frac{-20}{13} = 1.538\ldots$$

Miller capacitance

$$C_M = \left(1 + \frac{2}{13}g_m r_o\right)C_{gd} = \left(1 + \frac{20}{13}\right)C_{gd} = \frac{33}{13}C_{gd} = 2.538\ldots C_{gd}$$

Input capacitance

$$C_i = \left(10 + \frac{33}{13}\right)C_{gd} = \frac{163}{13}C_{gd} = 12.54\ldots C_{gd}$$

Time constant (resistance is same as before)

$$\tau_H = \frac{1}{\omega_H} = \sum_k C_k R_{k0} = \frac{163}{13}C_{gd}r_o = 12.54\ldots C_{gd}r_o$$

Frequency bandwidth (corner frequency)

$$f_H|_{cascode\ input} = \frac{\omega_H}{2\pi} = \frac{13}{326\pi C_{gd}r_o} = \frac{1}{25.08\ldots\pi C_{gd}r_o}$$

d) Compare bandwidths

$$f_H|_{cascode\ input}/f_H|_{standalone} = 32/25.08\ldots = 1.276\ldots$$

Cascade input stage (under these specific source and load conditions) has 28% higher bandwidth as compared to a standalone common source stage.

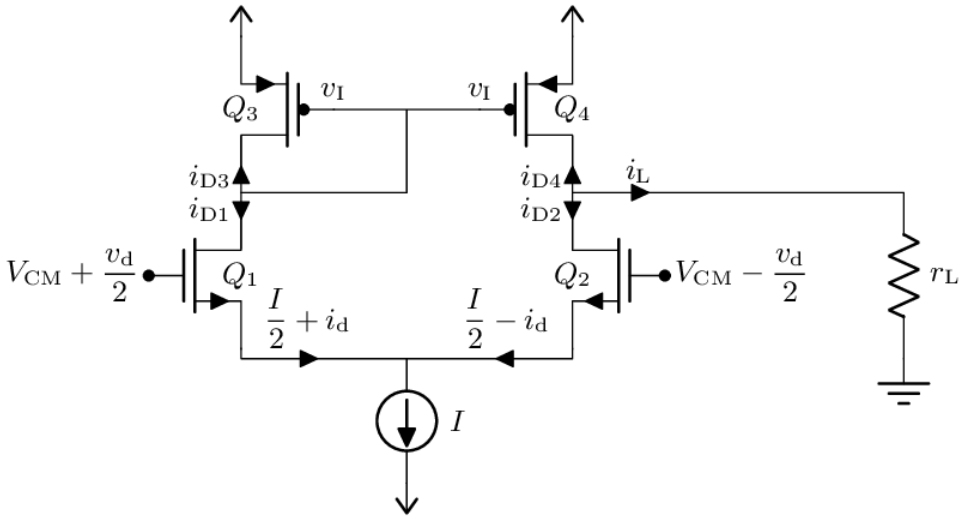
5 – Differential Amplifier **2p**

A differential amplifier with single ended output onto a load resistance, r_L, can be formed from the combination of an n-MOSFET differential pair (biased by a current sink, I) and a p-MOSFET current mirror. A differential input voltage is applied, producing a differential current, i_d, through the source nodes of the differential pair.

a) Draw the circuit schematic, then denote and quantify (ideal) bias and small signal components of the MOSFET drain currents, i_D, and the load current, i_L. (1.0p)

b) Why can we not use differential and common mode half circuits to analyze the characteristics of this MOSFET differential amplifier in detail? (1.0p)

a) Schematic of differential amplifier with all drain and load currents denoted



Ideal current components can be quantified

$$i_{D1} = \frac{I}{2} + i_d, \qquad i_{D2} = \frac{I}{2} - i_d, \qquad i_{D3} = -\frac{I}{2} - i_d, \qquad i_{D4} = i_{D3}$$

$$i_L = -i_{D2} - i_{D4} = 2i_d$$

b) Differential and common mode half circuits are only valid for symmetric circuits. The current mirror does not have equal input and output impedances. It thereby does not load the differential pair symmetrically.

6 – Memory Cells **(4p)**

Digital systems in CMOS technology frequently employ 6T static random access memory (SRAM) and 1T dynamic random access memory (DRAM) cells in memory blocks to enable sequential logic. Assume for read operations that the bit lines are precharged to the drive voltage, $v_B = v_{\bar{B}} = V_{DD}$, when the word line is activated, $v_W = V_{DD}$. Assume for write operations that the bit lines are precharged to desired data, $v_B = v_{Qn+1}$ and $v_{\bar{B}} = v_{\overline{Qn+1}}$, when the word line is activated, $v_W \geq V_{DD}$.

a) Draw the schematic of a 6T SRAM cell and denote the transistors Qn (pull down), Qp (pull up), and Qa (access). Also, assign the output of the left inverter in the latch to hold complemented

data $\bar{Q}$ and denote Q, S, R, and ϕ on their corresponding nodes. Finally, connect a word line, W, and bit lines, B and $\bar{B}$, to the appropriate terminals. (1.0p)

b) State the design criterion of $v_{\bar{Q}}$ for a non-destructive read logic 1 operation on the 6T SRAM cell and explain why it is achieved by appropriately limiting the size of the access transistor, Qa, in relation to the latch pull down transistor, Qn. (1.0p)

c) Draw the schematic of a 1T DRAM cell using an access transistor, Qa, and a storage capacitor, C_s, then denote the storage node Q and connect word and bit lines, W and B. (1.0p)

d) Explain why the word line should be boosted during the write logic 1 operation, $v_{Qn+1} = V_{DD}$, on a 1T DRAM cell? (1.0p)

a) Schematic of SRAM cell

b) Criterion $v_{\bar{Q}} < V_{tn}$ is used to design SRAM memory cell
This criterion requires, under steady state reading from bit lines held at the drive voltage, Qn (triode) to be big enough to conduct away the charges injected by Qa (saturation).

c) Schematic of DRAM cell

d) To avoid access the cutoff region of Qa for $v_Q > V_{DD} - V_{tn}$, which would not allow complete charging of the storage node to the drive voltage.