Exam – Modern Electronics (ETIN70) 2018-11-01 8.00-13.00

GOOD LUCK!
Total number of points = 20 [Grade limits, 3: 10p, 4: 14p, 5: 17p]
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1. BJTs (2p)

a) An engineer made a mistake during fabrication of an NPN BJT and exchanged the doping concentrations in the emitter and collector. How does this affect the electrical characteristics when operated in the forward active mode as compared to "correct" device? (1p)

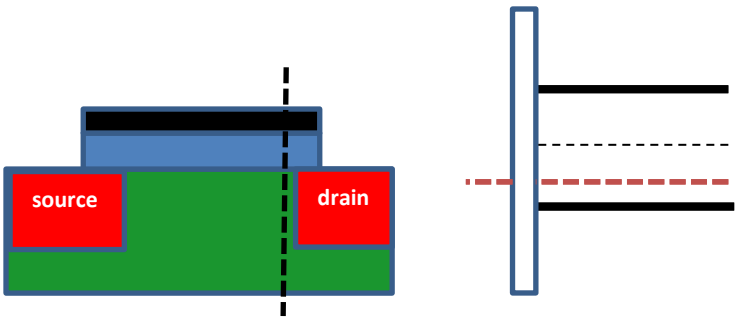
b) Describe the name and origin of the largest contribution to the intrinsic (can ignore e.g. overlapping capacitances due to device geometry) capacitance of a BJT operated in the forward active mode. If the base width is doubled, what happens to the capacitance assuming that recombination in the base and the Early effect can be neglected? (1p)

2. MOSFETs (4p)

a) Three different Si n-MOSFETs have been measured and the results can be seen in the table below. The source is grounded (V_S=0 V). Fill out the missing information in each row. Note that device 1 has been measured at two different bias conditions. You should present your full calculations for the values and motivate your answers for the operating modes. The three possible operating modes are cut-off, saturation and linear. k´/2*(W/L) = 2 mA/V^2 for all the devices. (2 p)

Device	V_t [V]	λ [V^{-1}]	V_{GS} [V]	V_{DS} [V]	I_D [mA]	Operating mode
1	**???**	**???**	0.75	1	0.545	**???**
1	**???**	**???**	1.75	1	4	**???**
2	0.5	0.03	2	2	**???**	**???**
3	-0.5	0.05	**???**	2	4.95	**???**

b) A MOSFET with V_t =1 V and λ=0.1 V^{-1} is biased at V_{DS}=1 V / V_{GS}=3 V and at V_{DS}=3 V / V_{GS}=2 V. Sketch the band structure perpendicular to the transport direction for these two bias points (similar to the right image) at the position close to the drain indicated by the dashed line in the figure to left. Make sure you draw the Fermi level position with respect to the bands correctly and indicate any differences for the two cases. (2 p)



3 – Linear Amplifier Concepts **(4p)**

Consider an n-MOSFET in common source (CS) configuration and its characteristics when operated as a linear amplifier element. The amplifier is fed from a signal source with resistance, r_S, and it feeds a load resistance, r_L. Neglect the body effect and all capacitances, internal and external, but take channel length modulation into account.

a) Draw the transistor symbol, then denote the input and output terminal voltages, v_I and v_O, and connect their common reference terminal to a suitable reference symbol. (0.5p)
b) Assume an appropriate mode of operation, then linearize the MOSFET drain current equation, $i_D(v_{GS}) = i_D(V_{GS} + v_{gs}) = I_D + i_d(v_{gs})$, and specify the associated small signal condition on the input voltage in relation to the overdrive voltage. (1.5p)
c) Draw the CS amplifier small signal schematic and use it to derive the input resistance, the output resistance, and the open circuit voltage gain. (1.0p)
d) Derive the voltage gain of the CS amplifier, then evaluate the result for the following list of load resistances, $r_L = \infty$, r_o, $\frac{1}{g_m}$, and 0. (1.0p)

4 – Cascode Amplifier **(4p)**

Analyze a cascode amplifier that consists of two integrated n-MOSFETs, which feeds a load resistance, $r_L = r_o$. Assume that the transistor sizes are matched, an intrinsic voltage gain $A_0 = 10$, and gate capacitances to source and drain where $C_{gs} = 10C_{gd}$. Also, the amplifier is fed from a signal source with resistance $r_S = r_o$. Neglect the body effect and external capacitances, but take channel length modulation into account. Note that it is instructive to think about the cascode amplifier as the combination of two separate amplifier stages.

a) Use Miller's theorem (approximation) and a time constant method to estimate the frequency bandwidth of a (standalone) CS amplifier (fed by the same source, and loaded directly by the load resistance, effectively omitting the CG stage of the cascode). (1.5p)
b) Derive the low frequency (neglect capacitances) load transformation of the CG amplifier stage of the cascade, for example by measuring the resistance seen looking into its input (use KCL node equations at source and drain to track the test current, followed by a KVL loop equation to determine the test voltage). (1.0p)
c) Use the methods and results from above to derive the low frequency partial gain and the input frequency bandwidth in the CS amplifier stage of a cascode amplifier (not the full gain of the whole cascode amplifier, and neglect capacitances of the CG stage). (1.0p)
d) How does the cascode amplifier frequency bandwidth compare to a (standalone) CS amplifier, if as above dominated by the Miller effect of the input CS amplifier stage? (0.5p)

5 – Differential Amplifier **2p**

A differential amplifier with single ended output onto a load resistance, r_L, can be formed from the combination of an n-MOSFET differential pair (biased by a current sink, I) and a p-MOSFET current mirror. A differential input voltage is applied, producing a differential current, i_d, through the source nodes of the differential pair.

a) Draw the circuit schematic, then denote and quantify (ideal) bias and small signal components of the MOSFET drain currents, i_D, and the load current, i_L. (1.0p)
b) Why can we not use differential and common mode half circuits to analyze the characteristics of this MOSFET differential amplifier in detail? (1.0p)

6 – Memory Cells **(4p)**

Digital systems in CMOS technology frequently employ 6T static random access memory (SRAM) and 1T dynamic random access memory (DRAM) cells in memory blocks to enable sequential logic. Assume for read operations that the bit lines are precharged to the drive voltage, $v_B = v_{\bar{B}} = V_{DD}$, when the word line is activated, $v_W = V_{DD}$. Assume for write operations that the bit lines are precharged to desired data, $v_B = v_{Qn+1}$ and $v_{\bar{B}} = v_{\overline{Qn+1}}$, when the word line is activated, $v_W \geq V_{DD}$.

a) Draw the schematic of a 6T SRAM cell and denote the transistors Qn (pull down), Qp (pull up), and Qa (access). Also, assign the output of the left inverter in the latch to hold complemented data $\bar{Q}$ and denote Q, S, R, and ϕ on their corresponding nodes. Finally, connect a word line, W, and bit lines, B and $\bar{B}$, to the appropriate terminals. (1.0p)
b) State the design criterion of $v_{\bar{Q}}$ for a non-destructive read logic 1 operation on the 6T SRAM cell and explain why it is achieved by appropriately limiting the size of the access transistor, Qa, in relation to the latch pull down transistor, Qn. (1.0p)
c) Draw the schematic of a 1T DRAM cell using an access transistor, Qa, and a storage capacitor, C_S, then denote the storage node Q and connect word and bit lines, W and B. (1.0p)
d) Explain why the word line should be boosted during the write logic 1 operation, $v_{Qn+1} = V_{DD}$, on a 1T DRAM cell? (1.0p)