Modern Electronics (ETIN70) – Formula

BJTs

Collector current (A) $$I_C = I_S\left(1+\frac{V_{CE}}{V_A}\right)e^{\frac{V_{BE}}{V_T}}$$

Transconductance (A/V) $$g_m = \frac{I_C}{V_T}$$

Input resistance (Ω) $$r_\pi = \frac{\beta}{g_m}$$

Output resistance (Ω) $$r_o = \frac{V_A}{I_C}$$

Base-charging capacitance (F) $$C_b = \tau_F g_m$$

I_s: saturation current (A)
V_{CE}: collector-emitter voltage (V)
V_A: Early voltage (V)
V_{BE}: base-emitter voltage (V)
V_T: thermal voltage = k*T/q = 26 mV at T=300 K (k: Boltzmann constant = 8.61733 x 10^{-5} (eV K^{-1}) or 1.38065×10^{-23} (J K^{-1}))
β: small-signal current gain
τ_F: base transit time (s)

MOSFETs

Drain current (triode/linear region) (A) $$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS}-V_t)V_{DS}-V_{DS}^2\right]$$

($k_n' = \mu_n C_{ox}$)

Drain current (active/saturation region) (A) $$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})$$

Transconductance (A/V) $$g_m = \sqrt{2\cdot\mu_n\cdot C_{ox}\frac{W}{L}I_D}$$

Output resistance (Ω) $$r_o = \frac{1}{\lambda I_{DS}}$$

Gate-source capacitance per unit area (saturation region) (F/m^2) $$C_{gs} = \frac{2}{3}WLC_{ox}$$

Transition frequency $$\frac{1}{2\pi f_T} = \frac{C_{gs}+C_{gd}}{g_m} + \frac{C_{gs}+C_{gd}}{g_m}\cdot(R_S+R_D)g_d + (R_S+R_D)C_{gd}$$

μ_n: electron mobility (m^2/Vs)
C_{ox}: gate oxide capacitance per unit area (F/m^2)
W: channel (gate) width (m)
L: channel (gate) length (m)
V_{GS}: gate-source voltage (V)
V_{DS}: drain-source voltage (V)
V_t: threshold voltage (V)
λ: channel length modulation parameter (V^{-1})
C_{gd}: gate-drain capacitance per unit area (F/m^2)
C_{gs}: gate-source capacitance per unit area (F/m^2)
R_S: source resistance (Ω)
R_D: drain resistance (Ω)
g_d: output conductance (A/V)

Amplifier characteristics

Source theorem $v_{oc} = R_s i_{sc}$

Load resistance power match $R_L = R_s$

Signal gain parameters $A_{vo} = \frac{v_o}{v_i}\Big|_{i_o=0}$, $A_{is} = \frac{i_o}{i_i}\Big|_{v_o=0}$,
$G_m = \frac{i_o}{v_i}\Big|_{v_o=0}$, $R_m = \frac{v_o}{i_i}\Big|_{i_o=0}$

Port resistances $R_i = \frac{v_i}{i_i}\Big|_{v_o=0}$, $R_o = \frac{v_o}{i_i}\Big|_{v_i=0}$

Signal gain relations $R_i A_{vo} = A_{is} R_o = R_i G_m R_o = R_m$

Intrinsic gain $A_0 = g_m r_o \gg 1$

Common source amplifier

Input resistance $R_i = \infty$

Output resistance $R_o = r_o$

Open circuit voltage gain $A_{vo} = -g_m R_o$

Voltage gain $A_v = -g_m(R_o || R_L)$

Common gate amplifier

Input resistance $R_i = \frac{r_o + R_L}{1 + g_m r_o}$ (load transformation)

Output resistance $R_o = r_o + (1 + g_m r_o) R_s$ (source transformation)

Open circuit voltage gain $A_{vo} = g_m R_o$

Common drain amplifier

Input resistance $R_i = \infty$

Output resistance $R_o = \frac{1}{g_m} \left|| r_o \right|| \frac{1}{g_{mb}}$

Open circuit voltage gain $A_{vo} = \frac{r_o}{r_o + \frac{1}{g_m}}$

Cascode MOS amplifier

Input resistance $R_i = \infty$

Output resistance $R_o = K r_{o1}$, where $K > 1$ depends on the CG stage

Open circuit voltage gain $A_{vo} = -g_m R_o$

MOS current mirror

Large signal current transfer $I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF}(1 + \lambda_2 [V_O - V_{GS}])$

Input resistance $R_i = r_{o1} || \frac{1}{g_{m1}}$

Output resistance $R_o = r_{o2}$

Small signal current gain $A_{is} = g_{m2}\left(r_{o1} || \frac{1}{g_{m1}}\right)$

MOS differential pair

Bias current to overdrive relation	$V_{OV} = \sqrt{\frac{I}{k_n'(W/L)}}$
Input operating range	$-\sqrt{2}V_{OV} < v_{id} < \sqrt{2}V_{OV}$
Drain/ gate quiescent levels	$V_D = V_{DD} - \frac{R_D I}{2}, V_G = V_{CM}$
Two-input amplification	$v_o = A_d(v_2 - v_1) + A_{cm}\left(\frac{v_2+v_1}{2}\right)$
Differential gain	$A_d = g_m(r_o \| \| r_D)$ where $r_D = R_{DD} \| \| R_L$
Common mode rejection ratio	$CMMR = \frac{-2g_m R_{SS}}{(\Delta R_D/R_D)+(\Delta g_m/g_m)}$
Input referred DC offset voltage	$V_{OS} = \sqrt{\left(\frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{V_{OV}}{2}\frac{\Delta(W/L)}{(W/L)}\right)^2 + (\Delta V_{tn})^2}$

CMOS differential amplifier

Differential gain	$A_d \approx g_m(r_{o2} \| \| r_{o4})$
Common mode gain	$A_{cm} \approx -1/(2g_m R_{SS})$

Frequency response

Miller approximation	$C_M = [1 + g_m(r_o \| \| R_L)]C_{gd}$
Transfer function	$T_n^m(s) = \frac{\sum_{k=0}^{m}(a_k s^k)}{\sum_{l=0}^{n}(a_l s^l)} = a_m \frac{\prod_{i=1}^{m}(s+Z_i)}{\prod_{j=1}^{n}(s+P_j)} = A\frac{\prod_{i=1}^{m}\left(1+\frac{s}{\omega_{Zi}}\right)}{\prod_{j=1}^{n}\left(1+\frac{s}{\omega_{Pj}}\right)}$
Single time constant high pass	$F_L(s) = T_{n=1}^{m=1}(s) = K\frac{1}{1-j\omega\tau_L}$
Low corner dominant pole	$\tau_{Pmin} = \frac{1}{\omega_{Pmax}} \approx 1/\sqrt{\sum_{j=1}^{n}\omega_{Pj} - 2\sum_{i=1}^{m}\omega_{Zi}}$
Method of SCTCs approximation	$\tau_L = \frac{1}{\omega_L} \approx 1/\sum_k \frac{1}{C_k R_{k0}}$
Single time constant low pass	$F_H(s) = T_{n=1}^{m=0}(s) = K\frac{1}{1+j\omega\tau_H}$
High corner dominant pole	$\tau_{Pmax} = \frac{1}{\omega_{Pmin}} \approx \sqrt{\sum_{j=1}^{n}\frac{1}{\omega_{Pj}} - 2\sum_{i=1}^{m}\frac{1}{\omega_{Zi}}}$
Method of OCTCs approximation	$\tau_H = \frac{1}{\omega_H} \approx \sum_k C_k R_{k0}$

Feedback analysis

Open loop gain	A
Feedback factor	β
Loop gain	$A\beta$
Amount of feedback	$(1 + A\beta)$
Closed loop gain	$A_f = A/(1 + A\beta)$

Output stages

Energy conservation $P_L + P_D = P_I + P_S$

Power efficiency $\eta = \frac{P_L}{P_S + P_I}$

Class A power efficiency $\eta_A \leq \frac{1}{4}\left(\frac{\widehat{V_o}}{IR_L}\right)\left(\frac{\widehat{V_o}}{V_{DD}}\right)$

Class B power efficiency $\eta_B = \frac{\pi}{4}\left(\frac{\widehat{V_o}}{V_{DD}}\right)$

Digital logic

De Morgan's law $\overline{A + B} = \bar{A}\bar{B} \Leftrightarrow \overline{AB} = \bar{A} + \bar{B}$

Operation midpoint V_M

Low state noise margin $NM_L = V_{OL} - V_{IL}$

High state noise margin $NM_H = V_{OH} - V_{IH}$

Charging transient $y(t) = Y_\infty - (Y_\infty - Y_{0+}) \exp\left(-\frac{t}{\tau}\right)$

Active charging equation $\Delta Q = I\Delta t = C\Delta V$

Inverter propagation delay $t_P = \frac{1}{2}(t_{PHL} + t_{PLH})$

Inverter (Q1-Q2) output capacitance $C = 2\left(C_{gd1} + C_{gd2}\right) + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$

Inverter dynamic power dissipation $P_{dynamic} = fCV_{DD}^2$

Inverter power delay product $PDP = P_D \times t_P$

Inverter energy delay product $EDP = PDP \times t_P$

Memory circuits

Clocked SR flip flop access criterion $\left(\frac{W}{L}\right)_{5,6} > 2\frac{k_p'}{k_n'}\left(\frac{W}{L}\right)_2$

Clocked SP flip flop propagation criterion $T > T_{min} = (t_{PHL})_{Qeq-Q2} + (t_{PLH})_{Q3-Q4}$

6T SRAM read criterion $\frac{(W/L)_a}{(W/L)_n} < 1/\left(\frac{V_{tn}}{V_{DD} - V_{tn}}\right)^2 - 1$

6T SRAM write criterion $\frac{(W/L)_p}{(W/L)_a} < \frac{k_n'}{k_p'}\left[1 - \left(1 - \frac{V_{tx}}{V_{DD} - V_{tx}}\right)^2\right]$

1T DRAM boost level $V_w = V_{DD} + V_{tn}$