Advanced AD/DA converters

Example of CT ΔΣ Modulator

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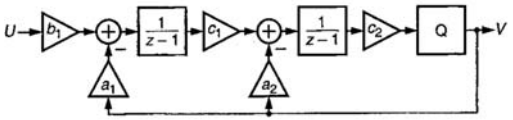
Overview

- 2nd-order CT modulator

2nd-order DT modulator (already treated)



Parameter	Symbol	Value	Units
Bandwidth	f_B	~1	kHz
Sampling Frequency	f_s	1	MHz
Signal-to-Noise Ratio	SNR	100	dB
Supply Voltage	VDD	3	V

a = 0.2653, 0.2212

b = 0.2653, 0, 0

c = 0.3185, 5.5874 (c_2 is not important in a single-bit quantizer)

Rounding →

a_1 = 1/4, a_2 = 1/4, b_1 = 1/4, c_1 = 1/3

From simulations, effective quantizer gain (including c_2) is approx. 16/3, and the NTF is

$$NTF(z) = \left(\frac{z-1}{z-1/3}\right)^2$$

2nd-order CT modulator

Microphone front-end, micropower operation (50μA, 1.8V), no pre-amp and anti-alias → CT DSM with input range of ±20mV, OSR≈300 – we want to achieve an SNR of 80dB

Parameter	Symbol	Value	Units
Signal band	B	100-10k	Hz
Supply Voltage	VDD	1.8	V
Current Consumption	IDD	50	μA
Input Voltage Range		−20 to 20	mV
Sampling Frequency	f_s	6.5	MHz
Signal-to-Noise Ratio	SNR	80	dB

2nd-order CT modulator – II

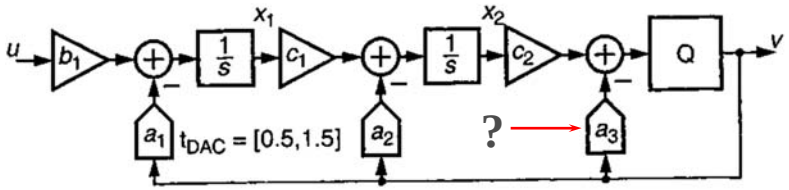
2nd-order single-bit, OSR=300 → SQNR > 100dB, good margin for achieving an overall SNR of 80dB

CIFB topology avoids peaking in the STF

DAC timing: [0.5 1.5] → duration of one clock cycle, with a delay of ½ clock cycle → enough for quantizer to resolve its input and for DAC setup time (overkill in this case, but example of a typical choice)

We start with the same NTF as in the previous DT modulator:

$$NTF(z)=\left(\frac{z-1}{z-1/3}\right)^2$$

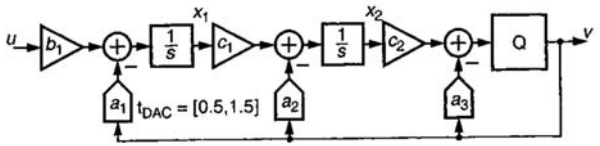


Coefficient values

Determination of CT coefficients – we start setting c_1 and c_2 to unity in the DT modulator (they only affect internal signal scaling) – the new a_1, a_2 coefficients in the DT modulator become

$$\begin{cases} a_1 (=b_1) = a_1 c_1 c_2 = \frac{1}{4}\frac{1}{3}\frac{16}{3} = \frac{4}{9} = 0.4444 \\ a_2 = a_2 c_2 = \frac{1}{4}\frac{16}{3} = \frac{4}{3} = 1.3333 \end{cases} \qquad \begin{cases} c_1 = 1 \\ c_2 = 1 \end{cases}$$

We have already described the algorithm to find $a_{1,CT}$ and $a_{2,CT}$ from a_1 and a_2. However, in this case the input pulse that determines the CT impulse response is still developing when the first sample is taken at t=1 (since the input pulse stops at t=1.5) → two CT coefficients are not enough to establish the identity between DT and CT!

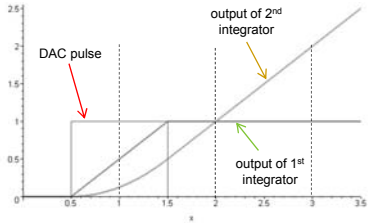


Coefficient values – II

Conversion equations again, but here we have to make a special case for the sample at n=1

DT

$$\begin{cases} \frac{a_{2,DT}}{z-1} & \rightarrow \quad a_{2,DT} \\ \frac{a_{1,DT}}{(z-1)^2} & \rightarrow \quad a_{1,DT}(n-1) \end{cases}$$



CT

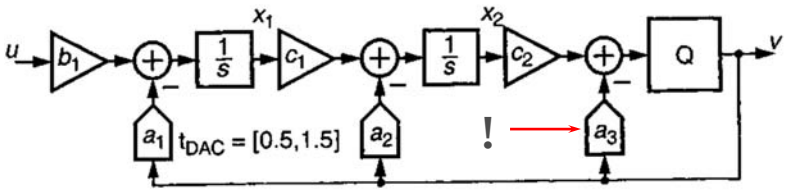
$$\begin{cases} \left[\frac{1}{s}\left(e^{-s\alpha_2 T} - e^{-s\beta_2 T}\right)\right]\cdot\frac{a_{2,CT}}{s} & \rightarrow \quad \begin{cases} a_{2,CT}(1-\alpha_2) & \text{if } n=1 \\ a_{2,CT}(\beta_2-\alpha_2) & \text{if } n\geq 2 \end{cases} \\ \left[\frac{1}{s}\left(e^{-s\alpha_1 T} - e^{-s\beta_1 T}\right)\right]\cdot\frac{a_{1,CT}}{s^2} & \rightarrow \quad \begin{cases} \frac{1}{2}a_{1,CT}(1-\alpha_1)^2 & \text{if } n=1 \\ a_{1,CT}\left[(\beta_1-\alpha_1)n + \frac{\alpha_1^2-\beta_1^2}{2}\right] & \text{if } n\geq 2 \end{cases} \end{cases}$$

Coefficient values – III

Simple calculations yield

$$\begin{cases} \frac{1}{2}a_{1,CT}(1-\alpha_1)^2 + a_{2,CT}(1-\alpha_2) = a_{2,DT} & \text{if } n=1 \\ a_{1,CT}(\beta_1-\alpha_1) = a_{1,DT} \\ a_{1,CT}\frac{\alpha_1^2-\beta_1^2}{2} + a_{2,CT}(\beta_2-\alpha_2) = -a_{1,DT} + a_{2,DT} & \text{if } n\geq 2 \end{cases}$$

Three equations, two variables → cannot be satisfied → the extra equality at n=1 requires an extra variable, $a_{3,CT}$, which only affects the impulse response at n=1!



Coefficient values

New equations:

$$\begin{cases} \frac{1}{2}a_{1,CT}(1-\alpha_1)^2 + a_{2,CT}(1-\alpha_2) + a_{3,CT} = a_{2,DT} & \text{if } n=1 \\ \begin{cases} a_{1,CT}(\beta_1-\alpha_1) = a_{1,DT} \\ a_{1,CT}\frac{\alpha_1^2-\beta_1^2}{2} + a_{2,CT}(\beta_2-\alpha_2) = -a_{1,DT} + a_{2,DT} \end{cases} & \text{if } n \geq 2 \end{cases}$$

With $\alpha_1 = \alpha_2 = 0.5, \quad \beta_1 = \beta_2 = 1.5$, we obtain

$$a_{1,CT} = \frac{4}{9} = 0.4444$$

$$a_{2,CT} = \frac{4}{3} = 1.3333$$

$$a_{3,CT} = \frac{11}{18} = 0.6111$$

Also with the Toolbox

This can be accomplished also with Matlab code using several functions in the DS toolbox

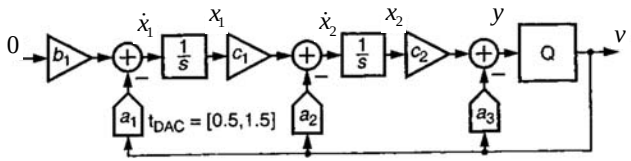
```
% Desired NTF and its impulse response
NTF = zpk([1 1], [1/3 1/3], 1, 1);      % zpk (zeros, poles, gain, sampling period)
n_imp = 3;                              % 3 samples to determine 3 aCT coefficients
y_desired = impL1(NTF, n_imp);          % impulse response of L1, 3 samples
% State-space description of CT loop filter as a 3-input, 1-output system
Ac = [0 0; 1 0];
Bc = [-1 0 0; 0 -1 0];
Cc = [0 1];
Dc = [0 0 -1];
td = 0.5;                               % input delay from DACs
sys_c = ss(Ac, Bc, Cc, Dc);             % sys_c embodies the CT state-space system
set(sys_c, 'InputDelay', td*[1 1 1]);
% CT-to-DT conversion and associated impulse response
sys_d = c2d(sys_c, 1);                  % c2d(sys_c, sampling period, conversion method)
imp_res = impulse(sys_d, n_imp);        % impulse responses, one from each of the 3 inputs
yy = squeeze(imp_res);                  % 3 response columns merged into a single array
% Solve for coefficients aCT → aCT= yy-1*y_desired
% The first row in yy and y_desired is zero (sample for n=0) and must be removed
aCT = (yy(2:end, 1:end))^(-1)*y_desired(2:end);
```

$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases}$

State-space formulation of CT modulator

State-space formulation of the CT modulator – we put all *c*'s to unity and consider the three *a*'s as three separate inputs, *y* being the output

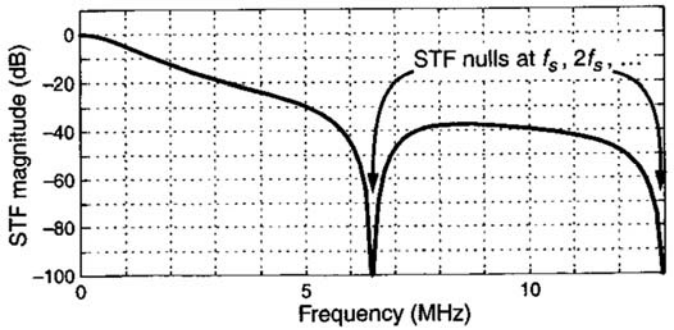
$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \Rightarrow \left[\begin{array}{c} \dot{x}_1 \\ \dot{x}_2 \\ y \end{array}\right] = \left[\begin{array}{cc|ccc} 0 & 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 \\ \hline 0 & 1 & 0 & 0 & -1 \end{array}\right] \left[\begin{array}{c} x_1 \\ x_2 \\ v_1 \\ v_2 \\ v_3 \end{array}\right]$$



Anti-aliasing

Ideal implementation → attenuation for frequencies aliasing to the passband is over 130dB! – finite DC gain in the loop filter makes the STF larger, but an alias suppression larger than 80dB is easily achievable

$$STF = L_{0c}(s)\,NTF(z)$$

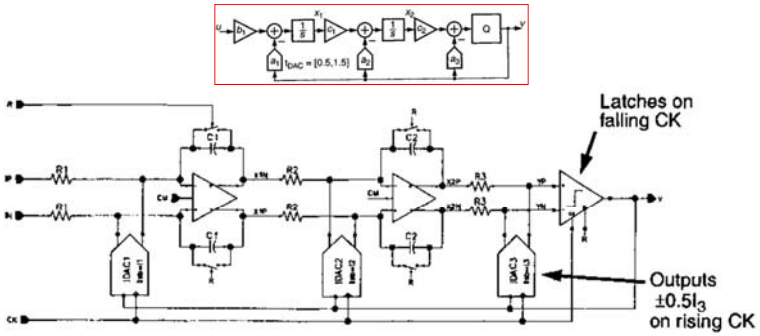


Component values in active-RC design

We start assuming $C_1 = 1pF;\ C_2 = 0.1pF;\ I_3 = 1\mu A$

We can find R_1 with $b_1 V_{fs} = \frac{V_{fs}}{R_1 f_{clk} C_1}$ (with V_{fs}=1 in a 1-b modulator) →

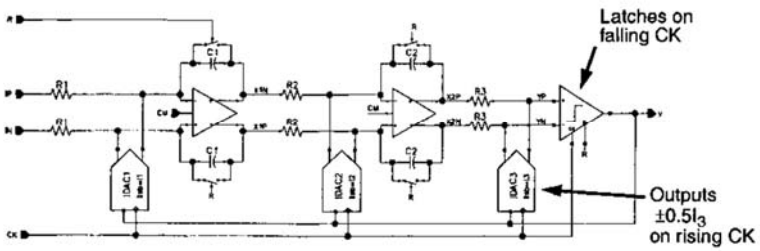
this equates the output of the 1st DT integrator with the output of the 1st CT integrator after a sampling period of $1/f_{clk}$



Component values in active-RC design – II

$$b_1 V_{fs} = \frac{V_{fs}}{R_1 f_{clk} C_1} \rightarrow R_1 = \frac{1}{b_1 f_{clk} C_1}; \qquad a_1 V_{ref} = \frac{V_{ref}}{R_{DAC1}} \cdot \frac{1}{f_{clk} C_1} \equiv \frac{I_1}{f_{clk} C_1} \rightarrow I_1 = a_1 V_{ref} f_{clk} C_1$$

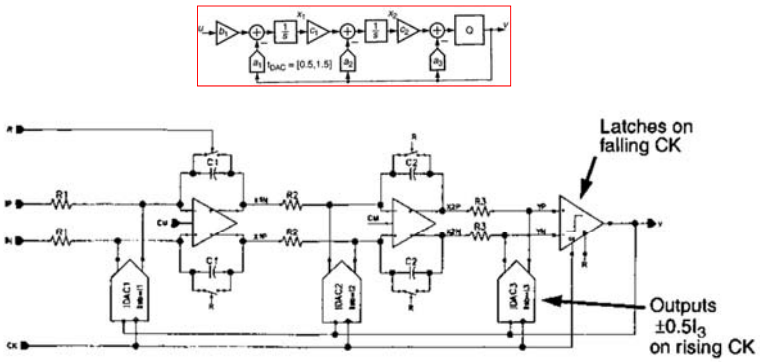
V_{ref} =1 in a 1b quantizer



Component values in active-RC design – III

$$R_1 = \frac{1}{b_1 f_{clk} C_1} \approx 346k; \qquad I_1 = a_1 f_{clk} C_1 = 2.88\mu$$

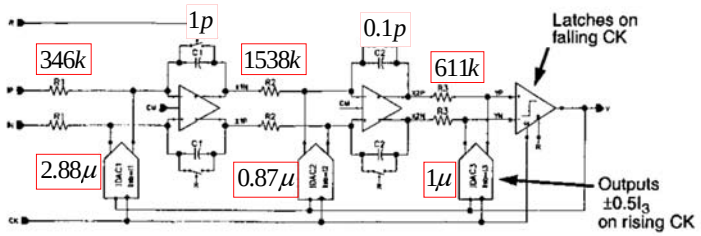
$$I_2 = a_2 f_{clk} C_2 = 0.87\mu; \qquad R_2 = \frac{1}{c_1 f_{clk} C_2} = 1538k; \qquad R_3 = \frac{a_3}{c_2 I_3} = 611k$$



Dynamic range scaling

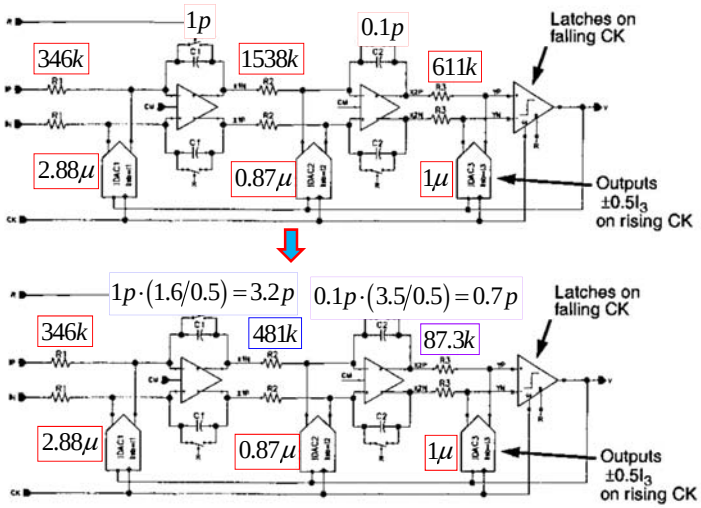
Dynamic range scaling could be done using the DT model of the modulator, but it would be valid only at the sampling instants → simulation on a behavioral model of the CT modulator is better

Simulations show peak values of 1.6V and 3.5V at the output of the first and second integrator, while we desire maximum peak swings of 0.5V



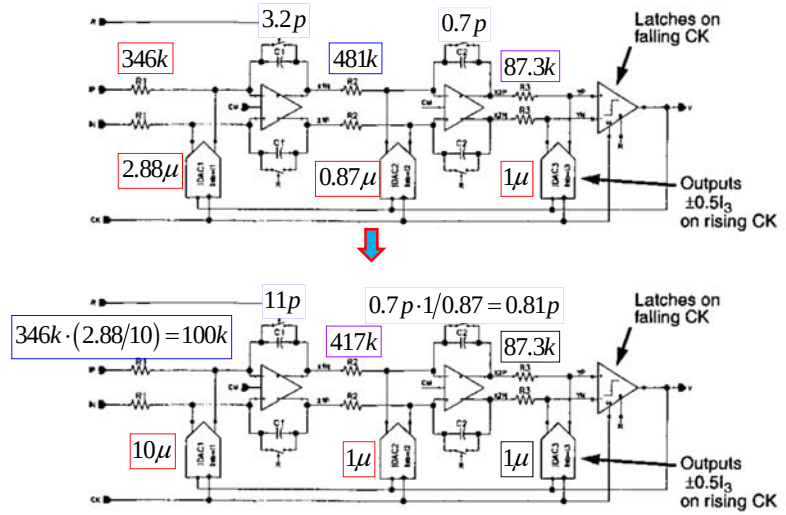
Dynamic range scaling – II

Scaling for maximum peak swings of 0.5V yields



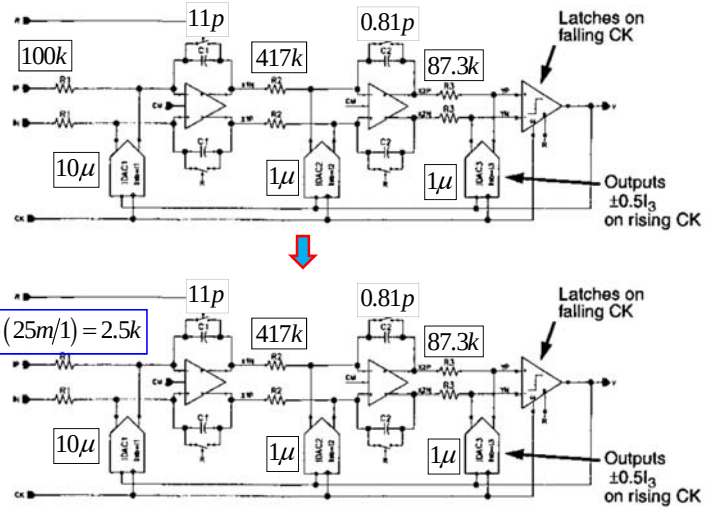
Dynamic range scaling – III

Increase I_1 to 10μ (good for noise performance), and I_2 to 1μ for simplicity, and re-scale:



Dynamic range scaling – IV

Finally, setting the FS input level 25% higher than the desired FS=20mV, the input resistance is rescaled as below:

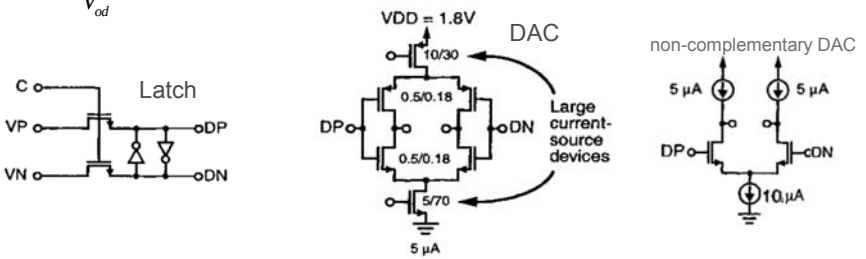


Implementation issues

C_1 is 11pF → rather large area → C_1 is inversely proportional to the clock rate → favorable having a relatively high clock frequency!

Complementary DAC (3dB noise advantage on non-complementary, as it only needs half as much current); current source are implemented with large and long MOS, with as high an overdrive as possible (leaving just enough range at the output) to minimize their noise contribution – in fact: the noise of the MOS current source is $i_n^2 = 4k_B T \gamma g_m$ → g_m must be minimized for a given current

$g_m = \frac{2I_{ds}}{V_{od}}$ minimized → the overdrive must be maximized (as I_{ds} is given)



Implementation issues

Furthermore: very long MOS have a low 1/f noise (which decreases with L^2); in this design, the DAC1 white current noise density is

$$I_{DAC1,noise} = 0.4\,pA/\sqrt{Hz}$$

which across the input resistances becomes

$$V_{DAC1,noise} = 2 \cdot R_1 \cdot I_{DAC1,noise} = 2nV/\sqrt{Hz}$$

This should be compared to the noise of the input resistors,

$$V_{R_1,noise} = \sqrt{4k_B T(2R_1)} = 9nV/\sqrt{Hz}$$

Thus, DAC1 noise is 12dB below the input noise; the SNR due to input resistors and DAC1 only is

$$SNR = 10\log\left(\frac{0.5V_{sig,FS}^2}{\left(2 \cdot R_1 \cdot I_{DAC1,noise}\right)^2 + 4k_B T(2R_1)}\right) = 10\log\left\{\frac{0.5\left(20 \cdot 10^{-3}V\right)^2}{\left[\left(2^2+9^2\right)\cdot\left(10^{-9}V\right)^2/Hz\right]\cdot 10^4 Hz}\right\} = 87dB$$

Implementation issues – II

$$SNR = 10\log\left(\frac{0.5V_{sig,FS}^2}{\left(2 \cdot R_1 \cdot I_{DAC1,noise}\right)^2 + 4k_B T(2R_1)}\right) = 10\log\left\{\frac{0.5\left(20 \cdot 10^{-3}V\right)^2}{\left[\left(2^2+9^2\right)\cdot\left(10^{-9}V\right)^2/Hz\right]\cdot 10^4 Hz}\right\} = 87dB$$

This is much lower (i.e. poorer) than the SQNR → doubling the DAC1 current (and C_1) would halve R_1, and the SNR would improve by 3dB (since $I_{DAC1,noise}$ increases by 3dB) – however, we cannot afford this, since most of the current will be needed in the first opamp (remember that our budget is 50uA), which must be low noise and capable to source/sink the sum of the input current and DAC1 current

Implementation issues

Assuming that a class-A opamp is used, the bias current in each output leg must be at least 5uA to match DAC1 – to reduce the maximum-to-minimum current ratio in the output devices, 10uA is a more reasonable value

Assuming the input-referred noise of the opamp to be the same as that of the input resistors, and that its 1/f noise is negligible, we must have for each MOS in the input pair:

Input-referred voltage noise → $4\gamma k_B T\frac{1}{g_m} = \frac{1}{2}\left(9nV/\sqrt{Hz}\right)^2 \quad \rightarrow \quad g_m = 270\,\mu A/V$

Assuming a square-law MOS, and an overdrive of 100mV, we obtain

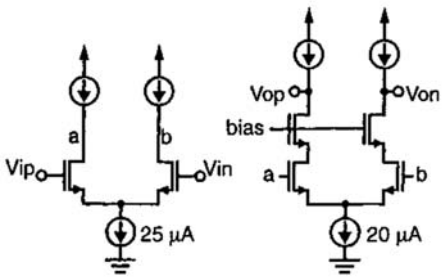
$$g_m = 2I_D/V_{od} \quad \rightarrow \quad I_D = 14\mu A$$

In a single-stage amplifier the current in the input differential pair flows in the output legs as well, which might seems a good feature to achieve both low noise and adequate output current – unfortunately, the transconductance of the input pair is $g_m/2 = 135\,\mu A/V$ → the differential voltage at the opamp input corresponding to an output current of 5uA will be close to 20mV, which is the assumed full-scale input (i.e., no margins)

Implementation issues

Two-stage architecture is needed – output stage is cascoded, so that the output resistance is comparable (hopefully higher) to R_2=420K (compensation and common-mode feedback are not shown)

The second amplifier in the modulator is required to supply currents that are approx. 10% of those of the first amplifier → scaling down the first amplifier by a factor 10 yields a second amplifier with negligible noise and distortion contributions



Implementation issues

Low-power comparator – 1uA of bias current, since speed requirement are relaxed, and the modulator is tolerant to the comparator offset

Power consumption of 5uW with a clock of 6.5MHz.