

General single-stage DSM – II

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)}$$
 $NTF(z) = \frac{1}{1 - L_1(z)}$

Conversely, given the desired STF and NTF, we obtain

$$L_0(z) = \frac{STF(z)}{NTF(z)} \qquad L_1(z) = 1 - \frac{1}{NTF(z)}$$

 L_1 must be large in the signal band, to reduce the NTF there $\rightarrow L_0$ must also be large to give an STF close to unity $\rightarrow L_0$ and L_1 have their poles in the same range; in fact L_0 and L_1 usually have the same poles, which are also the zeros of the NTF; L_0 and L_1 have in general different zeros

A typical case is when the STF is just a delay, and the NTF is an N-time differentiation:

from which

$$STF(z) = z^{-k} \qquad NTF(z) = (1 - z^{-1})^{N}$$

hich
$$L_{0}(z) = \frac{z^{-k}}{(1 - z^{-1})^{N}} = \frac{z^{N-k}}{(z - 1)^{N}}; \qquad L_{1}(z) = 1 - (1 - z^{-1})^{-N} = \frac{(z - 1)^{N} - z^{N}}{(z - 1)^{N}}$$

Higher-Order ΔΣ Modulators

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Higher-Order $\Delta\Sigma$ Modulators

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Remember: the reference voltage of the ADC is implicitly assumed to be unity in the equation above, and the same for the feedback DAC, which is in fact omitted in the schematic

From these equations we obtain: V(z) = STF(z)U(z) + NTF(z)E(z)

with
$$STF(z) = \frac{L_0(z)}{1 - L_1(z)}$$
 $NTF(z) = \frac{1}{1 - L_1(z)}$

Poles and zeros

The N poles common to L₀ and L₁ lie on the unit circle at z=1 N-k zeros of L₀ (for N>k) lie at z=0, and k zeros lie at z= ∞ The zeros of L₁ obey the equation $(1-z^{-1})^N = 1 \quad (=e^{j2\pi i})$

This yields one zero at infinity (for *i*=0 below), and the rest is given by



Other special case

Important special case: forward path gives $L_0=L+1$, L_1 unchanged \rightarrow



$$STF(z) = \frac{L(z)+1}{1+L(z)} = 1$$
 $NTF(z) = \frac{1}{1+L(z)}$

The input of the loop filter is therefore:

$$U - V = U - \left(STF \cdot U + NTF \cdot E\right) = \frac{-E}{1 + L}$$

This means that the loop does not contain the signal, but only the filtered quantization noise \rightarrow much relaxed demands on linearity!

Special case

Important special case: loop filter with single input, and only the difference u(n)-v(n) enters the loop \rightarrow



Realizability

There must be at least a clock delay in the loop containing L_1 and Q



Otherwise, a given value of y(n) would result in v(n)=y(n)+e(n), and this would pass through L₁ instantly and change y(n) during the same period \rightarrow the first sample of the impulse response of L₁(z) must be zero \rightarrow this means that $L_1(\infty)=0$

and therefore

$$NTF(\infty) \equiv H(\infty) = \frac{1}{1 - L_1(\infty)} = 1$$

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Realizability - II

If we assume the NTF to be

$$H(z) = \frac{b_{m}z^{m} + b_{m-1}z^{m-1} + \dots + b_{1}z + b_{0}}{a_{n}z^{n} + a_{n-1}z^{n-1} + \dots + a_{1}z + a_{0}}$$
$$H(\infty) = 1 \quad \Rightarrow \quad m = n, \qquad \frac{b_{n}}{a_{n}} = 1$$

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Stability considerations - II

The STF acts as a pre-filter \rightarrow stability is mainly determined by the NTF and by the number of bits in the quantizer

Unfortunately, there are no known necessary and sufficient NTF properties ensuring a stable operation!

The known results are either too conservative, or apply to special cases with DC inputs

The most widely used criterion for stability is the so-called Lee's rule:

A <u>1-bit</u> $\Delta\Sigma$ modulator is likely to be stable if $|\max|NTF(e^{j\omega})| = ||NTF(e^{j\omega})||$

<1.5

This is actually neither necessary nor sufficient! (in fact, it does not say anything about the maximum input signal!)

The maximum usually occurs at $\omega = \pi$ (i.e. at Nyquist), since this is farthest from the zeros (usually all close to z=1) and closest to the poles; an exception can be when high-Q poles exist in the NTF, in which case the peak may occur near the highest-Q pole.

Stability considerations

The linearized model of the modulator would predict that the sole loop transfer function L₁ would determine the stability properties of the modulator - this would neglect the non-linear limitations of the quantizer!

The range of input amplitudes for which the modulator is stable is called stable input range, and must be lower or equal to the full range of the first feedback DAC

In a higher-order single-bit modulator the stable input range is a few dB below the full range of the feedback DAC – this loss is usually the result of the non-linear effects of quantizer overload - in fact, the input to the quantizer is

Y(z) = STF(z)U(z) + (NTF(z)-1)E(z)

which shows that if the input *u* (filtered by the STF) approaches the edge of the quantizer overload, the addition of the filtered q-error may push ypast the overload range; this overload will increase E(z), which will aggravate the original overload, and so on in positive-feedback fashion To restore a stable operation of the modulator may require a reset, since just disconnecting the input may not be enough!

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More on instability

Replace the quantizer with a linear gain k and additive noise:



As we have already seen, k can be found through simulations, and is

$$k = \frac{\langle v, y \rangle}{\langle y, y \rangle} = \frac{E[|y|]}{E[y^2]}, \qquad [v(n) = sign(y(n))]$$

Therefore, we can write an improved linear NTF as

$$NTF_{k}(z) = \frac{1}{1 - kL_{1}(z)} = \frac{NTF_{1}(z)}{k + (1 - k)NTF_{1}(z)}$$

The locus of the roots of the denominator, drawn for 0<k<1, predicts the stability of the system

given by

More on stability

Here: root locus of a 5th-order modulator

$$NTF_{k}(z) = \frac{1}{1 - kL_{1}(z)} = \frac{NTF_{1}(z)}{k + (1 - k)NTF_{1}(z)}$$

k=0 k=1 → roots are poles of NTF₁

k=0 → roots are zeros of NTF₁

Stability → all roots inside the unit circle

This 5th-order modulator \rightarrow unstable for k < 0.547

We can also appreciate what happens by considering the Bode plot of the loop gain, $kL_1(z)$ – typically, the loop has its poles at or near DC \rightarrow high gain at low frequencies, decaying with N·20dB/dec

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Higher-Order $\Delta\Sigma$ Modulators

More on stability

More sophisticated approaches to assess stability have been proposed by, among others, Lars Risbo at DTU, now at TI-Denmark

In practice, extensive simulations are unavoidable!

We have already seen in the discussion of MOD2 that (rapidly and perhaps strangely) varying input signals can cause instability even if their amplitude is low – realistic worst-case input signals must be used \rightarrow square wave with the frequency of the dominant poles of the NTF \rightarrow usually well outside the signal band \rightarrow analog pre-filtering may be of great help

Loop gain – Bode plot

Loop gain with $k=1 \rightarrow$ conditional stability: if the gain drops sufficiently the phase at the 0dB crossing becomes lower than 180 degrees



The phase is 180 degrees for a loop gain of $1.83 \rightarrow$ if k = 1/1.83 = 0.547, the loop becomes unstable

|v(n)| is fixed in a single-bit quantizer \rightarrow reducing k is equivalent to increasing |y|and hence $|u| \rightarrow$ again, this confirms that instability can be avoided by limiting the input signal

Multi-bit stability

Consider a modulator with an M-step quantizer (i.e., with M+1 levels). The modulator is guaranteed (proof in book) not to experience overload

for any input u(n) such that $\max_{n} |u(n)| < M + 2 - ||h||_1$, where $||h||_1 = \sum_{n=0} |h(n)|$ and $h(n) = Z^{-1} [H(z)] = Z^{-1} [NTF(z)]$

Example: M=16, $H(z) = (1-z^{-1})^3 = 1-3z^{-1}+3z^{-2}-z^{-3} \rightarrow ||h||_1 = 8 \rightarrow$ any input with maximum value below 10 is guaranteed to be stable \rightarrow stable for inputs up to 62.5% of the full scale value of 16

Modulators with Nth-order differentiation for NTF and M= 2^{N+1} steps in quantizer \rightarrow sufficient condition: stable for arbitrary inputs up to 50% of the input range at least:

$$H(z) = (1 - z^{-1})^{N} = 1 - \binom{N}{1} z^{-1} + \binom{N}{2} z^{-1} - \dots$$

 $\|h\|_{1} = 1 + {N \choose 1} + {N \choose 2} + \dots = 2^{N}$ $\max_{n} |u(n)| < 2^{N+1} + 2 - 2^{N} = 2^{N} + 2 = \frac{M}{2} + 2$

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Multi-bit stability

If $M=2^N \rightarrow$ available range for signal is only 2, i.e. 1LSB!

If $M=2^{N+1} \rightarrow$ available range for signal is 0.5M+2 = 0.5(M+1)+1.5 > 50%

If $M=2^{N+2} \rightarrow$ available range for signal is over 75%

Extensive simulations show that for N=5 and M > 2^5 the condition is very stringent: slightly higher u(n) causes instability!

Extensive behavioral simulations \rightarrow a must!

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Higher-Order ΔΣ Modulators

Zero optimization example

Example: 5th order, OSR=32, both optimized and with all NTF zeros at DC



Zero optimization

Spreading zeros on the unit circle (i.e., at finite frequencies) \rightarrow total inband noise is reduced

Moving poles closer to zeros \rightarrow reduces the out-of-band NTF \rightarrow improved stability

Optimal zero location (assuming poles do not impact):

N	zero locations, normalized to ω_B	SQNR improvement
1	0	0 dB
2	±1/(√3)	3.5 dB
3	$0, \pm \sqrt{3/5}$	8 dB
4	$\pm \sqrt{3/7} \pm \sqrt{(3/7)^2 - 3/35}$	13 dB
5	$0, \pm \sqrt{5/9 \pm \sqrt{(5/9)^2 - 5/21}}$	18 dB
6	±0.23862, ±0.66121, ±0.93247	23 dB
7	0, ±0.40585, ±0.74153, ±0.94911	28 dB
8	±0.18343, ±0.52553, ±0.79667, ±0.96029	34 dB

Zero optimization example - simulation

Same example: simulation vs. linear model, both k=1 and optimal k=1.72(obtained, once again, a posteriori from the simulation data) - one more time, the optimal k case matches simulations really well

-6dBFS input, SQNR = 84dB



Zero optimization example - SQNR

SQNR less erratic than in lower-order modulators \rightarrow constant white noise assumption is more valid in higher-order modulators

Input below –40dBFS \rightarrow 7dB higher than expected – see spectrum in next slide



More on zero optimization

Even-order NTFs: no optimized zeros at DC \rightarrow no perfect noise suppression at DC \rightarrow if perfect DC reproduction is required, it is possible to place two zeros at DC, and optimize the other ones following the same noise-minimization procedure (zeros at DC also help reducing the probability of low-frequency idle tones)

N	zero locations, normalized to ω_B	SQNR improvement
1	0	0 dB
2	±1/(√3)	3.5 dB
3	$0, \pm \sqrt{3/5}$	8 dB
4	$\pm \sqrt{3/7} \pm \sqrt{(3/7)^2 - 3/35}$	13 dB
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Zero optimization example - SQNR - II

Low inputs \rightarrow spectrum is quite different from the expected \rightarrow linear model not enough! (lower in-band noise, tones around $f_s/4$, notch at $f_s/2$)



NTF pole optimization

Constraints:

- a) The NTF must satisfy the realizability condition $NTF(\infty) = 1$
- b) The out-of-band NTF gain, and hence the stability of the modulator, are largely determined by the NTF poles
- c) We assumed that only the NTF zeros are important in-band (i.e., only the NTF zeros determine q-noise shaping); furthermore, NTF poles are very often STF poles as well → the denominator of the NTF should be flat in-band!

These constraints entail a trade-off in the location of the poles (i.e., the closer they are to the zeros, the better the stability, but q-noise suppression becomes less effective) \rightarrow software tools available (e.g. Schreier's Delta-Sigma toolbox in Matlab)

Optimization procedure

If software is not available, cookbook recipe:

- Choose the modulator order based on the desired specifications (see SQNR plots in the next few slides)
- 2) Choose the NTF type usual choices are highpass transfer functions, like Butterworth, inverse Chebyshev, or maximally-flat-delay
- 3) Place the -3dB cutoff of the NTF slightly above the edge of the signal band



- 4) Now you have zeros z_i and poles p_i of the NTF: $H(z) = \prod_{i=1}^{n} \frac{1}{2}$
- 5) Predict the stability of the modulator for multi-bit quantization, with the formula $\max |u(n)| \le M + 2 \|h\|,$

and for single-bit with Lee's rule: $\max \left| NTF(e^{j\omega}) \right| < 1.5$

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Higher-Order ΔΣ Modulators

Empirical SQNR limits, 1b quantizer

Curves include the effect of input amplitude reduction to ensure stability \rightarrow accurate prediction of the performance of the non-linear modulator



Optimization procedure

Since the maximum value of the NTF on the unit circle usually occurs at z=-1 (i.e. $\omega = \omega_s/2$; even if the peak occurs elsewhere, its value is usually close to that at z=-1), Lee's rule requires

$$H(-1) = \prod_{i=1}^{N} \frac{1+z_i}{1+p_i} < 1.5$$

- 6) Confirm stability through extensive simulations
- 7) If stability not good → poles must be shifted further away from z=-1, while maintaining the flat gain in the signal band – can be achieved by reducing the cutoff frequency, which can be shown to reduce the peak NTF gain
- If stability is robust but the SQNR does not reach the predicted values, it may be beneficial to make the design more aggressive by increasing the cutoff frequency and repeating the stability test; steps 6-8 are iterated until a satisfactory performance is obtained

Higher-Order $\Delta\Sigma$ Modulators

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Empirical SQNR limits, 2b quantizer

Curves include the effect of input amplitude reduction to ensure stability \rightarrow accurate prediction of the performance of the non-linear modulator



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Empirical SQNR limits, 3b quantizer

Curves include the effect of input amplitude reduction to ensure stability \rightarrow accurate prediction of the performance of the non-linear modulator



Loop filter architectures – CIFB

$$L_{0}(z) = \sum_{i=1}^{N+1} \frac{b_{i}}{(z-1)^{N+1-i}} = \frac{b_{1} + b_{2}(z-1) + \dots + b_{N+1}(z-1)^{N}}{(z-1)^{N}}$$

$$L_{1}(z) = \sum_{i=1}^{N} \frac{-a_{i}}{(z-1)^{N+1-i}} = -\frac{a_{1}+a_{2}(z-1)+\ldots+a_{N+1}(z-1)^{N-1}}{(z-1)^{N}}$$

$$NTF(z) = H(z) = \frac{1}{1 - L_1(z)} = \frac{(z - 1)^N}{a_1 + a_2(z - 1) + \dots + a_N(z - 1)^{N-1} + (z - 1)^N} \equiv \frac{(z - 1)^N}{D(z)}$$

All zeros at z=1 (= DC); the a_i coefficients can be found by equating D(z) to the denominator of the desired NTF

Loop filter architectures - CIFB

CIFB - cascaded integrators with distributed feedback and distributed inputs



Loop filter architectures – CIFB

$$STF(z) = \frac{L_0(z)}{1 - L_0(z)} = \frac{b_1 + b_2(z - 1) + \dots + b_{N+1}(z - 1)^N}{D(z)}$$

The \mathbf{b}_{i} coefficients can be found by equating the numerator with the numerator of the desired STF

Usually, all \boldsymbol{a}_i are non-zero because of the needed poles for stable operation

The b_i, however, can be chosen more freely: e.g., all equal to zero except $b_1 \rightarrow STF = b_1/D(z)$ (all STF zeros lie at infinity) \rightarrow D(z) must be flat in the pass-band

Other possibility: $b_i=a_i$, $b_{N+1}=1 \rightarrow STF=1$, modulator output becomes

V(z) = U(z) + H(z)E(z)

Loop filter architectures – CIFB

The input of the ith integrator becomes (with $b_i=a_i$)

$$W_{i}(z) = X_{i-1}(z) - a_{i}V(z) + b_{i}U(z) = X_{i-1}(z) - a_{i}[U(z) + H(z)E(z)] + b_{i}U(z)$$

= $X_{i-1}(z) - a_{i}H(z)E(z)$



Thus, by recursion, the input signal u(n) is not present at the input of any integrator \rightarrow the loop processes only the quantization noise \rightarrow lower dynamic needed, especially in multi-bit quantizers \rightarrow less extensive dynamic range scaling needed \rightarrow more convenient coefficient values! Also, non-linearities do not distort the signal, since the signal is not there! Advantageous compared to previous choice (i.e, b_i=0 for i>1)

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Higher-Order ΔΣ Modulators

Coefficient scaling for optimal dynamic range

Scaling is accomplished by dividing the admittance of all input branches of a given integrator by a factor k, and multiplying with the same factor the admittance of all output branches of the same integrator – in this way, the rest of the circuit is unaffected, and so are the transfer functions



Coefficient scaling for optimal dynamic range

In general, the values of the feedforward/feedback coefficients yielding the desired NTF and STF do not guarantee any control on the internal modulator states (i.e. integrator outputs), which may exceed the limits imposed by the power supply voltage (or, more in general, may cause too much distortion) \rightarrow dynamic range scaling is a must – this is an issue common to all implementations of active filters!

Below \rightarrow example of 5th-order active-RC elliptic low-pass filter



Complex NTF zeros, CRFB architecture

 5^{th} order \rightarrow two pairs of complex zeros \rightarrow CIFB modified into "cascade of resonators with distributed feedback", CRFB (alternating non-delaying and delaying integrators), to keep the zeros on the unit circle



1st and 2nd integrators + feedback g_1 yields two complex poles in L_1 (and L_0), solutions of $p(z) = z^2 - (2 - g_1)z + 1$

These poles are on the unit circle at frequencies $\pm a_1$, with $\cos(a_1) = 1 - g_1/2$

Complex zeros, CRFB architecture

The same is of course true for the 3rd and 4th integrators + feedback g₂

If
$$\omega_1 \ll 1$$
, $\cos(\omega_1) \approx 1 - \omega_1^2/2 \rightarrow \omega_1 \approx \sqrt{g}$

One of the integrators in each resonator needs to be delay-free to insure that the poles are on the unit circle

In high-frequency modulators realized using SC integrators it is advantageous to have a delay in every integrator, reducing speed requirements \rightarrow the denominator of the resonator becomes now

$$p(z) = z^2 - 2z + (1 + g_1)$$

Poles are now outside the unit circle, at $1 \pm j \sqrt{g_1}$ If $\omega_1 \ll 1$, $\omega_1 \approx \sqrt{g_1}$ is still a good approximation

It should be noticed that the resonators by themselves are unstable, as clear from the previous analysis; however, they are embedded in a stable feedback system, which prevents local oscillations

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Higher-Order $\Delta\Sigma$ Modulators

CIFF with complex zeros

CIFF with complex zeros (for the sake of readability, only first and last feedforward paths are shown)



CIFF topology

Alternative topology: cascade of integrators with feedforward (rather than feedback) paths to create NTF zeros – CIFF topology



If $b_1=b_{N+1}=1$ and all other b_i are zero, then it can be shown that the loop filter does not process the input signal – same advantages as previously discussed

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Higher-Order $\Delta\Sigma$ Modulators



Multi-stage modulators

At moderate OSR values, a high SNR cannot be obtained with a 1-bit quantizer simply by raising the order of the modulator, because stability limits the permissible input signal amplitude



Multi-bit quantizer \rightarrow flash ADC – linearity issues, complexity grows exponentially with #bits

Different strategy \rightarrow multi-stage modulators! (with their own problems, of course...)

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Higher-Order ΔΣ Modulators

Leslie-Singh (L-0 cascade) structure

 $V(z) = z^{-k} \left[STF_1(z)U(z) + NTF_1(z)E_1(z) \right] - NTF_1(z) \left\{ z^{-k} \left[E_1(z) + E_2(z) \right] \right\}$ = $z^{-k} \left[STF_1(z)U(z) - NTF_1(z)E_2(z) \right]$

Therefore, NTF₁ shapes the q-error of the second stage, which can be made much smaller than the q-error of the first stage – the second stage has no feedback \rightarrow no latency issues \rightarrow can be implemented e.g. as a multi-bit pipeline ADC (easier than a multi-bit loop quantizer in the first stage) \rightarrow SQNR enhancement > 20dB

We can avoid the difficult subtraction yielding $e_1(n)$ by choosing $y_1(n)$ instead of $e_1(n)$ as input to the second stage:

$$Y_{1}(z) = V_{1}(z) - E_{1}(z) = STF_{1}(z)U(z) + \left[NTF_{1}(z) - 1\right]E_{1}(z)$$

Choosing now

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 $H_2(z) = \frac{NTF_1(z)}{NTF_1(z) - 1}$

or actually $H_2(z) \rightarrow z^{-1}H_2(z)$, to make it causal (the same delay of course for $H_1(z)$ as well) we obtain:

Higher-Order $\Delta\Sigma$ Modulators

Leslie-Singh (L-0 cascade) structure

 $L^{th}\text{-}order\,\Delta\Sigma$ modulator as first stage, zero-order ADC as second stage; the outputs of the two stages are digitally filtered and combined to obtained the overall output



The q-error e_{τ} of the first stage is extracted in the analog domain, and then converted into digital by the multi-bit second stage

$V(z) = H_1(z)V_1(z) + H_2(z)V_2(z)$

Usually H₁ implements the latency of the second ADC: $H_1(z) = z^{-k}$ H₂ is instead chosen as the digital equivalent of NTF₁

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Higher-Order ΔΣ Modulators

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Leslie-Singh (L-0 cascade) structure

$$V(z) = z^{-k} \left[STF_{1}(z)U(z) + NTF_{1}(z)E_{1}(z) \right]$$

$$-\frac{NTF_{1}(z)}{NTF_{1}(z)-1} z^{-k} \left\{ STF_{1}(z)U(z) + \left[NTF_{1}(z)-1 \right]E_{1}(z) + E_{2}(z) \right\}$$

$$= \frac{z^{-k}STF_{1}(z)}{1-NTF_{1}(z)}U(z) + \frac{z^{-k}NTF_{1}(z)}{1-NTF_{1}(z)}E_{2}(z)$$

 $NTF_1 \ll 1$ in-band \rightarrow the SQNR obtainable with this choice is very close to the one given by the previous circuit – a disadvantage though is that $y_1(n)$ contains the signal u(n) as well \rightarrow the second ADC must be able to handle much larger signals and must have a much higher linearity!

Leslie-Singh (L-0 cascade) structure

However, we have actually seen modulators where the loop filter only processes q-noise, but no signal, e.g. the CIFB modulator with $b_i=a_i$ and $b_{N+1}=1$. This yields STF(z)=1, and the output X_N of the last integrator is





MASH modulator

Obvious extension \rightarrow **M**ulti-st**A**ge noise-**SH**aping (MASH, probably worst acronym ever!) modulator, where the 2nd stage is yet another $\Delta\Sigma$ modulator



 $V_{1}(z) = STF_{1}(z)U(z) + NTF_{1}(z)E_{1}(z)$ $V_{2}(z) = STF_{2}(z)E_{1}(z) + NTF_{2}(z)E_{2}(z)$

Higher-Order $\Delta\Sigma$ Modulators

Leslie-Singh (L-0 cascade) structure

 $X_N(z)$ can be used as input to the second stage, as it does not contain the signal but only q-noise

It is possible to adopt the same procedure with other low-distortion architectures \rightarrow extract *y*-*u* \cong *e*, and use it as input to the 2nd stage

E.g.: 1^{st} stage in L-0 is a 2^{nd} -order low-distortion CIFF modulator (Silva-Steensgaard in this case:



 $X_2(z)$ can be used directly as input to the second stage!

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Higher-Order ΔΣ Modulators

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MASH modulator

For $E_1(z)$ to be cancelled, we require

$$H_1(z)NTF_1(z) = H_2(z)STF_2(z) \rightarrow H_1(z) = STF_2(z), H_2(z) = NTF_1(z)$$

STF₂ is often only a delay and easy to implement

The overall output becomes

 $V(z) = H_1(z)V_1(z) - H_2(z)V_2(z) = STF_2(z)V_1(z) - NTF_1(z)V_2(z)$ = STF_2(z)STF_1(z)U(z) - NTF_1(z)NTF_2(z)E_2(z)

A typical case is a MASH with two 2nd-order modulators (2-2 MASH) \rightarrow

 $STF_{1}(z) = STF_{2}(z) = z^{-2}$ $NTF_{1}(z) = NTF_{2}(z) = (1 - z^{-1})^{2}$ $V(z) = z^{-4}U(z) - (1 - z^{-1})^{4}E_{2}(z)$

MASH modulator

Noise shaping performance of a $4^{\text{th}}\text{-order single-loop modulator, but stability of a <math display="inline">2^{\text{nd}}\text{-order modulator!}$

In practice, the E₁ input to the second modulator needs to be scaled to fit within the stable input range (scaling factor usually $\frac{1}{4}$ if the 1st stage is single-bit, higher than $\frac{1}{4}$ if multi-bit – the inverse of the scaling factor must be included in H₂)

If the equation $H_1(z)NTF_1(z) = H_2(z)STF_2(z)$ does not hold, E₁ appears at the output filtered by

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STF_2(z)NTF_{1a}(z) - NTF_1(z)STF_{2a}(z)
```

where "a" denotes the actual value of the analog transfer function \rightarrow this may result in a dramatic SQNR deterioration \rightarrow this is the critical issue in all MASH modulators

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MASH modulator

Furthermore: multi-bit quantizer in the 2nd stage can be used without need of correction of DAC non-linearity – this is because the nonlinearity error of this DAC is multiplied by $H_2 = NTF_1 \rightarrow$ highpass filtered \rightarrow suppressed in the baseband! Also, the input of the 2nd stage does not contain any signal \rightarrow no harmonic distortion is generated! The small additional noise due to DAC non-linearities can be tolerated

MASH modulator

Another advantage of MASH is that is that the 2nd stage operates on e_1 , which is noise-like, even if it may contain some harmonic distortion \rightarrow the final e_2 is very similar to true white noise! E.g. below, the third harmonic is reduced by more than 30dB across the 2nd stage – no need of dithering in MASH



3-stage MASH

Three-stage MASH \rightarrow q-error of first and second stage can be (ideally) cancelled with

 $H_{1}(z)NTF_{1}(z) - H_{2}(z)STF_{2}(z) = 0$ $H_{2}(z)NTF_{2}(z) - H_{3}(z)STF_{3}(z) = 0$



3-stage MASH

 $V = [STF_1 \cdot U + NTF_1 \cdot E_1]H_1 - [STF_2 \cdot E_1 + NTF_2 \cdot E_2]H_2 + [STF_3 \cdot E_2 + NTF_3 \cdot E_3]H_3$ = $STF_1 \cdot H_1 \cdot U + NTF_3 \cdot H_3 \cdot E_3$

 $V(z) = STF_{1}(z)H_{1}(z)U(z) + \frac{\left[H_{1}(z)NTF_{1}(z)NTF_{2}(z)NTF_{3}(z)\right]}{STF_{2}(z)STF_{3}(z)}E_{3}(z)$

Since H_1 is an STF, the STFs are flat in the passband, the final q-error is e_3 filtered by the product of the three NTFs!

Three stages \rightarrow very high SQNR is desired \rightarrow extremely low q-noise required \rightarrow leakage of e_1 and e_2 [due to mismatch between analog transfer functions (STF_{1,2,3} and NTF_{1,2,3}) and digital ones (H_{1,2,3})] is critical and usually dominant

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Higher-Order $\Delta\Sigma$ Modulators

Noise leakage

2) In H₁₁ the effect of an imperfect NTF₁ dominates the effect of an imperfect STF₂: $H_{i1}(z) = H_{i}(z)NTF_{i}(z) - H_{2}(z)STF_{2}(z)$

This is because $H_2=NTF_1 \rightarrow errors$ due to imperfect STF₂ are shaped;

errors due to imperfect NTF_1 are not shaped, since H_1 =STF₁ has unity gain over the passband

3) Thus, we can approximate $STF_2 = H_1 = 1 \rightarrow$

$$H_{l1}(z) = NTF_{1}(z) - H_{2}(z) = NTF_{1a}(z) - NTF_{1i}(z)$$

with "a"=actual; "i"=ideal

4) Since NTF₁=1/(1-L₁), and L₁>>1, we can rewrite the above expression as

$$\left|H_{l1}(z)\right| \approx \left|\frac{1}{L_{1i}} - \frac{1}{L_{1a}}\right|$$

which is much simpler to handle than the original equations

Noise leakage

In single-stage high-order modulators, imperfections in the passive and active components of the loop filter change NTF and STF somewhat, but as long as the loop gain >>1, the q-noise will be shaped very well

In MASH, however, matching between the various analog vs. digital transfer functions is crucial

For the three-stage MASH, the leakage transfer function of e_1 and e_2 to the output are:

$$H_{l1}(z) = H_{1}(z) NTF_{1}(z) - H_{2}(z) STF_{2}(z)$$

$$H_{l2}(z) = H_{2}(z) NTF_{2}(z) - H_{3}(z) STF_{3}(z)$$

NTF NTF

Simplifying assumptions:

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1) The leakage of e_2 is less important than that of e_1 , since H_{12} represents higher-order noise shaping than H_{11} (e.g., in a 2-2-1 MASH, H_{11} is at most of order 2, while H_{12} is of order 4). Moreover, e_2 is smaller than e_1 if a multi-bit quantizer is used in the 2nd stage

Higher-Order ΔΣ Modulators

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Noise leakage

Example: 1-1 (or 1-1-1) MASH – loop filter of the first stage is a simple delaying integrator, with ideal transfer function

$$I_i(z) = \frac{a}{z-z}$$

If there is an error D in the nominal capacitance ratio used in the SCintegrator, and the opamp has a finite DC gain A, the actual transfer function becomes (D<<1, a/A <<1) c_2



Since $L_1(z) = -I(z)$, we have

$$|H_{l1}(z)| = \left|\frac{z-1}{a} - \frac{z-p'}{a'}\right| = \left|\frac{1}{a'}\right| \left|\frac{a}{A} + (z-1)\left[D + \frac{1+a}{A}\right] \right|$$
$$\approx \left|\frac{1}{A} + (z-1)\left[\frac{D}{a} + \frac{1+1/a}{A}\right]\right|$$

Noise leakage

$$\left|H_{I1}(z)\right| \approx \left|\frac{1}{A} + (z-1)\left[\frac{D}{a} + \frac{1+1/a}{A}\right]\right|$$

Thus, there is an unfiltered leakage component equal to e_1/A , and a component that is 1st-order filtered \rightarrow very high gain opamp required for the unfiltered error; if OSR is moderate, then also D<<1 is required \rightarrow very high matching between capacitors

An error in the path coupling the 1st stage to the 2nd stage will also add to $H_{l1}(z)E_1(z)$, but its effect at the overall output will be at least 1st-order filtered, since the error will pass through H₂

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Noise leakage $A_0 = \frac{a_1 a_2}{A^2};$ $A_1 = \frac{a_1 + a_2}{A}$ $A_2 = 4D + \frac{-2a_1 + b_1 + \alpha + 4}{A}$ First term \rightarrow unfiltered leakage, proportional to the inverse of the square of the opamp gain \rightarrow usually very small

Second term \rightarrow 1st-order filtered; Third term \rightarrow 2nd-order filtered; these two terms tend to dominate in typical situations

Noise leakage – 2-0 MASH



For a 2^{nd} -order first stage the leakage of e_1 will be reduced – the Taylor expansion of the leakage transfer function around z=1 (i.e. at DC) is

 $H_{l1}(z) = A_0 + A_1(1-z^{-1}) + A_2(1-z^{-1})^2 + \dots$

 $A_0 = \frac{a_1 a_2}{A^2}; \qquad A_1 = \frac{a_1 + a_2}{A}$

 $A_2 = 4D + \frac{-2a_1 + b_1 + \alpha + 4}{4}$

with

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