Advanced AD/DA converters

Introduction to ΔΣ Modulators

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Overview

- Nyquist-rate vs. oversampled converters
- Δ modulators
- ΔΣ modulators
- Higher-order ΔΣ modulators
- Bandpass ΔΣ modulators
- Multi-bit ΔΣ modulators
- ΔΣ DACs
- State-of-the-art and beyond

Nyquist-rate or oversampled?

Data converters are roughly divided into two subgroups: Nyquist-rate and oversampled

Nyquist-rate → usually, the converter has no memory → each input is processed independently of the other samples – the sampling rate can be theoretically as low as required by Nyquist's criterion (i.e. at least twice the signal bandwidth)

In these converters, linearity and accuracy is determined by the matching accuracy of the analog components used (resistors, capacitors, current sources, etc) – e.g. in an N-bit resistor-string DAC, matching must be better than 2^{-N} if the INL is to be below 0.5LSB

Practical issues limit matching to 0.02% at best → ENOB is 12b (but usually lower without extensive digital error correction)

In applications such as digital audio (and other as well) at least 18 bits are required – integrating converters can deliver this, but need 2^N clock cycles for 1 conversion → too slow for many applications!

Nyquist-rate or oversampled?

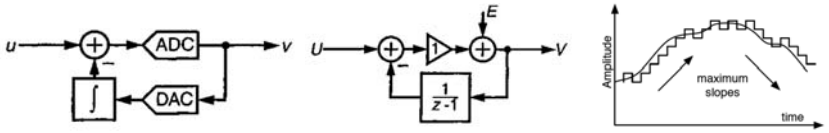
Oversampled converters can go beyond 20b of resolution at reasonable conversion speed, by employing a much higher sampling rate (by a factor typically between 8 and 512) than required by Nyquist, while generating each output by utilizing all previous inputs (through feedback)

Oversampling converters need a considerable amount of digital circuitry, besides some analog functions, and all functions must operate at the oversampling frequency

However, the crucial point is that the accuracy of the analog functions is relaxed (compared to Nyquist-rate converters), while faster operation and digital circuitry take advantage of the increased scaling in CMOS processes – as a whole, oversampled converters are quite digital-friendly, and this explains their enormous popularity, which makes them more and more attractive for applications that were once the exclusive domain of Nyquist-rate converters

From Delta converter to Delta-Sigma converter

Below: a Delta converter, with linear z-domain model and output signal



It contains low-resolution ADC and DAC, and an integrator, arranged in a feedback loop; it is very easy to analyze if we make the linear-model approximation above, where the quantization error introduced by the ADC is modeled as an additive q-noise at the output

The name "Delta modulator" comes from the fact that the output is the difference ("delta") of the input sample and the predicted value of that sample. Assuming a perfect DAC, a perfect integrator, a voltage reference of 1V and a sampling rate of 1Hz, the linear time-discrete model above is recovered, resulting in the difference equation

$$v(n) = \underbrace{u(n) - u(n-1)}_{\text{discrete-time derivative}} + e(n) - e(n-1)$$

Delta modulator

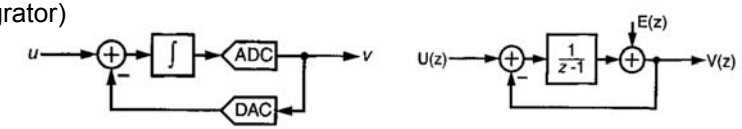
The advantage of this modulator is that the ADC *sees u(n)-u(n-1)* instead of *u(n),* which is much larger than *u(n)-u(n-1)* for an oversampled signal (since the signal then does not vary much from one sample to the following) → larger input signals can be allowed!

Disadvantages:

1) loop filter is in the feedback path → its non-linearities appear immediately at the output → very severe limitation
2) in the demodulator, we need a DAC and a demodulation filter, i.e. an integrator in the example treated here (more complex if the loop is more complex than just an integrator) → the demodulation filter has a high gain in the signal band → amplifies the DAC distortion as well as any noise picked up between modulator and demodulator (of course, the signal processing in the demodulator may be performed digitally to a great extent)

Delta-Sigma modulator

These drawbacks are avoided in the Delta-Sigma modulator, where the crucial difference is that now the integrator is in the forward path of the loop (now the signal "delta" at the input is summed ("sigma") by the integrator)



$$v(n) = u(n-1) + e(n) - e(n-1)$$

The output now contains a delayed replica of the input (and not the differentiation, as in the Delta modulator), while the error is still differentiated – demodulation does not need an integrator → in-band noise and distortion are not amplified!

Crucially, the quantization error is still differentiated, which means that this error is suppressed at low frequencies (compared to the sampling frequency) → if the loop filter has a high gain in the signal band, the in-band quantization "noise" is strongly attenuated → ***noise shaping***!

Delta-Sigma modulator

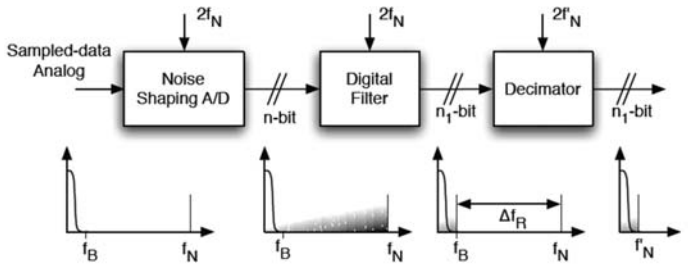
Any ADC non-linearity is combined with the quantization error, and is therefore strongly reduced; DAC non-linearities, on the other hand, appear at the output without shaping → major limitation

However, if the DAC is 1-bit, i.e. it only produces two levels, then it is inherently linear! (apart from 2nd-order effects, actually)

If a multi-bit DAC is used, digital correction and/or dynamic element matching (DEM) techniques can be used to improve linearity

Noise shaping

Most of the q-noise is shifted towards high frequencies (where it can be filtered off), removing it from the signal band → SNR largely improved → the ENOB can greatly exceed what would be allowed in terms of pure component matching



Noise shaping

The power spectral density of the q-noise is found as

$$q(n)=e(n)-e(n-1) \quad \rightarrow \quad Q(z)=\left(1-z^{-1}\right)E(z) \quad \rightarrow \quad S_q(f)=\left[2\sin(\pi fT)\right]^2 S_e(f)$$

where $S_e(f)$ is the PSD of the q-error (q-noise) of the internal ADC

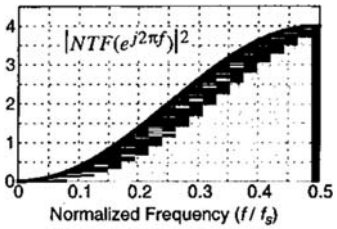
For "busy" input signals, the q-noise is approximately white, with power

$$e_{rms}^2=\Delta^2/12$$

where Δ is the quantization step; since the q-noise PSD is white between DC and $f_s/2$, we obtain

$$S_e(f)=\frac{\Delta^2}{6f_s}$$

The function $\left(1-z^{-1}\right)$ is the so-called noise transfer function (NTF) of the modulator, and is obviously a high-pass filter function → q-noise is suppressed at and near DC



Oversampling ratio

A very important parameter in Delta-Sigma modulators is the *oversampling ratio* (OSR) – if f_B is the maximum frequency of the input signal, the OSR is defined as

$$OSR=\frac{f_{Nyq}}{f_B}=\frac{f_s/2}{f_B}=\frac{f_s}{2f_B}$$

The OSR defines how much faster the modulator is operated, compared to a Nyquist converter (which ideally has OSR=1)

Integrating the q-noise over the signal band yields, for OSR >> 1:

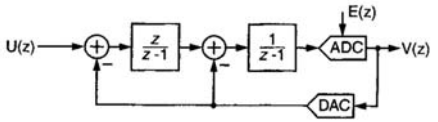
$$q_{rms}^2=\int_0^{f_B} S_q(f)\,df=\frac{e_{rms}^2}{f_s/2}\int_0^{f_B}\left[2\sin(\pi fT)\right]^2 df$$

$$\approx\frac{e_{rms}^2}{f_s/2}\int_0^{f_B}4(\pi fT)^2\,df=\frac{e_{rms}^2}{f_s/2}\frac{4\pi^2 f_B^3T^2}{3}=\frac{\pi^2e_{rms}^2}{3}\frac{8f_B^3}{f_s^3}=\frac{\pi^2e_{rms}^2}{3\cdot OSR^3}$$

As expected, q-noise decreases with increasing OSR; for a doubling of the OSR, q-noise power drops by a factor 8 = 9dB = 1.5b, which is good (but not very good!)

Higher-order single-stage ΔΣ modulators

A way of improving the SNR of the modulator, apart from increasing the OSR, is to use a higher-order loop filter; e.g., the 2nd-order below



Again, a linear analysis yields $V(z)=z^{-1}U(z)+\left(1-z^{-1}\right)^2E(z)$, and therefore the NTF is now a 2nd-order highpass filter:

$$NTF(z)=\left(1-z^{-1}\right)^2 \quad \rightarrow \quad \left|NTF\left(e^{j2\pi fT}\right)\right|=\left[2\sin(\pi fT)\right]^4$$

which yields the q-noise over the signal band

$$q_{rms}^2=\frac{\pi^4e_{rms}^2}{5\cdot OSR^5}$$

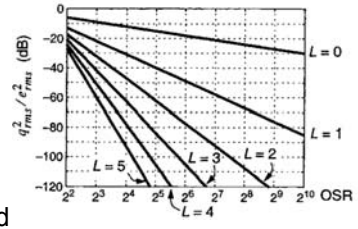
In this case, doubling the OSR yields 2.5 bits of additional resolution, which is much better!

Higher-order single-stage ΔΣ modulators

Example: if $\Delta = 2 \rightarrow e_{rms}^2 = 1/3$ for single-bit quantization, we get an ENOB of 19 bits for OSR=256 (but only 13 bits for a first-order modulator) – actually, this is optimistic, since a 2nd order single-bit modulator displays so-called quantizer overload → $e_{rms}^2 > 1/3$ → ENOB=17b is more reasonable – however, a doubling of the OSR still yields 2.5 more bits.

In general, an L[th]-order modulator has $NTF(z) = (1 - z^{-1})^L$, and

$$q_{rms}^2 = \frac{\pi^{2L} e_{rms}^2}{(2L+1) \cdot OSR^{2L+1}}$$

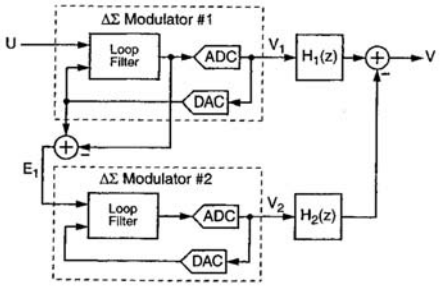


→ the extra number of bits for an OSR doubling is (L + 0.5)

However, higher-order modulators can only accept smaller input signals compared to lower-order modulators, because of stability reasons → the SNR gain is not what would be extracted from the figure → more than 60dB discrepancy in a 5[th]-order modulator!

Multi-stAge noise-SHaping (MASH) modulators

Two (or more) modulators in cascade



The q-error of the first modulator is found in the analog domain, and then used as the input of the second modulator; we obtain

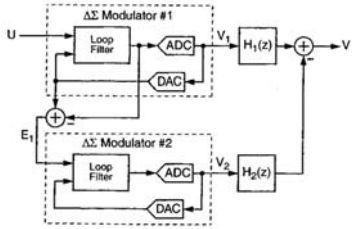
$$V_1(z) = STF_1(z)U(z) + NTF_1(z)E_1(z)$$
$$V_2(z) = STF_2(z)E_1(z) + NTF_2(z)E_2(z)$$

Multi-stAge noise-SHaping (MASH) modulators

The two digital filters H_1 and H_2 are designed such that E_1 is cancelled at the overall output – this requires

$$H_1(z)NTF_1(z) - H_2(z)STF_2(z) = 0$$

Typically, we choose $\begin{cases} H_1 = k \cdot STF_2 \\ H_2 = k \cdot NTF_1 \end{cases}$



with a suitable *k* giving a unity signal gain

Overall, we obtain $V = H_1V_1 - H_2V_2 = k \cdot STF_1 \cdot STF_2 \cdot U - k \cdot NTF_1 \cdot NTF_2 \cdot E_2$

A typical case is that both modulators are 2nd order:

$$STF_1 = z^{-1}, \quad STF_2 = 0.5z^{-1}, \quad NTF_1 = NTF_2 = (1 - z^{-1})^2$$

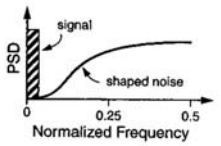
with *k*=2, we obtain $V = z^{-2}U + 2(1 - z^{-1})^4 E_2$

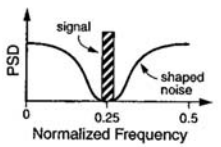
Thus, the noise shaping is that of a 4[th] order modulator, but the stability behavior is that of a 2nd order modulator! (however – and it is a big however! – perfect cancellation of E_1 is very difficult to achieve)

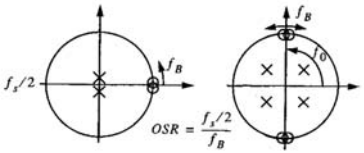
Bandpass ΔΣ modulators

Radio receivers → the signal is concentrated on a narrow band of width f_B, centered around a much higher frequency f_0 → modulator must have an NTF with a band-stop (rather than highpass) character → NTF zeros located at f_0 – the bandpass modulator is found from the lowpass prototype via z-domain mapping: for instance $z \rightarrow -z^2$ maps DC to $\pm f_s/4$ (i.e. z = ±j) → high SNR for frequencies near $f_s/4$

It is also clear that this mapping doubles the order of the modulator (in the same way as when we derive a bandpass filter from a lowpass prototype)







Multi-bit ΔΣ modulators

Single-bit DAC (and ADC) in the modulator result in high linearity; however, single-bit ADCs (i.e. comparators) have an ill-defined gain factor, and stability considerations result in a reduction of the allowable input swing, and hence of the achievable SNR

Multi-bit quantizer: the ADC gain is well defined, and the no-overload range of the modulator is increased; furthermore, the q-noise is reduced by 6dB for each added bit in the quantizer → very high SNR is possible even at moderate OSR!

The problem of the DAC non-linearity must be solved → trimming is a brute-force approach, but more popular is the manipulation of the DAC elements so as to reduce the in-band portion of the errors introduced by the DAC non-linearities → mismatch shaping!

Mismatch shaping is increasingly effective at higher OSR values

More advanced digital techniques are effective also at low OSR values

ΔΣ DACs

Same motivation as for ΔΣ ADCs: it is "impossible" to obtain linearity/accuracy better than 12 bits with Nyquist-rate DACs!

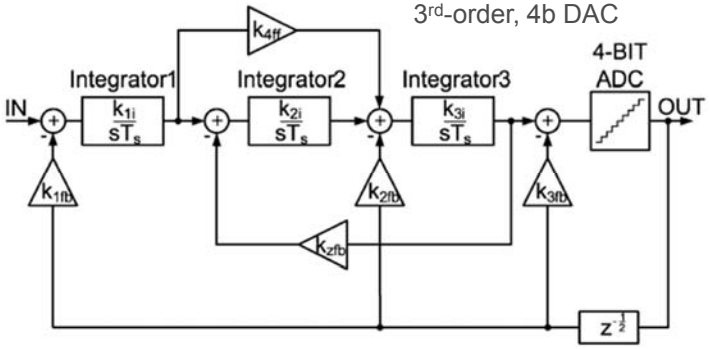
Operating a digital ΔΣ modulator with a high OSR, a high resolution (e.g. 18 bits) data stream can be converted into a single-bit data stream having the same baseband information → the large truncation noise is shaped by the loop so as to make the in-band part of this noise negligible → a two-level very linear DAC can now be used, while the out-of-band truncation noise is removed by a simple lowpass filter

As in the case of analog modulators, single-bit truncation may lead to instability → limited effectiveness of noise shaping – multi-bit truncation improves shaping and makes the design of the analog lowpass filter much easier – in-band DAC linearity is improved with the same techniques of mismatch shaping already mentioned

ΔΣ modulators – state-of-the-art

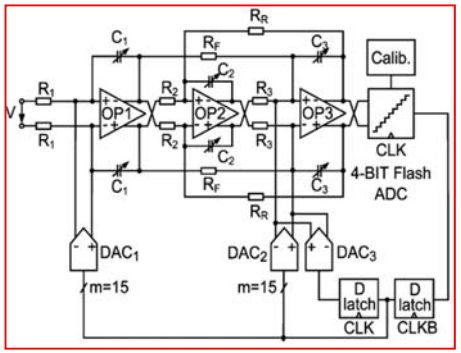
"**A 20-mW 640-MHz CMOS Continuous-Time ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB**", Mitteregger et al, IEEE Journal of Solid-State Circuits, Dec. 2006

Continuous-time, 3rd-order, 4b DAC

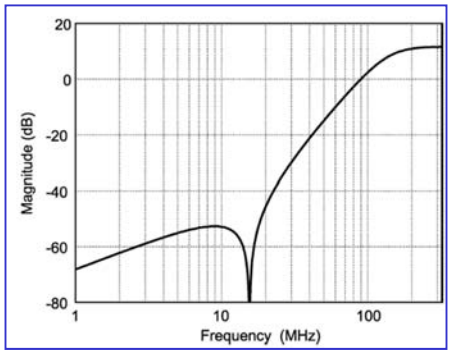


Mitteregger et al.

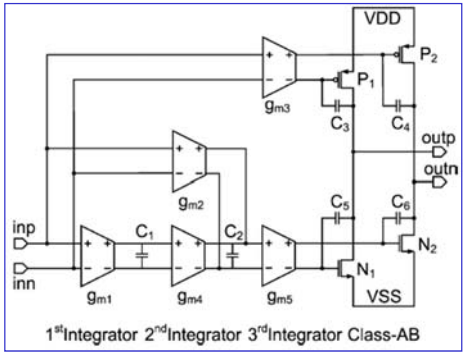
Modulator design – more details

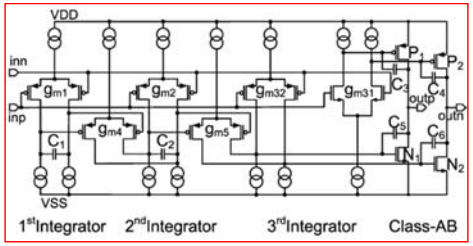


NTF minimizes the in-band quantization noise

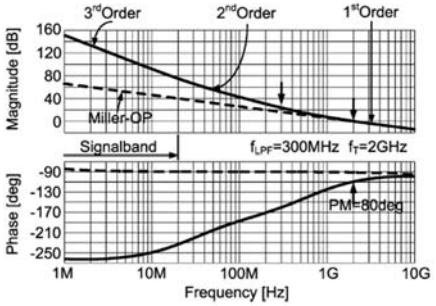


Mitteregger et al.



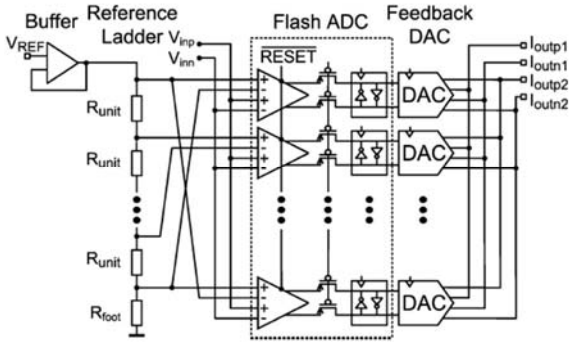


Opamp design is one of the most critical step → high gain, high bandwidth, high slew-rate, etc



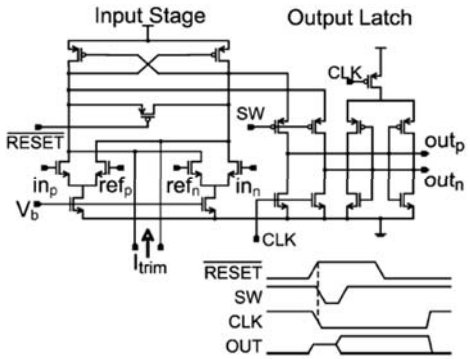
Mitteregger et al.

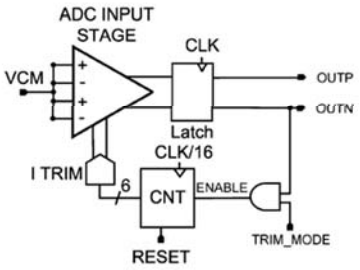
4-bit quantizer with 4-bit flash ADC, reference voltage generation, feedback DAC



Mitteregger et al.

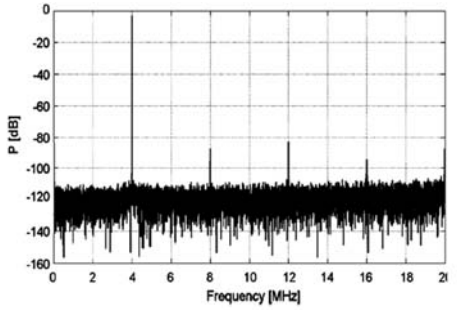
Left: comparator schematic of the 4-bit flash ADC (double differential input stage and a regenerative latch at the output)
Right: schematic of the flash ADC trimming circuit.

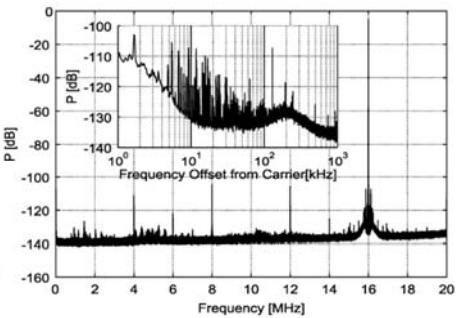




Mitteregger et al.

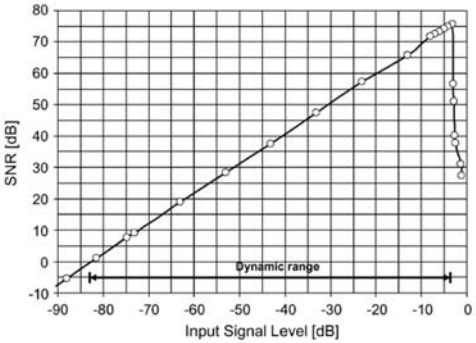
FFT (32 768 points) for a 4-MHz and a 16-MHz full-scale input signal – SNR is 76 dB in both cases



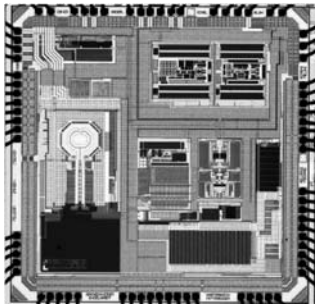


Mitteregger et al.

SNR versus input signal level for a 3.68-MHz signal. Peak SNR is 76 dB. Dynamic range is 80 dB.



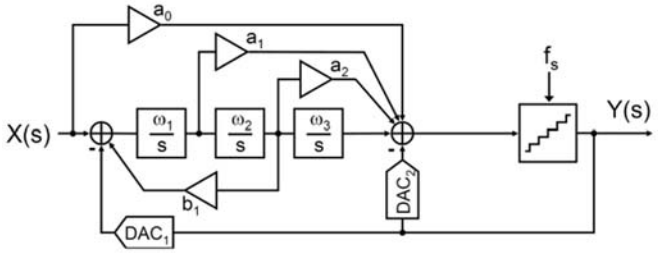
Sampling Frequency		640MHz
Conversion Rate		40MS/s
Input Range		0-20MHz
Peak SNR		76dB
THD		-78dB
Peak SNDR		74dB
ENOB		12
Process		1.2V 130nm 1P8M CMOS
Chip Area		8.6mm^2
Power	Modulator	20mW
	Decimator 40MS/s	18mW
	PLL 2.56GHz	12mW
	I/O 1.8V	4mW



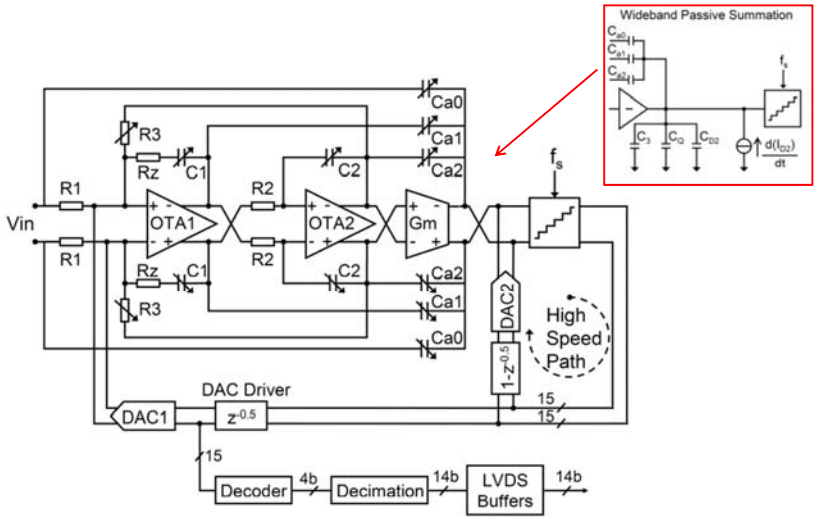
State-of-the-art – II

"**A 4GHz Continuous-Time ΔΣ ADC with 70dB DR and –74dBFS THD in 125MHz BW**", Bolatkale et al, IEEE Journal of Solid-State Circuits, Dec. 2011

Continuous-time, feedforward architecture, 3rd-order, 4b DAC

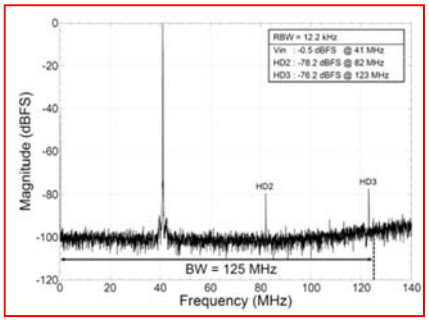


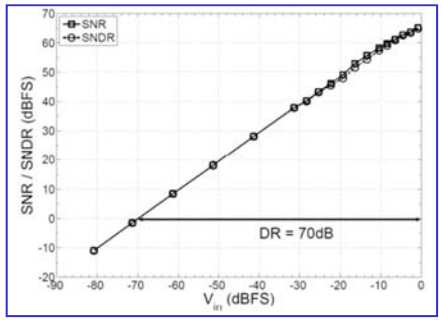
Bolatkale et al.

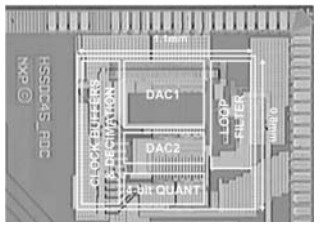


LVDS = low-voltage differential signaling

Bolatkale et al.



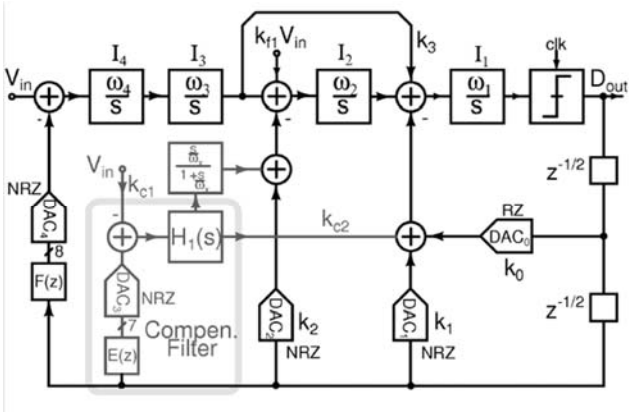




Architecture	ΔΣ
F_s (GHz)	4
BW (MHz)	125
DR (dB)	70
SNR (dB)	65.5
SNDR (dB)	65
Power (mW)	260
V_{DD} (V)	1.1/1.8
Area (mm^2)	0.9
Technology	45nm CMOS
FOM (pJ/conv.)[b]	0.71[a]
FOM (pJ/conv.)[c]	0.40[a]

ΔΣ modulators – state-of-the-art – III

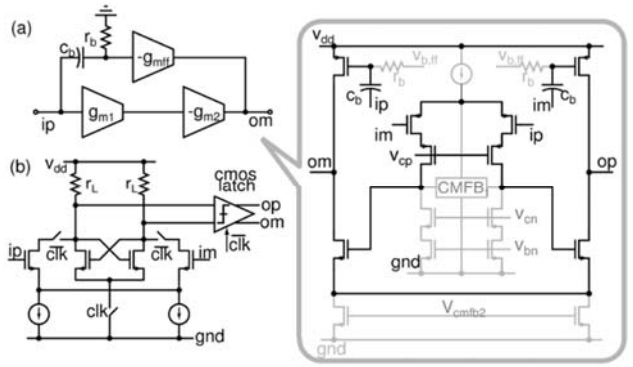
"**A 15mW 3.6GS/s CT-ΔΣ ADC with 36MHz Bandwidth and 83dB DR in 90nm CMOS**", Shettigar and Pavan, ISSCC 2012, Feb. 2012; JSSC Dec. 2012.



CT, 4th-order, 1b DACs

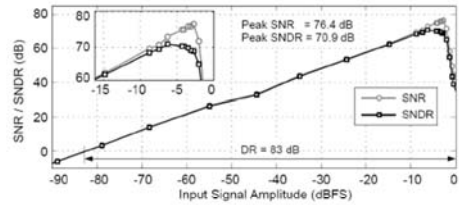
1st DAC with FIR → reduces sensitivity to clock jitter, and relaxes demand on loop filter linearity

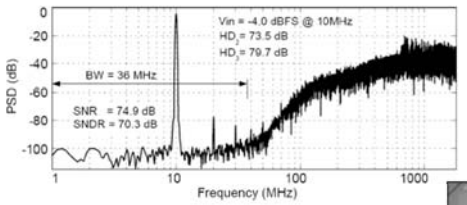
ΔΣ modulators – state-of-the-art – III



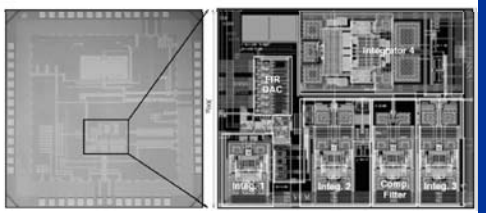
a) feedforward-compensated 2-stage opamps
b) quantizer

ΔΣ modulators – state-of-the-art – III





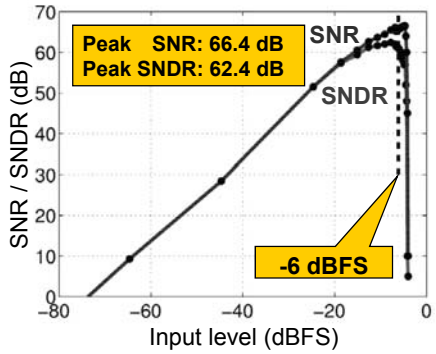
	This work
CMOS Feature Size	90nm
Active area	0.12mm²
Supply voltage	1.2V
Sampling rate	3.6GHz
P_d	15mW
BW	36MHz
DR	83dB
SNRmax	76.4dB
SNDRmax	70.9dB
$P_d/2BW\cdot2^{(DR-1.76)/6.02}$	18fJ
$P_d/2BW\cdot2^{(SNRmax-1.76)/6.02}$	38.6fJ
$P_d/2BW\cdot2^{(SNDRmax-1.76)/6.02}$	72.8fJ
$DR+10\log_{10}(BW/P_d)$	176.8dB

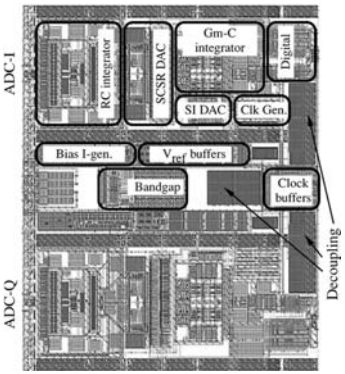


What we have done – Martin Anderson

1.92MHz BW, 3rd-order, 1-b DAC, OSR=81

Measured input amplitude sweep



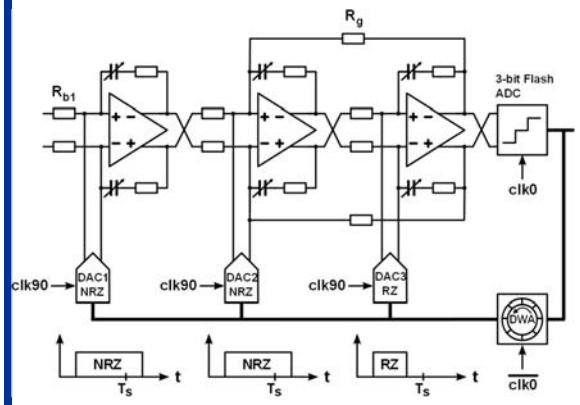


-1.2 / 1.8V, 5mW
- 90nm RF CMOS
- I & Q ΔΣ Modulators, BW=1.92MHz
- 0.48 x 0.62 = 0.3mm²

M. Anderson and L. Sundström, " Design and Measurement of a CT ΔΣ ADC with Switched-Capacitor Switched-Resistor Feedback", IEEE JSSC Feb. '09

What we have done – Mattias Andersson

9MHz BW, 3rd order, 3-b DAC, OSR=16



Quantizer
- 3-bit flash ADC
- Digital offset calibration

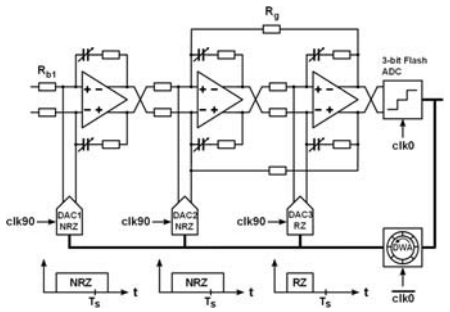
CT Active-RC loop filter
- Three integrators
- Folded-cascode opamps

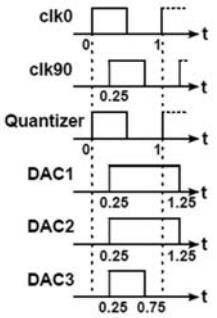
Three DACs
- Outermost DACs: NRZ
- Innermost DAC: RZ

DWA dynamic element matching (DEM) → DAC linearization + high-frequency shaping of mismatch noise

M. Anderson et al, "A 7.5mW 9MHz CT ΔΣ Modulator in 65nm CMOS with 69dB SNDR and Reduced Sensitivity to Loop Delay Variations", A-SSCC Nov. '12

What we have done – Mattias Andersson

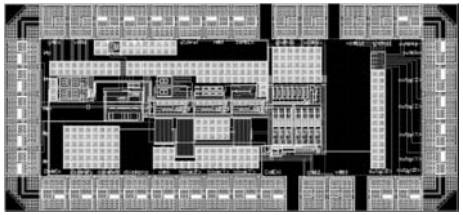




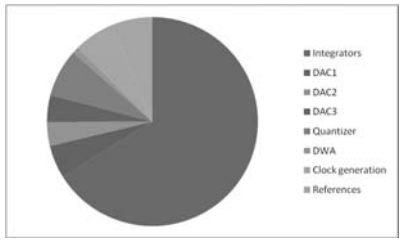
- I/Q clock phases exploiting RX LO
- Compensation of excess loop delay not needed
- Reduced GBW in 3rd integrator
- Enhanced robustness to excess loop delay variations

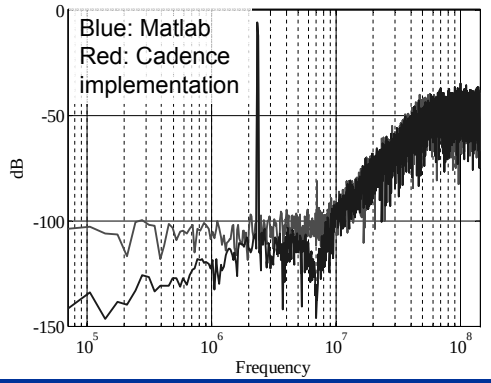
What we have done – Mattias Andersson

Core area: 400um x 200um



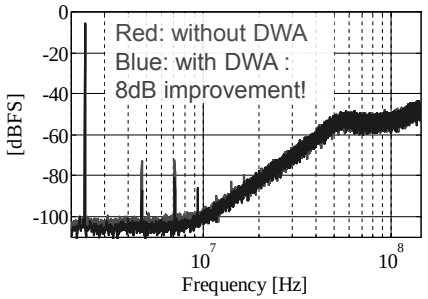
f_B	9MHz
f_s	288MHz (4 phases)
SNDR	71dB
HD3	-78dB
I_{vdd}	6mA
Area	0.1mm²

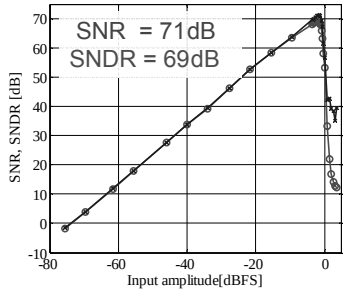




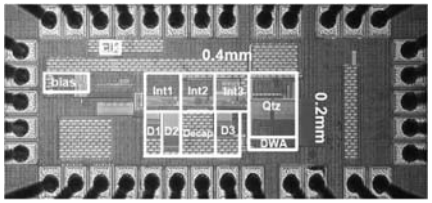
What we have done – Mattias Andersson

Measurement results



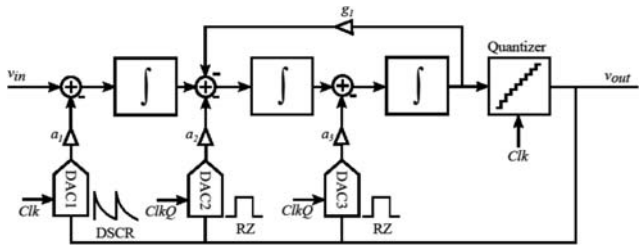


fs (MHz)	288
BW (MHz)	9
SNR (dB)	71
SNDR (dB)	69
DR (dB)	72
Power (mW)	7.5
Area (mm²)	0.08
Tech. (nm)	65
Vdd (V)	1.2
FoM (fJ/c.)	181



What we have done – Dejan Radjen

125kHz BW, 3rd order, 3-b DAC, OSR=16

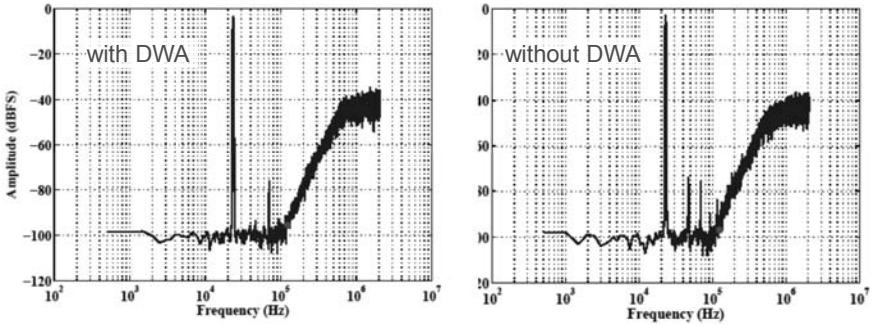


- Very-low-power, 3rd-order, 3-bit DAC, CT ΔΣ converter with modified feedback pulses for clock jitter tolerance
- Folded-cascode opamps
- DWA DEM

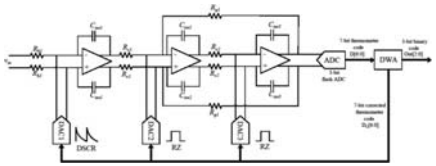
D. Radjen et al, "A continuous time delta-sigma modulator with reduced clock jitter sensitivity through DSCR feedback", Analog Integr Circ Sig Process, vol. 73, pp. 21-31, 2013

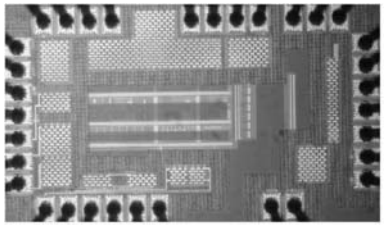
What we have done – Dejan Radjen

Measurement results

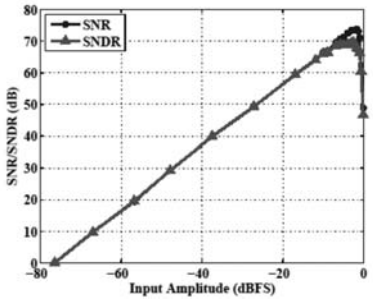


What we have done – Dejan Radjen

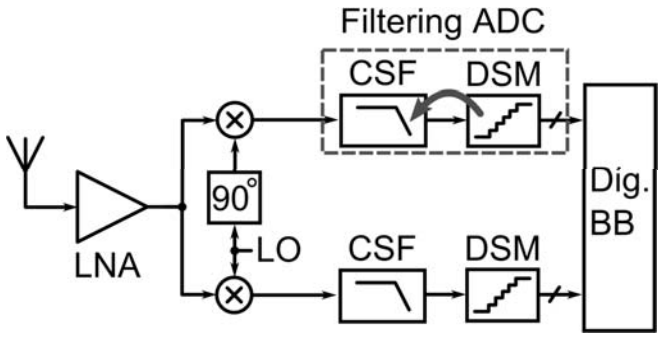




f_B	125kHz
f_s	4MHz
SNDR	70dB
HNR	74dB
I_{vdd}	420μA
V_{dd}	0.9V



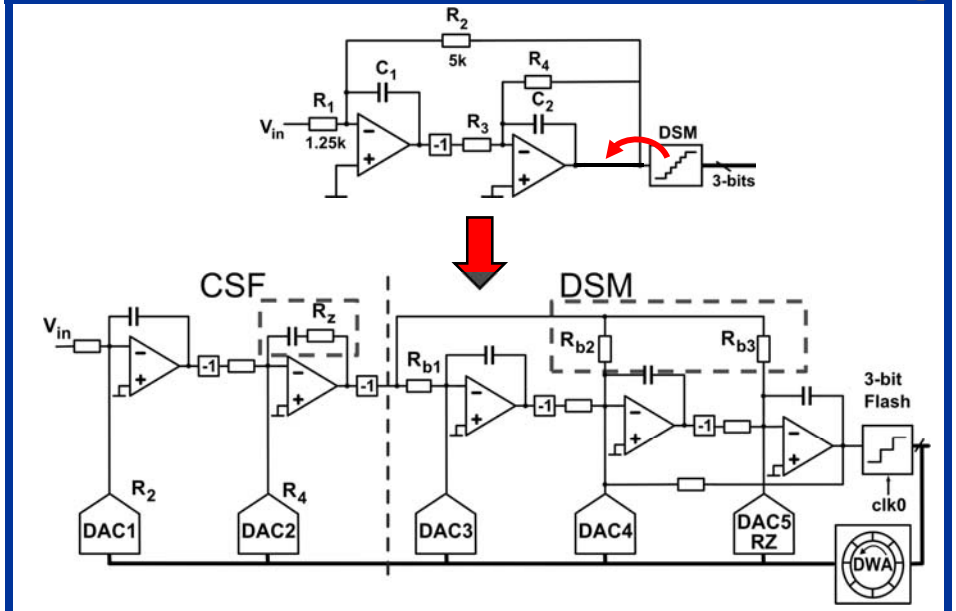
What we have done – Mattias Andersson



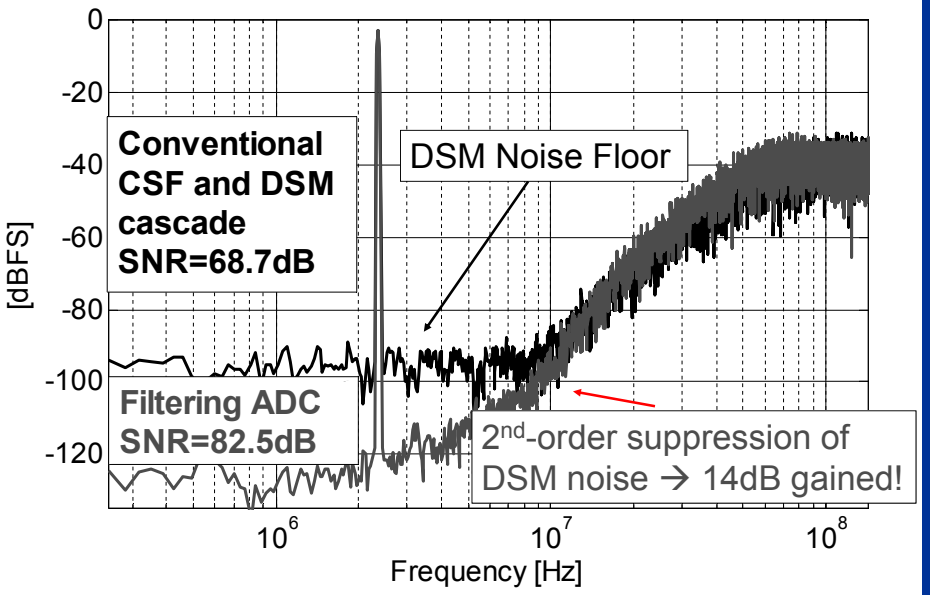
- Move DSM inside CSF → Filtering ADC
- Much lower requirements on DSM → power saved!!

M. Anderson et al, " A 9MHz Filtering ADC with Additional 2nd-order ΔΣ Modulator Noise Suppression", in Proc. 2013 ESSCIRC, pp. 323–326, Sept. 2013

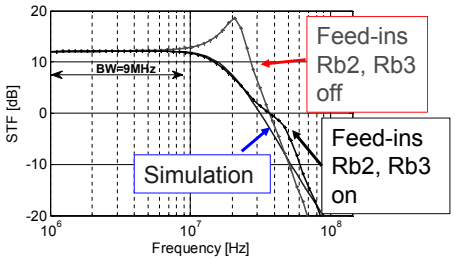
What we have done – Mattias Andersson

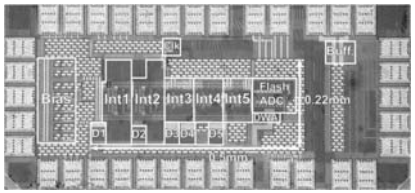


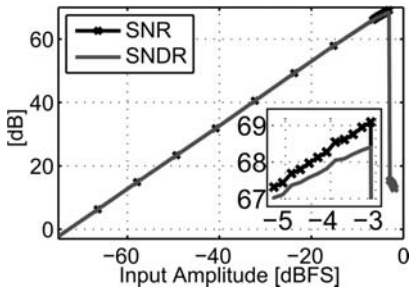
What we have done – Mattias Andersson



What we have done – Mattias Andersson







Parameter	This work	[1]	[2]	[8]	[9]
BW (MHz)	9	1	6	6.5	5
fs (MHz)	288	64	405	96	160
SNDR (dB)	68.4	59	74.6	70.9	69.5
f_{-3dB} (MHz)	16.9	3	–	–	–
Gain (dB)	12	0-40	–	–	–
IRN (nV/$\sqrt{Hz}$)	8.1	280*	–	–	–
In-band IIP3 (dBV_{rms})	11.5	19*	–	–	–
Out-of-band IIP2 (dBV_{rms})	72	–	–	–	–
Out-of-band IIP3 (dBV_{rms})	27	–	–	–	–
Tech. (nm)	65	180	90	180	130
Vdd (V)	1.2	1.8	1.2-1.8	1.8	1.2
Power (mW)	11.3	2	54	122**	6
DR at BW×4 (dB)	80	65	90	–	–
FOM1 at BW×4 (fJ/c.)	77	700	180	–	–
FOM2 (fJ)	0.075	1.98	–	–	–