# DSP-design

ERIK LARSSON

# Product we use and depend on…

# ….include electronics

Integrated circuit

CPU UDL SRAM
DSP DSP DRAM
PCI ROM

Printed-circuit-board

System

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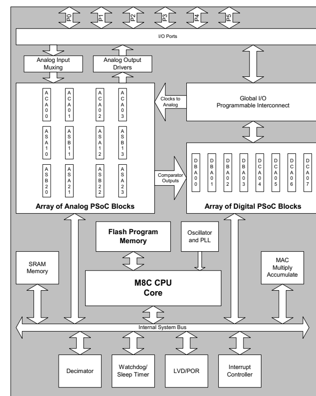
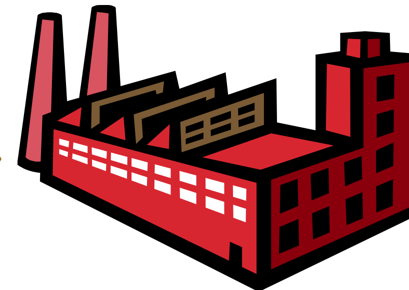
# Developing electronics

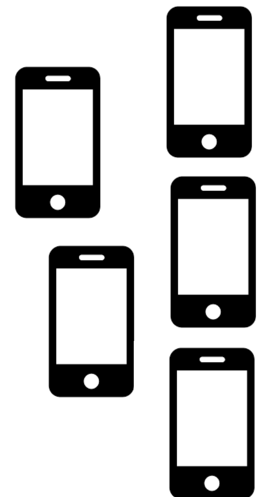
**Design**

**Design specification**



**Production**



**Product**

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# Your new smartphone

- Let say your new smartphone does not work
  - Is there warranty, you get it repaired or replaced
- When the manufacturer received a customer return
  - Try to figure out what is wrong with the product

# Manufacturer of Iphone 5 components

- ARM - processor
- Samsung – manufactures the ARM processor
- Skyworks Solutions – GSM/GPRS/EDGE/CDMA power amplifier
- Triquint Semiconductor – WCDMA/HSUPA power amplifier
- Avago Technologies – Dual-band LTE and FBAR duplex module
- Qualcomm – RF power management and LTE modem
- STMicroelectronics gyroscope linear accelerometer
- Murata Manufacturing – Wi-Fi module
- Texas Instruments – touchscreen SoC
- Broadcom – touchscreen controller
- Cirrus Logic – audio chip
- Sony – battery and image sensor

# One component (IC)

**SUN SPARC M7**
**10 000 000 000**
**transistors (2015)**

**AMD Epyc**
**19 200 000 000**
**transistors (2017)**

Transistor count

2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300

Date of introduction

1971
1980
1990
2000
2011

curve shows transistor count doubling every two years

16-Core SPARC T3
Six-Core Core i7
Six-Core Xeon 7400
10-Core Xeon Westmere-EX
Dual-Core Itanium 2
8-core POWER7
Quad-core z196
Quad-Core Itanium Tukwila
8-Core Xeon Nehalem-EX
AMD K10
POWER6
Itanium 2 with 9MB cache
Six-Core Opteron 2400
AMD K10
Core i7 (Quad)
Core 2 Duo
Cell
Itanium 2
AMD K8
Barton
Atom
Pentium 4
AMD K7
AMD K6-III
AMD K6
Pentium III
Pentium II
AMD K5
Pentium
80486
80386
80286
68000
80186
8086
8088
8085
6800
6809
8080
Z80
8008
MOS 6502
4004
RCA 1802

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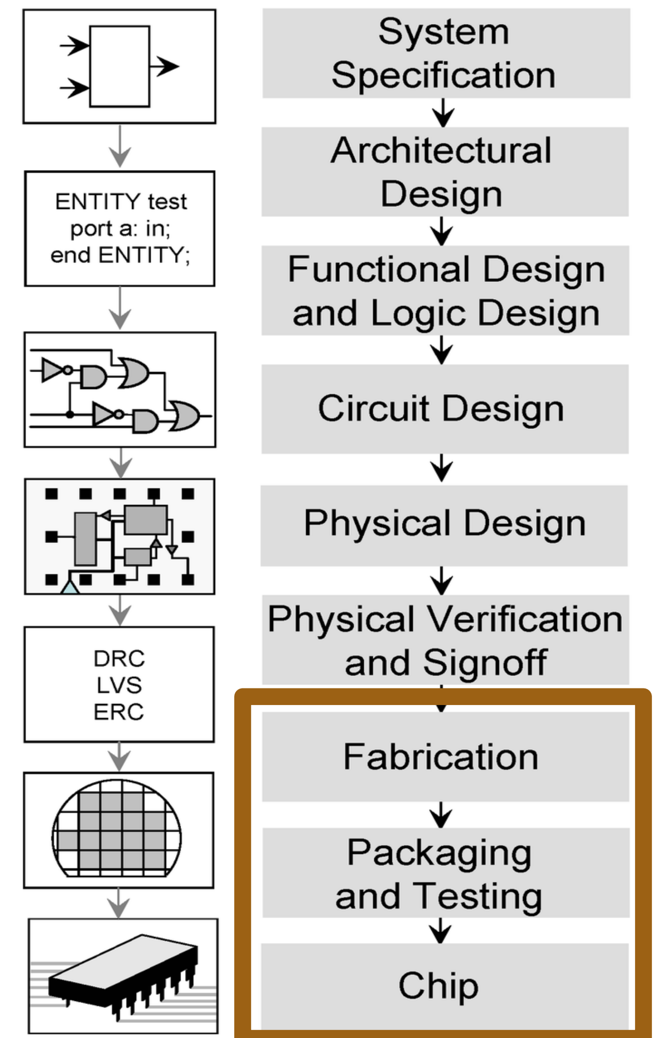
# The development

| | | Intel 4004 | Apple A13 | Difference |
|---|---|---|---|---|
| | Introduction | 1971 | 2019 | 48 years |
| Features of the development | Transistors | 2300 | 8.5 billions | 3.7million times |
| | Clock frequency | 740KHz | 2.65GHz | 3500 times |
| | Clock period | 1351351ps | 377ps | 3500 times |
| | Technology | 10µm | 7nm | 1400 times |

**Human hair (20µm)**
**is 1000 times thicker**

# Design steps for an IC

- Feasibility study and die size estimate
- Function analysis
- System Level Design
- Analogue Design, Simulation & Layout
- Digital Design, Simulation & Synthesis
- System Simulation & Verification
- Design For Test and Automatic test pattern generation
- Design for manufacturability (IC)
- Tape-in
- Mask data preparation
- Tape-out
- Wafer fabrication
- Die test
- Packaging
- Post silicon validation and integration
- Device characterization
- Tweak (if necessary)
- Datasheet generation
- Ramp up
- Production
- Yield Analysis / Warranty Analysis Reliability (semiconductor)
- Failure analysis on any returns
- Plan for next generation chip using production information if possible



# IC manufacturing

Design specification

Silicon ingot

Slicer

Blank wafers

20 to 40 processing steps

Patterned wafers

Wafer tester

Tested wafer

Dicer

Tested dies

Bond die to package

Packaged dies

Part tester

Tested packaged dies

Ship to customers

silicon chip

19 mm

5 mm

notch

small dot

plastic case

0.1 inch

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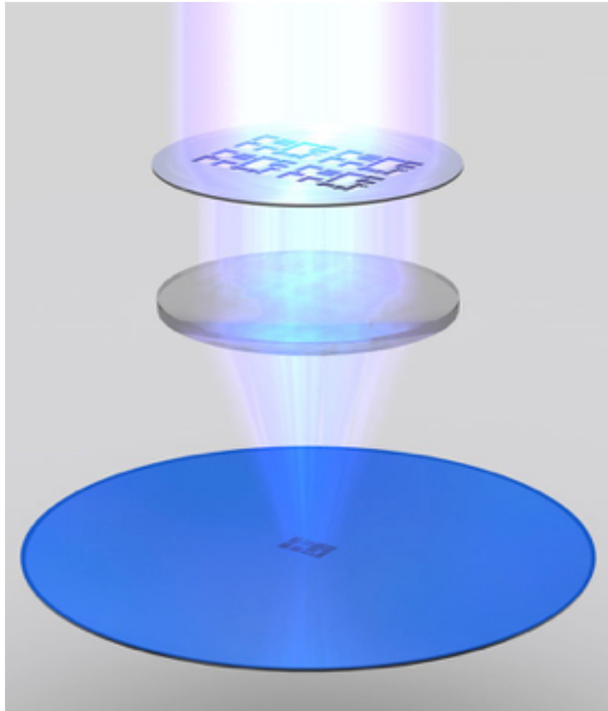
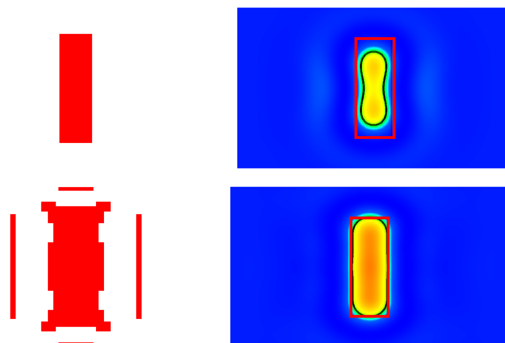
# IC manufacturing





- The cost to set up a modern 45 nm process is $200–500 million
- The purchase price of a photomask can range from $1,000 to $100,000 for a single mask.
- As many as 30 masks (of varying price) may be required to form a complete mask set.
- A few “re-spins” increase cost and delay time-to-market.

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# The development….

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| | Clock frequency | 740KHz | 2.65GHz | 3500 times |
| | Clock period | 1351351ps | 377ps | 3500 times |
| | Technology | 10µm | 7nm | 1400 times |
| Challenges due to development | Impact of 50ps timing mistake | 0.0037% | 13% | 3500 times |
| | Impact of 1 nm manufacturing mistake | 0.01% | 14% | 1400 times |

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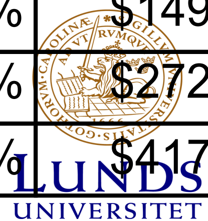
# Cost of defects

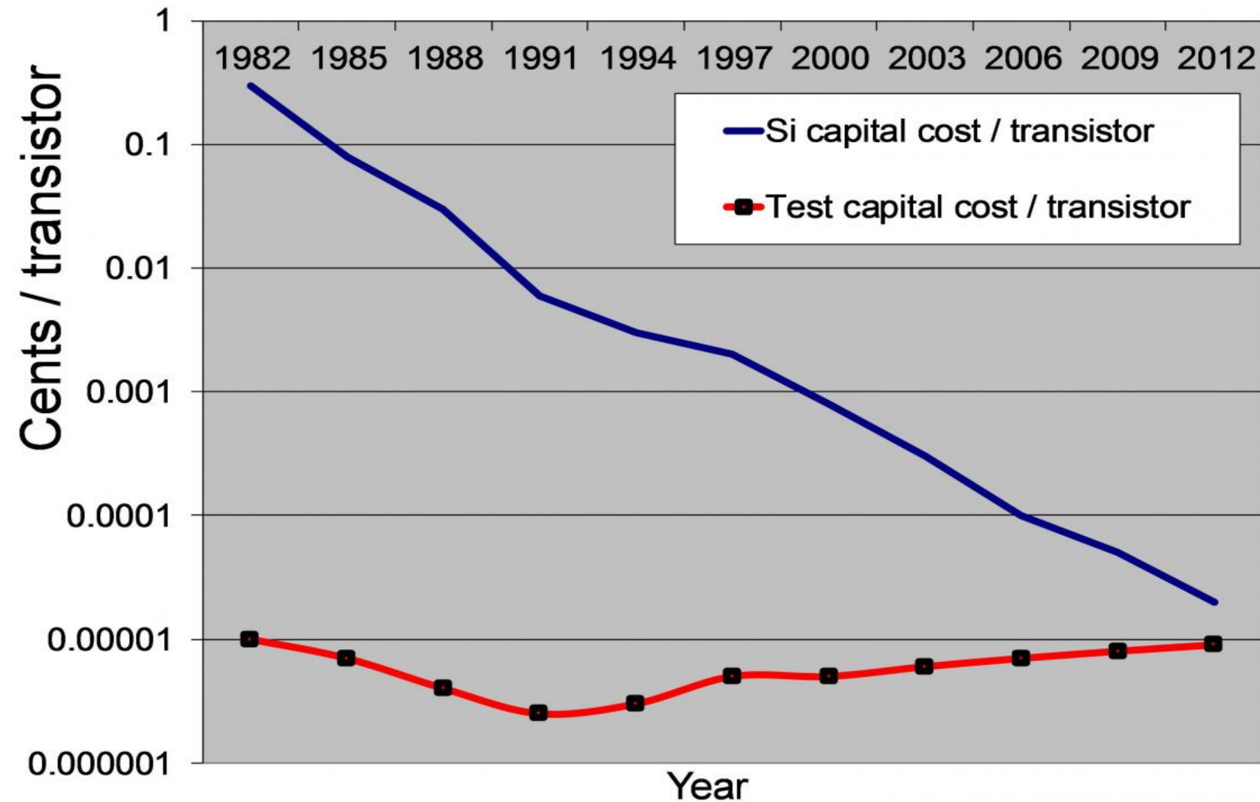
- Yield is good devices over produced devices
- Perfect manufacturing results in 100% yield
  - No need of test!

**No defects: 1200/181=$6.62**

| Chip | Layers | Wafer cost | Defect/cm$^2$ | Area (mm$^2$) | Dies/Wafer | Yield | Die Cost |
|---|---|---|---|---|---|---|---|
| 386DX | 2 | $900 | 1.0 | 43 | 360 | 71% | $4 |
| 486DX2 | 3 | $1200 | 1.0 | 81 | 181 | 54% | $12 |
| PowerPC 601 | 4 | $1700 | 1.3 | 121 | 115 | 28% | $53 |
| HP PA 7100 | 3 | $1300 | 1.0 | 196 | 66 | 27% | $73 |
| DEC Alpha | 3 | $1500 | 1.2 | 234 | 53 | 19% | $149 |
| SuperSPARC | 3 | $1700 | 1.6 | 256 | 48 | 13% | $272 |
| Pentium | 3 | $1500 | 1.5 | 296 | 40 | 9% | $417 |



# Cost per transistor

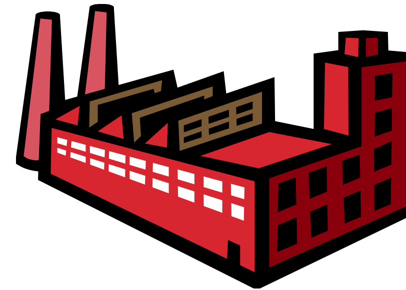



Beth Martin, Addressing Moore's Law with the First Law of Real Estate: Location, location, location, 08-02-2015, SemiWiki.com

# Cost for returns and repair

- The total cost of consumer electronics returns and repairs attributed to U.S. consumers was estimated at $13.8 billion (2007).
  - That is about 500 SEK per person/year
- No Trouble Found (NTF) is referring to a system or component that has been returned to the manufacturer or distributor for warranty replacement or service repair, but operates properly when tested. This situation is also referred to as No Defect Found (NDF) and No Fault Found (NFF).
  - Total cost of return and repair: $13.8 billion (2007) of which 20% is NTF (100 SEK per person/year)

# Product creation and analysis flow



# From design to a product

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# Design, verification and test

- Design synthesis: Given a function, develop a procedure to manufacture a device using known materials and processes.
- Verification (pre-silicon): Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given function.
- Test (post silicon): A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

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# Verification vs. test

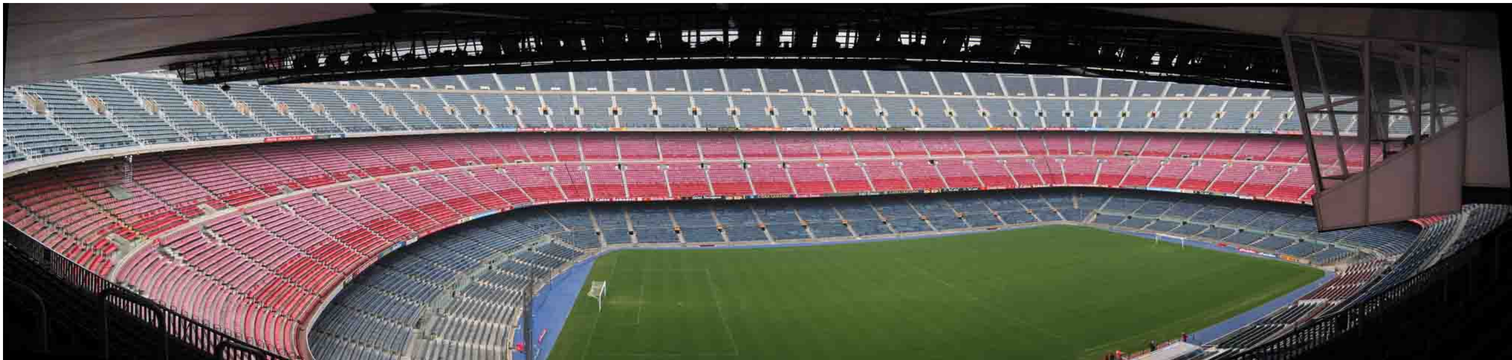
- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed <u>once</u> prior to manufacturing.
- Responsible for quality of design.

- Verifies correctness of manufactured hardware.
- Two-part process:
  - Test generation: software process executed once during design
  - Test application: electrical tests applied to hardware
- Test application performed on <u>every</u> manufactured device.
- Responsible for quality of devices.

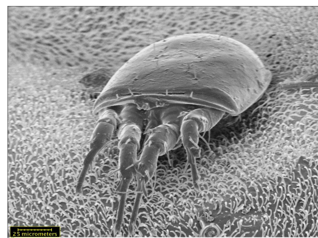
# Test vs. diagnosis

- Each seat in a football stadium is a chip to be sold
- Test challenge:  tell if there is a bug on any of the seats
- Diagnosis challenge: for a given seat to tell where the bug is

**A number of seats (chips)**



**A seat (chip)**



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# Test vs. diagnosis

Yield

Re-spins and process adjustments

Pass/fail testing

Diagnosis

First silicon

Ramp-up

Volume production

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# Returning to your broken smartphone

- Q: What can a manufacturer do so that you will not return with a product that is broken?
  - A: Make it free from defects and ensure quality!
    - » Q: What is a defect?
    - » Q: What is quality?
- **Vectors** generated against a **fault model** to measure **quality.** As few vectors as possible to keep cost low

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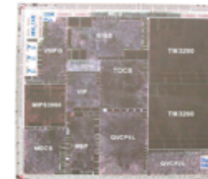
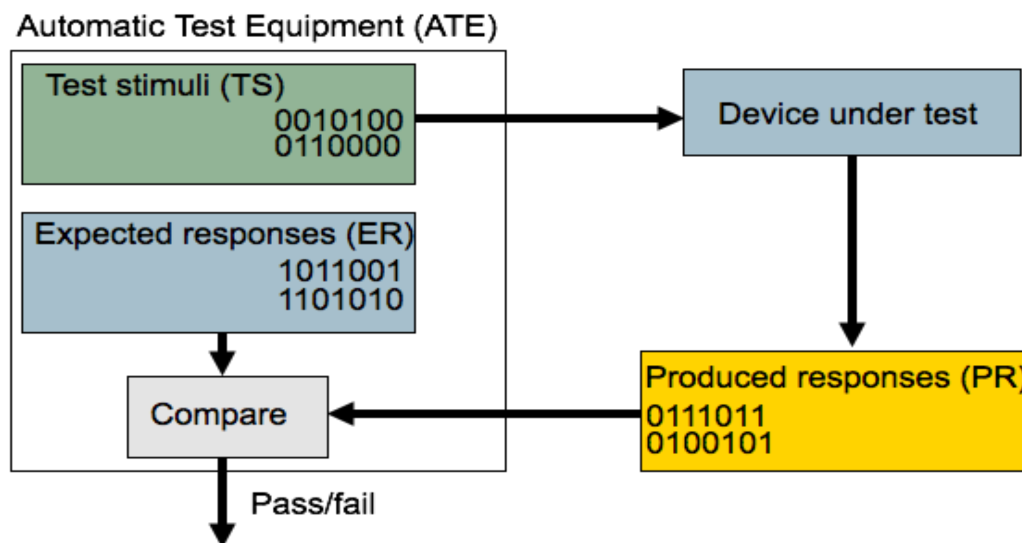
# Verification (Pre-silicon)

- Formal method – not applicable on industrial designs
- Simulation based – a test bed applying vectors
  - Lack of:
    - » Reference point
    - » Fault model
    - » Quality metric

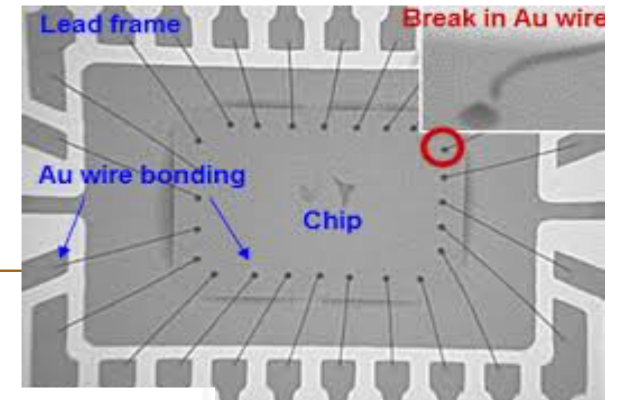
# Test (Post silicon)

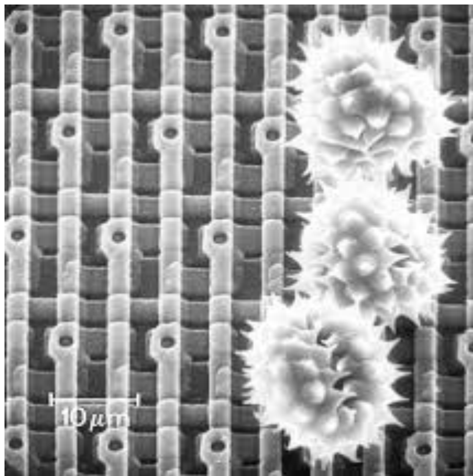
- Check if design specification match manufactured silicon





# Defects



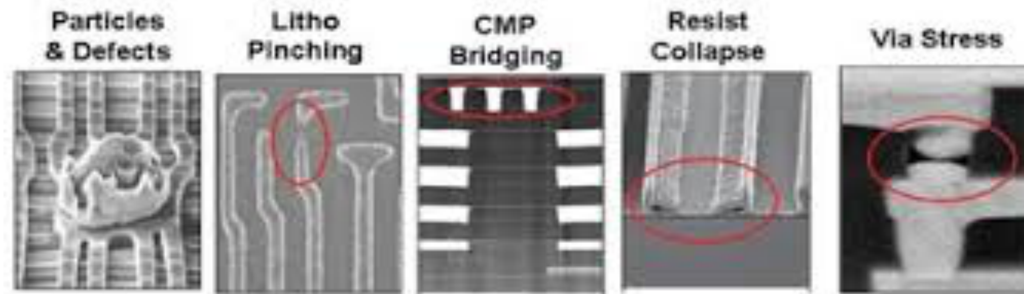
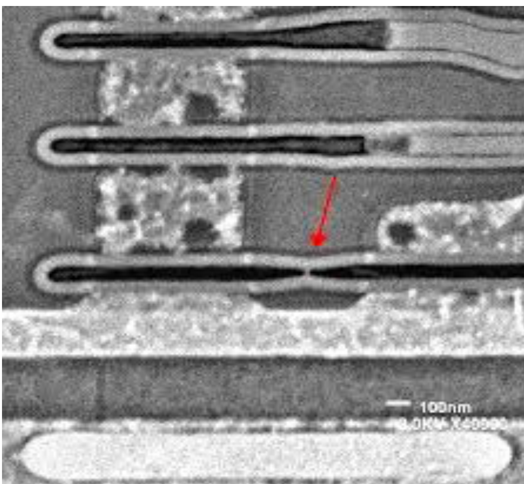




*Figure 3 Both feature-related and particle defects cause a chip to fail.*



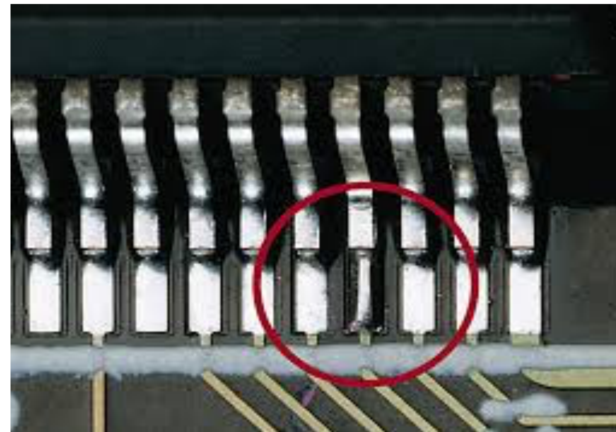



Fig. 1. With "tombstoning" only one side of a two-leaded chip component may be soldered to the target pad, but its other termination may not come in contact with the associated target pad. Photo courtesy of IPC-610

# Defects, faults and fault models

- Example: assume a break system in a car
- A defect is if there is weak joint in the brake fluid pipe (could be due to manufacturing mistake)
- A fault is if the weak joint break (but still you could drive the car and there is no problem unless you break)
- A failure is when you there is a fault in the braking system and you break.

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# Defects, faults and fault models

- Real defects too numerous and often not analyzable
- A fault model
  - identifies targets for testing
  - makes analysis possible
- A defect manifests itself as a fault
- A fault is modeled by a fault model
- Example of fault models:
  - Stuck-at Fault, Bridging Fault, Shorts (Resistive shorts), Opens, Delay Faults, Transient Fault

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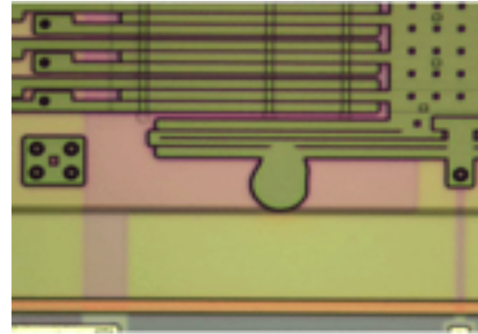
# Defects, faults, fault models

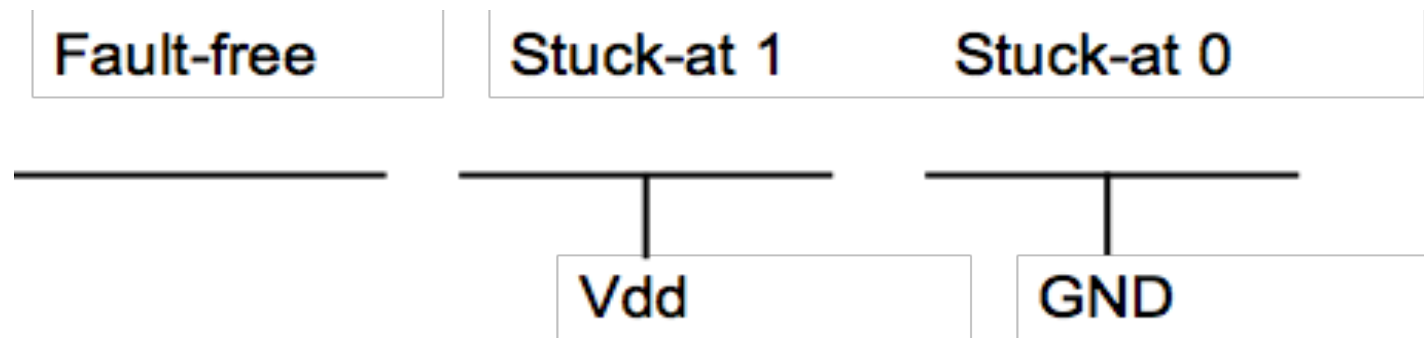
- Stuck-at: assumes that a line is stuck-at 0 or stuck-at 1
  - Simple fault model but there is a fault coverage metric
- Resistive bridge: assumes that there is a bridge between neighboring lines
  - Need layout and need to decide which resistive values to use
- Timing faults
  - Need two vectors (set up and apply)

# Defects, faults and fault models

- Example of a defect:



- Example of a fault model:




- A defect manifests itself as a fault
- A fault is modeled with a fault model

# Perfect test vs. real test

- Perfect test:
  - Detects all defects
  - Pass all functionally good devices
- Real test:
  - Based on analyzable fault models
  - Some good chips are rejected (yield loss)
  - Some bad chips pass test (test escape)

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# Outcome of test

- Good IC that **pass** the test -> this chip is sold
- Bad IC that **fail** the test -> this chip is not sold
- Bad IC that **pass** the test -> test escape //a bad chip is sold (lose costumer confidence)
- Good IC that **fail** the test – yield loss //a good chip is thrown away (lose money)

| | | Outcome of test | |
|---|---|---|---|
| | | Pass | Fail |
| Status of IC | Good | Sold | Yield loss |
| | Bad | Test escape | Not sold |

# Test escape and yield

- Assume 2 million ICs manufactured with yield 50%
  - 1 million GOOD shipped
  - 1 million BAD shipped
- Target DPPM (Defective parts per million) = 100
- For 100 BAD parts in 1 million shipped (DPPM=100)
  - Test must detect 999900 out of all the 1000000 BAD
    - » Test coverage: 99.99% (999900/1000000)

# DPPM and yield

- Consider 1 Million parts. Assume test coverage: 99.99% (100 escapes per million defective)
- DPPM @ 50% yield = 100
- DPPM @ 10% yield
  - » 0.1 million GOOD -> shipped
  - » 0.9 million BAD -> 90 test escapes (900000*(100%-99.99%))

  DPPM = 90/0.1=900
- DPPM @90% yield
  - » 0.9 million GOOD -> shipped
  - » 0.1 million BAD -> 10 test escapes (100000*(100%-99.99%))

  DPPM=10/0.9=11

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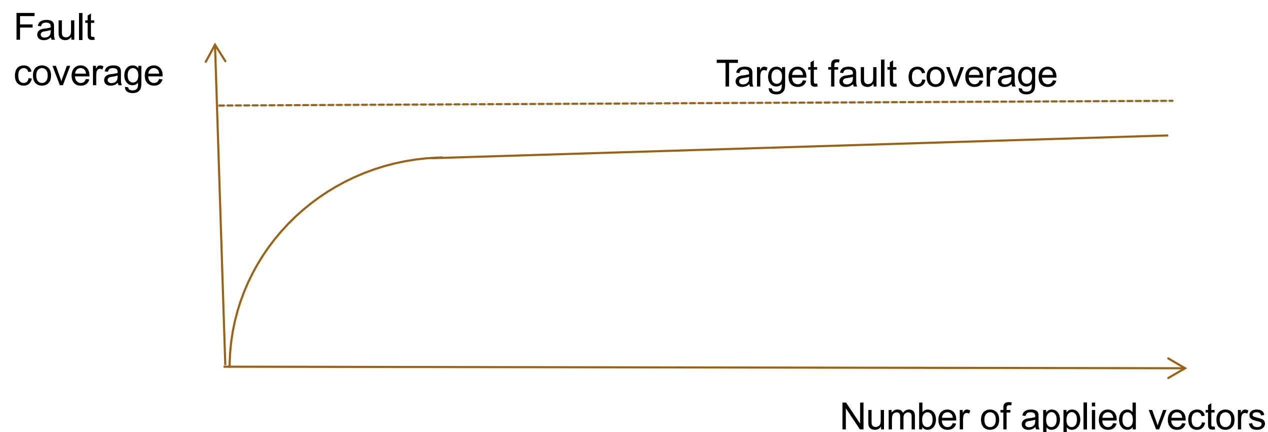
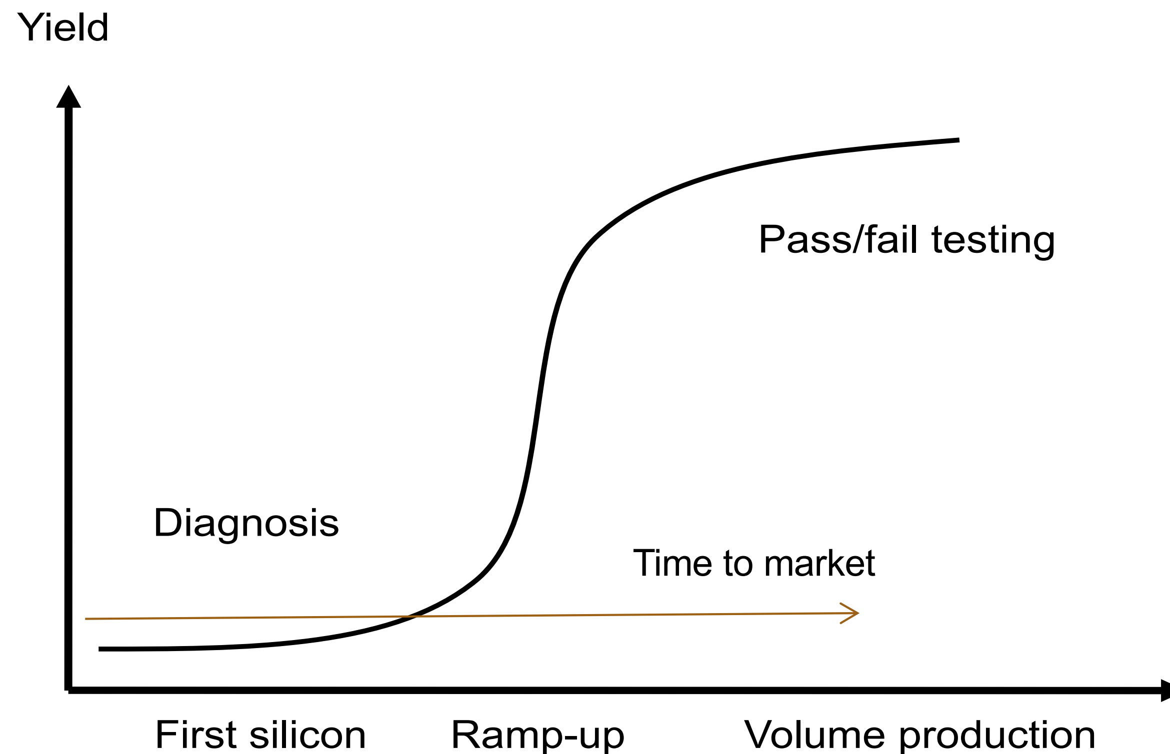
# Objective of test generation

- Specify the test vector
- Determine correct response (expected response)
- Evaluate cost of test (# patterns related to cost)
- Evaluate quality of test
  - Fault coverage = No of faults detected / No. faults modeled



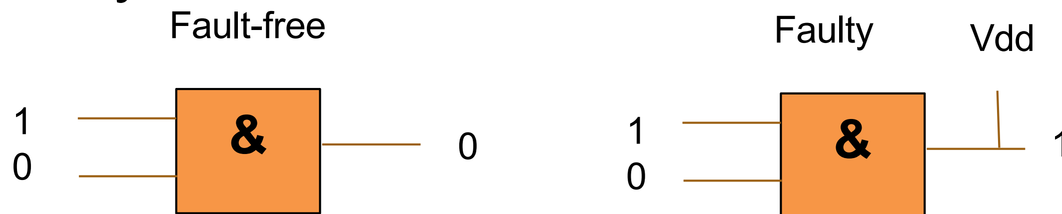
# What is the vectors good for?

- Diagnosis: enough information to pinpoint root cause of defects
- Pass/fail: enough information to determine if a device is good or bad



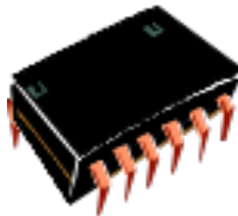
# Test generation

- Example: create a test to check if output connected to Vdd
- Requirement: response from fault-free case must be different from faulty case




- At manufacturing:

Apply stimuli:
1
0

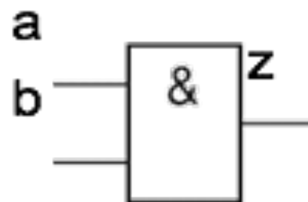


Produced response:
1

- Test pattern: test vector + expected test response
- Produced test response is compared against expected test response

# Exhaustive tests

- Try all possible alternatives
- For a 2-input design, $2^2$ (4) vectors are needed:




| a | b | z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

- For a 30-input design, $2^{30}$ (1073741824) vectors are needed
- If we apply 1 vector per second, it will take 34 years to test the circuit ($2^{30}$/(60*60*24*365)=34)

# General scheme for test generation

For a given fault model

While fault coverage < desired limit {

    Select an uncovered fault

    Generate test for the fault

    Evaluate fault coverage

}

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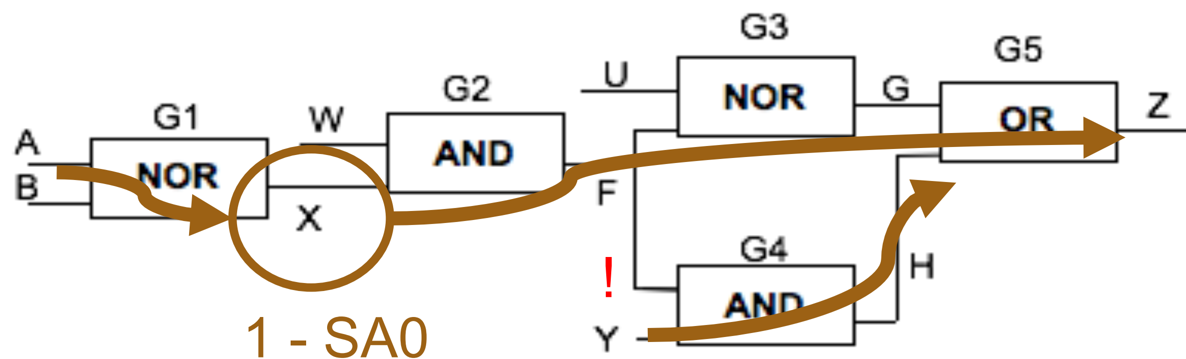
# Single stuck-at fault

- One line at the time is fixed to logic value 0 (stuck-at-0) or 1 (stuck-at-1)




- For the stuck-at fault model there are for a circuit with n lines 2*n possible faults
- Quality of a test is given by:

  fault coverage = faults detected / total number of faults

- Example: 12 lines (24 faults) detect 15 faults:
  f.c.=15/24 (63%)

# Single stuck-at fault

- A basic ATPG (automatic test-pattern generation) algorithm
  - activate one fault at a time
  - work backward from the fault origin to the PIs (primary inputs)
  - work forward from the fault origin to a PO (primary output)
  - work backward from the PO to the Pis to generate the sensitized path.

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# Ways to reduce number of test vectors

- Fault collapsing
- Equivalence rules
- Test compaction
- Fault simulation

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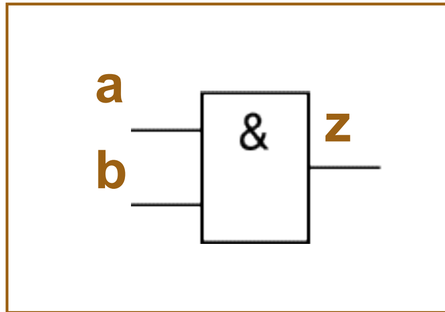
# Fault collapsing




- Value fault free/faulty (v/vf)
- Stuck-at 0 on a: a=1/0, b=1 -> z=1/0 //vector (stimulus) 11
- Stuck-at 0 on b: b=1/0, a=1 -> z=1/0 //vector (stimulus) 11
- Stuck-at 0 on z: b=1, a=1 -> z=1/0 //vector (stimulus) 11
- Stuck-at 1 on a: a=0/1, b=1 -> z=0/1 //vector (stimulus) 01
- Stuck-at 1 on b: a=0/1, b=1 -> z=0/1 //vector (stimulus) 10
- Stuck-at 1 on z: a=0, b=x -> z=0/1 //vector (stimulus) 0x or x0

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# Test compaction

- ATPG generates too many vectors; faults are covered by several vectors
- Static test set compaction tries to remove vectors after the use of ATPG
- Dynamic test tries to remove vectors during ATPG

| | $f_1$ | $f_2$ | $f_3$ | $f_4$ | $f_5$ | $f_6$ | $f_7$ |
|---|---|---|---|---|---|---|---|
| $v_1$ | x | | x | | x | | |
| $v_2$ | | | | | | x | x |
| $v_3$ | x | | | | x | | x |
| $v_4$ | | x | x | x | x | | |

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# Fault simulation

- Given
  - A circuit
  - A sequence of test vectors
  - A fault model
- Determine
  - Fault coverage - fraction (or percentage) of modeled faults detected by test vectors
  - Set of undetected faults
- Motivation
  - Determine test quality and in turn product quality
  - Find undetected fault targets to improve tests

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# Commercial ATPG tools

- Commercial ATPG tools are
  - for combinational circuits
  - make use of a random test generation for 60-80% of the faults (easy to detect) and deterministic test generation for the remaining part (hard to detect)
- Examples of commercial ATPG tools:
  - Encounter Test - Cadence
  - TetraMax - Synopsis
  - FastScan, FlexTest - Mentor Graphics

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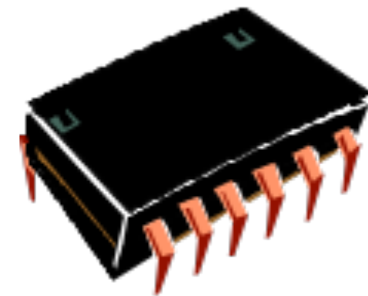
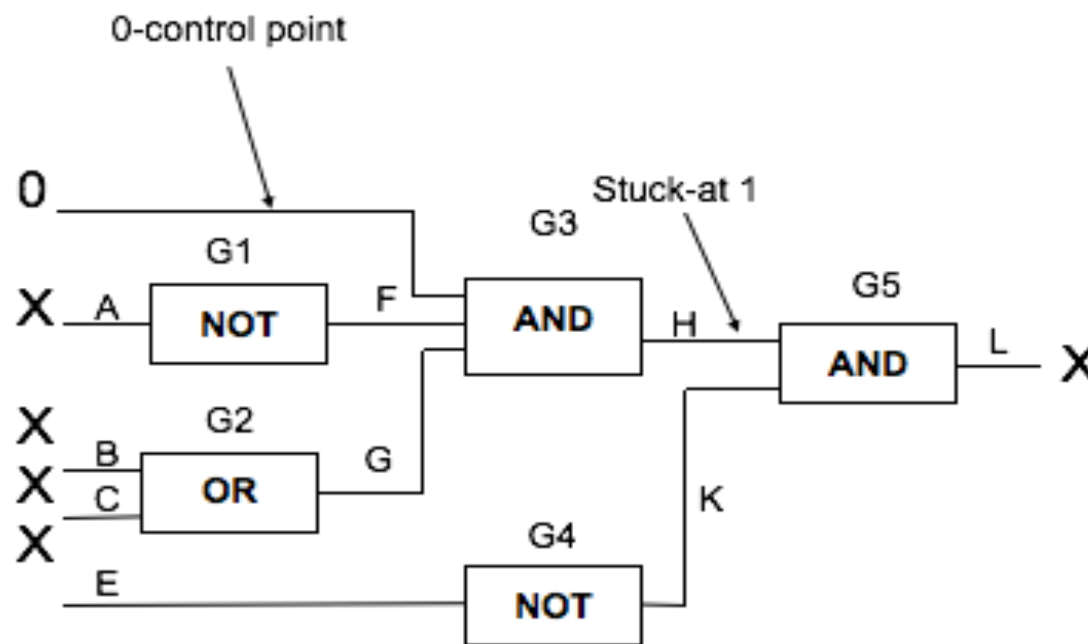
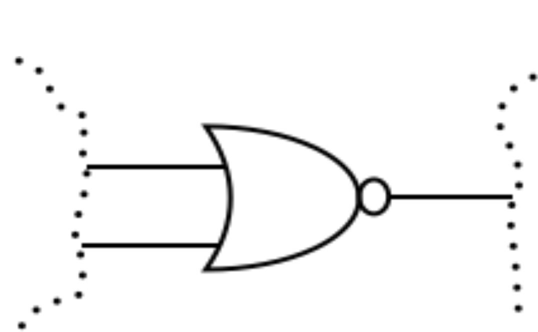
# Test point insertion

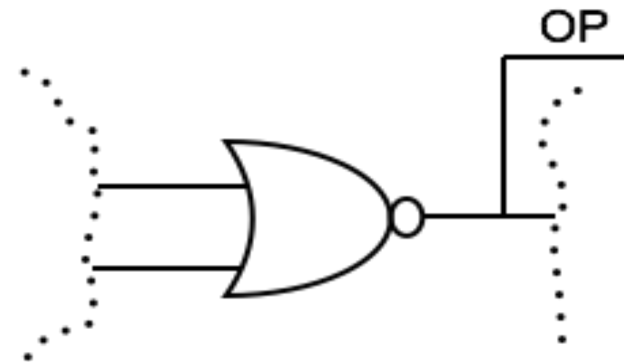
- Add a test point to ease test generation
- Access to chip internal is only through pins

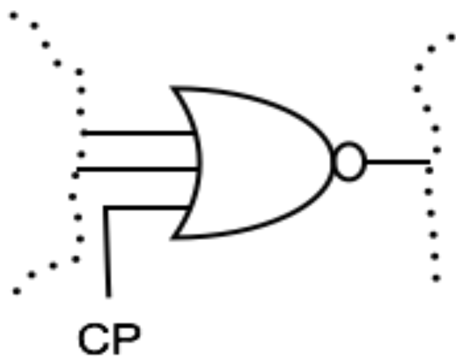


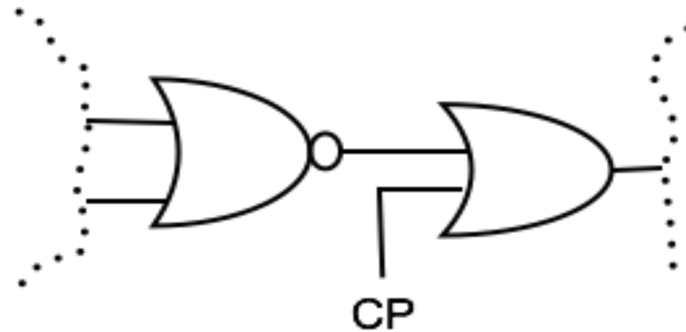


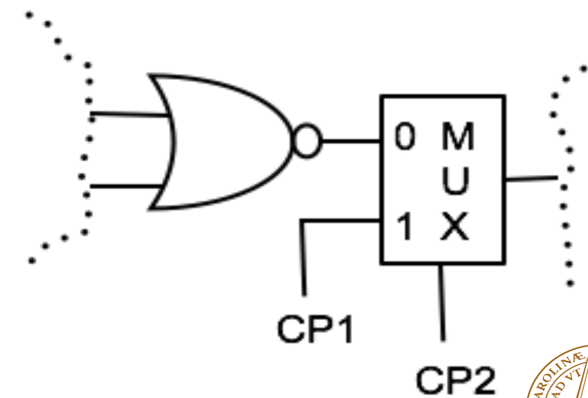
# Test point insertion



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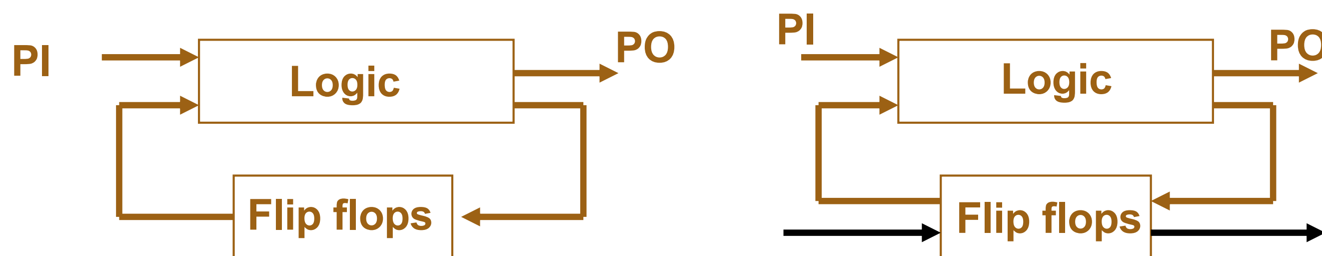
# Scan

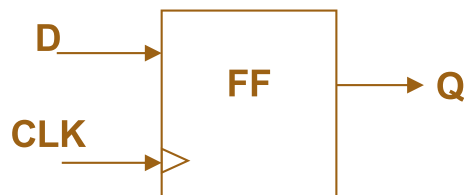
- Problem: ATPG works for combinational logic while most ICs are sequential
- Solution: Provide a test mode in which flip flops can be accessed directly
- Registers (FFs) provide virtual primary inputs/primary outputs

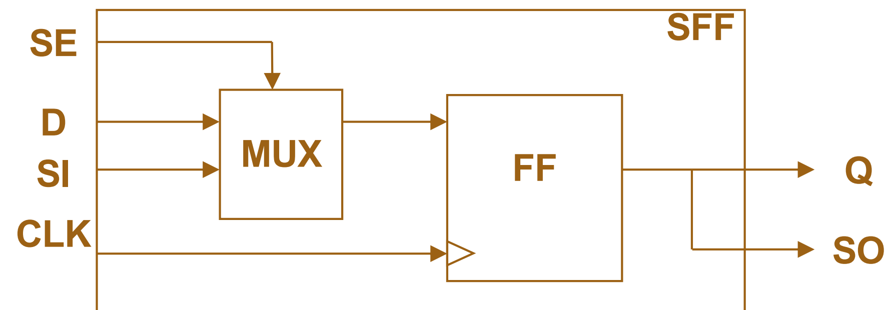



1. **Write flip flops**
2. **Stimulus at inputs**
3. **Normal cycle launch/capture**
4. **Observe output**
5. **Read flip flops**

# Scan

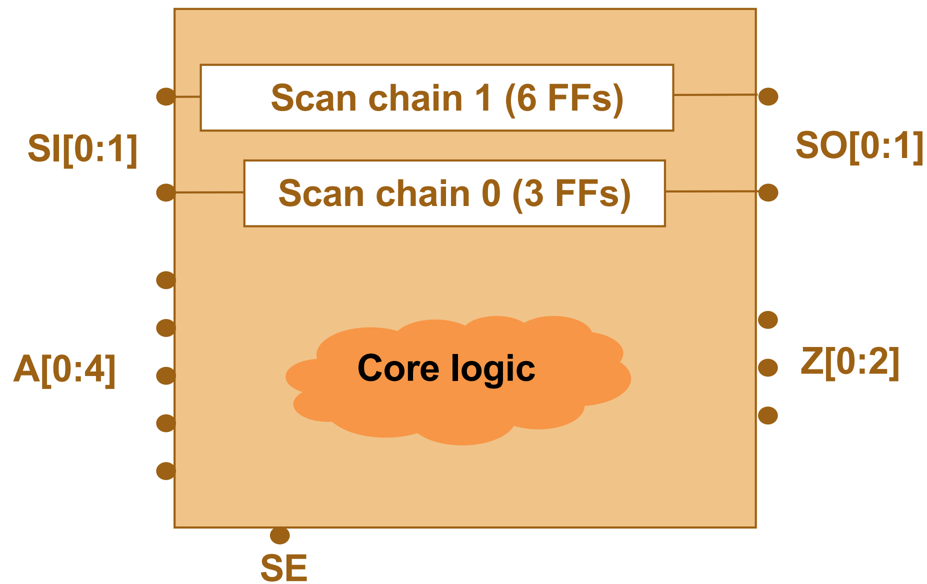
- Replace flip flop (FF) with scan flip flop (SFF): extra multiplexer on data input
- Connect SFFs to form one or more scan chains
- Connect multiplexer control signal to scan enable

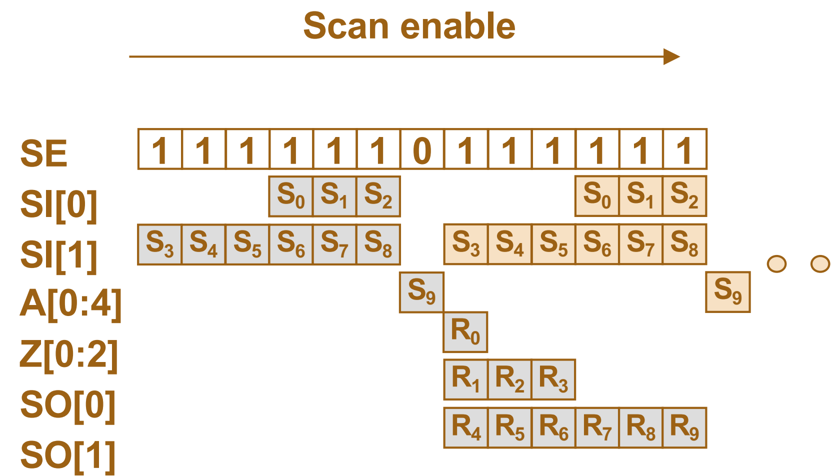



SE: Scan enable
SI: Scan input
SO: Scan output

# Scan application



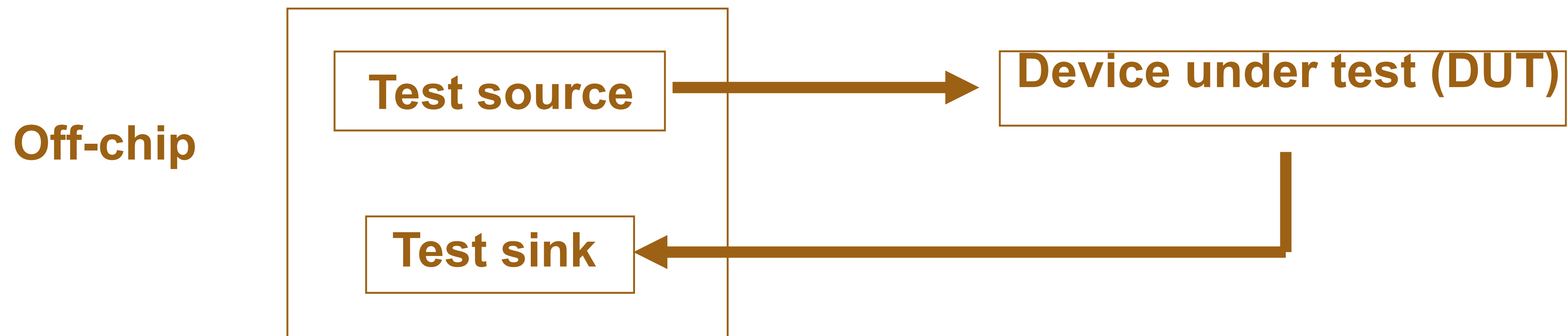



# Scan

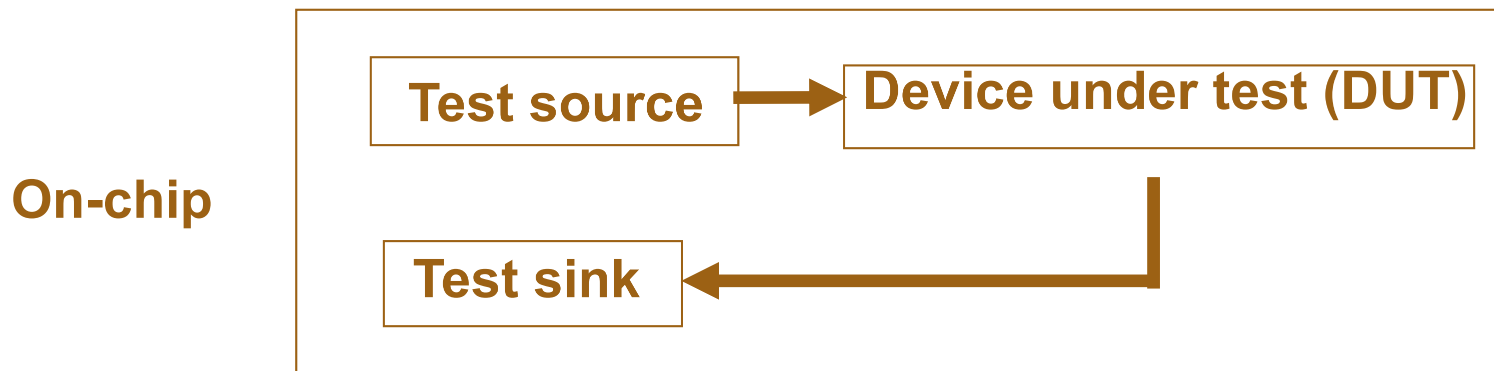
- Scan Benefits
  - Automatic scan insertion
  - ATPG
  - High fault coverage
  - Short test development time
- EDA tools
  - For scan insertion
  - Partial scan selection
  - Scan stiching
- Scan Costs
  - Silicon area
    - » Mux, scan chain, scan enable
  - Performance reduction
    - » Multiplexer in time-critical path
  - IC pins
    - » Scan-in (SI), scan-out (SO), scan_enable (SE)
  - Test time
    - » Serial shifting is slow

# Built-In Self-Test

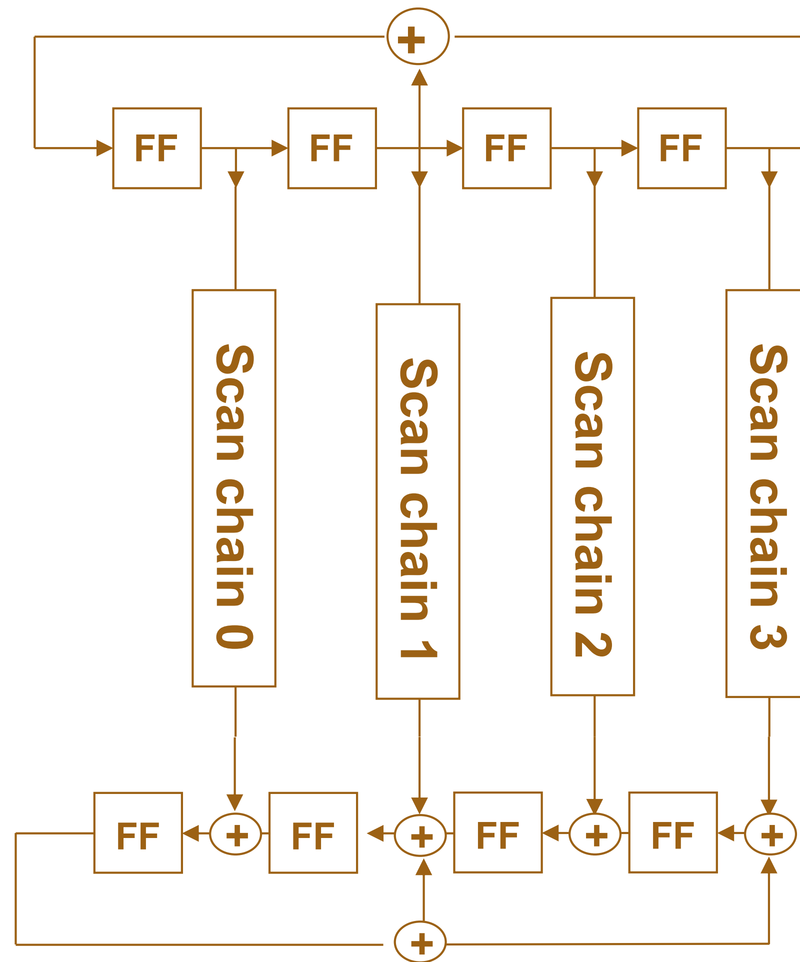
Off-chip




On-chip



# STUMPS: Self-testing using MISR and parallel shift register sequence generator




Scan chain 3

0001
1000
0100
1010
0101
0010
0001
1000
0100
1010
0101
0010
0001

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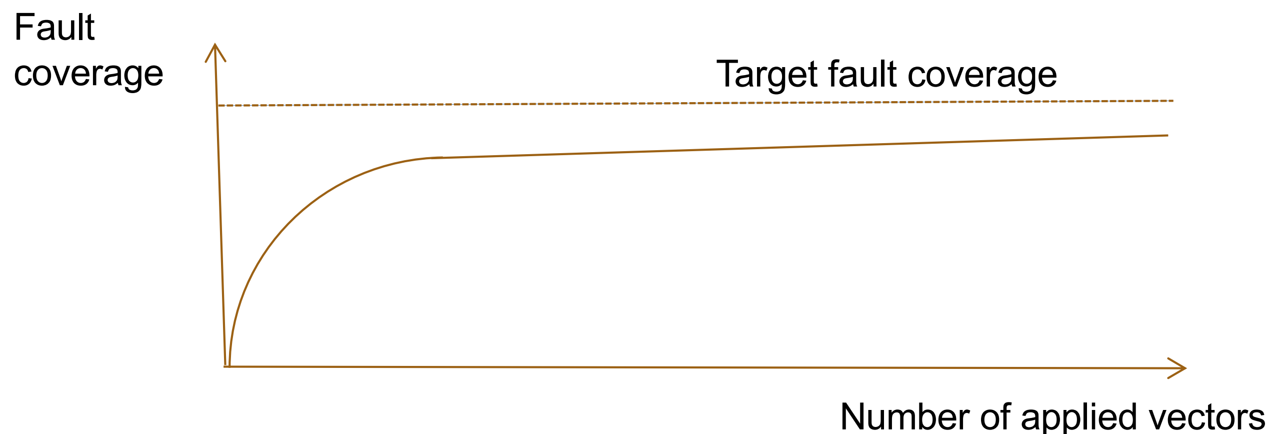
# Built-In Self-Test

- Difficult to reach high test coverage
  - Typically much lower than ATPG
- Diagnostic resolution is low
  - Only a MISR signature at the end of the testing



# Random pattern resistant faults

- The effectivness of a test is given based on the test's fault coverage, length, and hardware/data storage requirement.
- Probabilty to create a 1 at the output; $1/2^n$ where n is the number of inputs. n=2; P=0.25, n=4; P=0.0625

# Printed Circuit Board (PCB) testing

- Given a Printed Circuit Board (PCB) composed of a set of components (ICs) where each component is tested good.
- The main objectives are to ensure that all components are:
  - correct (the desired ICs are selected)
  - mounted correctly at the right place on the board and
  - ensuring that interconnections are functioning according to specification
- Problems that may occur:
  - A component is not placed where it should be,
  - A component is at its place but turned wrongly,
  - A component is correct but the interconnection is not correct, for example due to bad soldering.

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# Boundary Scan (IEEE std. 1149.1)

- The Joint European Test Action Group (JETAG), formed in mid-80, became Joint Test Action Group (JTAG) in 1988 and formed the IEEE std. 1149.1.
- The IEEE std. 1149.1 consists of:
  - Test Access Port (TAP)
  - TAP Controller (TAPC),
  - Instruction Register (IR), and
  - Data Registers (DR)

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# Boundary Scan (IEEE std. 1149.1)

BSC BSC BSC BSC
Core logic
BSC BSC BSC BSC
TDI
Bypass
TDO
Instruction Register
TMS
TCK
TAP Controller
TRST

BSC BSC BSC BSC
Core logic
BSC BSC BSC BSC
TDI
Bypass
TDO
Instruction Register
TMS
TCK
TAP Controller
TRST

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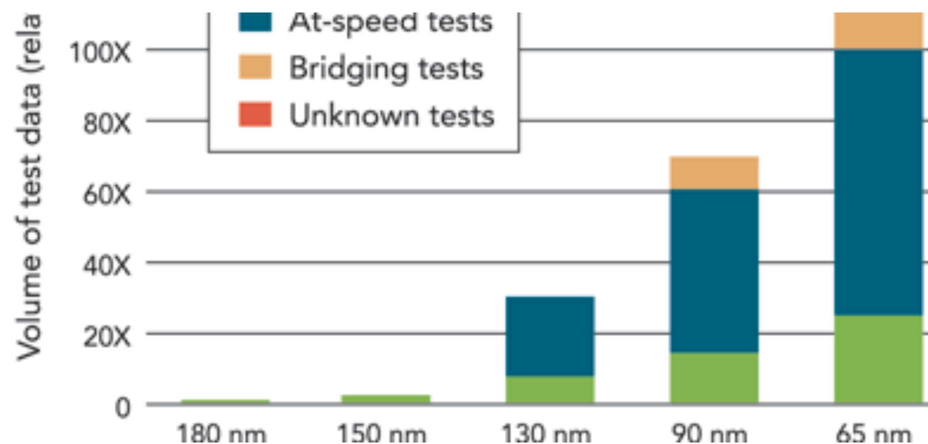
# Conclusions

- To producing products with high quality, start work during design time
- To measure quality, there is a need of a metric that tells the quality of a test
- Transistor count increase – adds test time
- Smaller transistors (new defect types, process variations)



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