32. (a) The retimed filter is shown in Figure 13.

(b) The folded architecture is shown in Figure 14.

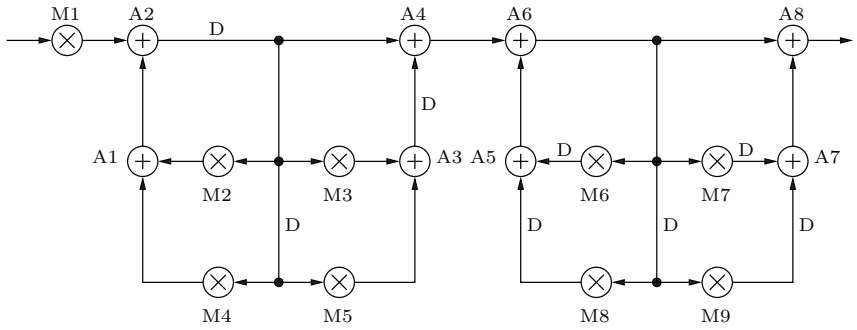

Figure 13: Retimed biquad filter.

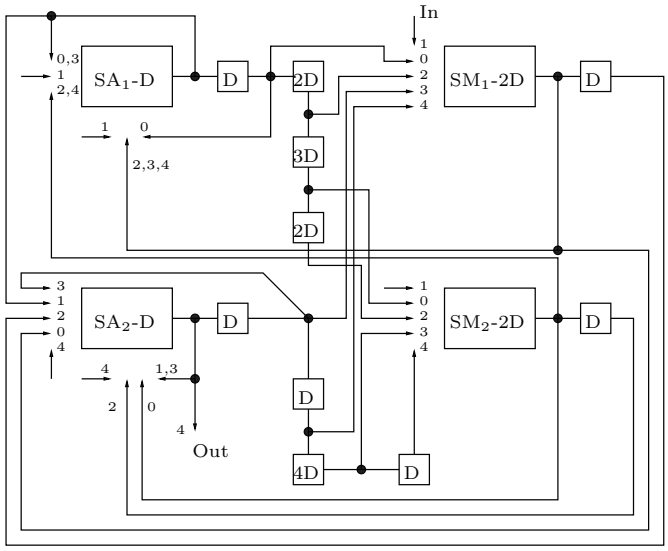

Figure 14: Folded biquad filter.

33. (a) The retimed filter is shown in Figure 15.

(b) The folded architecture is shown in Figure 16.

(c) Lifetime analysis shows that there are actually only 8 registers (compared to 10) needed.

34. (a) The pipelined/retimed filter is shown in Figure 17.

(b) The folded architecture is shown in Figure 18.

(c) There are at least 4 registers needed (compared to 9), see Figure 19.

(d) Less arithmetic units at the cost of controller overhead and latency.

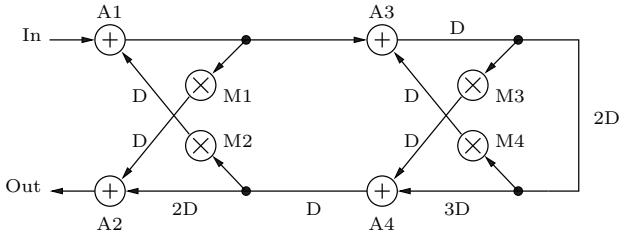

Figure 15: Retimed lattice filter.

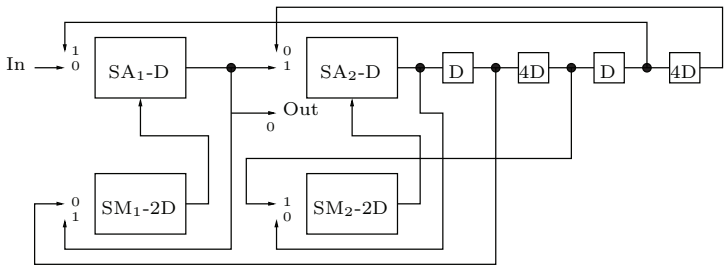

Figure 16: Folded lattice filter.

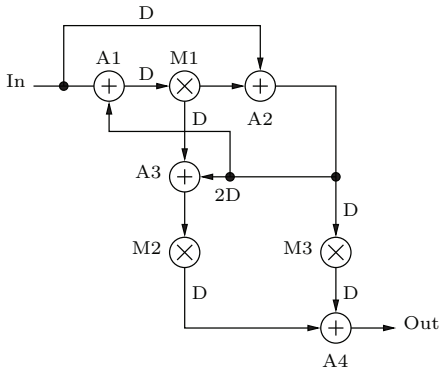

Figure 17: Pipelined/retimed IIR filter.

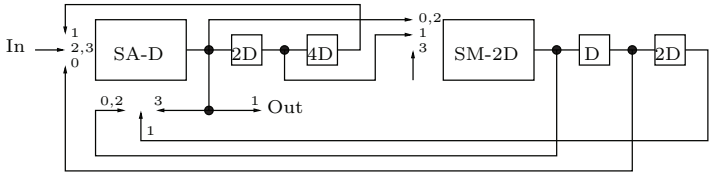

Figure 18: Folded IIR filter.

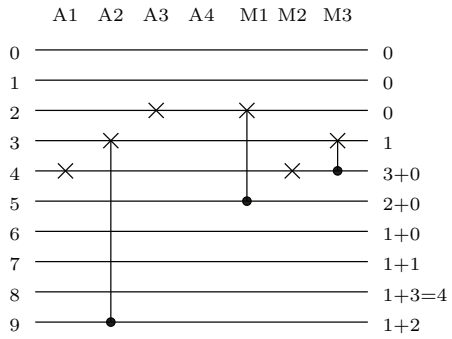

Figure 19: Lifetime chart.